Title: Processor Design

Description of the Directed Study: Integrated circuits are at the heart of every complex electronic device. Learning to design architecture for general purpose devices allows for the creation of several complex devices from a single architecture. This course will explore the fundamentals of the theory behind processor architecture and its design. Starting from an electronics perspective and converting to a computer engineering and science perspective, student(s) will explore a comprehensive set of topics surrounding the design of general processing components such as CPUs and GPUs.

Reading list:

Computer Architecture: A Quantitative Approach 5th Edition
by John L. Hennessy (Author), David A. Patterson (Author)

Modern Processor Design: Fundamentals of Superscalar Processors 1st Edition
by John Paul Shen (Author), Mikko H. Lipasti (Author)

Course objectives:

- Understand the inner workings of integrated circuits
- Gain the skills to implement basic Computer Architecture Principles
- Gain the skills to develop Instruction Sets
- Gain the skills to understand various levels of basic parallelism

Program design that includes 8-10 hours of academic work each week:

- Class: 3 Hours a week
- Reading Homework: 2-3 Hours a week
- Labs: 2-3 Hours a week
- Final Project: Replaces the reading homework and labs during the end of the course

Number of meetings and times planned per week: 3 Meetings

Proposed assessments: (All likely done with Lucid and Alchrity)

- Week 1 to 3 | Lab 1: I/O (USB)
- Week 3 to 4 | Lab 2: Controlled Circuits
- Week 4 to 5 | Lab 3: ALU and Leveraging Memory
- Week 5 to 7 | Lab 4: Simple Reduced Instruction Set
- Week 6 to 8 | Lab 5: Parallelism
- Week 7 to X | Final Project: Full Implementation of Simple General Processor

Syllabus:

Week	General Week Topic	Meeting 1	Meeting 2	Meeting 3
1	Introduction and Review	Binary and Boolean Logic	RTL Component Design	FPGA Basics
2	Alchrity, Lucid, & I/O	Lucid Crash Course	Basic I/O with LEDs	Serialization
3	Synchronous Logic	Registers / Shift Registers	FSMs and Controllers	Handshaking | Lab 1 Due
4	Quantitative Analysis of General Processors and Memory	Trends and Performance	ROMs and RAM (Alchrity)	Memory Hierarchy | Lab 2 Due
5	Instruction Sets	Reduced vs. Complex vs. Minimal	Operations and Instructions	A look at RISC-V | Lab 3 Due
6	Instruction-Level Parallelism	ILP Fundamentals	Limitations and Exploiting ILP	Pipelining
7	Data-Level Parallelism	Vector Architectures	SIMD Instruction Set	GPU Architectures | Lab 4 Due
8	Thread-Level Parallelism	Shared-Memory Architectures	Synchronization: The Basics	Multicore Processors: Performance | Lab 5 Due
9	Warehouse-Scale	Computer	Cloud	Crosscutting

	Computers and Analog Computing Basics	Architecture of Warehouse-Scale Computers	Computing	Issues and Analog Computing
10	Final Project Work	Checkin	Checkin	Final Due