



**OPENHW**<sup>GROUP</sup>  
PROVEN PROCESSOR IP



**CORE-V™**

# OpenHW Group 2020 BHAG

BIG HARRY AUDACIOUS GOAL

## **CORE-V™ Chassis**

- production ready,
- CORE-V CV64A & CV32E cores,
- deep sub-micron SoC,
- on an eval board,
- running Linux / Zephyr
- Tapeout 2H, 2020



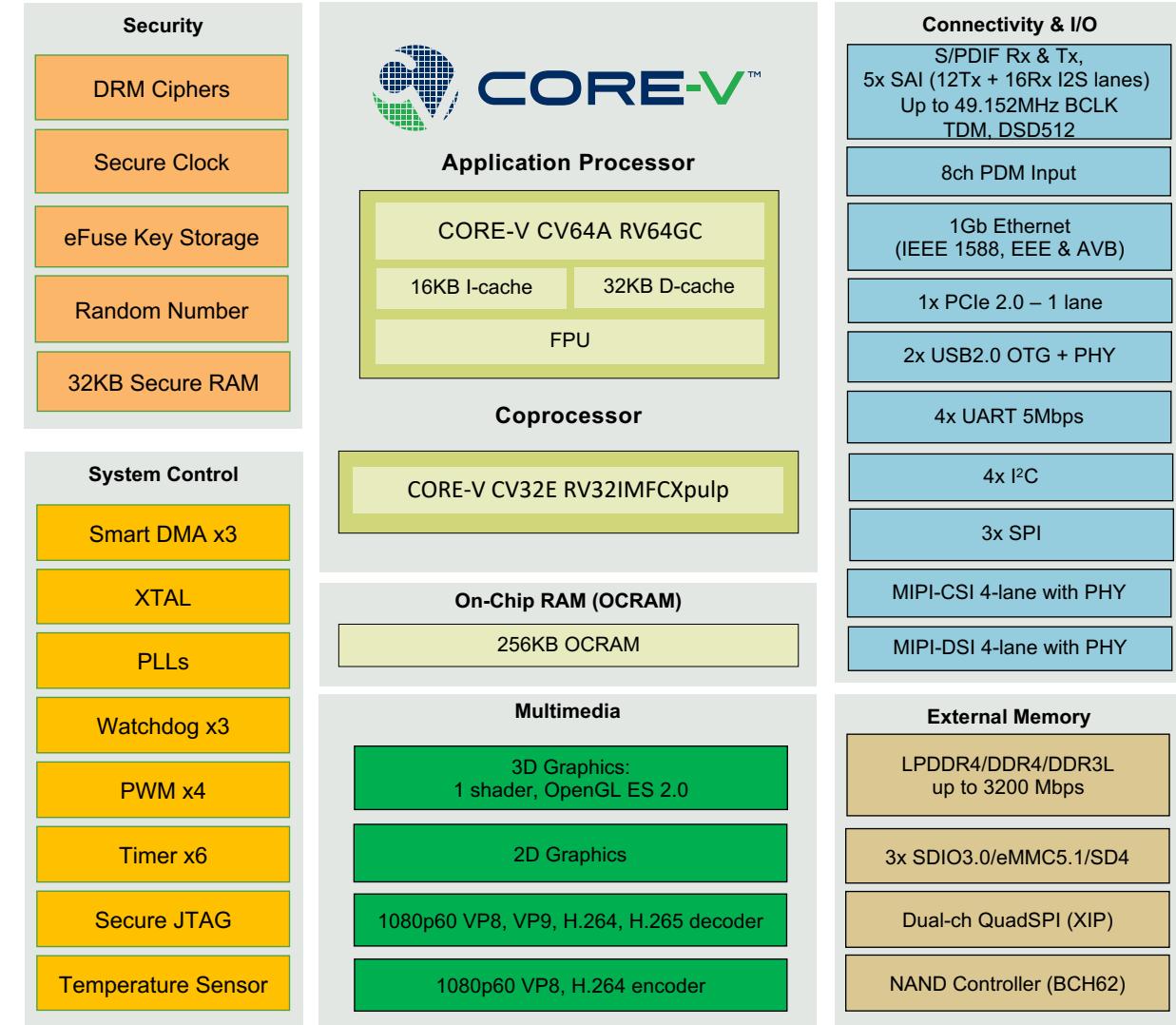
CORE-V™

# Chassis – tapeout 2H 2020



CORE-V Chassis based on NXP iMX Platform CORE-V™

- Linux capable 1.5GHz CV64A host CPU and CV32E coprocessor
- X32/x16 (LP)DDR4, DDR3L memory
- 3D / 2D GPUs with OpenGL support
- MIPI-DSI / CSI display / camera controllers
- Security: DRM Ciphers, key storage, random number generator, etc.
- GigE MAC
- PCIe 2.0 x1 port
- 2 USB 2.0 interfaces
- 3 SDIO interfaces for boot source, storage, etc



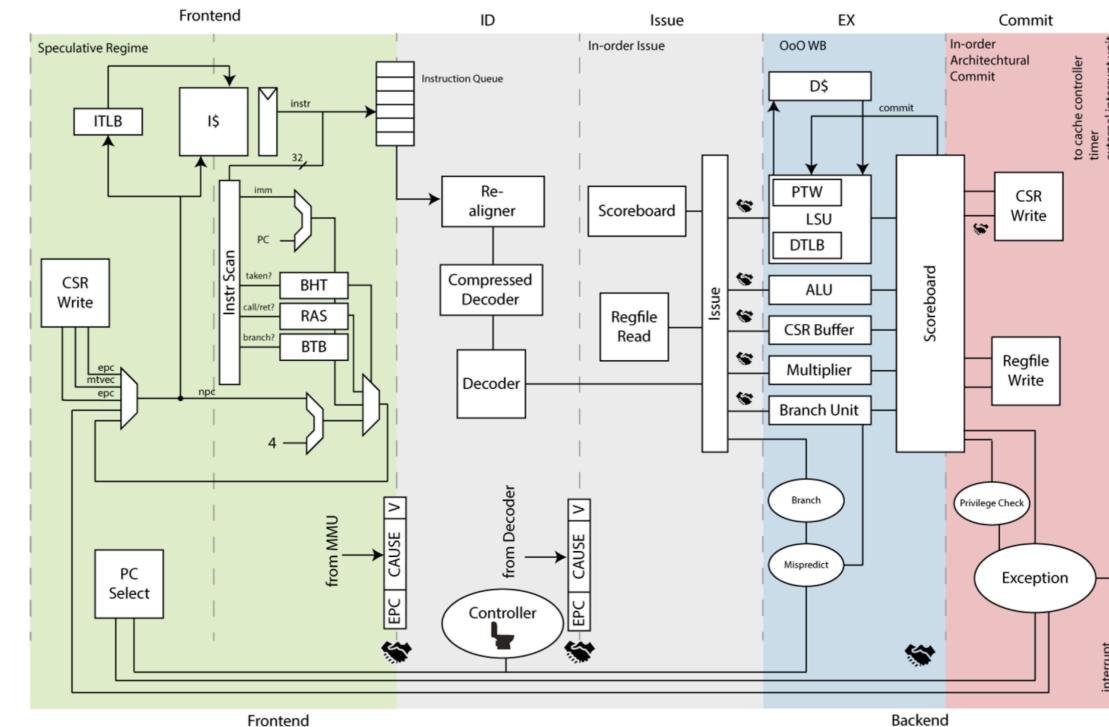


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CV64A Processor IP



- CV64A application 64bit RV64GC processor core IP (Ariane core)
- Linux Capable
  - Tightly integrated D\$ & I\$
  - M, S & U privilege modes
  - TLB, SV39
  - Hardware PTW
- Optimized for performance
  - Frequency: 1.5GHz
  - Area:~175kGE
  - Critical path: ~25 logic levels



- 6-stage pipeline
  - In-order issue
  - Out-of-order write-back
  - In-order commit

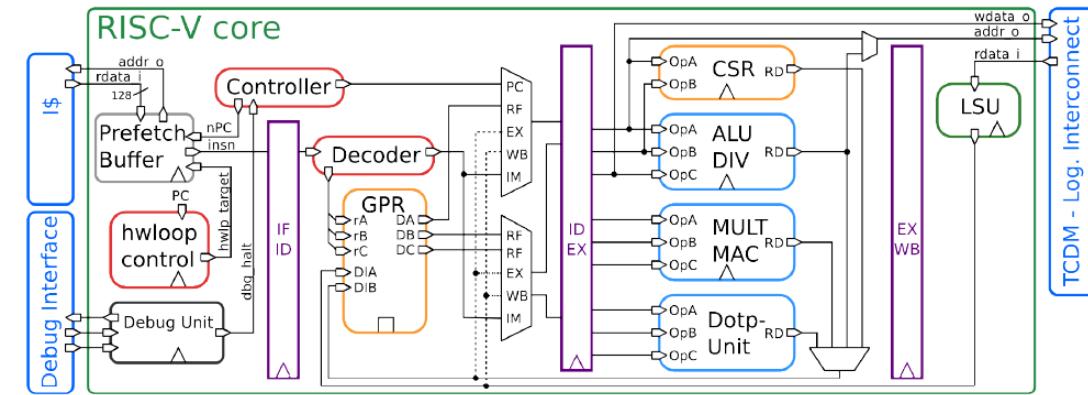


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# CV32E Processor IP



- CV32E embedded 32bit RV32IMFCXpulp processor core IP (RI5CY core)
  - 4-stage pipeline
  - 70K GF22 nand2 gate equivalents gate + 30KGE for FPU
  - Coremark/MHz 3.19
- Includes various extensions
  - pSIMD, Fixed point, Bit manipulations, HW loops
- Silicon Proven
  - SMIC130, UMC65, TSMC55LP, TSMC40LP, GF22FDX



- Floating Point Unit
  - Iterative DIV/SQRT (9 cycles)
  - Parametrizable latency for MUL, ADD, SUB, Cast
  - Single cycle load, store

# CORE-V™ Chassis Ecosystem



Alibaba Group  
阿里巴巴集团

BTA DESIGN SERVICES  
your project, our team

ETH zürich  
**FUTUREWEI**

GREENWAVES TECHNOLOGIES

HUAWEI

MYTHIC

NXP SILICON LABS

THALES

ultraSOC

VeriSilicon

CORE-V™

CV32 &  
CV64  
Cores

System  
Verilog RTL

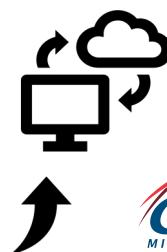


IBM Cloud  
bluespec  
imperas  
metrics

Cloud Based  
Verification



RTL Simulation  
Formal Methods  
Stimulus



CMC  
MICROSYSTEMS

Alibaba Group  
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HUAWEI

EMBEDCOSM®

GREENWAVES TECHNOLOGIES

NXP

SILICON LABS

Security	Connectivity & I/O
CMC Clock	SD SPI (1/2x), VBUS (2x) (raw)
Secure Clock	100MHz, 200MHz, TDM, DSDR2
Random Number	1000s/sec
32Bit Secure RAM	16bit (IEEE 1394, AUI)
System Control	PCIe (2.0 - 3.0)
SmartClock	PCIe Gen 3.0
RTAI	PCIe Gen 2.0
PLLs	PCIe Gen 1.0
Watchdog	PCIe Gen 1.0
PEM41	PCIe Gen 1.0
Tunnel	PCIe Gen 1.0
Processor	PCIe Gen 1.0
Memory	PCIe Gen 1.0
Secure TAG	PCIe Gen 1.0
Temperature Sensor	PCIe Gen 1.0
Processor	External Memory
CORE-V CPU	LPDDR4/DDR4/DDR3
CORE-V CV32 RV32IMC CPUip	1Gb DRAM
On-Chip RAM (ROM/RAM)	2MB OROM
2MB ORAM	2MB ORAM
Multimedia	3D Graphics, Camera, Display, 3D Stereo
3D Graphics	3D Graphics
Camera	1080P, 30fps, 12.0MP sensor
Display	Virtual GPU, H.264 encoder
Temperature Sensor	Temperature Sensor

GCC /  
LLVM &  
OS ports

Device  
Under  
Test

MPW  
Layout &  
Fab

VeriSilicon

Eval  
Boards



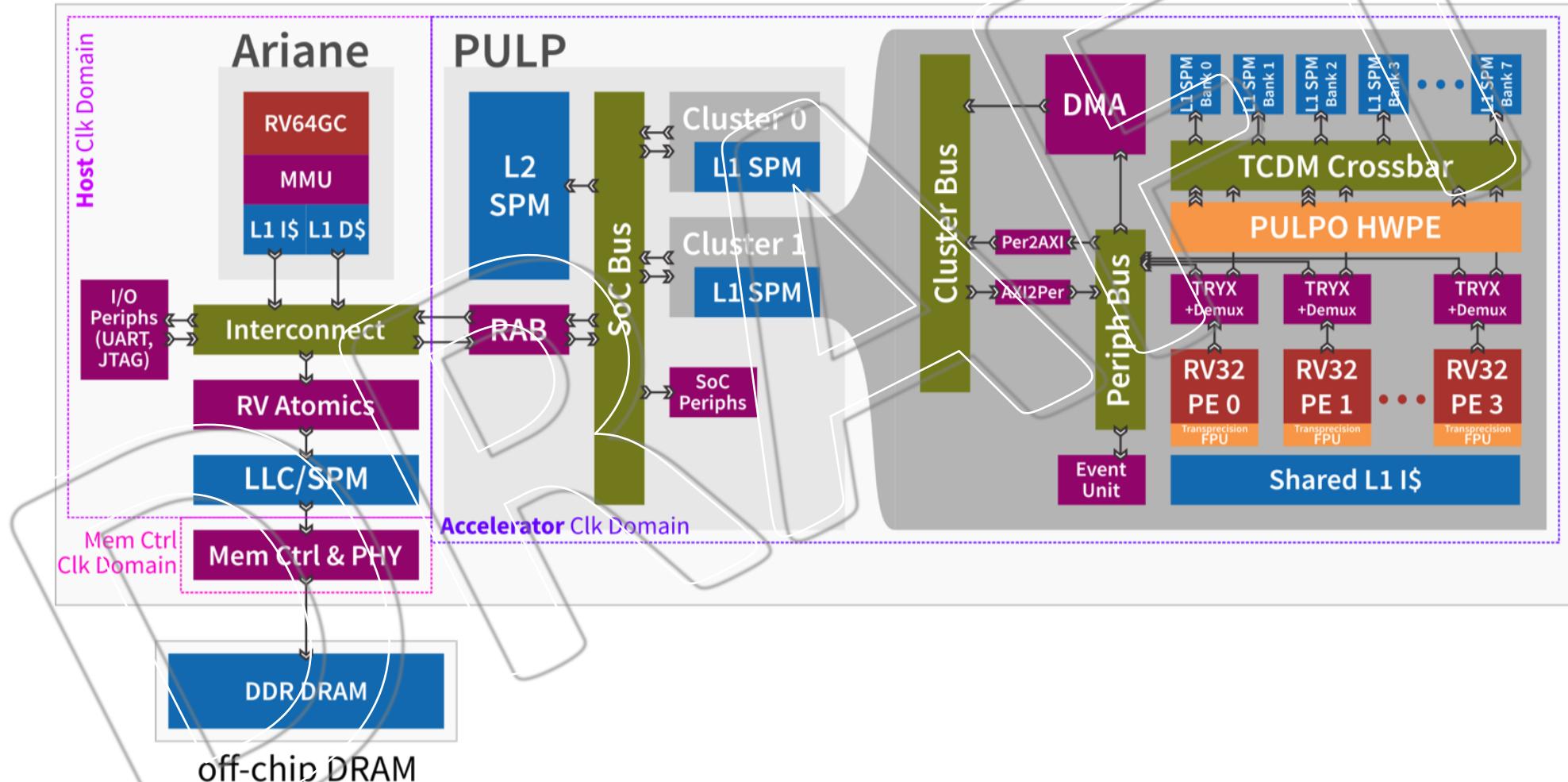
CORE-V Chassis  
Protos

CMC  
MICROSYSTEMS NXP

ultraSOC

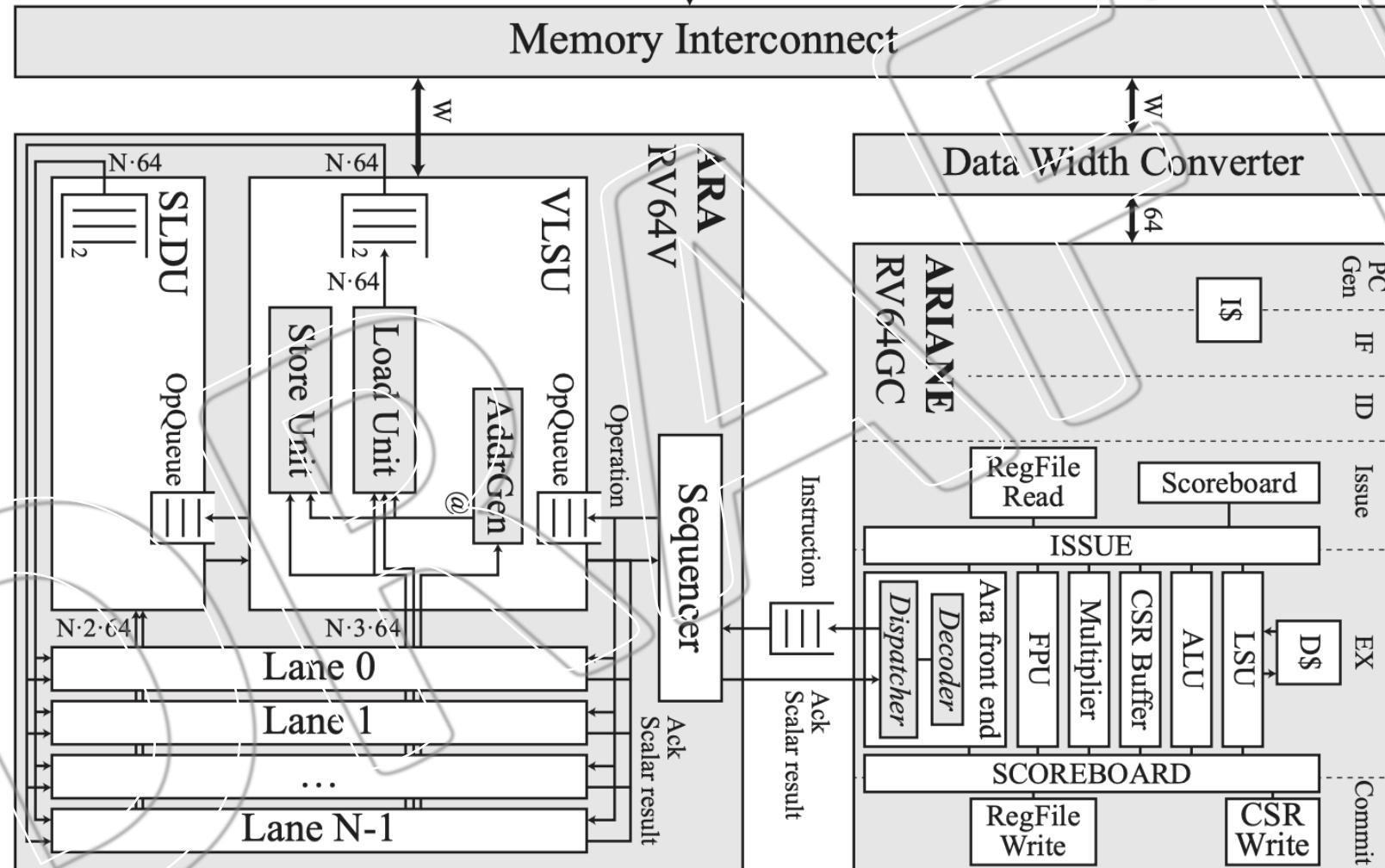


# CORE-V™ Chassis - Possible Processor Complex – CV64 + CV32 cluster





# CORE-V™ Chassis - Possible Processor Complex - CV64A + CV64V Vector Core



# CORE-V Chassis – Call for Participation



- Join the OpenHW Group to drive the CORE-V Chassis project
  - CV64A and CV32 verification test bench
  - CV64A bus interfaces and cache coherency support
  - CV64A IPC improvements
  - CV64A and CV32E OS porting / development environment
  - ... and more ...