

**School of Electronics Engineering (SENSE)**

**VIT Chennai**

**VLSI Make-a-thon Report (E1 Slot)**

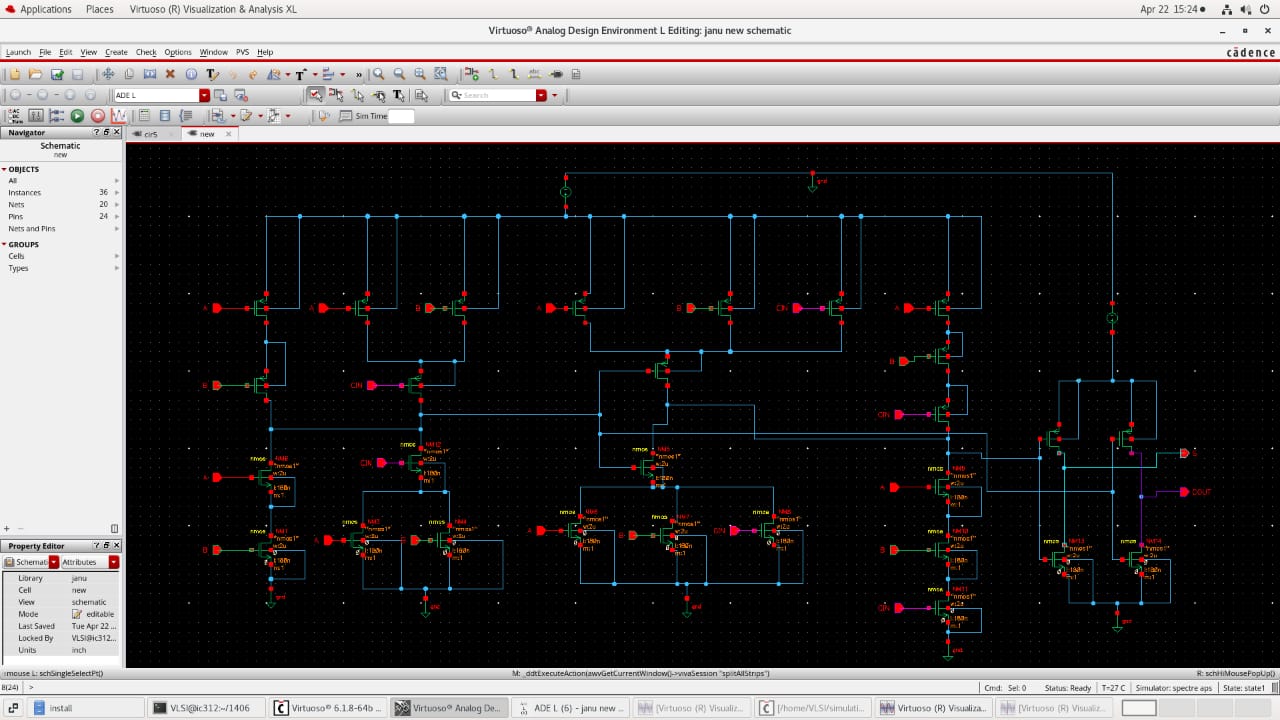
**GROUP 11**

**Team members:**

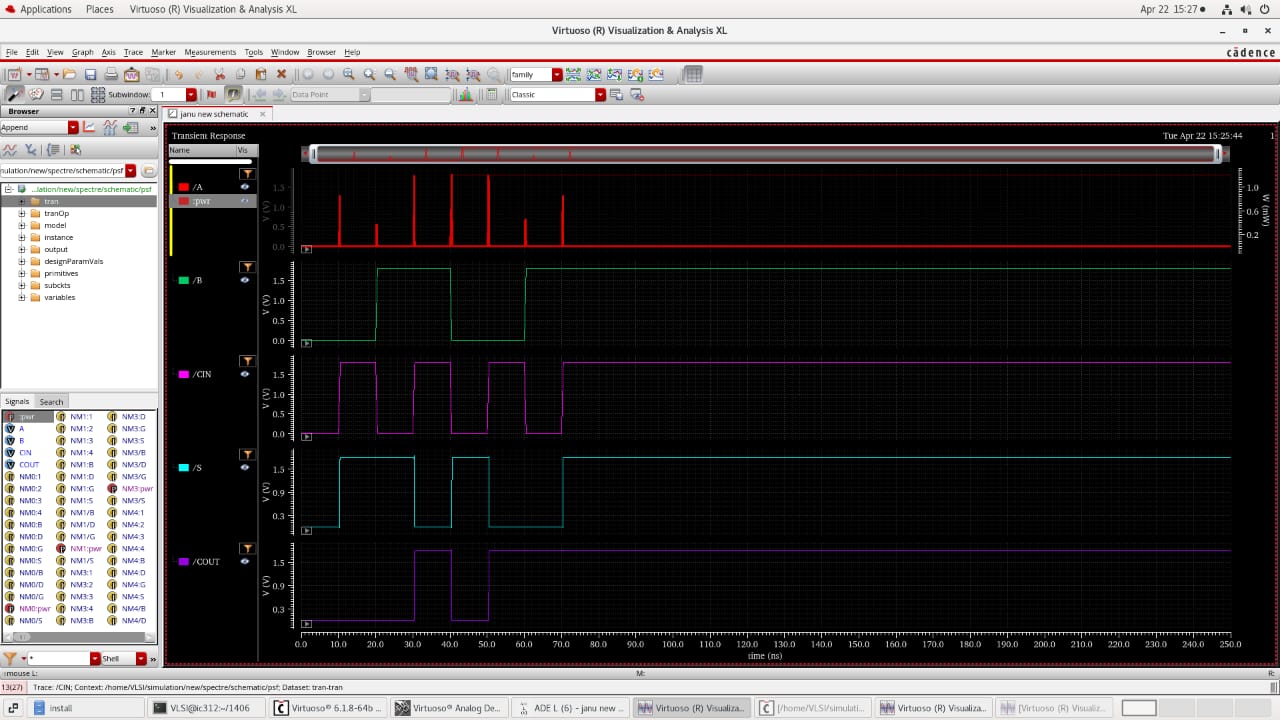
* **23BEC1451 - R Prateek**
* **23BEC1406 – VL Janani**
* **23BEC1460 – Suvishesh D**

1. **CIRCUIT 01**

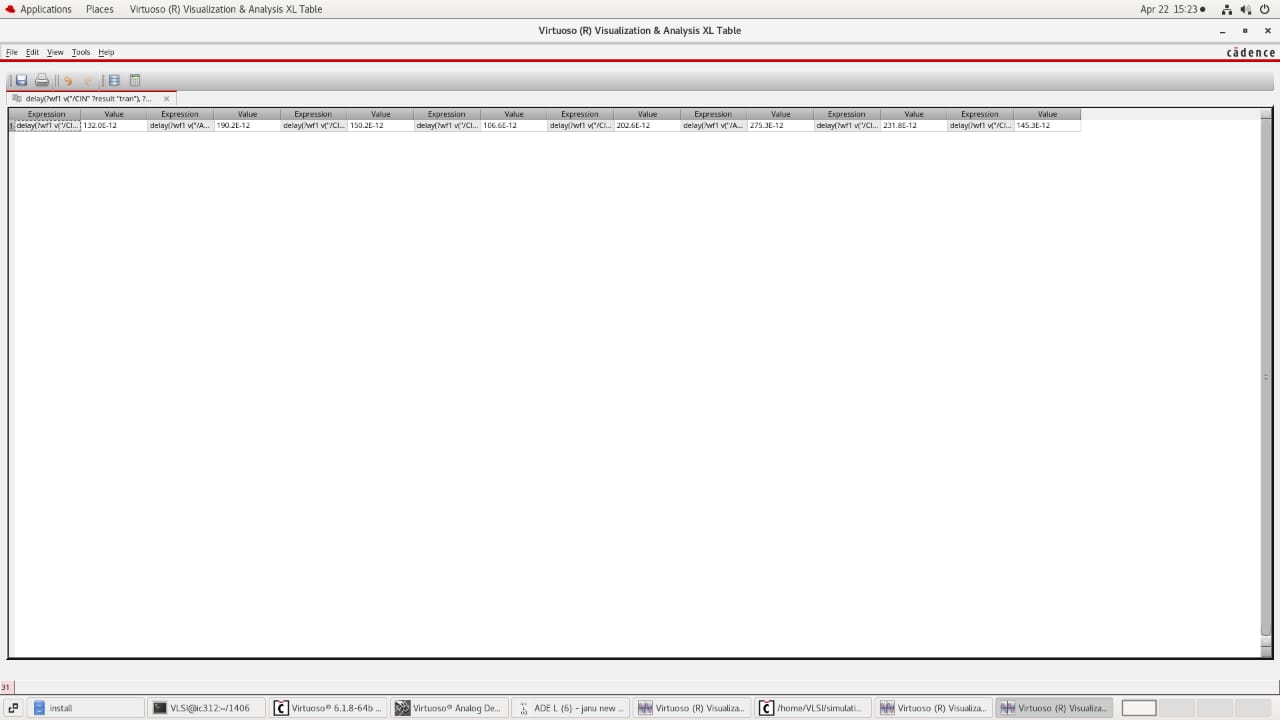
**Schematic:**

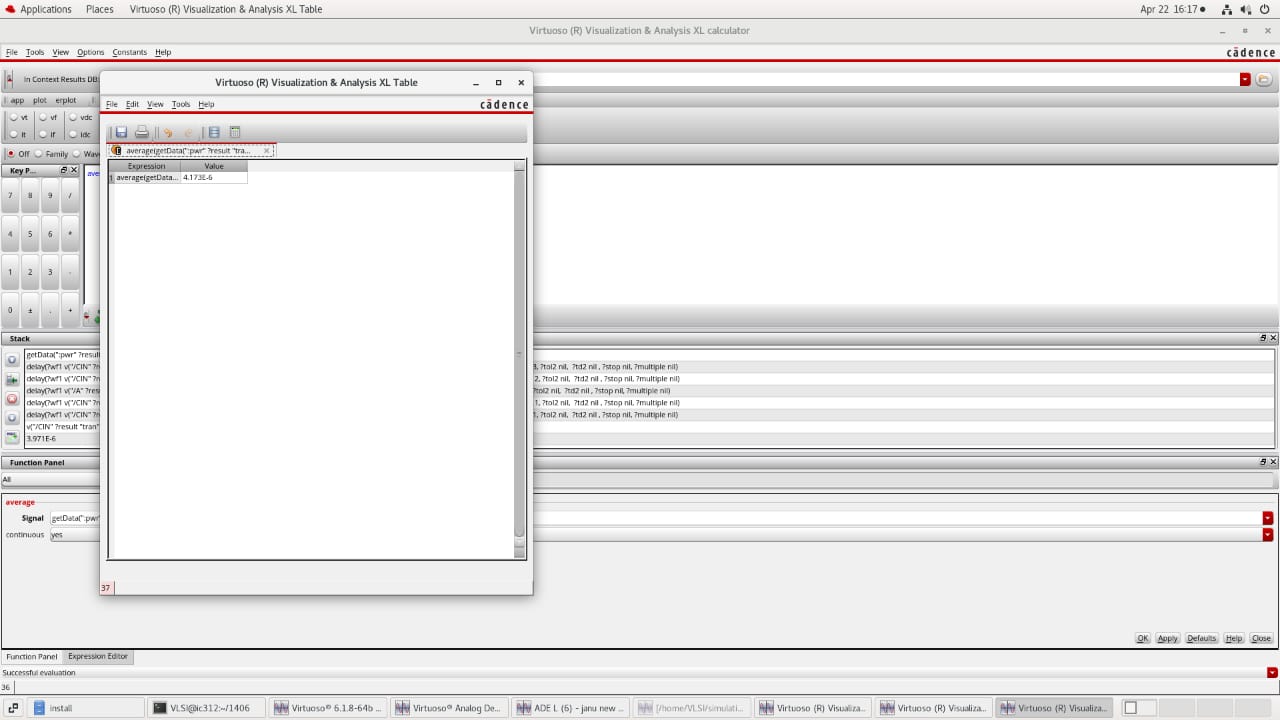


**Output Waveform:**

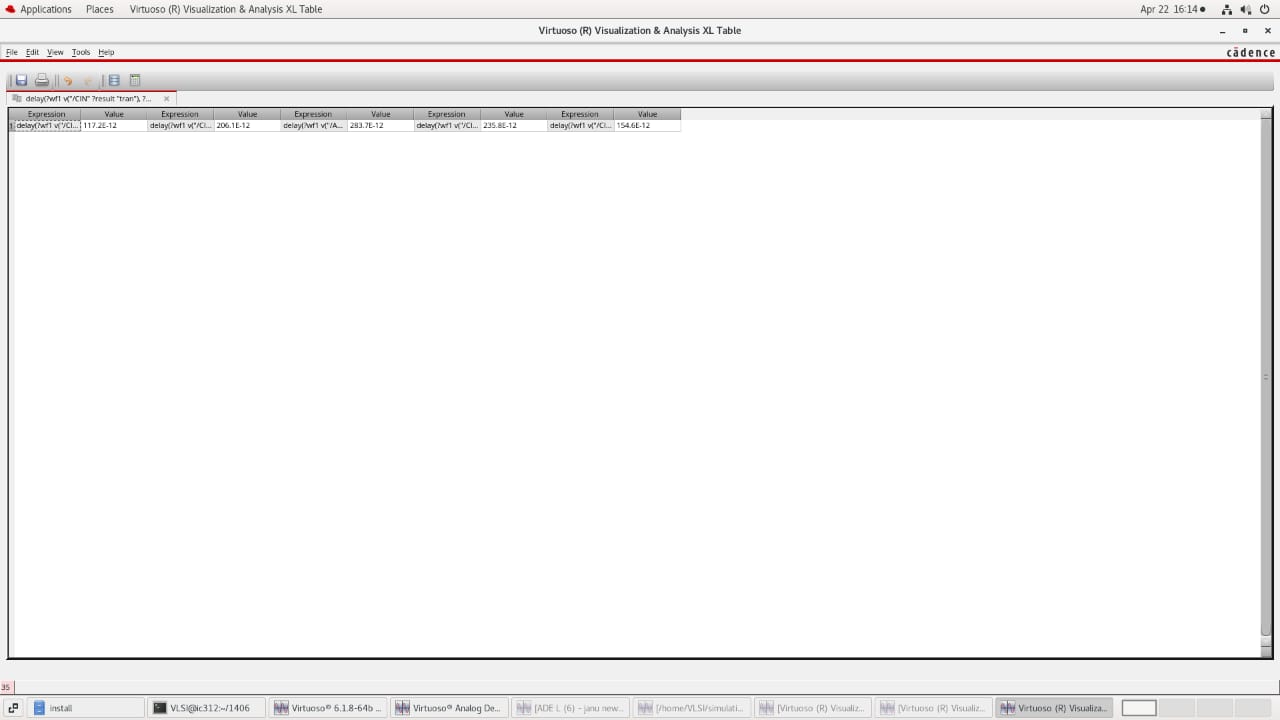


**Delay & Power Calculations (Pre-Sizing)**



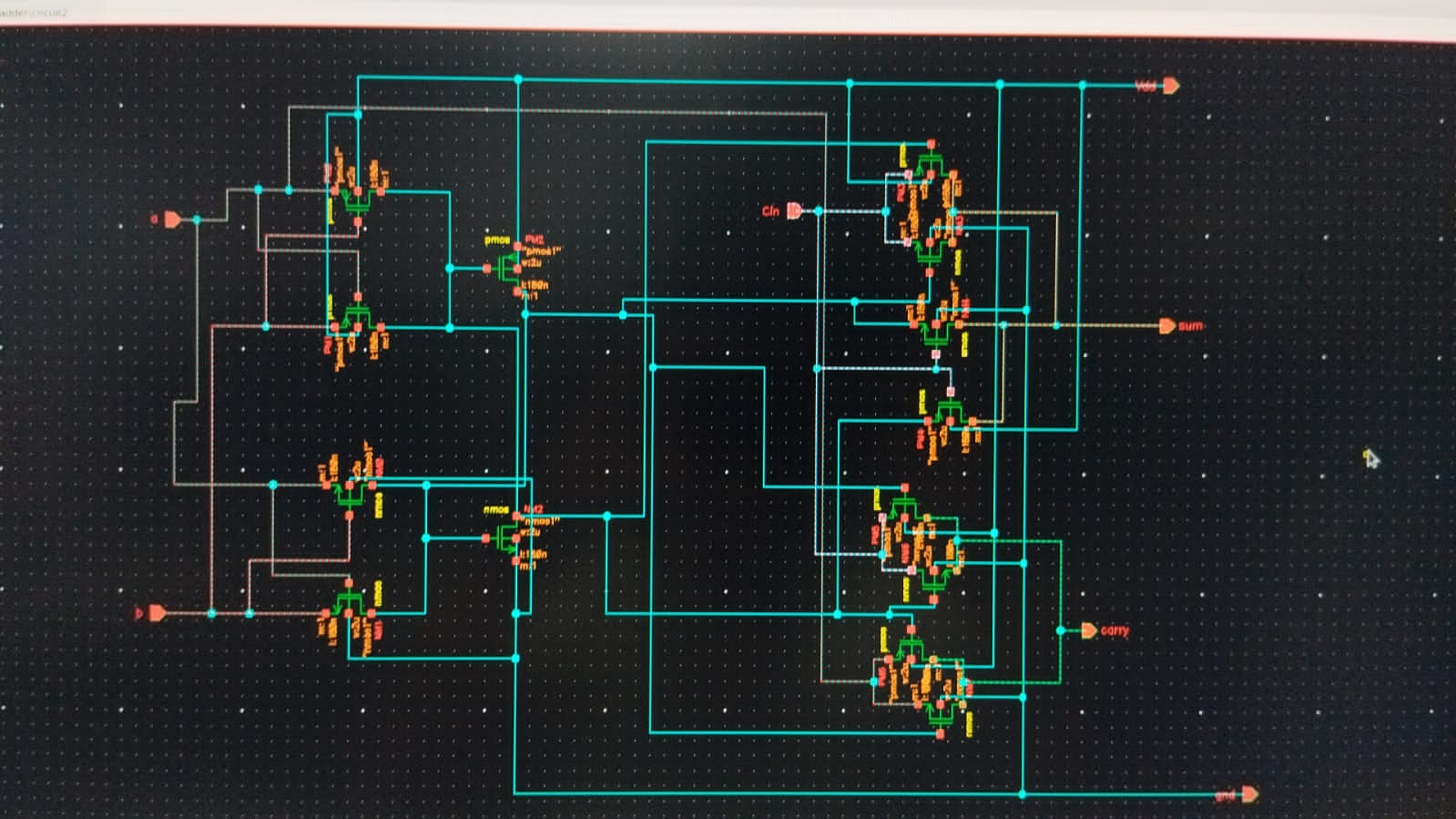


**Delay Calculations (Post-Sizing)**



**Inference: Max delay is R1A & R2S – 301.4 x 10^(-12)**

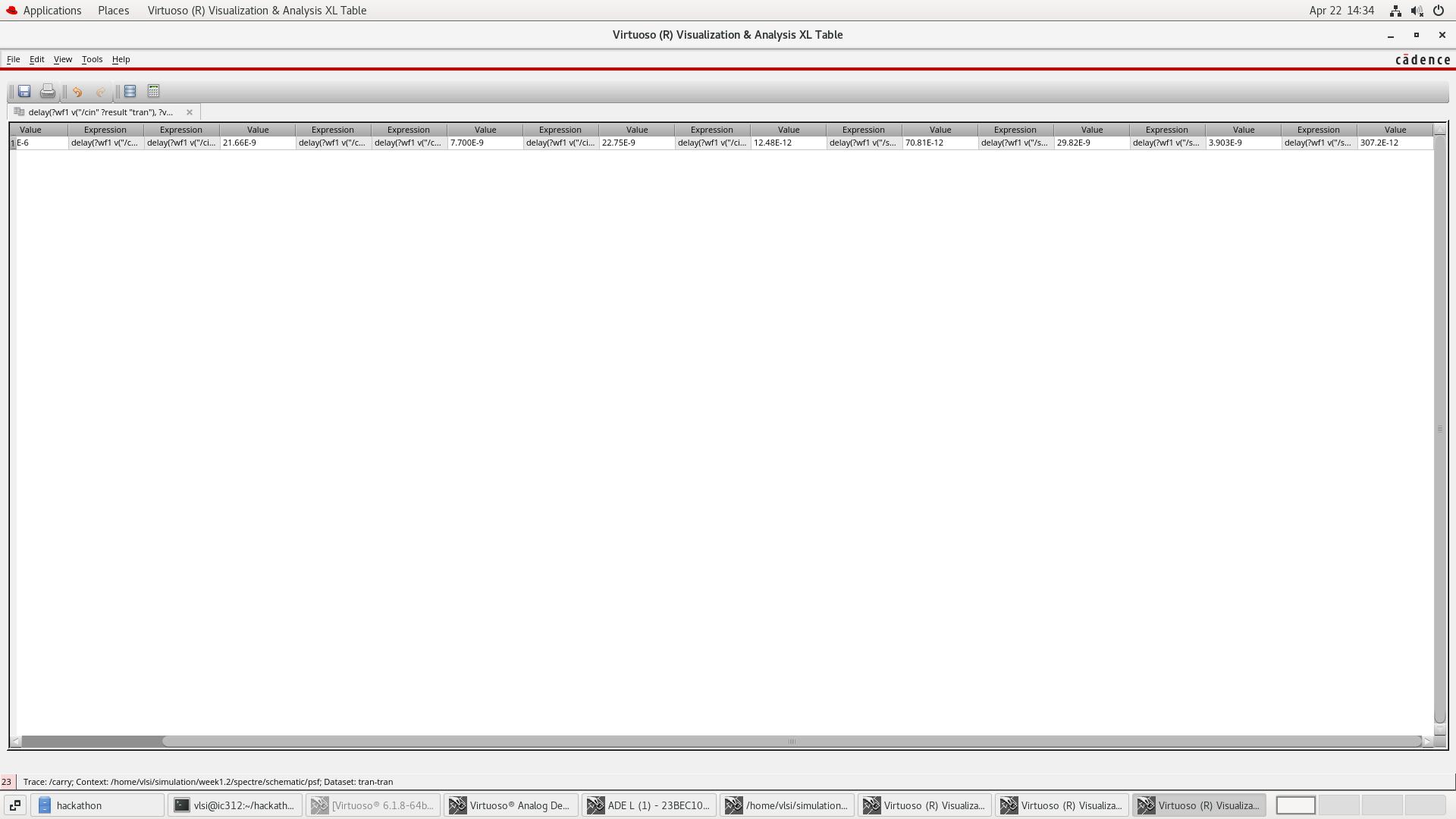
1. **Circuit 02**

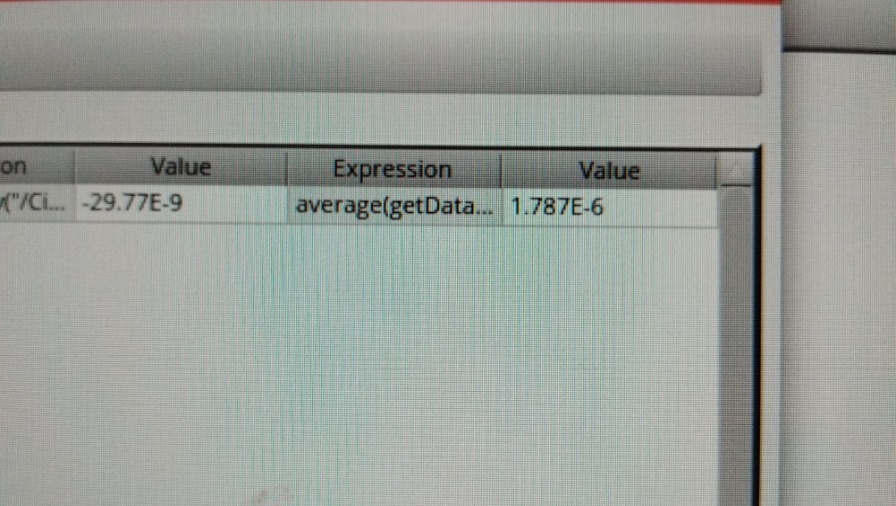


**Output waveform:**

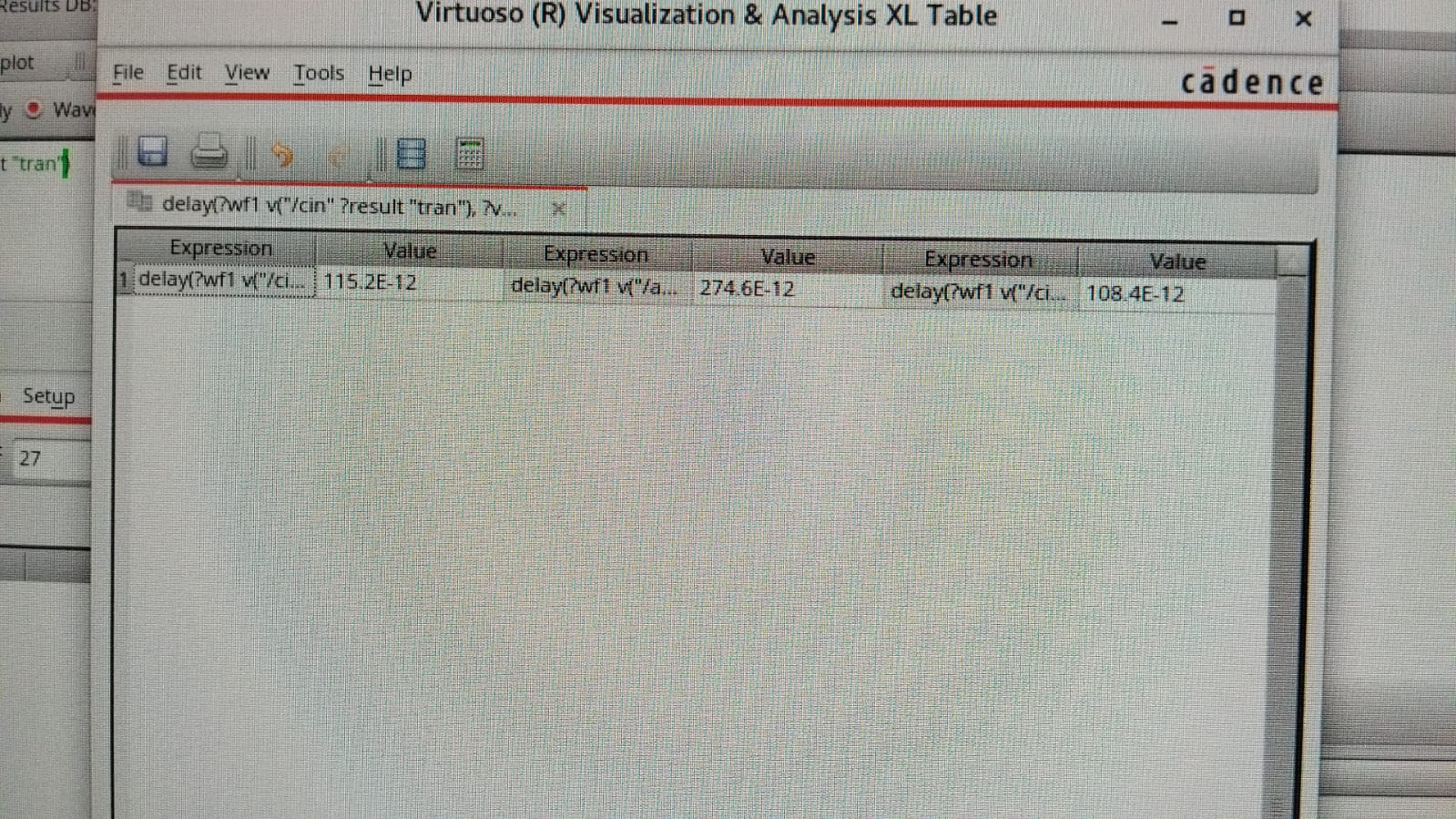


**Delay & Power Calculations (Pre-Sizing)**





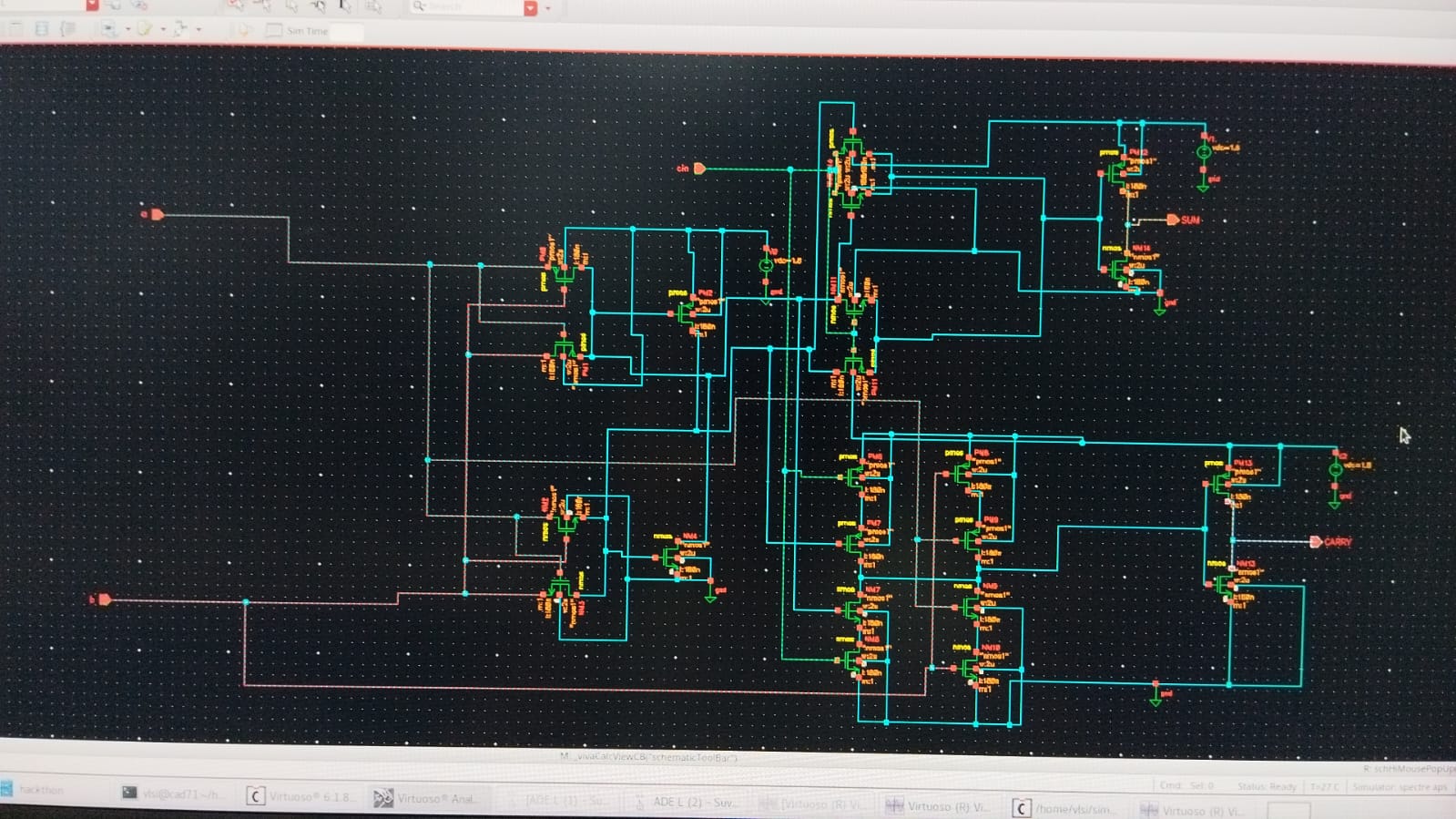
**Delay Calculations (After Sizing)**



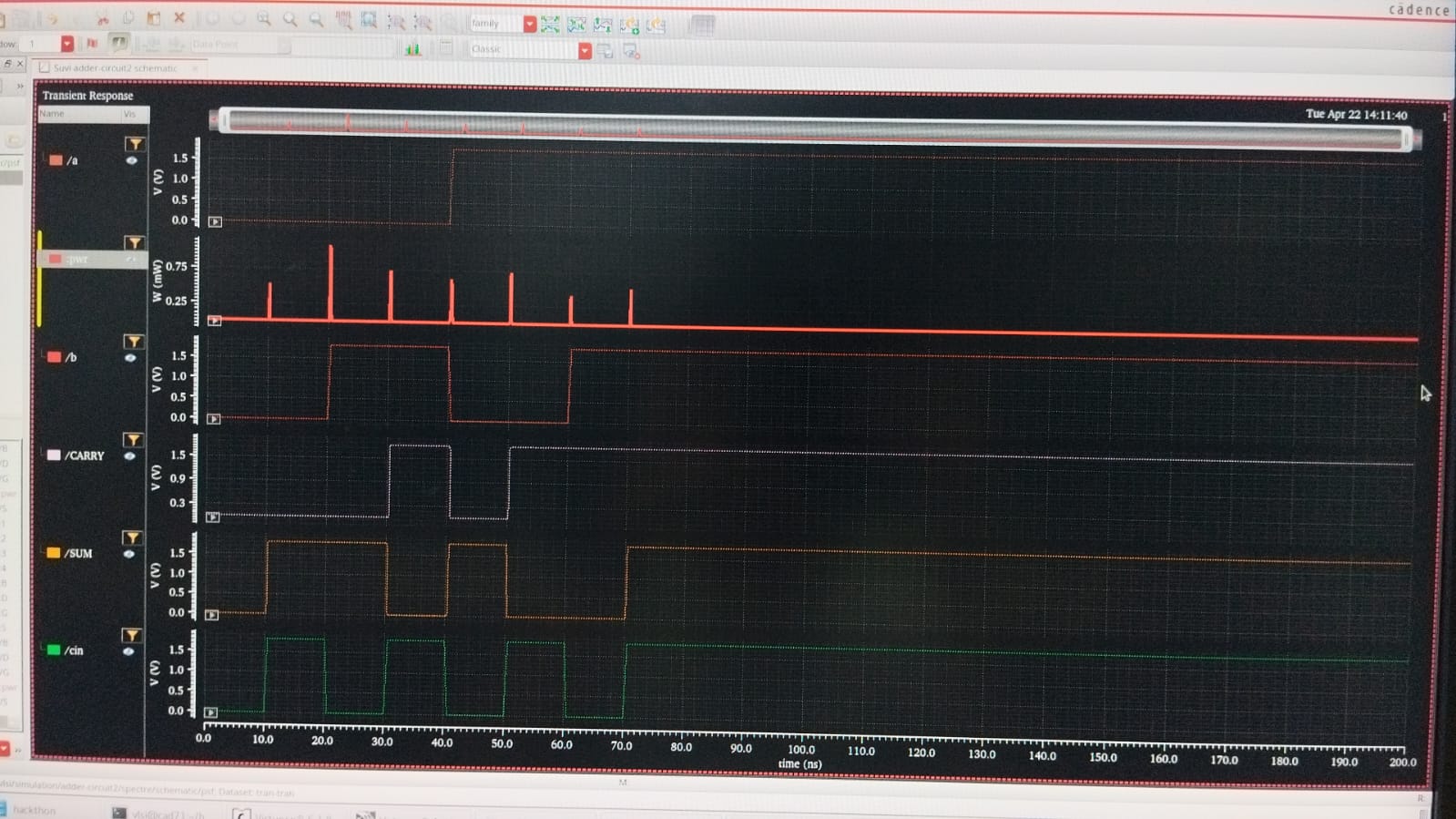
**Inference: Max Delay is R4Cin & R3S – 29.77 x 10^(-9)**

1. **Circuit 03**

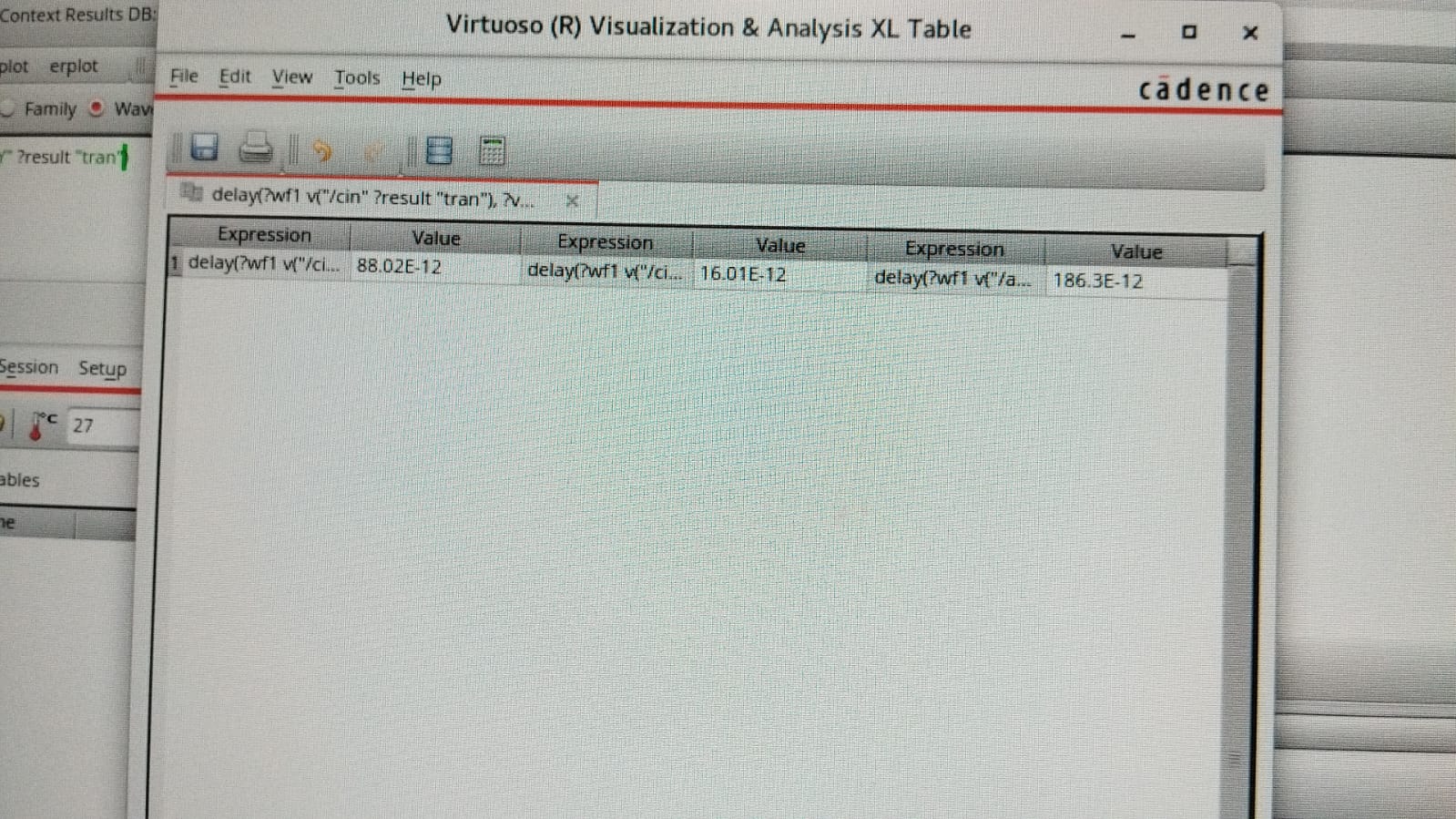
**Schematic:**

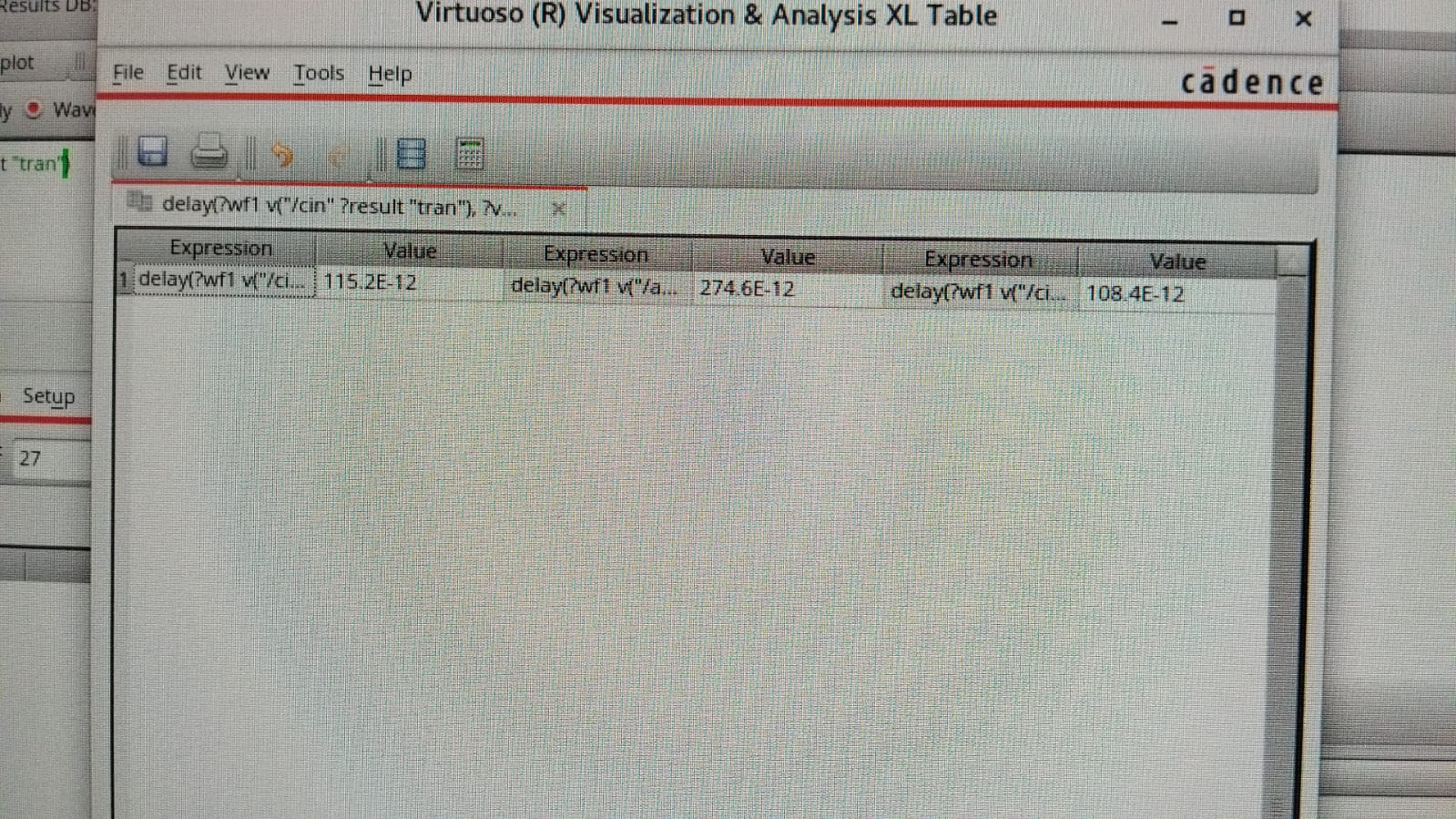


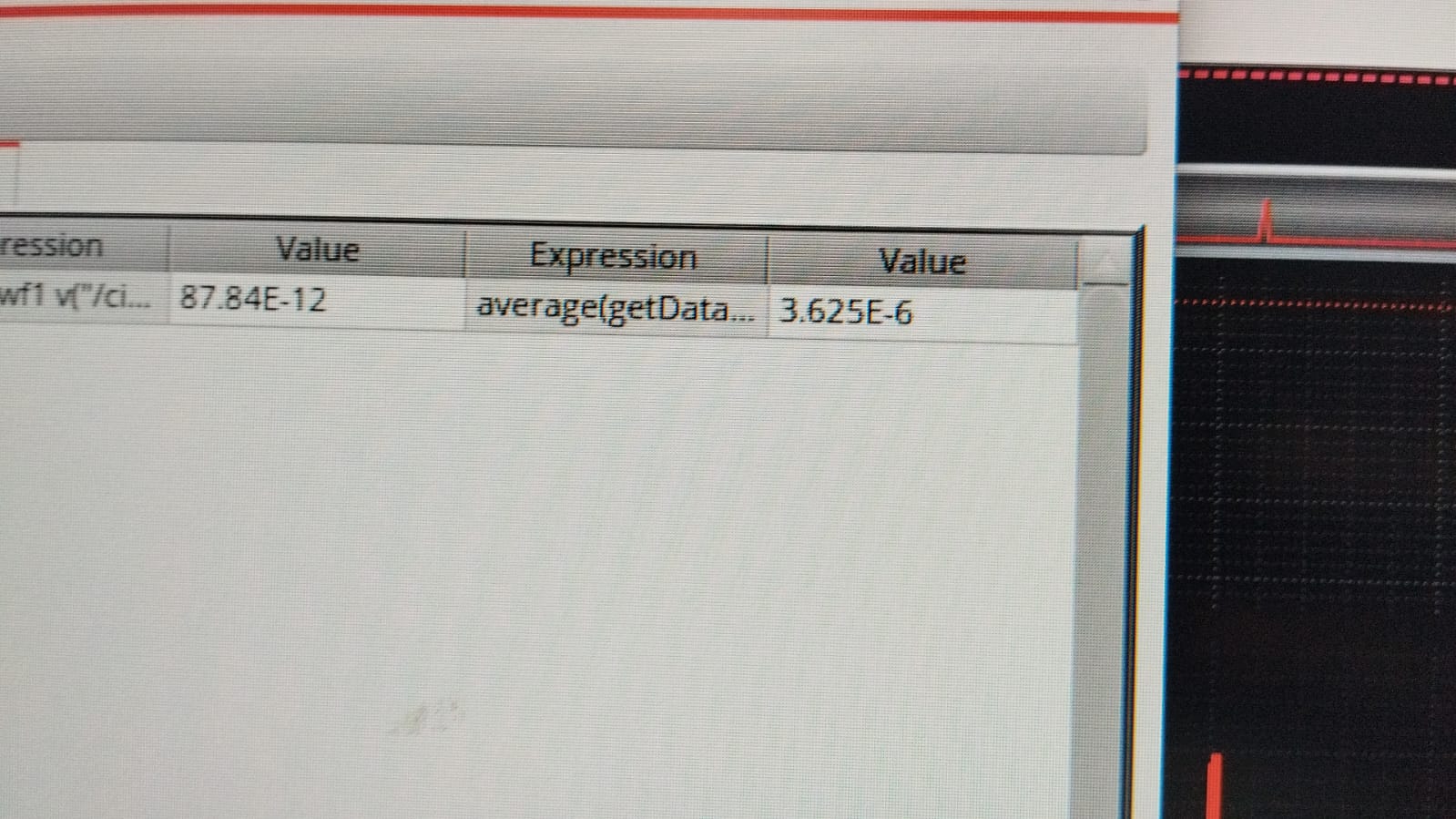
**Output Waveform:**



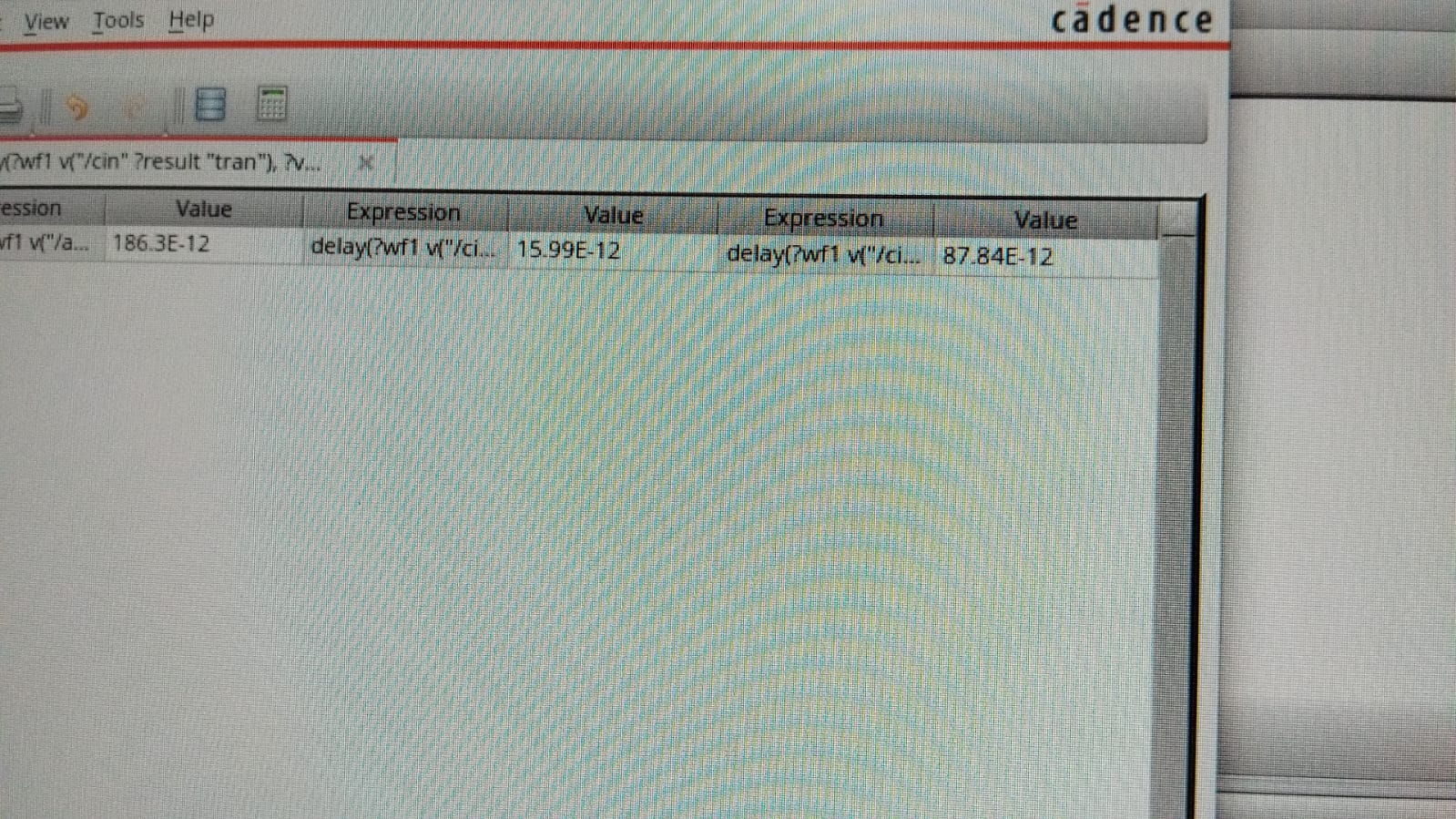
**Delay & Power Calculations (Pre-Sizing)**







**Delay Calculations (Post – Sizing)**

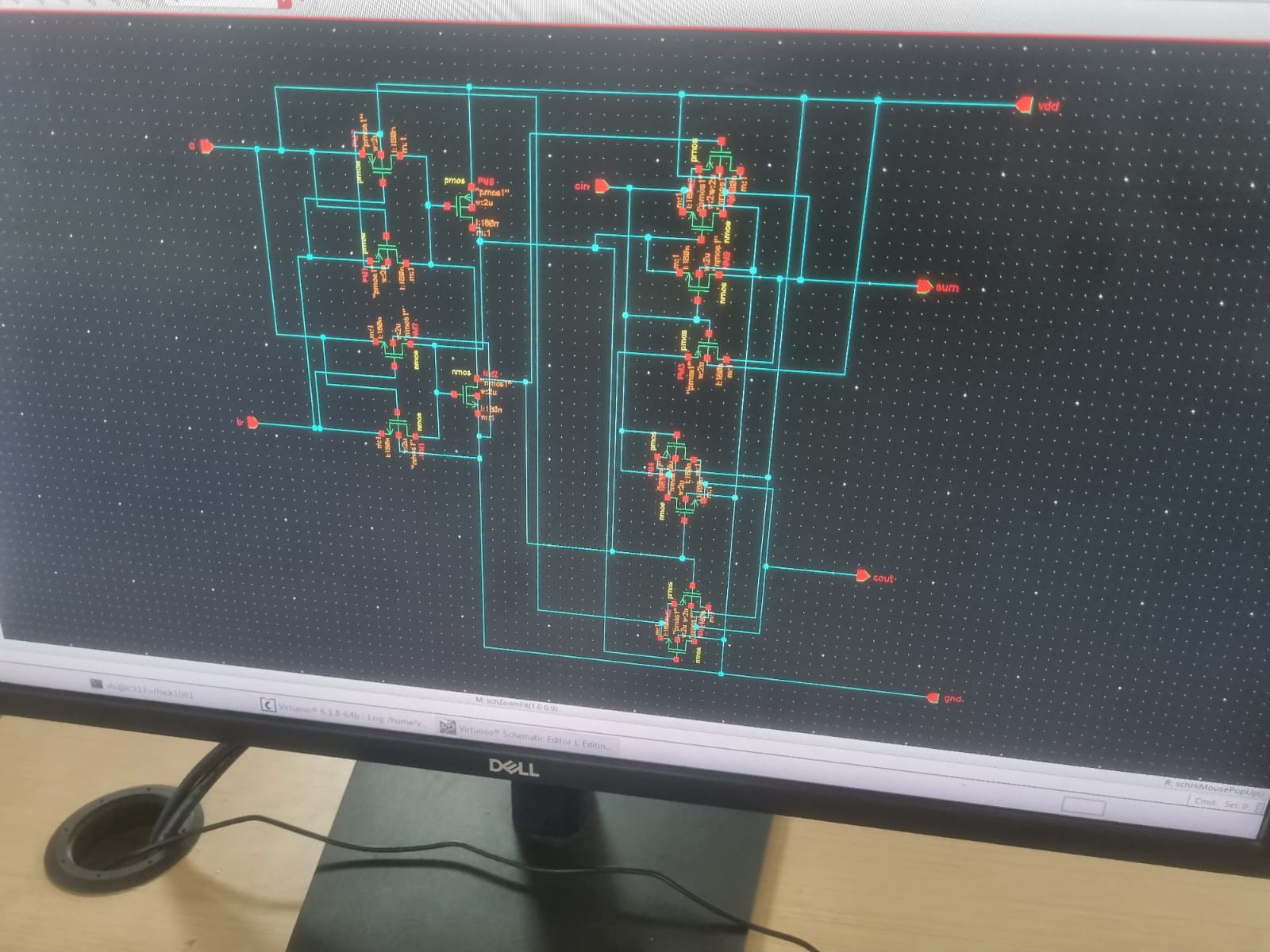


**Inference: Max Delay is R1A & F1Co – 274.6 x 10^ (-12)**

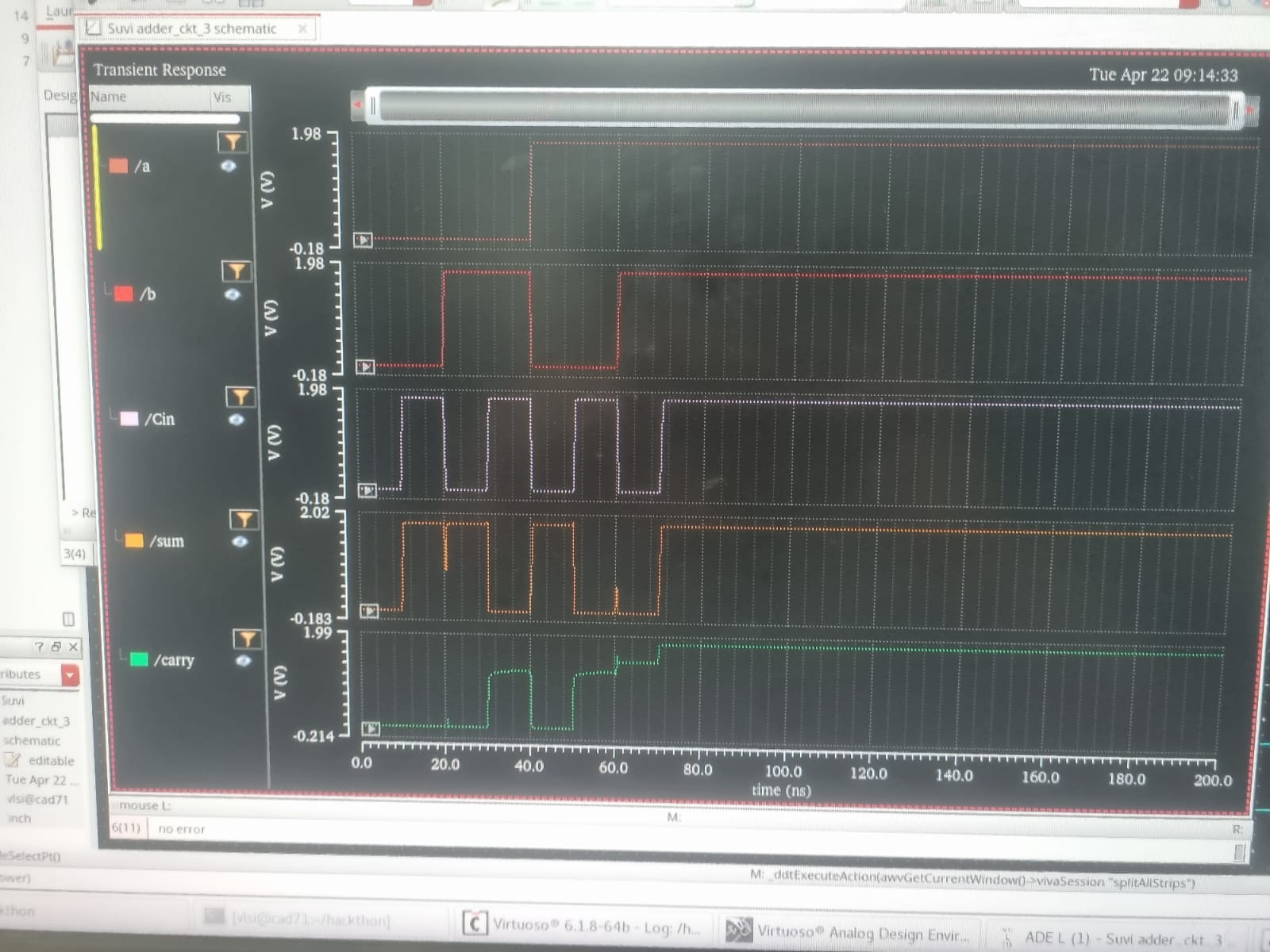
Circuit 03 was found to have the least maximum delay amongst all the full-adder circuits, so its symbol was created and was further used to implement the 4-bit multiplier.

1. **Circuit 04**

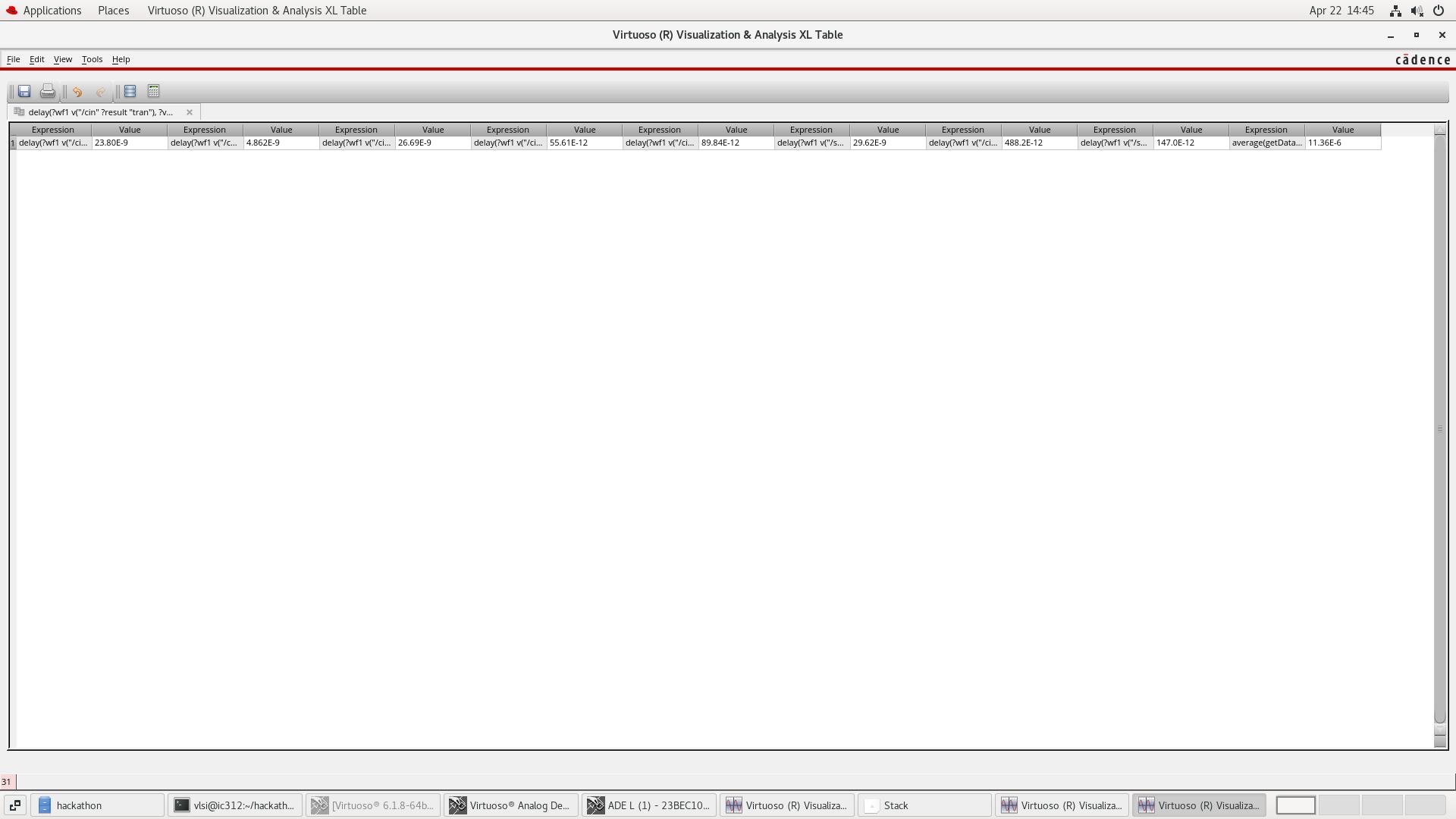
**Schematic:**



**Output waveform:**

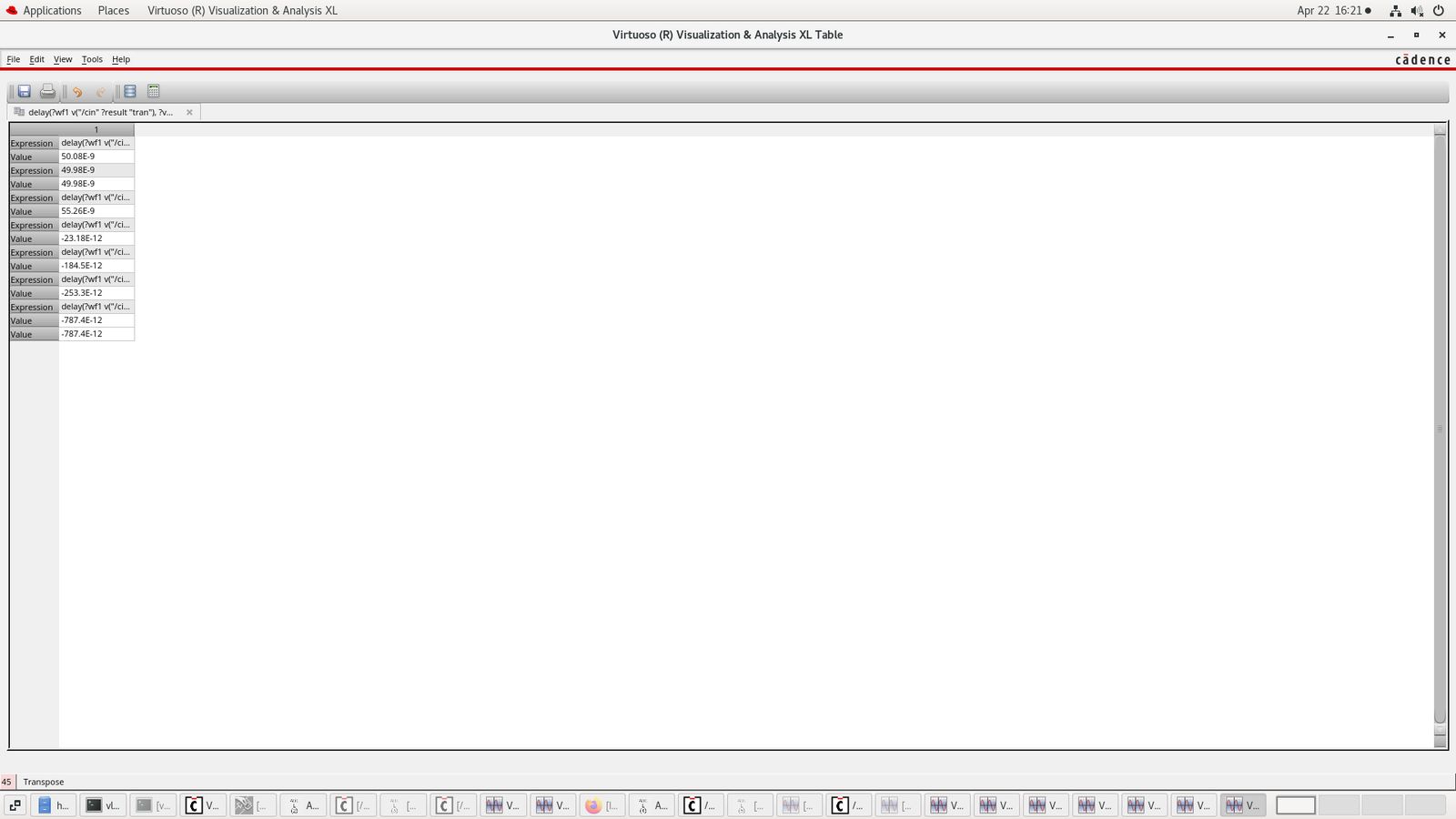


**Delay Calculations & Power (Pre-Sizing)**



**Power: 81.89 x 10^ (-6)**

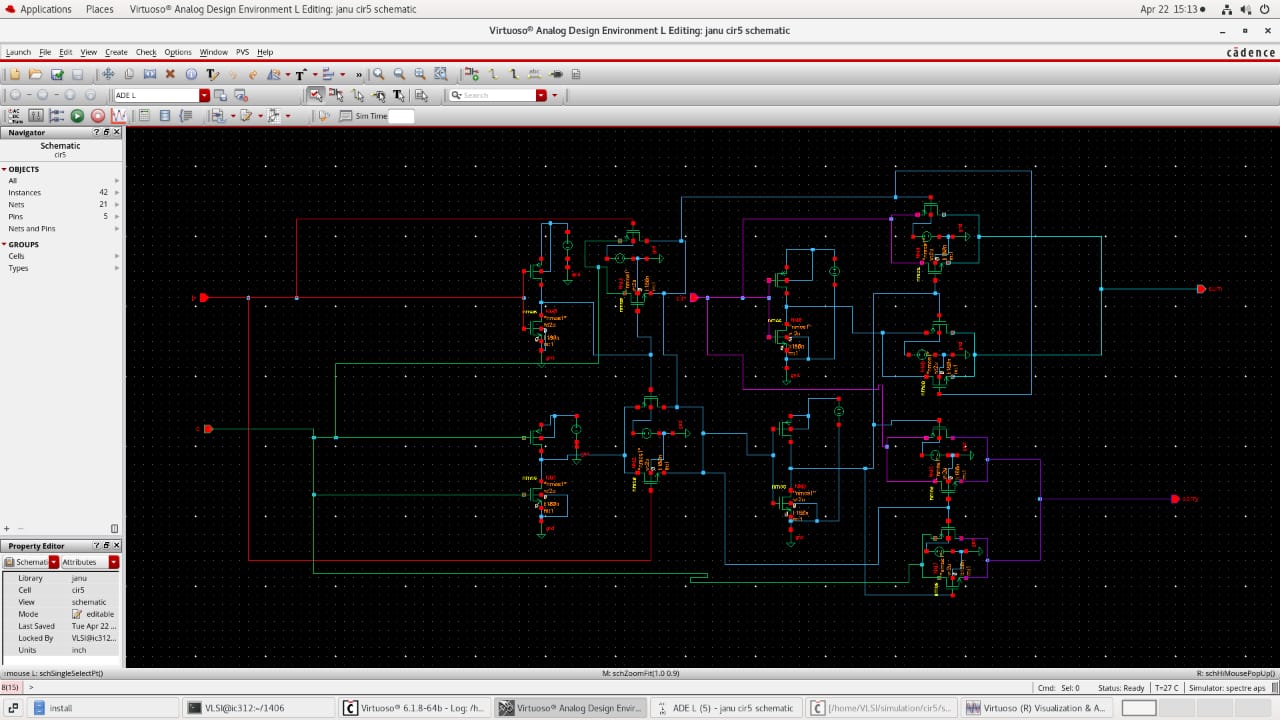
**After Sizing:**



**Inference: Max Delay is R4Cin & R3S – 29.76 x 10^ (-9)**

1. **CIRCUIT 05**

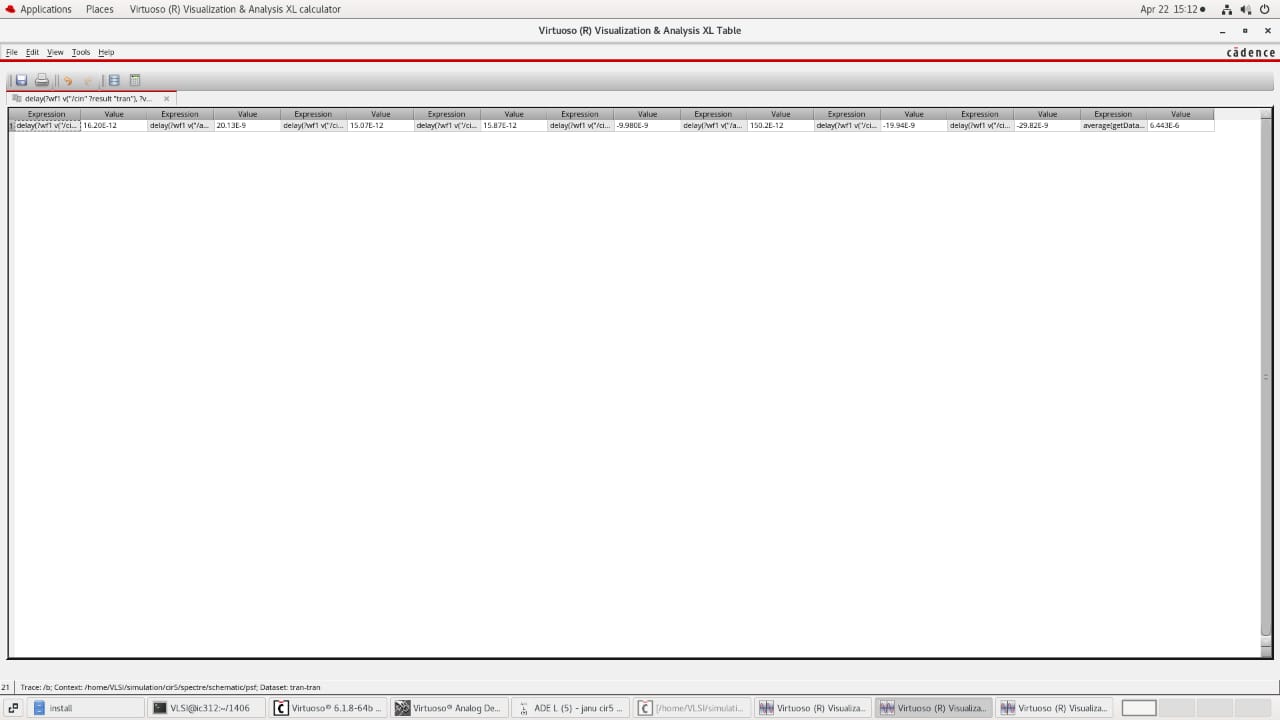
**SCHEMATIC:**

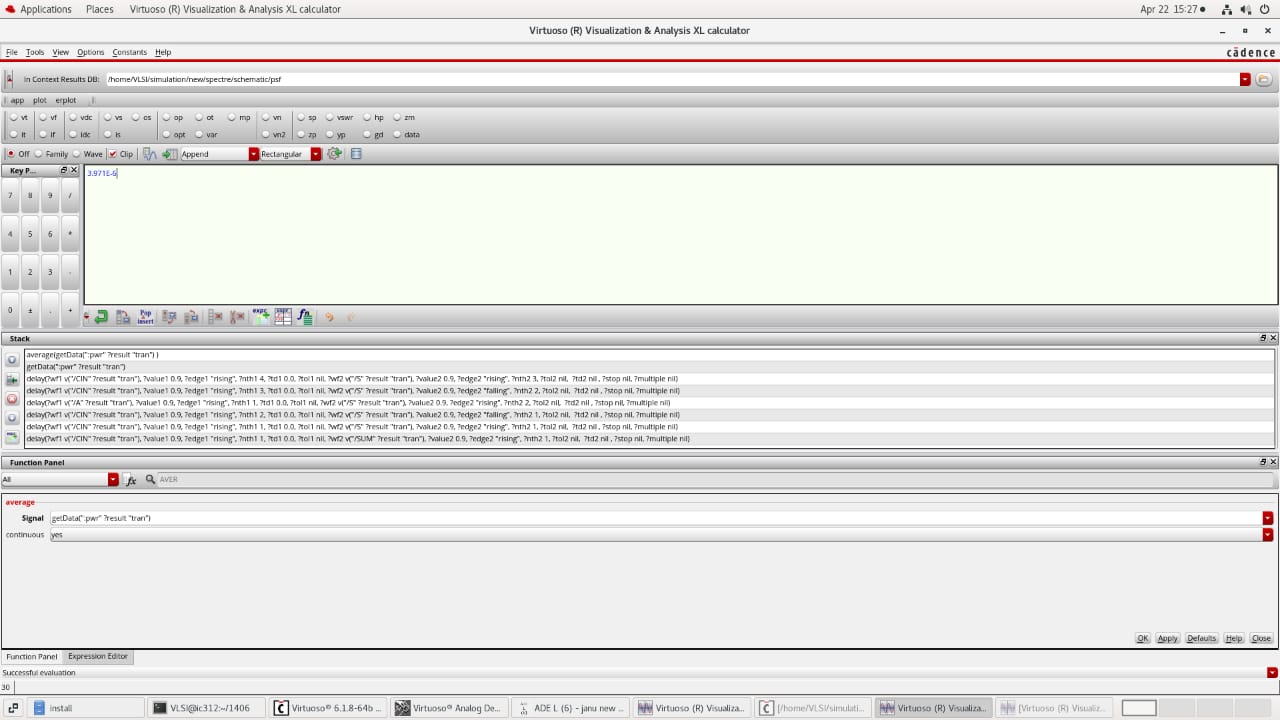


**OUTPUT WAVEFORM:**

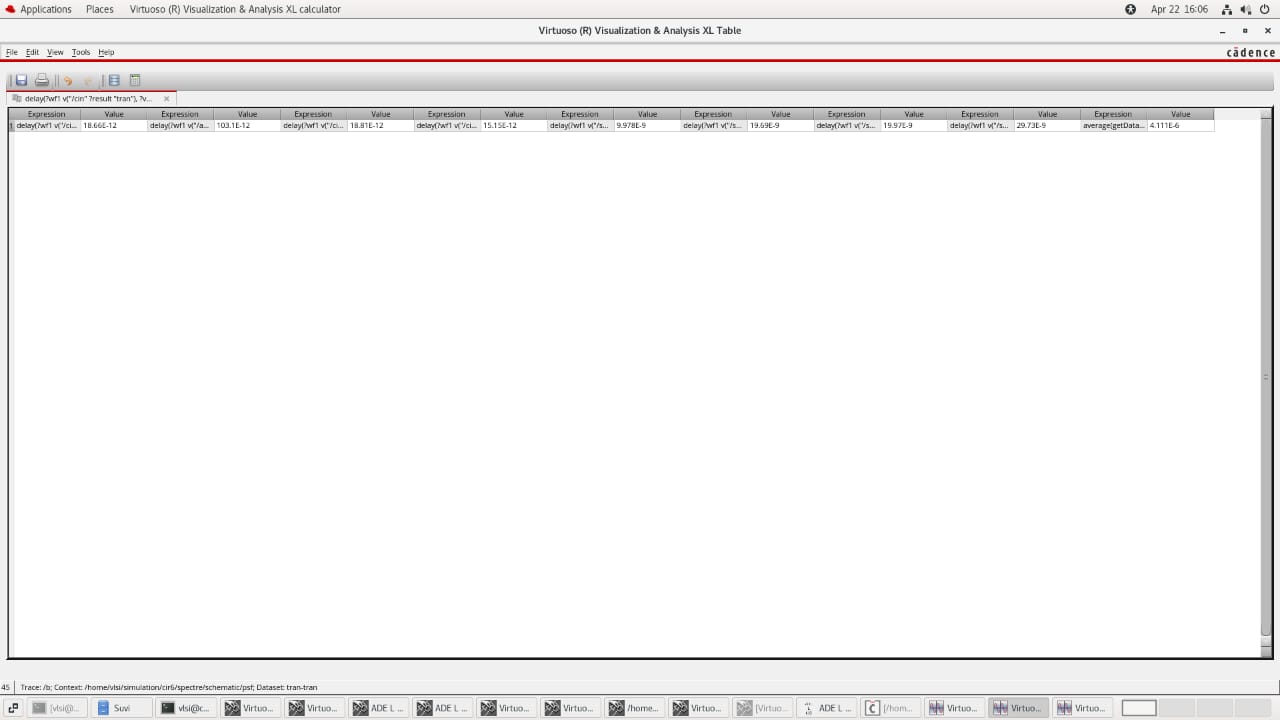


**DELAY & POWER CALCULATIONS (Pre-Sizing):**





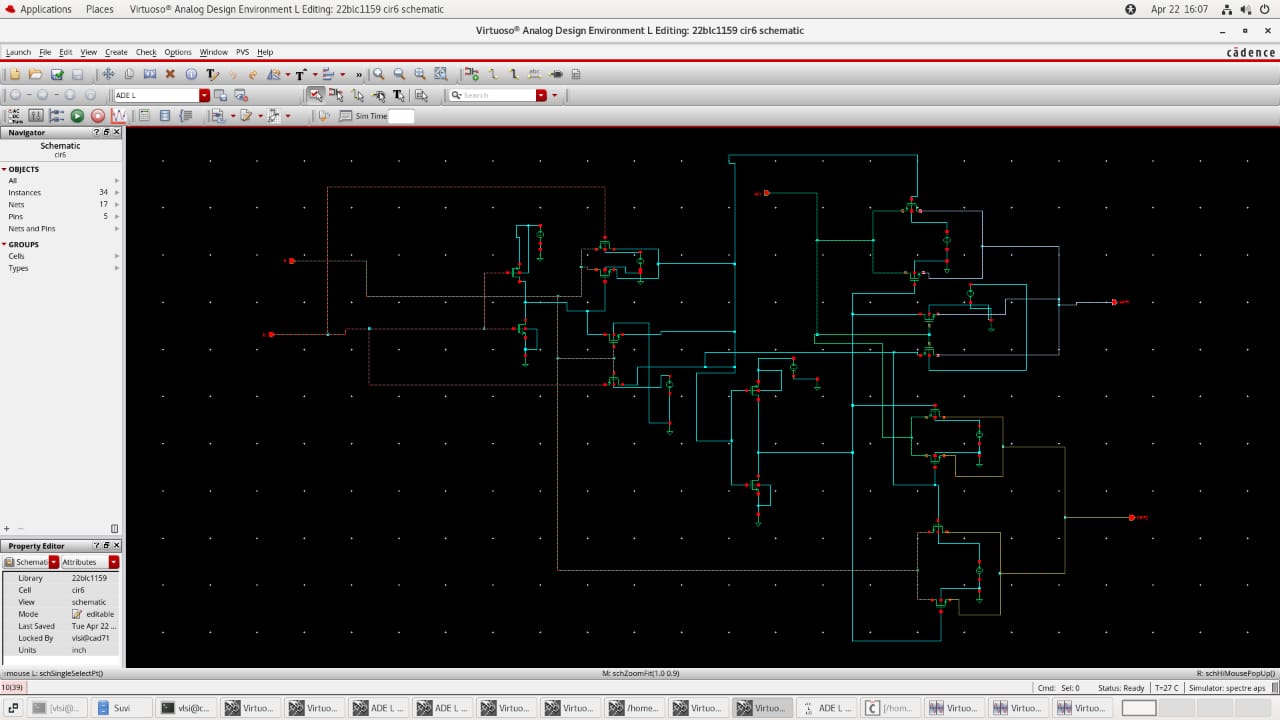
**After Sizing:**



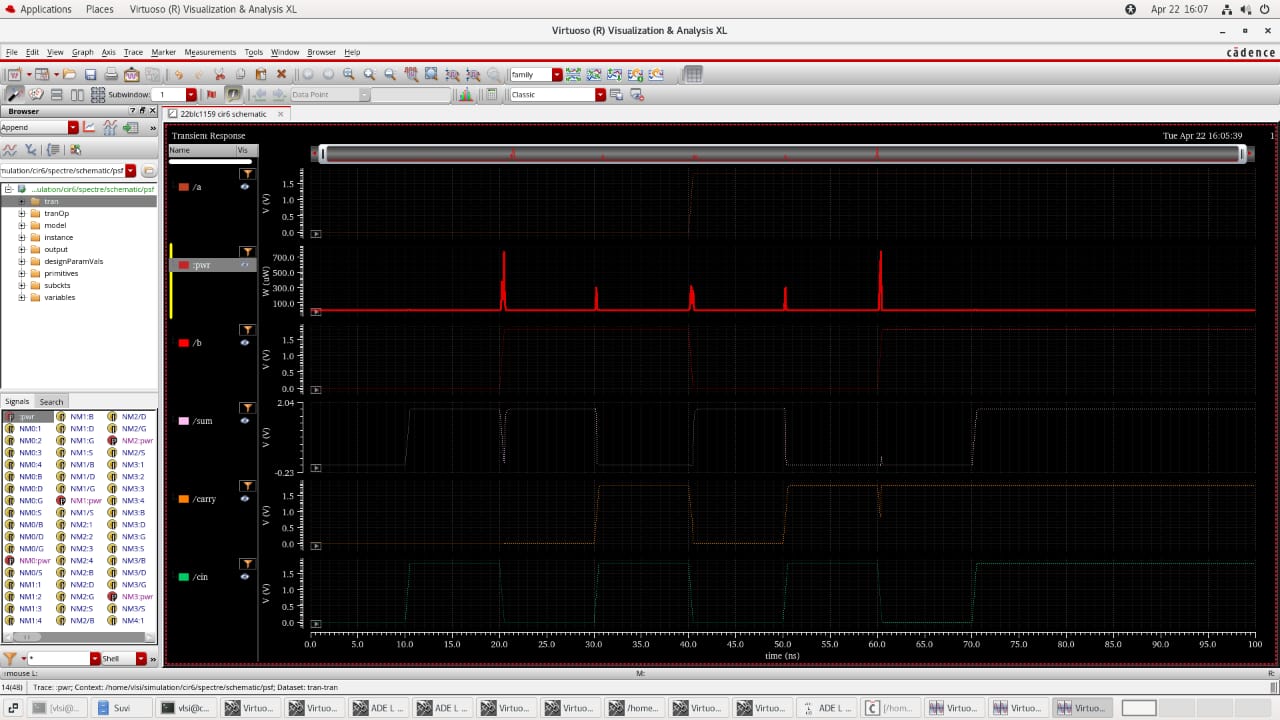
**Inference: Max Delay is R4Cin & R3S: 29.82 x 10^ (-9)**

1. **CIRCUIT 06**

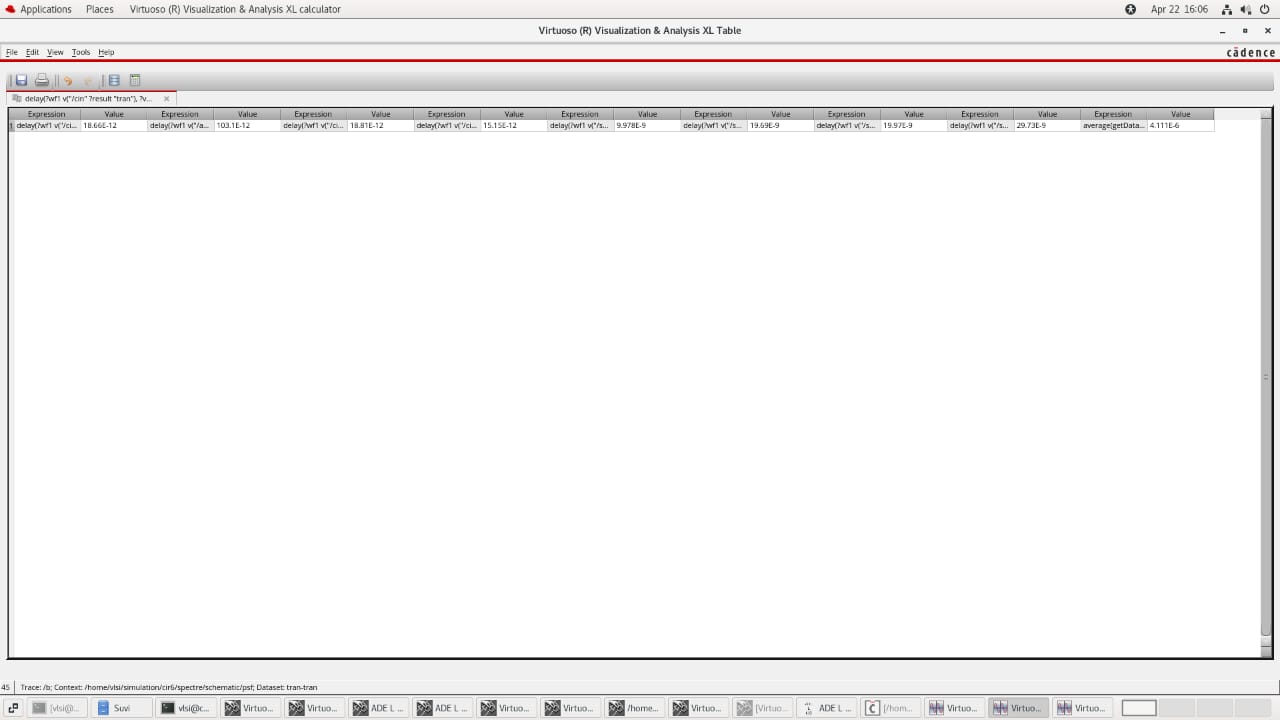
**SCHEMATIC:**



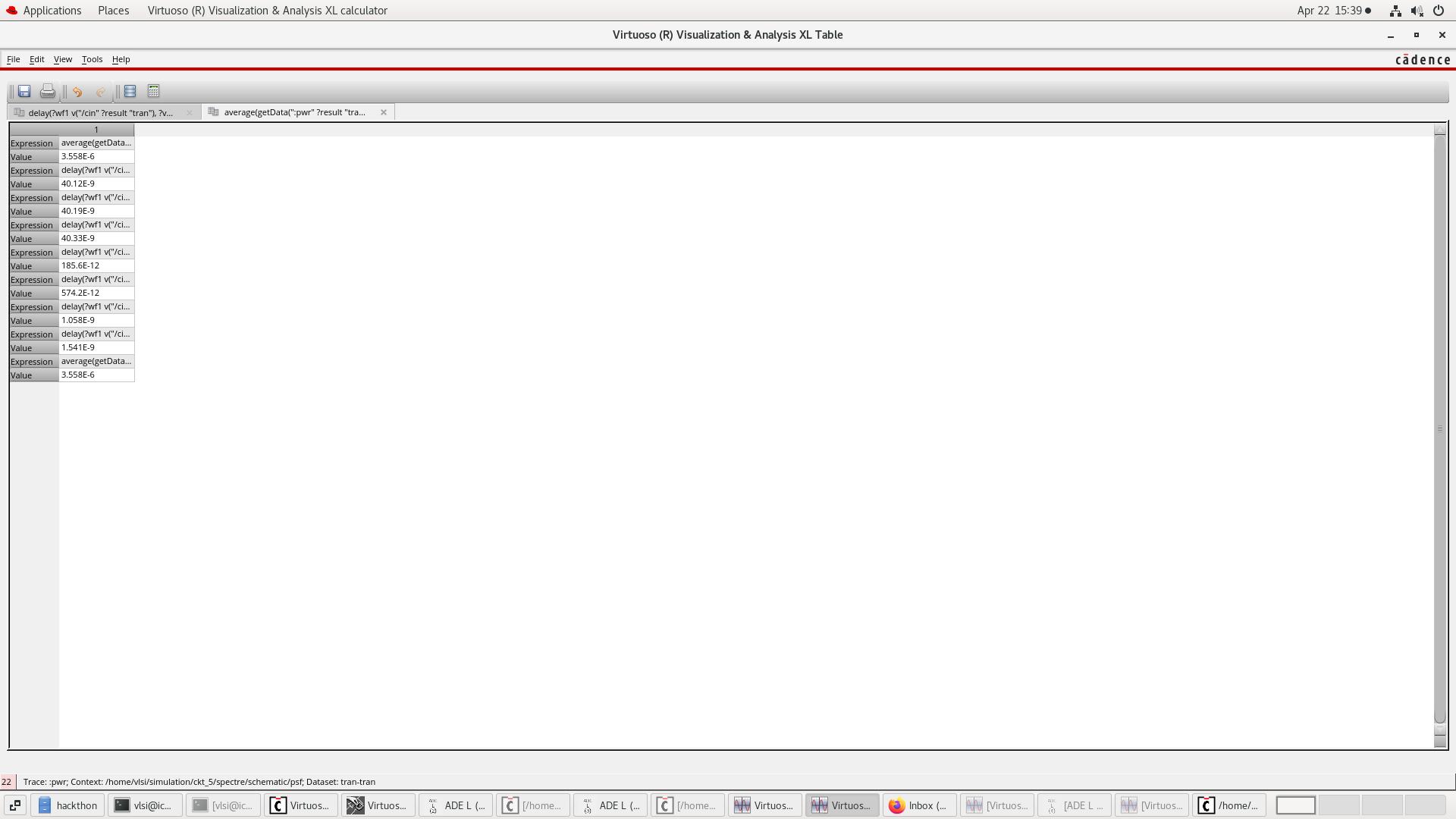
**OUTPUT WAVEFORM:**



**DELAY & POWER CALCULATIONS (PRE-SIZING)**

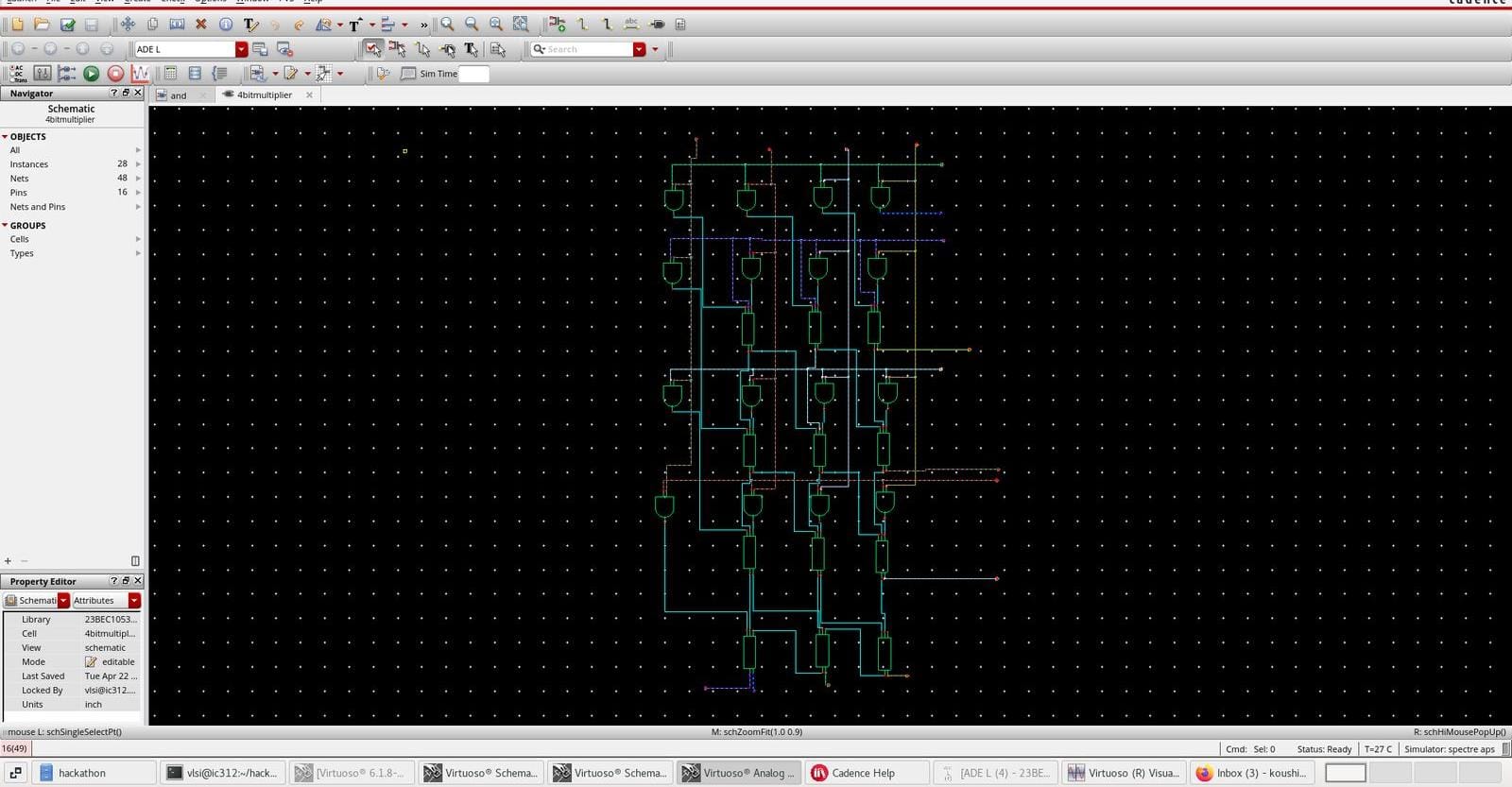


**AFTER SIZING:**



* **Implementing Multiplier using FA (Circuit 03) & 2-input NAND**

**Schematic**



**Output Waveform**



**Result: The 4 bit multiplier was succesfully implemented using full adder (the one with the least delay) & a 2 input nand gate, and it’s output waveform is noted for various inputs.**