CONNECTOR PERFORMANCE STANDARD FOR OUTLINES OF SOLID STATE AND RELATED PRODUCTS

PS-002

DDR4 288 Pin U/R/LR DIMM Connector Performance Standard

(Double Data Rate 4)

JEDEC
SOLID STATE TECHNOLOGY ASSOCIATION

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(From JEDEC Board Ballot JCB-15-30, formulated under the cognizance of the JC-11.14 Subcommittee on Microelectronic Assemblies.)

1 Scope

This standard defines the form, fit and function of DDR4 connectors for U/R/LR modules supporting channels with transfer rates as high as 3.2 GT/S. It contains mechanical, electrical and reliability requirements for a one-piece connector mated to a module with nominal thickness of 1.40 mm. The intent of this document is to provide Performance Standards to enable connector, system designers and manufacturers to build, qualify and use the DDR4 connectors in client and server platforms.

1.1 Connector overview

DDR4 U/R/LR DIMM connectors share the same mechanical definition and dimensions. The 288 pin, 0.85 mm pitch vertical connector is defined for applications where a 1.40 mm nominal thickness module card vertically enters the connector, perpendicular to the system board.

2 References

The following references provide normative requirements as specified in the body of this document:

- JEDEC DDR4 MO-309 Module Outline
- JEDEC DDR4 SO-016 (PTH), SO-017 (SMT), SO-019 (PF) Socket Outlines
- EIA-364-1000: Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets used in Controlled Environment.
- EIA-364-05: Contact Insertion, Release and Removal Force Test Procedure for Electrical Connectors
- EIA-364-13: Mating and Unmating Force Test Procedure for Electrical Connectors and Sockets
- EIA 364-23: Low Level Contact Resistance Test Procedures for Electrical Connectors and Sockets
- EIA-364-27: Shock Test Procedure for Electrical Connectors
- EIA-364-28: Vibration Test Procedure for Electrical Connectors and Sockets
- EIA-364-29: Contact Retention Test Procedure for Electrical Connectors
- EIA-364-31: Humidity Test Procedure for Electrical Connectors and Sockets
- EIA-364-32: Thermal Shock Test Procedure for Electrical Connectors and Sockets
- EIA 364-70: Temperature Rise Versus Current Test Procedure for Electrical Connectors and Sockets
- Agilent Application Note, " Agilent Network Analysis Applying the 8510 TRL Calibration for Non-Coaxial Measurements" Product Note 8510-8A
- JEDEC JESD22-B102 Solderability
- JS709A Defining "Low-Halogen" Electronic Products
- SPP-023 Standard Practices and Procedures - Module Insertion/Extraction Procedure for DIMM and Mini DIMM Connectors

3 Acronyms, terms, and definitions

Table 0 — Terms and Definitions

Term	Description
BOL	Beginning of Life
dB	Given in dB-volts, i.e., 20log10(V2/V1)
DUT	Device under test
DDR	Double Data Rate
EIA	Electronics Industry Alliance
EOL	End of Life
JEDEC	JEDEC Solid State Technology Association
System board	PCB on which the DDR4 connector is mounted
Vertical connector	A connector that accepts a module perpendicular to the system board

4 Pin numbering

This section describes pin numbers in DDR4 connectors, The DDR4 U/R/LR DIMM connector pin list is shown in Table 0 — .

Table 0 — DDR4 U/R/LR DIMM Number Sequence

Pin#			Pin#
1	Pin	Pin	145
2	Pin	Pin	146
3	Pin	Pin	147
4	Pin	Pin	148
5	Pin	Pin	149
6	Pin	Pin	150
7	Pin	Pin	151
8	Pin	Pin	152
9	Pin	Pin	153
10	Pin	Pin	154
11	Pin	Pin	155
12	Pin	Pin	156
13	Pin	Pin	157
14	Pin	Pin	158
15	Pin	Pin	159
16	Pin	Pin	160
17	Pin	Pin	161
18	Pin	Pin	162
19	Pin	Pin	163
20	Pin	Pin	164
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Pin#			Pin#
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Pin#			Pin#
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133	Pin	Pin	277
134	Pin	Pin	278
135	Pin	Pin	279
136	Pin	Pin	280
137	Pin	Pin	281
138	Pin	Pin	282
139	Pin	Pin	283
140	Pin	Pin	284
141	Pin	Pin	285
142	Pin	Pin	286
143	Pin	Pin	287
144	Pin	Pin	288

5 Connector Socket Outline

5.1 DDR4 Connector Overview

A primary consideration for DDR4 development was maintaining form factor continuity with DDR3 and 2 DIMMs per Channel (2DPC) route-ability across all platform segments. The objective was to scale the connector in an evolutionary manner to fit within the platform volumetric and cost constraints. The mounting technology is anticipated to be primarily plated-through hole (PTH), while press fit (PF) and surface mount (SMT) are available as well. DDR4 connectors are uniquely keyed to prevent interchangeability with the previous connector generations. The pin count increase to 288 pins is primarily due to 1:1 S:G ratio required by signaling performance scalability. In order to maintain volumetric parameters comparable to previous generation DIMMs and provide a higher pin count, the connector pin pitch was reduced to 0.85 mm. The tighter pitch was considered conducive for high volume manufacturing and assembly. Form factor signal synergy is maintained to support a common controller definition across all platform segments.

5.2 Socket Outline

A general view of the DDR4 U/R/LR DIMM connector with inserted module is shown in Figure 1 — . The basic socket outlines are shown in Figure 2, Figure 5 — , and Figure 4 . Detailed outlines refer to JEP95, SO-016 Plated Through Hole (PTH), SO-017 Surface Mount (SMT), and SO-019 Press Fit (PF) Outlines. All dimensions are in millimeters.

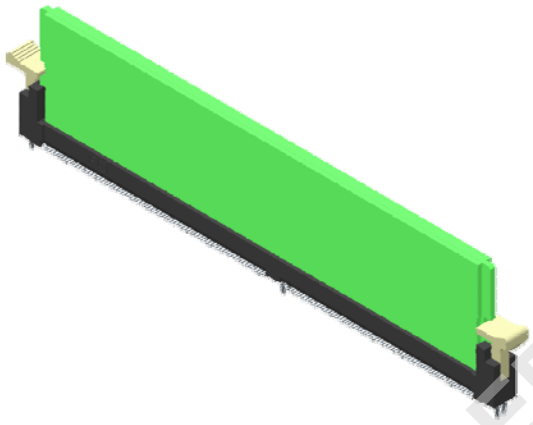

Figure 1 — DDR4 socket and module (SMT)

Figure 2 — Plated Through Hole (PTH) Connector Socket Outline

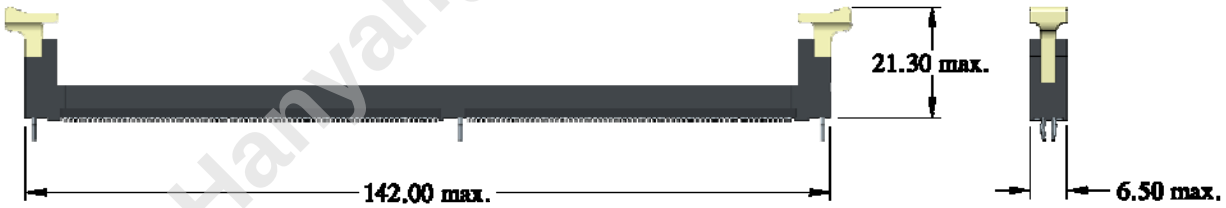

Figure 5 — Surface Mount (SMT) Connector Socket Outline

Figure 4 — Pressfit (PF) Connector Socket Outline

6 Module Outline

6.1 Module mechanical dimensions

DDR4 U/R/LR DIMM modules share the same mechanical definition and dimensions. The total volumetric envelope is maintained between DDR3 and DDR4. Tightened tolerances on module slot and pad dimensions, in addition to smaller sized pads, are necessary for equivalent mating/shorting performance compared to DDR3. The DDR4 U/R/LR DIMM outline is shown in Figure 5 — .

For the detailed outline, refer to JEDEC JEP95, MO-309.

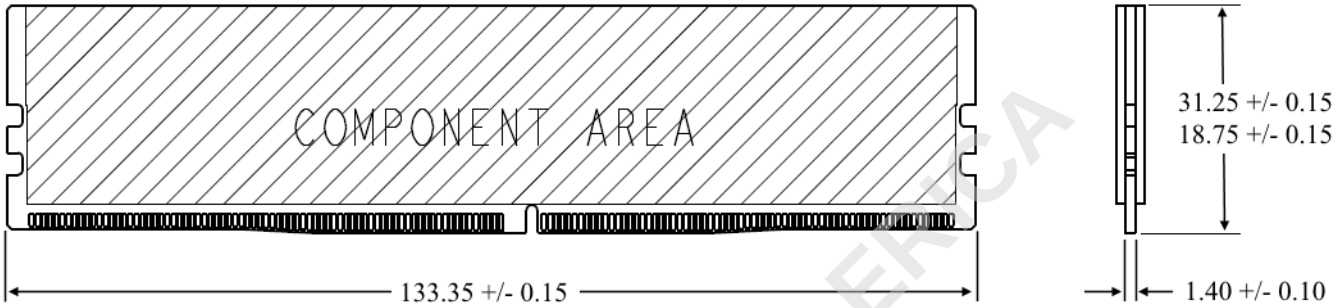

Figure 5 — DDR4 U/R/LR DIMM Module Outline

6.2 Step and ramp feature

In order to reduce the insertion force, a step and ramp feature is required on the DDR4 U/R/LR DIMM module. The step and ramp feature allows the connector pins to engage the module gold fingers in a sequential manner. The ramp area locates within one byte zone to limit the contact parasitic variation impact. There are two step and ramp zones at the bottom edge of the module.

For the detailed outline, refer to JEDEC JEP95, MO-309.

6.3 DIMM gold finger plating options

External tie bar will be needed on DIMM top/bottom layer, inner tie bar is not allowed for plating. Selective gold plating is not allowed.

Gold finger plating options are for reference see JEDEC JEP95, MO-309.

7 Reliability requirements

Testing shall be performed per EIA 364-1000 test groups 1, 2, 3, and 4 for 3, 5, or 7-year life cycle requirements. A minimum 5 samples are to be tested per subgroup.

7.1 Mechanical and other requirements

Table 3 — Mechanical and other requirements

Mechanical Test Description	Procedure	Requirement
Insertion Force (Module to Connector)	EIA-364-13 Axial Tension/Compression machine such as an Instron Tensile Tester. Rate: 25.4 mm/min. Use the JEDEC GS-010-1 Insertion Gauge.	106.8 N Maximum
Retention Force - Terminal	EIA 364-29	300 gf minimum per pin; maximum movement of contact of 0.38 mm
Retention Force - Forklock	EIA 364-29	13.3 N minimum per forklock; maximum movement of 0.38 mm
Insertion Force - Connector to Board	EIA-364-05 Axial Tension/Compression machine such as an Instron Tensile Tester. Rate: 12.7 mm/min.	75 N maximum
Unmating Force	EIA-364-13 Axial Tension/Compression machine such as an Instron Tensile Tester. Rate: 12.7 mm/min. Use the JEDEC GS-010-2 Extraction Gauge.	19.77 N minimum
Durability (mating/unmating)	EIA-364-99 GS-010-1 Insertion Gauge. Perform 25 cycles plug and unplug cycles at a rate of 25.4 mm/minute	LLCR and no nickel plating exposed
Additional Tests	**Procedure**	**Requirement**
Solderability - Lead Free	JESD22-B102; Condition C, 8 hours ± 15 minutes steam precondition.	95% coverage minimum
Lead Free Process ability	260 °C, 5 seconds.	No physical damage to connector per visual inspection at 24 inches. No magnification

7.2 Reliability test conditions

Table 4 — Reliability test sequence

Test	Test Group			
	1	2	3	4
Low Level Contact Resistance	1,4,6	1,4,6,8	1,3,5,7	1,4,6,8,10
Reseating	5	7		9
Vibration			4	
Mechanical Shock			6	
Durability (preconditioning)	2	2	2	2
Temperature Life	3			
Temperature Life (preconditioning)				3
Thermal Shock		3		
Cyclic Temp and Humidity		5		
Mixed Flowing Gas				5
Thermal Disturbance				7

7.2 Reliability test conditions (cont'd)

Table 7 — Reliability test conditions

Reliability Test Description	Procedure	Requirement
Durability (preconditioning)	EIA-364-09, perform 5 plug/unplug cycles	no evidence of physical damage
Temperature Life Temperature Life (preconditioning)	EIA-364-17, Method A (without electrical load) 60 °C field temperature. Test Temperature and Test Duration per EIA 364-1000 Table 8 60 °C field temperature. Test Temperature and Test Duration per EIA 364-1000 Table 9	electrical, mechanical and environmental criteria
Low Level Contact Resistance (LLCR)	EIA-364-23 (termination of connector to board carrier shall be included in the measurements)	Refer to Table 5.4.2
Shock Unpackaged	EIA-364 -27 Trapezoidal shock 50 g, ± 10% Duration 11 ms Velocity change 170 inch/sec, ± 10% Three drops in each of six directions are applied to each of the three samples Shock and Vibration board, Annex D	electrical, mechanical and environmental criteria
Vibration Unpackaged	EIA-364 -28 Random profile: 5 Hz @ 0.01 g2/Hz to 20 Hz @ 0.02 g2/Hz (slope up) 20 Hz to 500 Hz @ 0.02 g2/Hz (flat) Input acceleration is 3.13 g RMS 10 minutes per axis for all 3 axes on all samples Random control limit tolerance is ± 3 dB Shock and Vibration board, Annex D	no discontinuities of ≥ 1 microsecond electrical, mechanical and environmental criteria
Cyclic Temperature and Humidity	EIA-364-31B, Method III without conditioning, initial measurements, cold shock and vibration. Ramp times should be 0.5 hour and dwell times should be 1.0 hour. Dwell times start when the temperature and humidity have stabilized within specified levels, perform 24 cycles in mated condition	electrical, mechanical and environmental criteria
Thermal Shock	EIA-364-32, Method A, Table 2, Test Condition 1, -55 °C to 85 °C, perform 5 cycles in mated condition	electrical, mechanical and environmental criteria
Thermal Disturbance	EIA-364-1000 Cycle the connector between 15 ±3 °C and 85 ±3 °C, as measured on the part. Ramps should be a minimum of 2 °C/minute. Dwell times should ensure that the contacts reach the temperature extremes (a minimum of 5 minutes), humidity is not controlled; perform 10 cycles in mated condition.	electrical, mechanical and environmental criteria
Mixed Flowing Gas	EIA-364-65, class IIA, Option 4. Expose all specimens in the mated condition for the total mixed flowing gas exposure duration per Table 4.	electrical, mechanical and environmental criteria
Reseating	Manually unplug/plug the connector. Perform 3 cycles	No evidence of physical damage

7.3 Environmental requirements

Table 6 — Connector environmental requirements

Environmental Requirements	Procedure	Requirement
Flammability	UL 94 V-0	
Lead Free	RoHS compliant per IEC 62474	RoHS directive (2011/65/EU)
Low Halogen	1000 ppm max Cl when used in a flame retardant 1000 ppm max Br when used in a flame retardant Per JS-709A Standard (Clause 4)	Sample combustion followed by ion chromatography as specified in British Standard Methods BS EN 114582/2007, Characterization of waste – Halogen and sulfur content – Oxygen combustion in closed systems and determination methods OR US EPA-5050 (BOM Preparation Method for Solid Waste)

7.4 Electrical requirements

Table 7 — Connector electrical requirements

DC Electrical Requirements	Procedure	Requirement
LLCR (Contact resistance)	EIA364-23B Subject mated contacts assembled in housing to 20 mV maximum voltage at 100 mA maximum current	Post Stress: the resistance change, which is defined as the change in LLCR between the reading after stress and the initial reading shall not exceed 10 mΩ
LLCR Contact resistance, Initial	EIA-364 -23	10 mΩ Max
Withstanding Voltage	EIA-364-20, Condition I. 500 V ac at sea level.	One minute hold with no breakdown or flashover.
Insulation resistance	EIA-364 -21	1M Ω minimum
Current carrying capability at 30 °C temperature rise per contact	EIA-364 Test Procedure 70 Detail in Annex C	0.75 amp/pin (THM) De-rated

Annex A (informative) LLCR Measurements

A.1 Reference equipment

- Micro-ohmmeter (such as Keithly 580; Agilent 4338B)
- Cable with clamper or pogo pins

A.2 Test fixture

Figure A.1 and Figure A.2 illustrate LLCR measurement examples using 4-terminal technique.

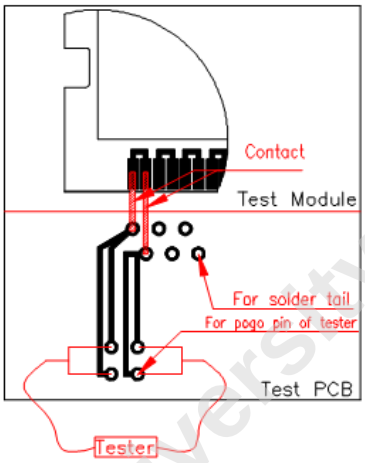

Figure A.1 — 4-wire connection example (two pins in series)

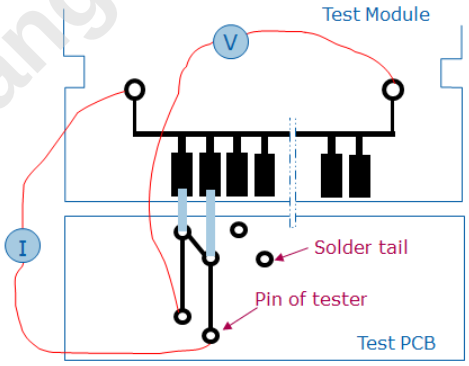

Figure A.2 — 4-wire connection example (two pins in parallel)

Annex B (informative) Current Carrying Capability Testing

B.1 Reference equipment

T-Rise Method (Reference EIA 364-70 Method 2)

B.2 Test procedure

The method summary as follows: Minimum of 5 connector samples.

- Ambient system temperature stabilized (testing to occur at ambient system temperature)
  - Current necessary to produce the specified temperature of 30 °C. (Do not exceed maximum connector temperature rating e.g. 105 °C)
  - Test multiple contacts in the same housing per wiring diagram.
  - Test single contact in housing per wiring diagram.

Report results per EIA 364-70 table “test documentation Annex”.

B.3 Test board daisy chain connection

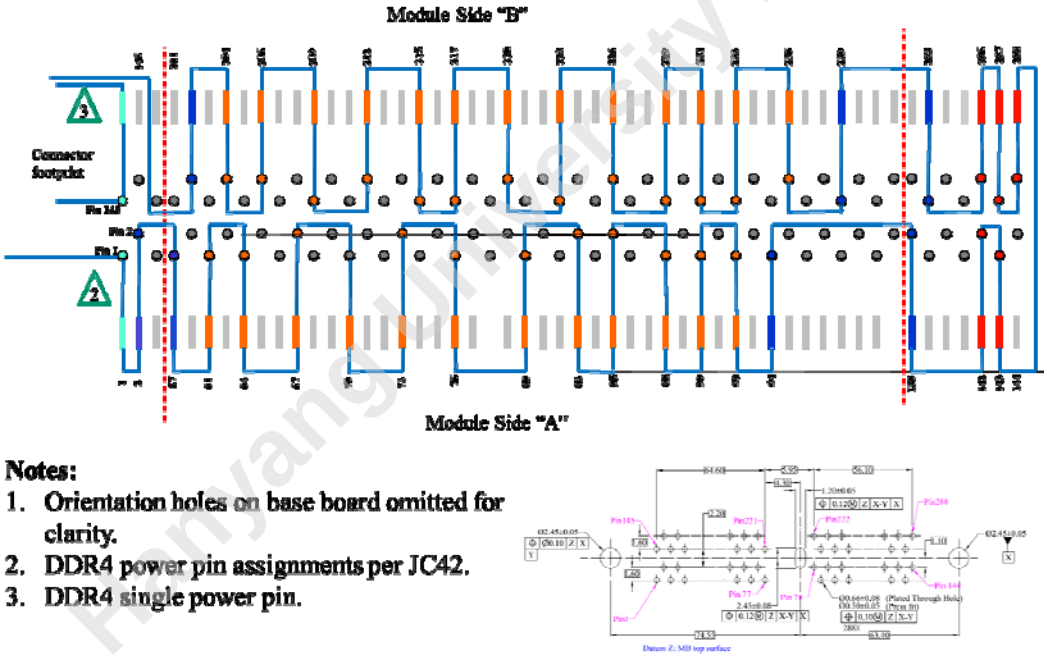

Figure B.1 — Daisy chain connection

Annex C (informative) Shock and vibration test board

C.1 Shock and vibration

Shock and Vibration Test Board to be specified by OEM/ODM due to various system layouts.

C.2 Test Module - weight and center of gravity

- Module weight 40 ± 2 grams. Center of gravity 18-20 mm from the module mating edge (bottom of the module where gold fingers reside).
- Module thickness: 1.30 ± 0.1 mm.
- Module to check continuity.

C.3 Shock unpackaged

C.3.1 Purpose

To ensure the boards are sufficiently robust to withstand shocks when shipped in a system. Board Un-packaged testing does not pre-qualify a board for shipping as an un-mounted unit inside a shipping container.

C.3.2 Quantity

- Investigation: 1 Board
- Validation: 3 Boards

C.3.3 Test Conditions

- Trapezoidal shock 50 g ± 10%.
- Velocity change 170 inch/sec, ± 10%.
- Three drops in each of six directions are applied to each of the three samples.

C.4 Vibration unpackaged

C.4.1 Purpose

To ensure the board is sufficiently robust to withstand vibration when mounted in a system, which is being shipped. Board unpackaged testing does not pre-qualify a board for shipping as an un-mounted unit inside a shipping container.

C.4.2 Quantity

- Investigation: 1 Board
- Validation: 3 Boards

C.4.3 Test Conditions

Random profile:

- 5 Hz @ 0.01 g2/Hz to 20 Hz @ 0.02 g2/Hz (slope up)
- 20 Hz to 500 Hz @ 0.02 g2/Hz (flat)
- Input acceleration is 3.13 g RMS
- 10 minutes per axis for all 3 axes on all samples
- Random control limit tolerance is ± 3 dB

CHANGE RECORD

IF THE CHANGE INVOLVES ANY WORDS ADDED OR DELETED (EXCLUDING DELETION OF ACCIDENTALLY REPEATED WORDS), THE CHANGE IS INCLUDEC. PUNCTUATION CHANGES MAY OR MAY NOT BE INCLUDEC.

INITIAL ISSUE: A	Date: May 2015	JC11 Item Number: 14-177

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