Indian Institute of Technology, Delhi
ELL304: Analog Electronic Circuits
Minor 2, October 9, 2016

General instructions: No books, no notes. Assume $kT/q = v_T = 25$ mV. For BJTs, assume V_{BE} is 0.7 volts. For the MOS devices, $I_D = \mu C_{ox}/2 \cdot (W/L) \cdot (V_{GS} - V_T)^2$. Assume μC_{ox} for nMOS as well as pMOS devices are identical. Ignore g_{mb}. For every MOS device, $g_m r_o$ is 20.

1. In the circuit schematic of Fig. 1, the (W/L) of the individual devices are indicated in the schematic.

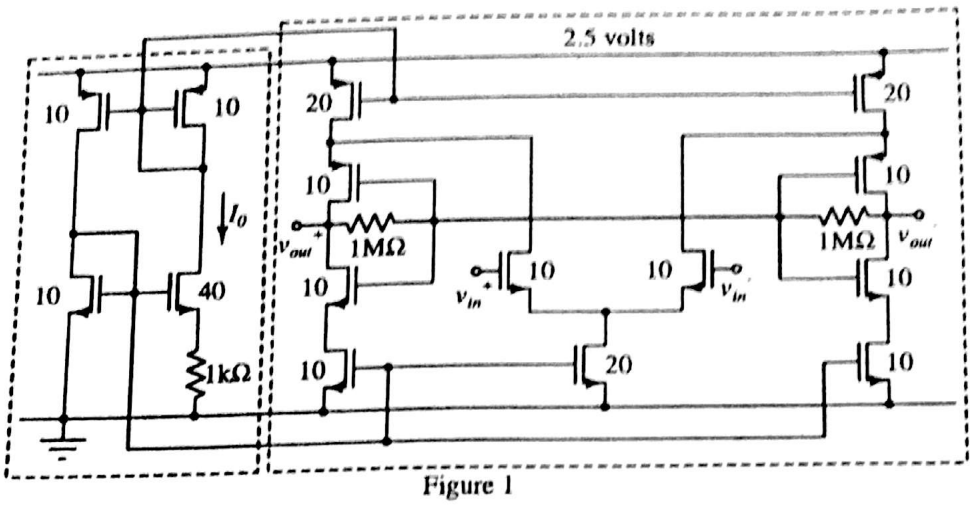

Figure 1

(a) For the circuit in the left dashed region, evaluate an expression for the current I_0. (3 marks)

(b) Evaluate the g_ms of the essential devices in the right dashed region. *Hint: g_m should be a* ~~*quantity*~~*. Not an expression. Value of μC_{ox} will not be given.* (2 marks)

numerical

(c) Draw the small signal incremental differential mode half circuit. If you could not answer the earlier questions, assume that the current is such that the g_m of each of the devices in the differential pair is 0.1 mS. Evaluate the differential mode gain. (2+4 marks)

(d) Draw the small signal common mode half circuit, showing essential parameters. (2 marks)

2. In the common-emitter amplifier shown in Fig. 2, what is the gain at DC? What should be the impedance at the emitter such that the gain increases $\sqrt{2}\times$? What is the +3 dB frequency? What is the gain when frequency is $3\times$ the +3 dB frequency? (4×1 marks)

3. The top view of an nMOS device is as shown below in Fig. 3(a). It has a width of 2 μm, a length of 1 μm. An analog circuit designer implemented the device as shown in Fig. 3(b).

(a) Is his implementation correct? (1 mark)

(b) What are the possible advantages and disadvantages of the implementation of Fig. 3(b) over the device of Fig. 3(a)? (2 marks)

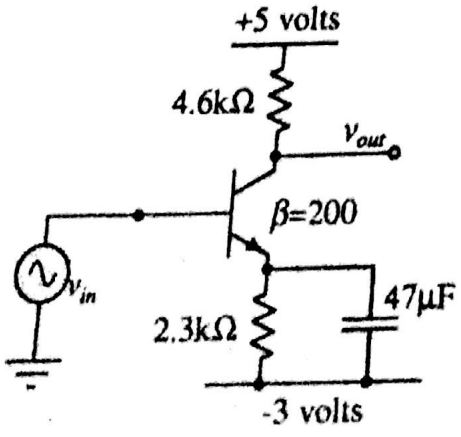

Figure 2

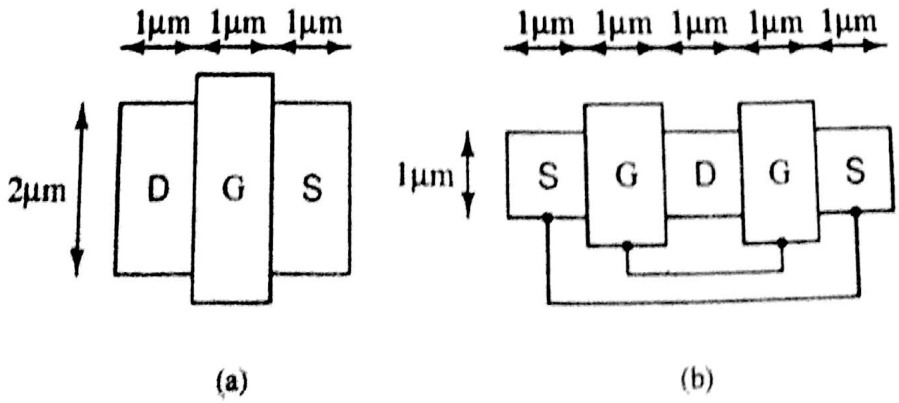

Figure 3