MINOR 2

(ELL305) Computer Architecture

2016

Time: 1 Hour | **Max. Marks: 25**

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Group: - 01 **Serial Number as in Attendance Sheet: -**

N. B.: Do the calculations on last page attached. This is **open book / notes examination**, but **exchange** to each other is strictly **prohibited**. **NO CLARIFICATIONS.**

Take the value of *m n* = 74 for this question paper

Q1 (a): - The values assigned to various registers are:

DS = 20 *m n* H,	**DI = 10 *m n* H,**	**SI = 03F0 H,**	**DX = 02D0 H,**
SS = 40 *m n* H,	**SP = 30 *m n* H,**	**BP = 20 *m n* H,**	**BX = 1234 H**

Calculate and write the physical address of destination operand for the instructions below: **(3)**

i) **MOV** **[BP + SI + 0FFFF H], AL**
Physical Address = 3463 H **H**

ii) **PUSH BX**
PUSH CX
PUSH SS
PUSH CS
PUSH DX
PUSH ES

Physical address of least *significant* byte of DX = ~~306F~~ ~~306F~~ 306A **H**

ii) **MOV** **[BX+ DI + 7C H], AL**
Physical Address = 2324 **H**

CALCULATION SPACE:

2074 H
03F0 H
0FFF H
3463 H

1234
1074
7C
2324

DH | DL

3064
-9
306A

(b): - Write the contents of 'AX' in *hexadecimal* after every numbered operation in the following:

(This is a **continuous** program which starts from AX = 0000 H and is executed sequentially) (3)

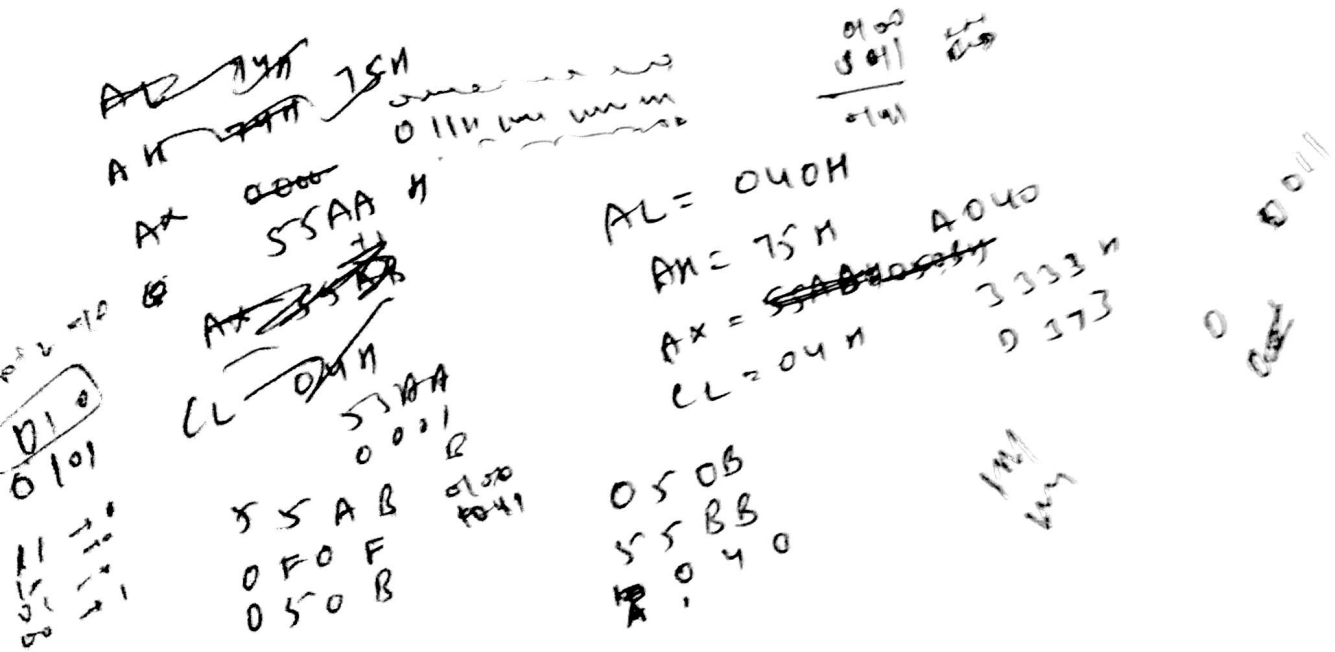
```
        MOV     AL, m n H
        MOV     AH, m n H
        AND     AX, 0FFFF H
        OR      AX, 55AA H

(1)     TEST    AX, 0234 H      New value of AX = CA1E H

        INC     AH,
        MOV     CL, 04 H
(2)     SHL     AL, CL          New value of AX = 0CE1 H
        ADD     AX, 0001 H
        AAA
        AND     AX, 0F0F H
(3)     AAD                     New value of AX = 0C02 H

        XOR     AX, 55BB H
        DCR     AL
(4)     OR      AX, 3333 H      New value of AX = B373 H
```

CALCULATION SPACE:



Q2: - (8086 based) What will be the value in **AX** after executing the following instructions? Give the answer in both hexadecimal and binary. (Numbers are **decimal** if they are not indicated with 'H') (2)

```
        MOV     AL, 15
        MOV     AH, 14
        XOR     AL, AL
        MOV     CL, 03
        SHR     AX, CL
        ADD     AL, 90 H
        ADC     AH, 0
```

ANSWER: Final AX in decimal = 0000 0010 0110 1110

Final AX in Hexadecimal = 026EH

CALCULATION SPACE:

AL → 90H AL = 15

AH = 14

CL = 01

AX = 1

AX2 0E0F

AX : 0E F0

1110 1111 0

1001 0000

2 6 E 0

Q3 (a): - suppose a processor (clock rate **500** MHz) with a base CPI of **1.0**, assuming all references hit in the L_1 cache. Assume a main memory access time of 200ns, including all the miss handling. Suppose miss rate per instruction at L_1 cache is **5 %.** How much faster will the machine be if we add a L_2 cache that has **20** ns access time for either a hit or a miss and is large enough to reduce miss rate to main memory to **2** %? **(3)**

CALCUTION & ANSWER:

L_1 → 1 cycle → 2 ns

MM → 200 ns

Average time = 2 + 0.05 (200) = 12 ns

L_1 → 2 ns 5% miss

L_2 → 20 ns ← 3% handled here

MM → 200 ns 2%

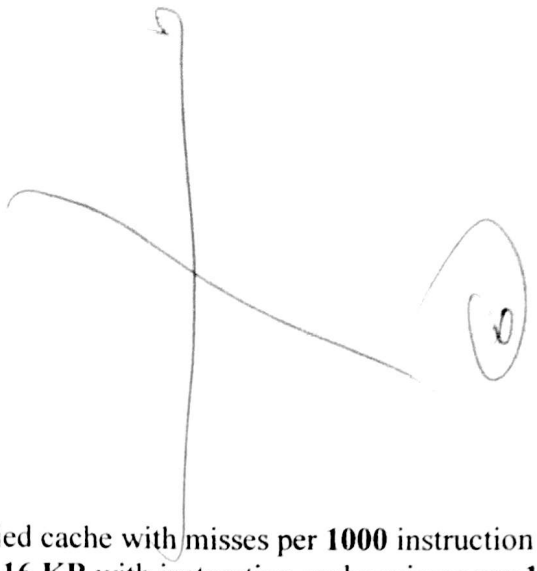
$T = 0.95 \times 2 + 0.03(20) + 0.02(200) = 6.5$ ns

(speed up) faster = 12/6.5 = 1.846 times faster machine

(b): - Let us consider a fully associative write-back cache with cache entries that start empty. Consider the following sequence of five memory operations and find, which address is not in the cache for no-write allocate. **(1)**

Write Mem [100]
Write Mem [100]
Read Mem [200]
Write Mem [200]
Write Mem [100]

Neat Discussion & ANSWER:



Q4 (a): - Let us consider **32 KB** unified cache with misses per **1000** instruction equals. **43 .3** and instruction / data split caches each of **16 KB** with instruction cache misses per **1000** as **3 .82** and data cache as **40.9**; Assume that:

- **26 %** of the instructions are data transfer instructions;
- **74 %** of memory references are instruction references; and
- Hit takes **1** clock cycle where the miss penalty is **100** cycles and
- A load or store takes one extra cycle on unified cache
- Assuming write-through caches with write-buffer and ignore stalls due to write buffer – Find the average memory access time in each case
- Hint: To solve this problem first find the miss rate and then average memory access time.

(4)

CALCULATION & ANSWER:

32 KB

16 Kb → 3.82

16 Kb → 40.9

43.3 misses per 1000 instructions / data

26% instructions are data transfer

74% of memory ref. & inst ref.

Hit → 1 clock

Miss → 100 clock

$M = \frac{40.9}{1000} (\quad 0.26 \times$

AMAT = $1 + \%.\text{read} (1 - HI) \times M + \%.\text{write} \times M$

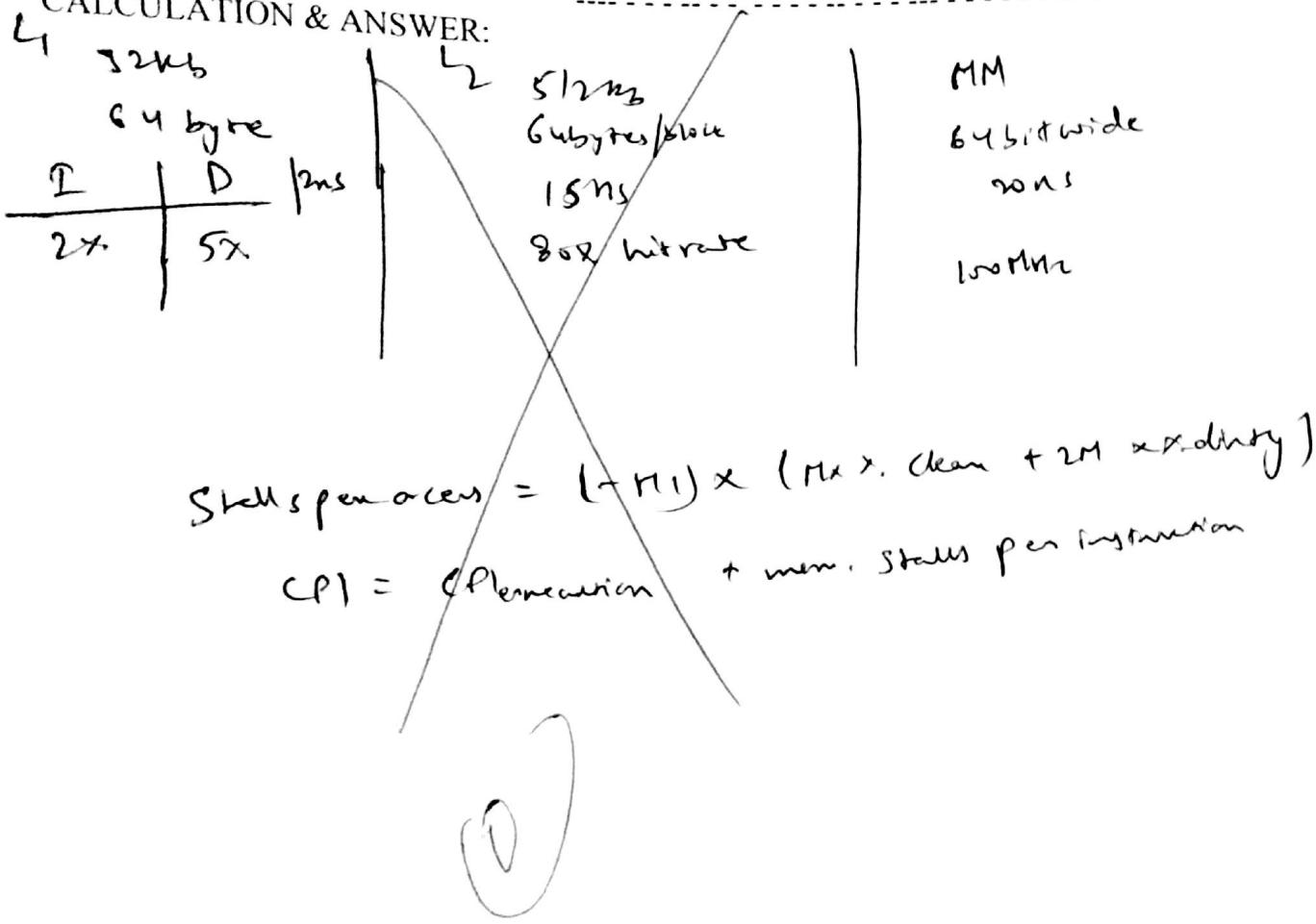
$= 74 (3.3) + 26 (6.3)$

$= 2.63$

1/2

(b): - You are building a computer system with in-order execution that runs at **1 GHz** and has a CPI of **1**, with no memory accesses. The memory system is split L_1 cache. Both the I-cache and the D-cache are direct mapped and hold **32 KB** each with block size **64** bytes. The I-cache has a **2 %** miss rate, and the D-cache is a write-through with **5 %** miss rate. The hit time for both the I-cache and the D-cache is **1 ns**. The L_2 cache is a unified write-back with a total size of **512 KB** and a block size of **64** bytes. The hit time of the L_2 cache is **15 ns**. L_2 write miss takes **15 ns**. The local hit rate of the L_2 cache is **80 %.** The **64**-bit wide main memory has an access latency of **20 ns**, after which any number of bus words may be transferred at the rate of one bus word (64-bit) per bus cycle on the 64-bit wide **100 MHz** main memory bus. Compute the CPI considering memory accesses. **(5)**

CALCULATION & ANSWER:



Q5: - Draw neat schematic diagram of 8086 based controller board with following feature. **(4)**

It should be able to drive a stepper motor in clock wise and anti-clock wise rotation. Show the scheme (By port pins only) and indicate the programming steps needed. If a delay routine of 10 mile second is given what maximum RPM you may achieve using a stepper motor of 7.2 degree per step rotation.

DIAGRAM & ANSWER: