Indian Institute of Technology, Delhi
ELL304: Analog Electronic Circuits
Major, November 20 2016

General instructions: No books, no notes. Total marks for this exam is 40.

1. In theory the gain of a common-drain circuit is limited to 1. Explain why in practice, the gain of the common-drain circuit is limited to 0.7 to 0.8 only. (3 marks)
2. Explain why it is not ok to apply a floating (not grounded) signal voltage source between the two input terminals of a differential amplifier. (3 marks)
3. Explain why the output impedance of a voltage regulator is inductive. (3 marks)
4. Explain why the p-substrate of a chip is connected to ground, and the n-wells in the chip are connected to the highest potential on the chip. (2 marks)
5. Why is a class-A power amplifier probably not a good design? Explain. (2 marks)
6. We can conceptually visualize a 1:100 step-up transformer as a voltage amplifier. In this course, why did we design electronic circuits, instead? (2 marks)
7. Consider the circuit in Fig. 1. The trapezoids refer to ideal transconductance cells, G_{m1} and G_{m2}. Come up with an expression for the compensation capacitance, C_c, such that the phase margin of the complete circuit is 60°. You may use any approximation that you find convenient, in the interest of time. Further, indicate a technique to nullify the RHP zero caused by the C_c. Find an expression for the value of the additional component used. (6 + 3 marks)
8. The pnp device in Fig. 2 has a β of 100. Assume V_{BE} is-0.7 V. Choose values of resistors appropriately such that I_C is 1 mA, the amplifier has an approximate gain of 5, and maximum possible symmetric peak-to-peak swing is obtained at the output. Make sure the current through R_1, R_2 is 20× the base current required by the device. (6 marks)
9. In the circuit of Fig. 3, the device Q2 has a junction area m times larger than that of Q1, and as a result its reverse saturation current is m times larger than that of Q1. Assume that the current mirroring is ideal. Come up with an expression for the differential output voltage. (3 marks)
10. f_T is the frequency at which the current gain of a MOS device becomes equal to 1. Come up with an expression for f_T of a MOS device. (3 marks)
11. Draw the circuit diagram (no component values needed) of a complete operational transconductance amplifier. The amplifier should be differential input, single-ended output. Incorporate in your circuit diagram all bias circuit details. Do not forget to incorporate the compensation capacitor(s) and such details. Clarity and neatness will carry weight in this question. (4 marks)

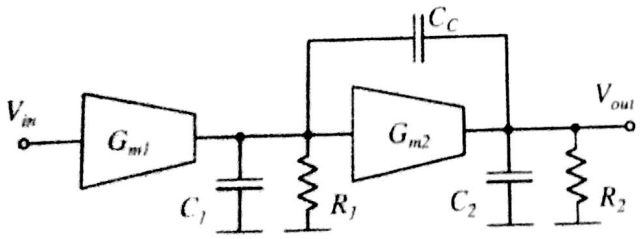

Figure 1

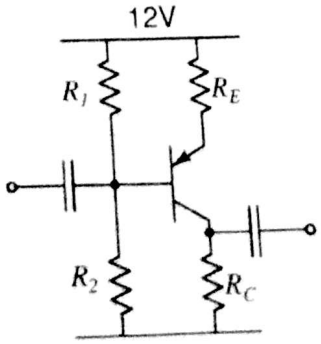

Figure 2

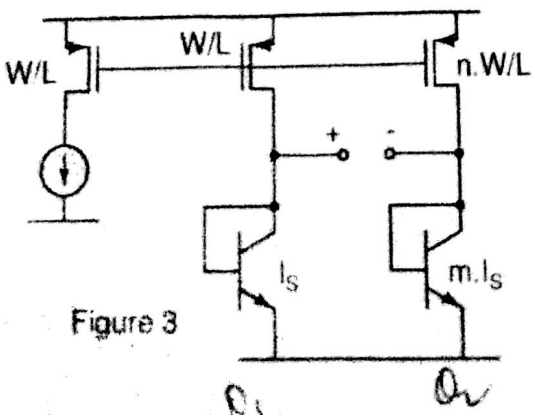

Figure 3