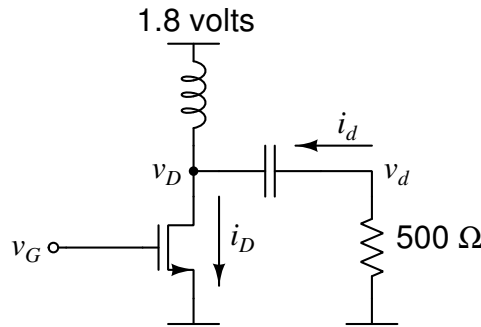


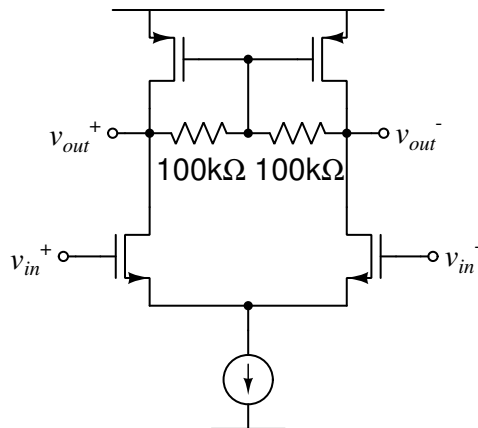
Indian Institute of Technology, Delhi
ELL304: Analog Electronic Circuits
Major, 22 November 2017

1. An op-amp is to be designed with the following specifications: (1) Unity gain bandwidth of 50 MHz ($2\pi \times 50 \times 10^6$ radians/second). (2) It has to drive a load capacitance, C_L of 10 pF. (3) A phase margin of 60° is required. Assume that you are building a 2-stage cascaded op-amp, with g_{m1} , R_1 in the first stage and g_{m2} , R_2 in the second stage. Assume C_1 , C_{01} and the parasitic C_{12} are negligibly small relative to the load capacitance and the compensation capacitance that you will apply. Use approximate calculations to arrive at your design using the steps that follow.
 - (a) First compute g_{m2} . (3 marks)
 - (b) The required DC gain of the op-amp is specified to be 52 dB (400). Assume the two stages contribute equal DC gain. Compute the value of R_2 . (1 mark)
 - (c) Assume that the first stage of the op-amp is budgeted 10% area and bias current, and the second stage of the op-amp is budgeted 90% area and bias current. Compute the value of g_{m1} . (2 marks)
 - (d) Compute R_1 . (1 mark)
 - (e) Compute C_C . (2 marks)
 - (f) Assume that to maximize swing at the outputs of each stage, both the first and second stage devices operate with a gate-overdrive voltage of 0.2 volts only. What should be the total current needed in your design if the first stage is differential and the second stage is single-ended? (2 marks)
 - (g) Draw the schematic of your op-amp. Show all devices including current mirrors. The op-amp should be a self-biased active-load op-amp. You should indicate ratios of important devices. A neat and clean schematic will impress your teacher. (4 marks)
2. In the circuit below, the inductor and the capacitor are so large that the current through the inductor is constant and the voltage across the capacitor is constant. The MOS device has to be in saturation at all times. V_G is $V_T + 0.2$ volts.



- (a) What is the maximum amplitude of i_d such that the device remains in saturation at all times? (1 mark)
- (b) What is the maximum amplitude of v_d such that the minimum current is 0? (1 mark)
- (c) Assume that the current i_d is $g_m v_g$ even for large amplitudes. What is the required g_m such that the maximum i_d is achieved when the amplitude of v_d is maximum? What is the value of v_g required? (2 marks)
- (d) If $i_D = K(v_{GS} - V_T)^2$, what is the corresponding value of K required for the device? (1 mark)
- (e) What is the efficiency of this power amplifier? (Ratio of power delivered to 500 Ω to the power absorbed from the power supply.) (2 mark)
- (f) Now discard the assumption that i_d is $g_m v_g$ even for large amplitudes. If the amplitude of v_g is 50 mV, what is the efficiency of the power amplifier? (3 marks)

3. In the schematic below, the nMOS devices have a g_m and g_o of 1 mS and 20 μ S respectively. The pMOS devices have a g_m and g_o of 0.5 mS and 10 μ S respectively.



- What is the differential mode gain of the circuit? (Differential output divided by differential input) (3 marks)
 - What is the common mode gain of the circuit? Assume that the output conductance of the current source is 10 μ S. (Average of outputs divided by average of inputs) (4 marks)
 - What is the CMRR? Give your answer in dB. (3 marks)
4. Give short answers to each of the following questions: (Total 5 marks)
- What are the benefits of a differential as opposed to a single-ended design? (1.5 marks)
 - We can conceptually visualize a 1:100 step-up transformer as a voltage amplifier. Why did you, at all, study ELL304 then? (1 mark)
 - Which of the two circuits is more linear? (a) The source-degenerated common-source amplifier, or (b) the ordinary common-source amplifier. Why? (1 mark)
 - A MOS device is biased in strong inversion but is being used as a switch that is ON. Grade the parasitic capacitances of the device relative to each other. (For example, your answer could be $C_{gs} > C_{gd} > C_{sb} > C_{db}$.) (1.5 marks)