MINOR 1
(EEL324) Digital Hardware Design
2013

Time: 1 Hour **Max. Marks: 25**

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N. B.: Do the calculations on continuation sheet provided. This is **open book / notes examination,** but **transfer** of notes to each other is strictly **prohibited.**

Q1:- Use the non-restoring division algorithm for the signed integers with **n = 3.** **(4)**

The numbers are;

Dividend 'D' = 010010

Divisor 'V' = 0100

2's complement of divisor = 1100

Compute and place the values in the table below:

Step #	Action	S	A (accumulator register)	Q (quotient register)
	Start	0	00010	0010
1	Shift left	0	00100	0100
2	Subtract V from A. Set last bit to 1 if +ve	0	0100 0110	0100
3	Shift left	0	1100	1010
4	Subtract V from A.	1	0100 0000	1010
5	Shift left and	0	0001	0100
6	add V to A	0	0001	0100

Answer:

Quotient = 0100

Remainder = 0010

D+1

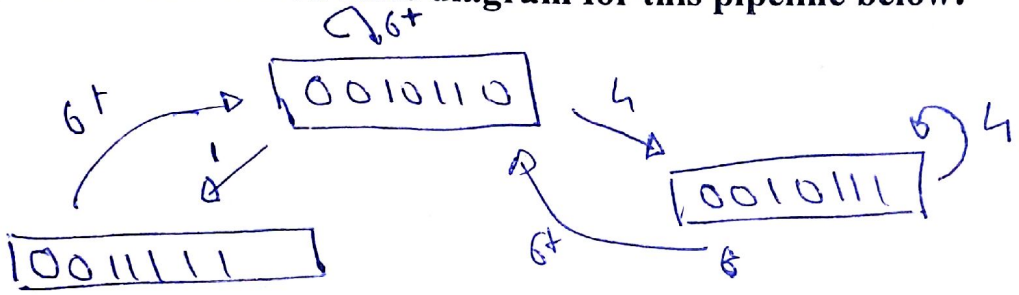
n=3

Q2:- In a processor with on-chip cache the operations instructions fetch, instruction decode, address generate, operand fetch, execute, operand store and program counter update is performed as given in reservation table. Compute results as mentioned for the reservation table below: **(3 ½)**

OPERATIONS	→ Time						
	1	2	3	4	5	6	7
Memory Operation	X			X		X	
Instruction Decode		X					
Address Generation			X				
Execute					X		
Update PC							X

Answer: (a) Collision vector (in $C_7\ C_6 \ldots C_1$ format) = 0 0 1 0 1 1 0

(b) Draw the reduced state diagram for this pipeline below:



3

(c) All Simple cycles: (1,6) (4,6)

(d) Greedy cycles: (1,6) (4)

(e) Latency sequence that can achieve the MAL. = before delay, no latency sequence
after delay => (3) (1,5)

(f) If delay is needed then,
The new collision vector (in above format) = 0 0 0 0 1 1 0 f

Q3: - Design a single-input, single-output synchronous sequential circuit (using D flip-flop) that is to have the following characteristics;

- No 3 consecutive output bits can be 1.
- The output will be 1 if, of 3 consecutive input bits, just two are 1, unless it conflicts with the first requirement.

A possible input/output sequence, for example;

X: 0000 1101 0111 0010 1011 0110
Z: - -00 0110 0110 1000 1011 0110

(3 ½)

Answer (Only diagram without calculations / equations):

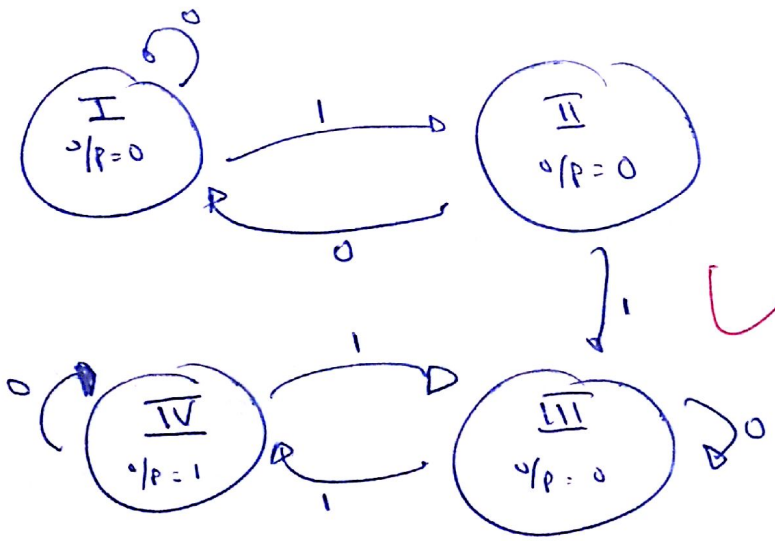
Q4: - A synchronous sequential network has one input (**X**) and one output (**Z**). The output **Z** stays at '**0**' until at least a pair of consecutive **1**'s occurs. If there has been an odd number of **1**'s in the input (**X**) since the first pair of **1**'s, the output changes to '**1**' and remains at '**1**' until an even number of **1**'s in (**X**) occur, at which time the output (**Z**) changes to '**0**'. In other words once there has been a pair of **1**'s in the input, the output should reflect whether the total number of **1**'s since the first pair of consecutive **1**'s is odd or even. **(4)**

(a):- Determine the output (**Z**) if the input (**X**) is the sequence --- **1010 1101 0011 10**

Answer: Z = 00000001110100

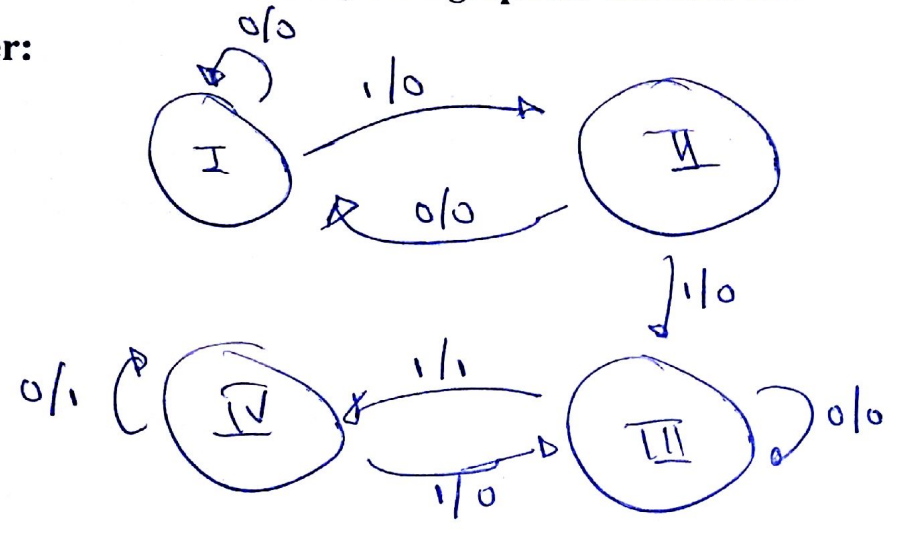
(b):- Determine a 4-state Moore state graph for this network.

Answer:



(c):- Determine a 4-state Mealy state graph for this network.

Answer:



Q5: - Find a logic expression in simplest SOP form for the VEM below. **(3)**

CD \ AB	00	01	11	10
00	0: 0	4: 0	12: 1	8: 1
01	1: $E+F$	5: $\bar{E}+F$	13: 1	9: F
11	3: EF	7: $\bar{E}$	15: $\bar{E}+\bar{F}$	11: 0
10	2: 0	6: 0	14: $\bar{F}$	10: $E\bar{F}$

ANSWER: - Minimized SOP function:

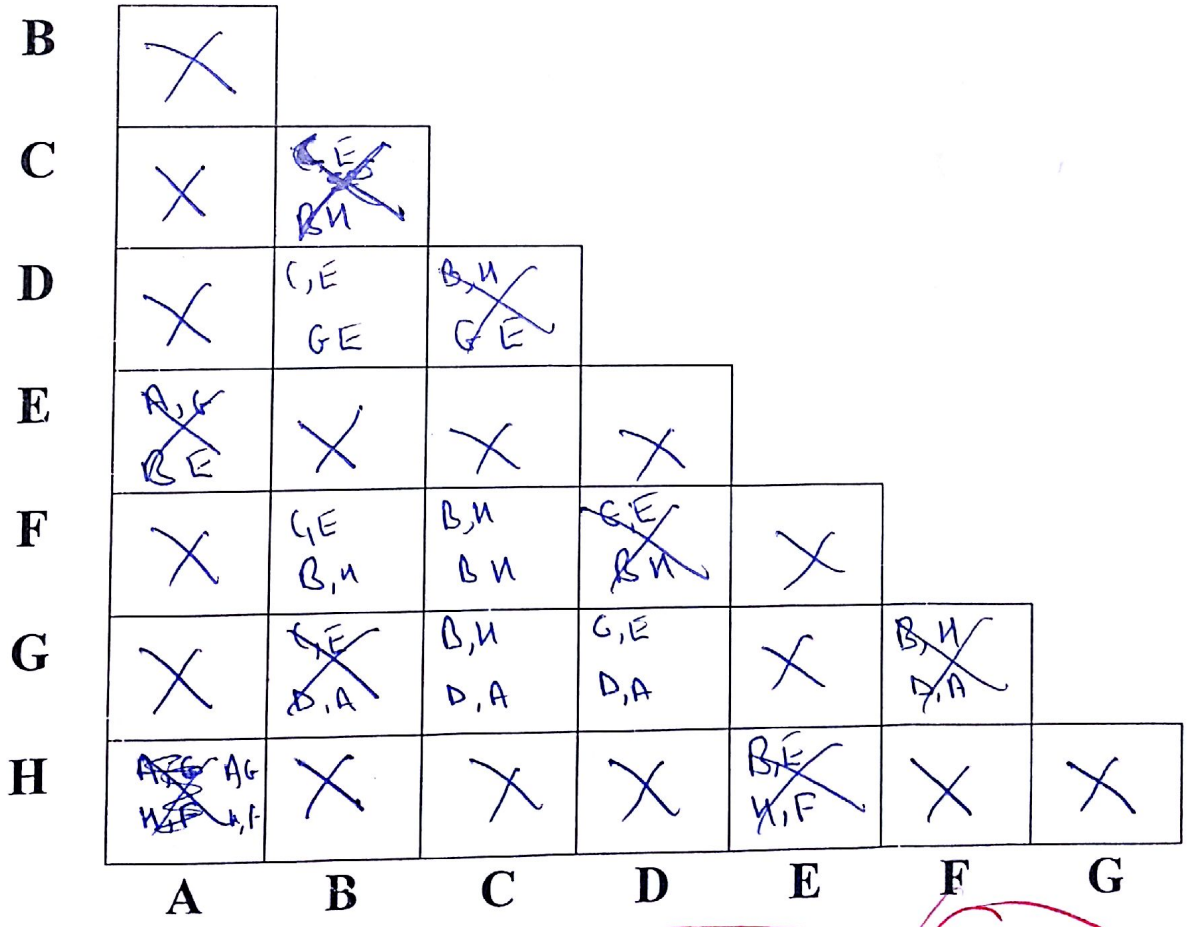
F (A, B, C, D, E, F) =

Q6:- Find out the equivalence in the table given using implication chart method.

List the equivalence clearly. **(3)**

P.S.	Next State		OUT PUT	
	X=0	X=1	X=0	X=1
A	A	G	0	1
B	C	E	0	0
C	B	H	0	0
D	G	E	0	0
E	B	E	0	1
F	B	H	0	0
G	D	A	0	0
H	H	F	0	1

Answer:

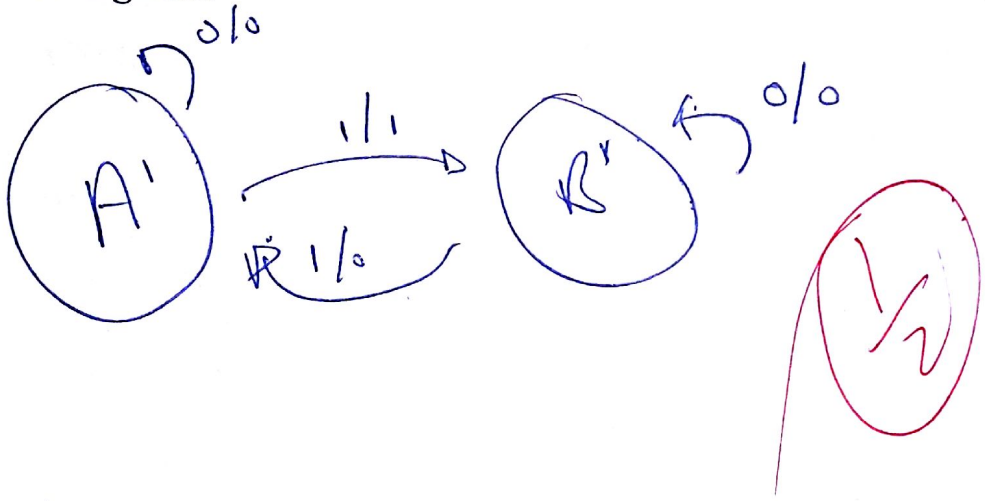


The following equivalence is there:

C = F = G ; B = D

(H = A) = E

Reduced state diagram:



Q6: - Minimize the logic function using **Quine-McCluskey** method. **(4)**

Y (A, B, C, D) = Σ m (0, 1, 2, 5, 6, 7, 8, 9, 10, 14)

The list of all prime implicants is as:

~~1,5~~ 5,7 ~~6,7~~ 0,1,8,9 ~~0,2,8,10~~ 2,6,10,14

(0 - 0 1), (0 1 – 1), (0 1 1 -), (- 0 0 –), (- 0 – 0), (- - 1 0).

Mention all essential prime implicants. Write the minimized function in SOP form. Write separately all terms to remove static-1 hazard if any. Use the space below.