ELECTRICAL ENGINEERING DEPARTMENT
EE201N DIGITAL ELECTRONIC CIRCUITS
MAJOR TEST

Date: November 25, 2013 Time: 3:30PM to 5:30PM

Note: Think before you ink. Write your Name, Entry Number and Group before you start filling up the main answer script and additional sheets if any.
A script without name or entry number will not be evaluated!
An incorrectly entered group number will attract 1 negative mark to pay for the efforts to locate your group number and enter your marks.
Where an explanation is asked for an answer without explanation will not beget any marks.
Keep your ID Card on the Table so that your identity can be verified at the time of marking your attendance.

Q1. a) Find out the logic realized by the TTL circuit given Fig. Q1a. Give explanations to arrive at your answer. (3 Marks)

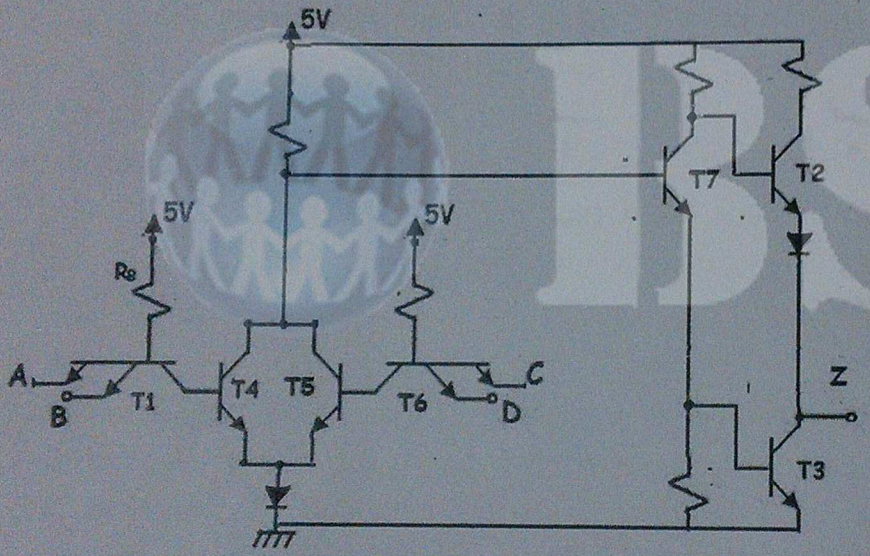

Fig. Q1a

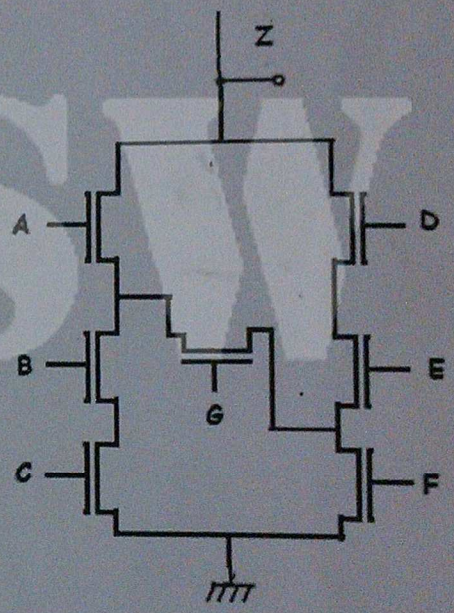

Fig. Q1c

b) Draw a CMOS gate to realize the function f(CBA) = Π (3, 5, 7) after minimization. (3 Marks)

c) Fig. Q1c gives the pull down (NMOS portion) of a CMOS logic. Write down the logic realized and commplete the circuit drawing the ~~pll down~~ pull up (PMOS portion) of the logic. (3 Marks)

Q2. a) Realize the following fuction using only 2 input NAND gates.

$$f(D,C,B,A)=D\bar{B}\bar{A}+CBA+C\bar{B}\bar{A}+\bar{D}C\bar{B}+\bar{D}\bar{C}A$$ (3 Marks)

b) Use only 4 to 1 Multiplexers to realize the function

$$f(D,C,B,A)=\Sigma(1,3,5,6,7,9,10,11,12,13,14,15)$$ (3 Marks)

Q3. A soft-drink wending machine with a choice of 2 different varieties of soft drinks is to be designed as a state machine. The events to be identified and executed are:

1. Recognise the insertion of a token and prompt choice
2. On registering the choice dispense the drink of choice.
3. If choice not registered return to rest state and eject the token.
4. Give an alarm if the choice of soft drink is not available and eject the token.
5. If the can is picked up return to the rest state else wait till the can is picked up.
6. Return to rest state if the can is not picked up in 5 minutes.

Identify and label the number of inputs required and the number of outputs to be generated and draw the State Transition Diagram to design the required machine. (8 Marks)

Q4. (a) Design two synchronous modulo 5 counters to count in the sequence (1,4,6,7,3). Use appropriate choice of +ve edge triggered T and D flipflops respectively to realize the counter using minimum number of logic gates. You may designate the output of the left most FF to be Q_2 and the right most as Q_0. (6 Marks)

(b) For your design, identify the maximum clock (square wave) frequency that can be used if the setup time, hold time and delay of each flip flop is 10 nsec. 8 nsec. and 12 nsec. respectively. The delay of each of the logic gates used, if any, is 5 nsec. (3 Marks)

Q5. Develop a finite state machine to implement a *parity-bit generator* that employs a Hamming code to generate the parity-bit. In this parity-bit generator, a 4-bit sequqential data is to be received; the first 3 bits constitute the message, and the fourth bit is always 0 (equivalent to a blank). This data when coded will have the 3-bit message, with added additional bit making the parity of the resulting (4)-bit sequential data odd. If the number of 1's in the 3-bit message is odd, the parity bit is to remain 0. If the number of 1's is even, a 1 bit is to be generated and inserted in the fourth position to make the parity of the 4-bit string odd. In either case, after the fourth bit, transition is to be to a reset state, in which the machine is ready to receive the next message sequence to be coded. Draw the State Transition Diagram and the design of the required machine. (8 Marks)

CHEERS and GOOD LUCK