Lab #16

Title: SERIAL LOAD SHIFT REGISTER
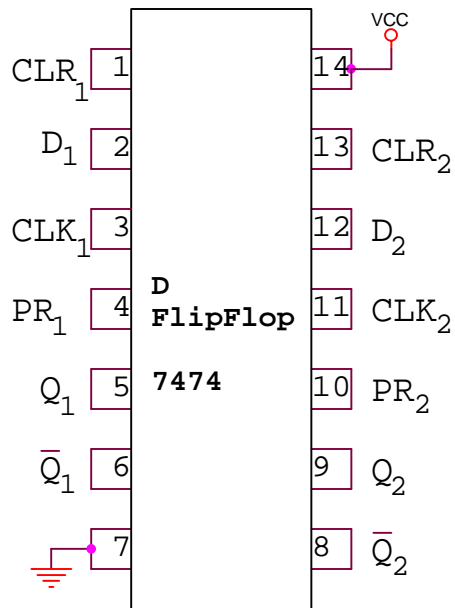
Materials:
[2] 7474 dual D flip-flop ICs
[1] clock (single pulse)

Procedure:

1. Insert 2 7474 ICs into the breadboard.
2. As drawn in class, wire a 4-bit, serial load, shift-right register. Use an input switch for the data (serial load) and one for the CLR input. Connect a single-pulse clock to the CLK input.
3. Clear data from the shift resister by placing the CLR switch to 0 and then back to 1. This is shown on lines 1 and 2 of Table 16-1.
4. Operate the shift register according to Table 16-1. Observe and record the results.

Questions: (answer on a separate piece of paper – **"Draw" means you must use a template**):

1. **Draw** a logic symbol diagram for an 8-bit serial load shift-register. Use eight D flip-flops. Label the inputs CLR, data, CLK; label the outputs A, B, C, D, E, F, G, and H.
2. The circuit constructed in this experiment could be described as a _____ (parallel, serial) -in _____ (parallel, serial) -out register.

CLR$_1$ [1]   VCC

D$_1$ [2]   [14]

CLK$_1$ [3]   [13] CLR$_2$

PR$_1$ [4]   **D FlipFlop**   [12] D$_2$

Q$_1$ [5]   **7474**   [11] CLK$_2$

$\overline{Q}_1$ [6]   [10] PR$_2$

[7]   [9] Q$_2$

[8] $\overline{Q}_2$

	Inputs			Outputs			
Line	Clear	Data	Clock pulse number	LED Indicators			
				A	B	C	D
1	0	1	0	0	0	0	0
2	1	1	0	0	0	0	0
3	1	1	1				
4	1	0	2				
5	1	0	3				
6	1	0	4				
7	1	0	5				
8	1	1	6				
9	1	1	7				
10	1	0	8				
11	1	0	9				
12	1	0	10				
13	1	0	11				
14	1	1	12				
15	1	1	13				
16	1	1	14				
17	1	1	15				
18	1	1	16				
19	1	0	17				
20	1	0	18				

Table 16-1 A serial Shift Register