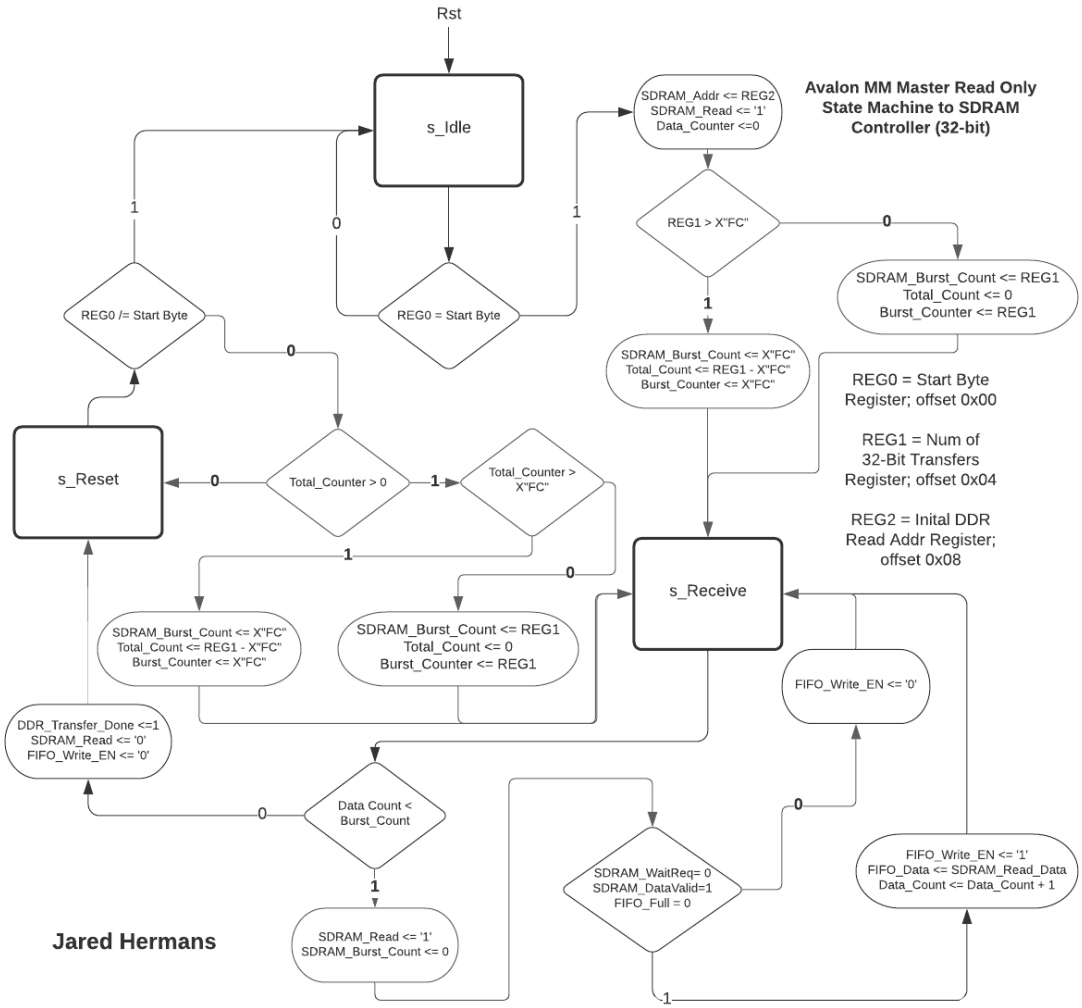
Description:

This IP is configured to use the SDRAM controller on the HPS to read DDR memory. The IP has 4 control registers which are accessed by software which specify the start address of the DDR transaction, the number of double-word (32-bit) reads, and the start bit. The additional 4th register goes high when the transaction completes. Once the transaction completes the IP must be reset by writing 0x0 in the start bit register.

The IP is capable of reading a 32-bit value from memory every clock cycle. The data is input into a FIFO buffer. The output of the buffer is 128 bits wide and it supports separate read and write clocks. With a $225\ MHz$ read clock on a DE-10 Standard SoC, the IP was measured to read at $770\ {}^{MB}/_{S}$. Read clocks at $250\ MHz$ and above cause timing issues in which the IP will not perform as expected.

State Machine:



Implementation:

In QSYS, an Avalon MM bus master, created using a state machine, connects to the f2h_sdram0_data Avalon Slave in the Arria V/Cyclone V Hard Processor System. It is important that the width of the SDRAM Avalon Slave is 32-Bits which is the same width as the Avalon Master. The HPS SDRAM clock and the SDRAM clock of the IP must be the same clock. A clock of up to $200\ MHz$ was tested.

The Control Avalon MM Slave of the IP can be connected to either h2f_lw_axi_master or h2f_axi_master in the HPS IP. To write to the control registers via software, the address offsets must be added to the bus addresses.

The FIFO buffer is generated from Intel's IP catalog. It is set up to output 128-bit output values so the number of transactions should be divisible by 4. The output data width can be easily changed by regenerating the IP.

Address Offsets:

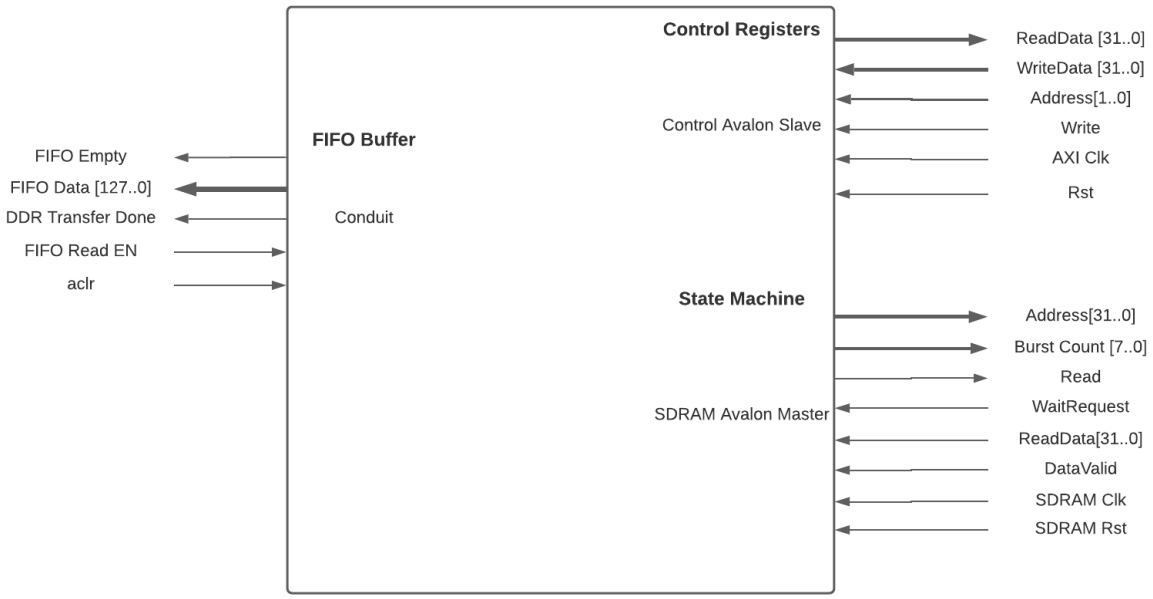
- Start Byte offset: 0x00 (Write) - Write 0x1 to this address to start the transaction. Only do so when the start address and number of transactions have been specified. Once the transfer is complete, write 0x0 to this address to reset it or the IP will not perform another read.
- Number of transactions offset: 0x04 (Write) - Write the number of 32-bit transactions for the IP to perform to this address.
- Initial DDR address offset: 0x08 (Write) - Write the initial DDR 32-bit address value from which to start reading from.
- DDR Transfer Done offset: 0x0C (Read) - This address reads 0x0 when IP is in idle state and in transfer state. Value goes to 0x1 as soon as last value is registered into buffer.

Conduit Ports:

There are several signals that can be exported to your VHDL code from the IP. These signals are:

- FIFO_aclr - asynchronous clear for FIFO buffer
- FIFO_Read_EN - read enable for buffer
- FIFO_Data - output data from buffer (128-bit)
- FIFO_Empty - buffer empty signal
- DDR_Transfer_Done - Done signal for DDR read. Goes high as soon as last value is registered into the buffer.

Diagram:


Control Registers
ReadData [31..0]
WriteData [31..0]
Address[1..0]
Control Avalon Slave
Write
AXI Clk
FIFO Buffer
FIFO Empty
FIFO Data [127..0]
Rst
DDR Transfer Done
Conduit
FIFO Read EN
aclr
State Machine
Address[31..0]
Burst Count [7..0]
Read
SDRAM Avalon Master
WaitRequest
ReadData[31..0]
DataValid
SDRAM Clk
SDRAM Rst