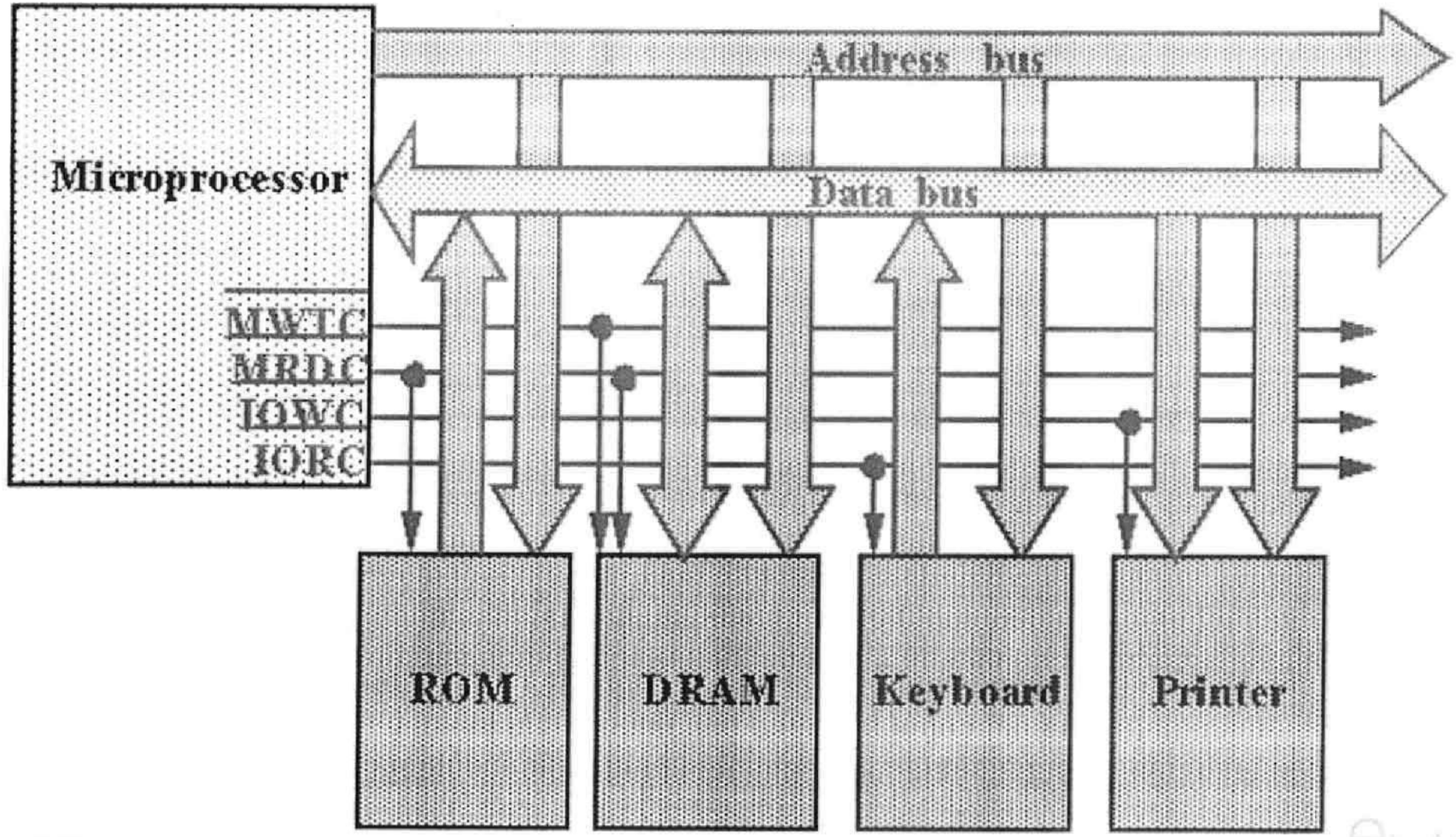
UNIT 3 Syllabus

- Memory Interfacing & I/O interfacing
- Parallel communication interface {**8255 PPI**} Important
- Serial communication interface {**8251 USART**} Important
- D/A and A/D Interface {**ADC 0800/0809,DAC 0800**}
- Timer {or counter} – {**8253/8254 Timer**}
- Keyboard /display controller {**8279**} Important
- Interrupt controller {**8259**}
- DMA controller {**8237/8257**} Important
- Programming and applications Case studies
  1. Traffic Light control Important
  2. LED display
  3. LCD display
  4. Keyboard display interface
  5. Alarm Controller

Data Transfers

- **Synchronous** ----- Usually occur when peripherals are located within the same computer as the CPU. Close proximity allows all state bits change at same time on a common clock.
- **Asynchronous** ----- Do not require that the source and destination use the same system clock.

Memory & IO Interfacing



MEMORY DEVICES

I/O DEVICES

- interface memory (RAM, ROM, EPROM'...) or I/O devices to 8086 microprocessor. Several **memory chips** or **I/O devices** can connected to a microprocessor. An address decoding circuit is used to select the required I/O device or a memory chip.

IO mapped IO V/s Memory Mapped IO

Memory Mapped IO

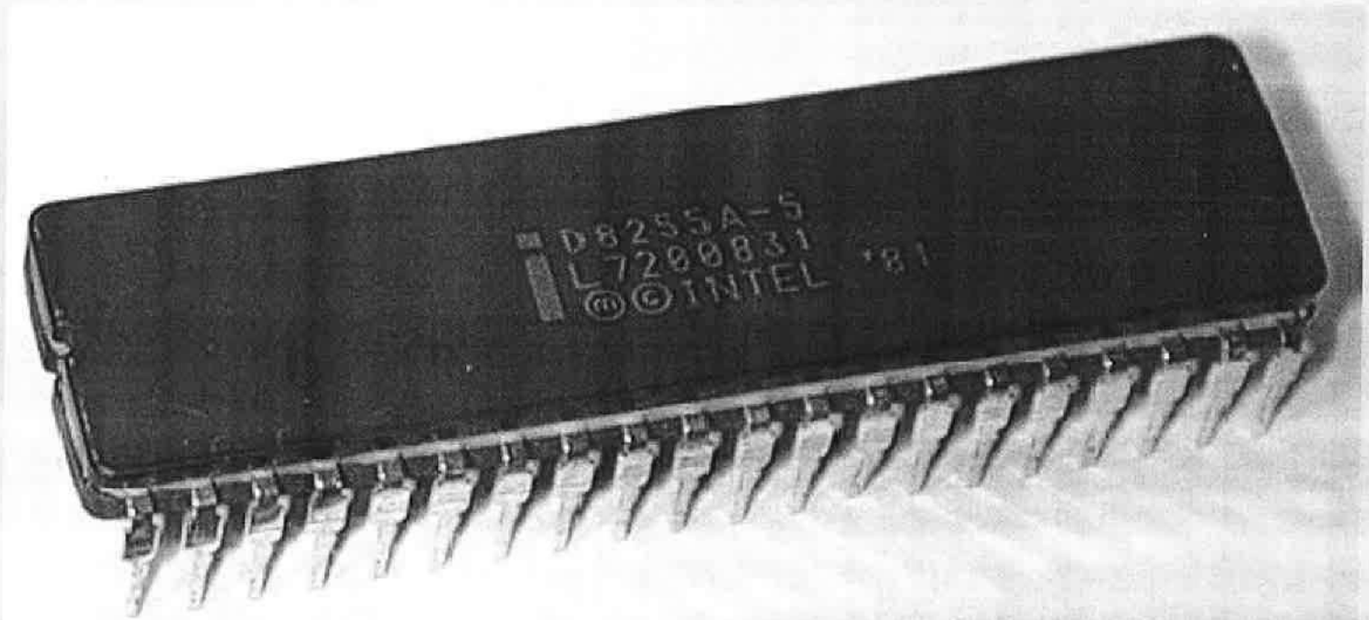
- IO is treated as memory.
- 16-bit addressing.
- More Decoder Hardware.
- Can address 2^{16}=64k locations.
- Less memory is available.

IO Mapped IO

- IO is treated IO.
- 8- bit addressing.
- Less Decoder Hardware.
- Can address 2^{8}=256 locations.
- Whole memory address space is available.

Memory Mapped IO	IO Mapped IO
• Memory Instructions are used.	• Special Instructions are used like IN, OUT.
• Memory control signals are used.	• Special control signals are used.
• Arithmetic and logic operations can be performed on data.	• Arithmetic and logic operations can not be performed on data.
• Data transfer b/w register and IO.	• Data transfer b/w accumulator and IO.

Parallel communication interface INTEL 8255

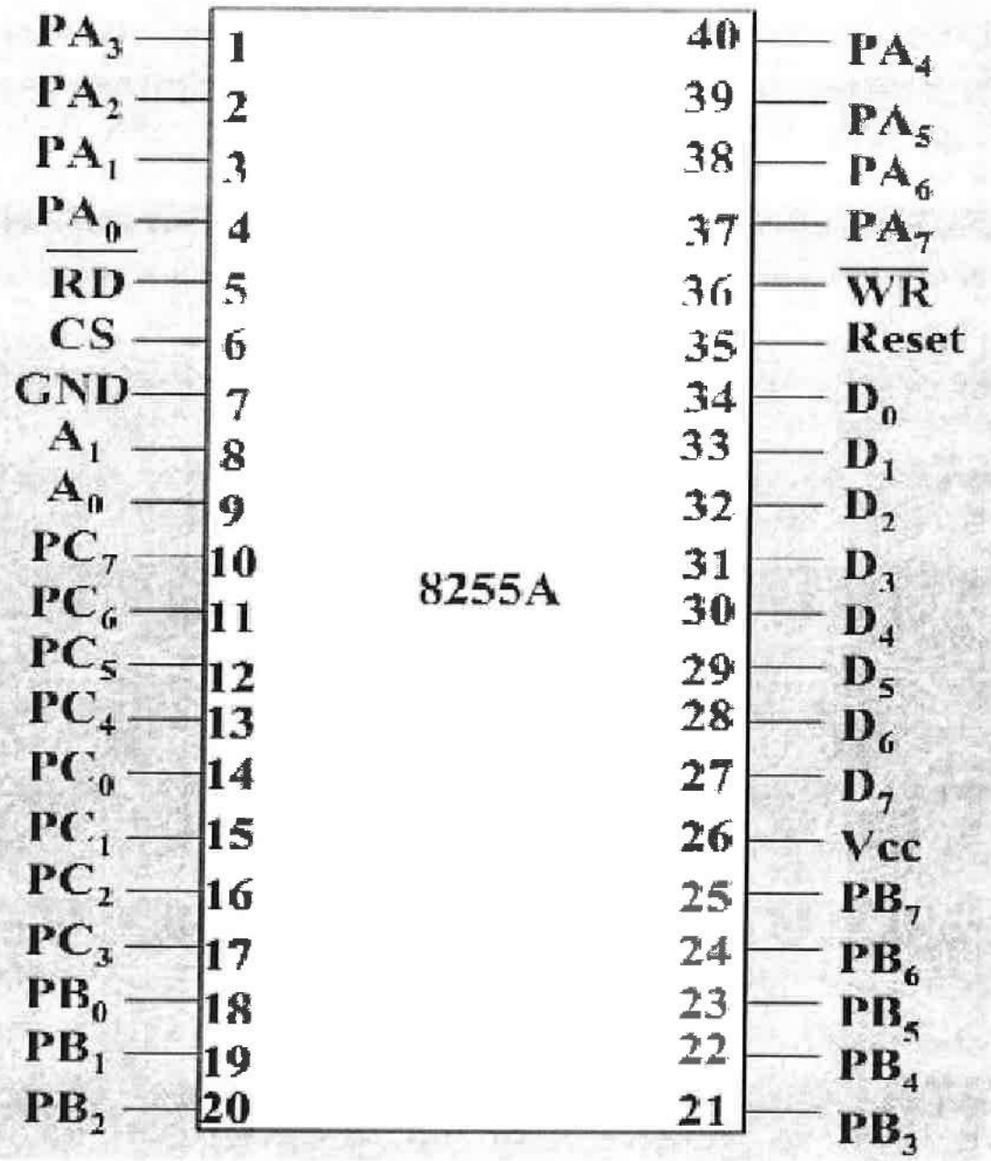


Presented by C.GOKUL,AP/EEE , Velalar College of Engg & Tech, Erode

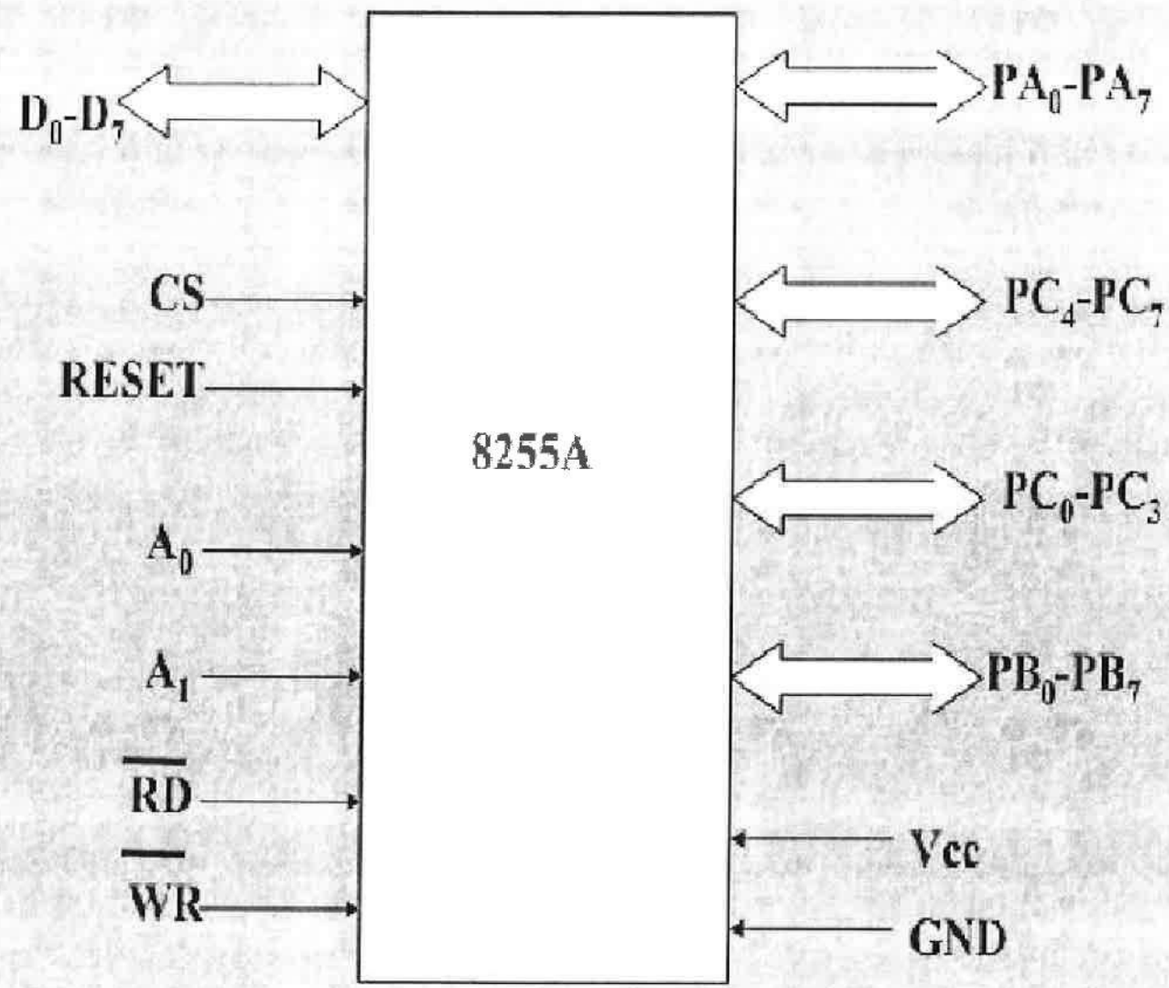
8255 PPI

- The **8255** chip is also called as **Programmable Peripheral Interface**.
- The Intel's 8255 is designed for use with Intel's 8-bit, 16-bit and higher capability microprocessors
- The 8255 is a 40 pin integrated circuit (IC), designed to perform a variety of interface functions in a computer environment.
- It is flexible and economical.

PIN DIAGRAM OF 8255



Signals of 8085



8255 PIO/PPI

- It has **24 input/output** lines which may be individually programmed.
- 2 groups of I/O pins are named as

  Group A (Port-A & Port C Upper)

  Group B (Port-B & Port C Lower)
- **3 ports**(each port has 8 bit)

  Port A lines are identified by symbols **PA_0-PA_7**

  Port B lines are identified by symbols **PB_0-PB_7**

  Port C lines are identified by **PC_0-PC_7 , PC3-PC0**

ie: **PORT C UPPER(PC7-PC4) , PORT C LOWER(PC3-PC0)**

D0 - D7: data input/output lines for the device. All information read from and written to the 8255 occurs via these 8 data lines.

$\overline{\text{CS}}$ (*Chip Select*). If this line is a logical 0, the microprocessor can read and write to the 8255.

RESET : The 8255 is placed into its reset state if this input line is a logical 1

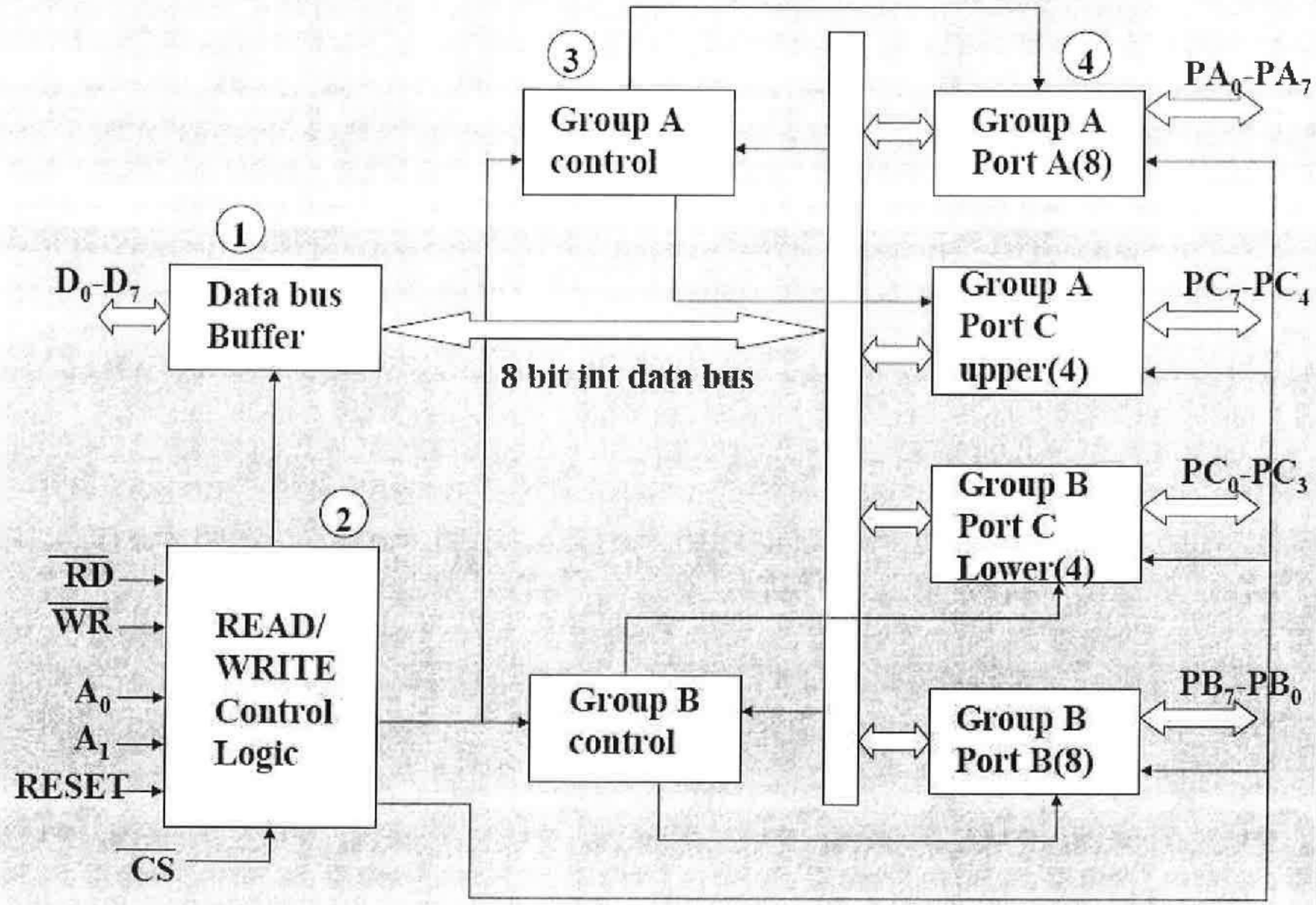
- **$\overline{RD}$:** This is the input line driven by the microprocessor and should be **low** to indicate **read operation** to 8255.
- **$\overline{WR}$:** This is an input line driven by the microprocessor. A **low** on this line indicates **write operation**.
- **A1-A0 :** These are the address input lines and are driven by the microprocessor.

Control Logic

- $\overline{CS}$ signal is the master Chip Select
- A0 and A1 specify one of the two I/O Ports

$\overline{CS}$	A1	A0	Selected
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Register
1	X	X	8255 is not selected

Block Diagram of 8255A



Block Diagram of 8255 (Architecture)

It has a 40 pins of 4 parts.

1. Data bus buffer
2. Read/Write control logic
3. Group A and Group B controls
4. Port A, B and C

1. Data bus buffer

- This is a tristate bidirectional buffer used to interface the 8255 to system data bus. Data is transmitted or received by the buffer on execution of input or output instruction by the CPU.

2. Read/Write control logic

- This unit accepts control signals (RD, WR) and also inputs from address bus and issues commands to individual group of control blocks (Group A, Group B).
- It has the following pins.

$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RESET , A1 , A0

3. Group A and Group B controls

- These block **receive control** from the **CPU** and **issues commands** to their respective ports.

  Group A - PA and PCU (PC7 –PC4)

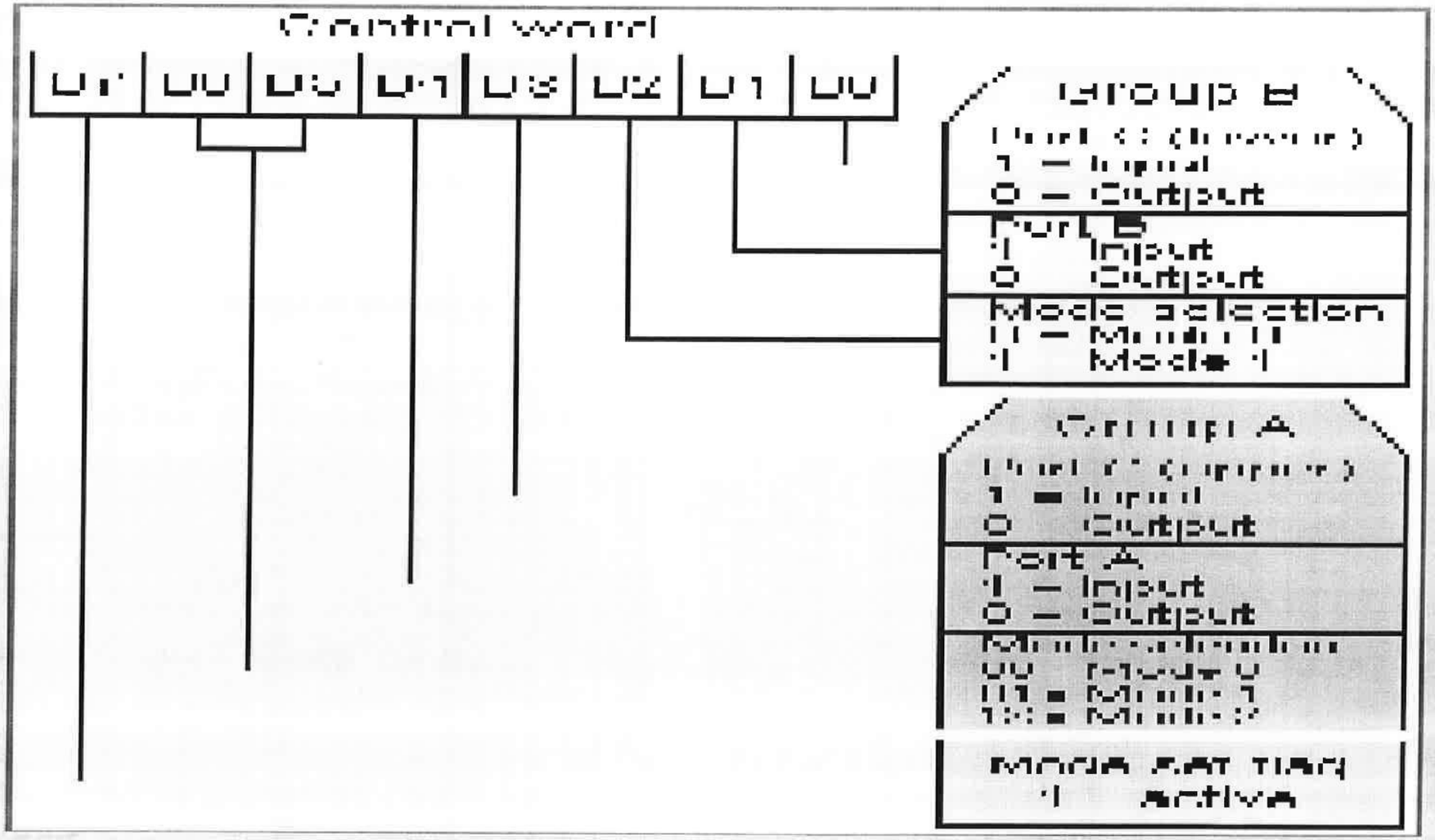
  Group B – PB and PCL (PC3 –PC0)

a) Port A: This has an 8 bit latched/buffered O/P and 8 bit input latch. It can be programmed in 3 modes – **mode 0, mode 1, mode 2.**

b) **Port B:** It can be programmed in **mode 0, mode1**

c) **Port C :** It can be programmed in **mode 0**

CONTROL WORD REGISTER(CWR)



Modes of Operation of 8255

- Bit Set/Reset(BSR) Mode
  - Set/Reset bits in Port C
- I/O Mode
  - Mode 0 (Simple input/output)
  - Mode 1 (Handshake mode)
  - Mode 2 (Bidirectional Data Transfer)

1. BSR Mode

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	X	X	X	B_2	B_1	B_0	S/R

Always 0 for BSR mode

Don't care

Port C bit select

Set/Reset

8255 Control Register format for BSR Mode

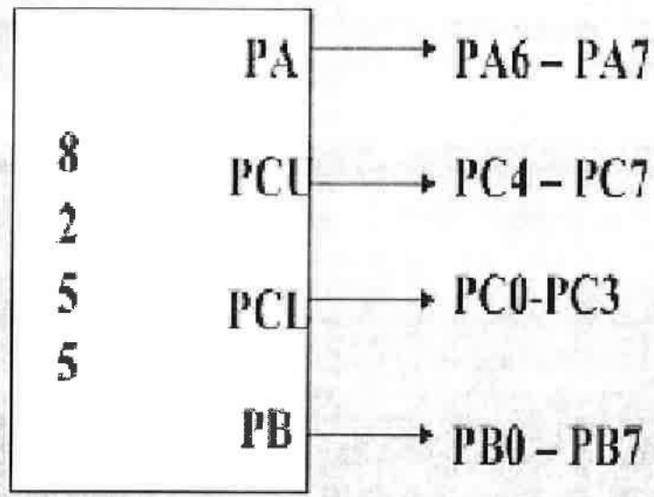
B3	B2	B1	Bit/pin of port C selected
0	0	0	PC_0
0	0	1	PC_1
0	1	0	PC_2
0	1	1	PC_3
1	0	0	PC_4
1	0	1	PC_5
1	1	0	PC_6
1	1	1	PC_7

Concerned only with the 8-bits of Port C.
Set or Reset by control word
Ports A and B are not affected

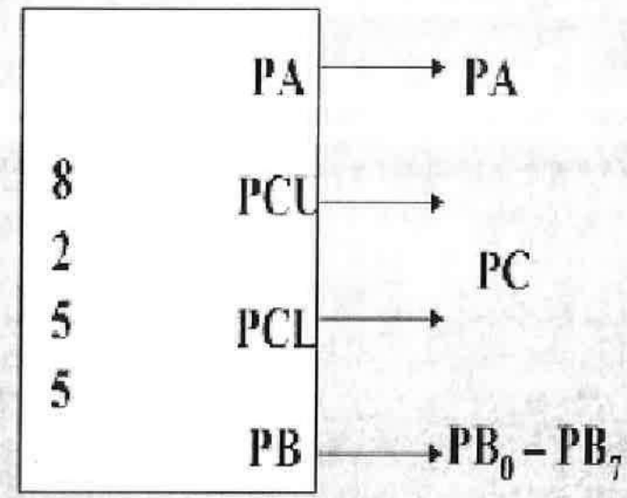
2. I/O MODE

a) Mode 0 (Simple Input or Output):

- Ports A and B are used as Simple I/O Ports
- Port C as two 4-bit ports
- **Features**
  - Outputs are latched
  - Inputs are not latched
  - Ports do not have handshake or interrupt capability



All Output



Port A and Port C acting as O/P. Port B acting as I/P

Mode 0

b) Mode 1: (Input or Output with Handshake)

- Handshake signals are exchanged between MPU & Peripherals
  - **Features**
    - Ports A and B are used as Simple I/O Ports
    - Each port uses 3 lines from Port C as handshake signals
    - Input & Output data are latched
    - interrupt logic supported

c) Mode 2: Bidirectional Data Transfer

- Used primarily in applications such as data transfer between two computers
- Features
  - Ports A can be configured as the bidirectional Port
  - Port B in Mode 0 or Mode 1.
  - Port A uses 5 Signals from Port C as handshake signals for data transfer
  - Remaining 3 Signals from Port C Used as – Simple I/O or handshake for Port B

Find control word

(1) Port A: output with handshake

(2) Port B: input with handshake

(3) Port CL: output (4)Port CU: input

⌘ **Solution:**

1	0	1	0	1	1	1	0

$= AE_H$

Find the control word for the register arrangement of the ports of Intel 8255 for mode 0 operation.

- Port A: Output, Port B: Output,
- Port CU: Output, Port CL: Output

Solution:

1	0	0	0	0	0	0	0

$= 80_H$

The control word register for the above ports of Intel 8255 is 80_H.

Find the control word for the register arrangement of the ports of Intel 8255 for mode 0 operation.

- Port A: Input, Port B: Input,
- Port CU: Input, Port CL: Input

<u>Solution</u>:

1	0	0	1	1	0	1	1	= $9B_H$

The control word register for the above ports of intel 8255 is 9BH.

Basics of serial communication

1. **Transmitter:**

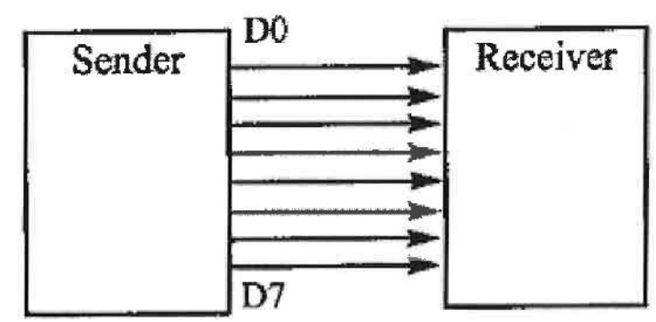
- A parallel-in, serial-out shift register

Serial Transfer

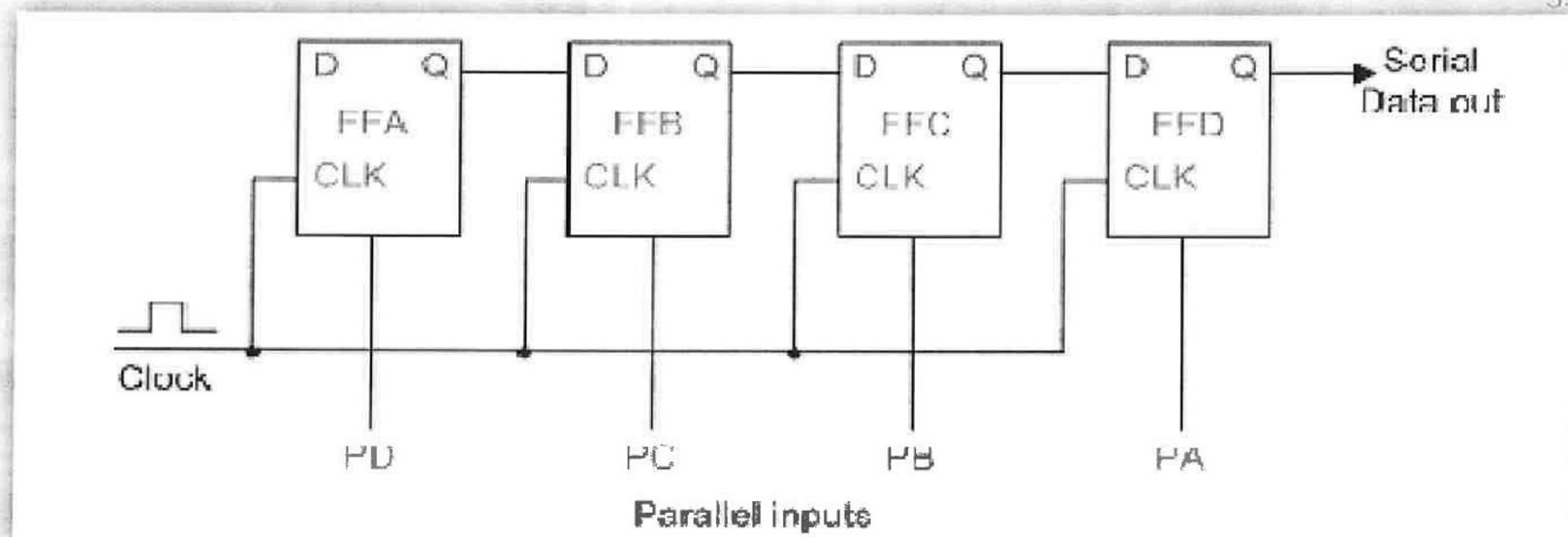
2. **Receiver:**

- A serial-in, parallel-out shift register.

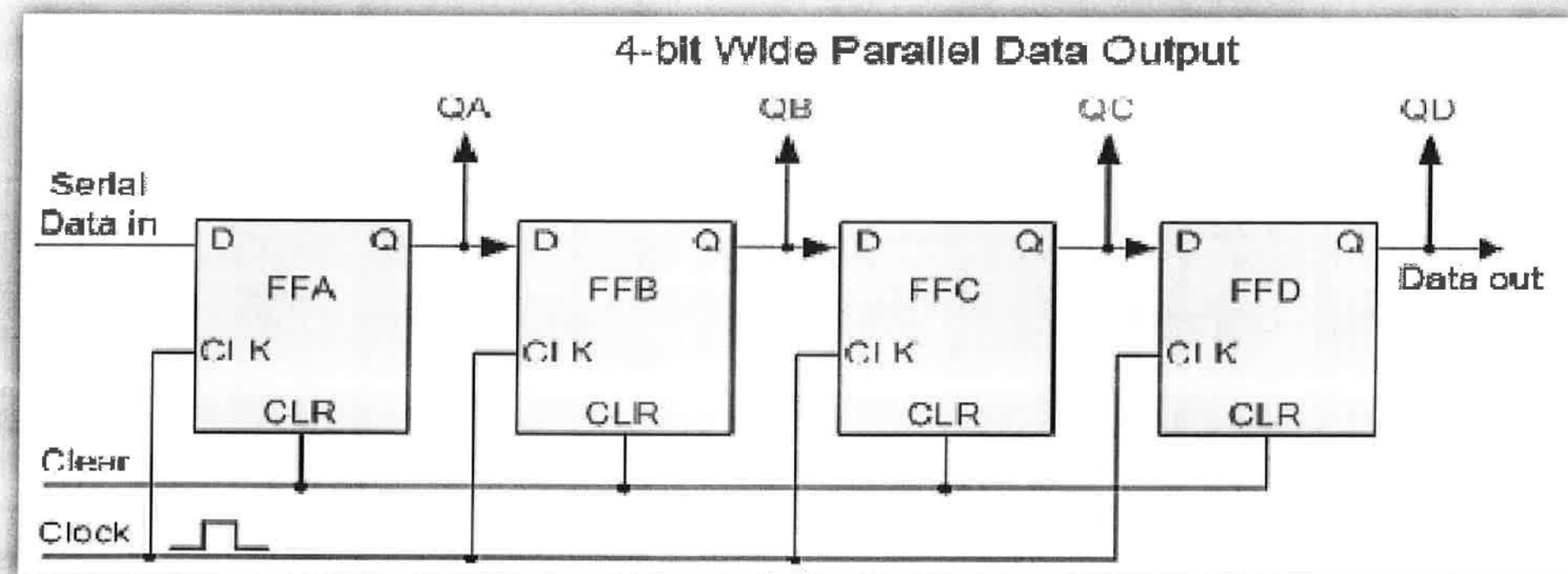
Parallel Transfer



TRANSMITTER



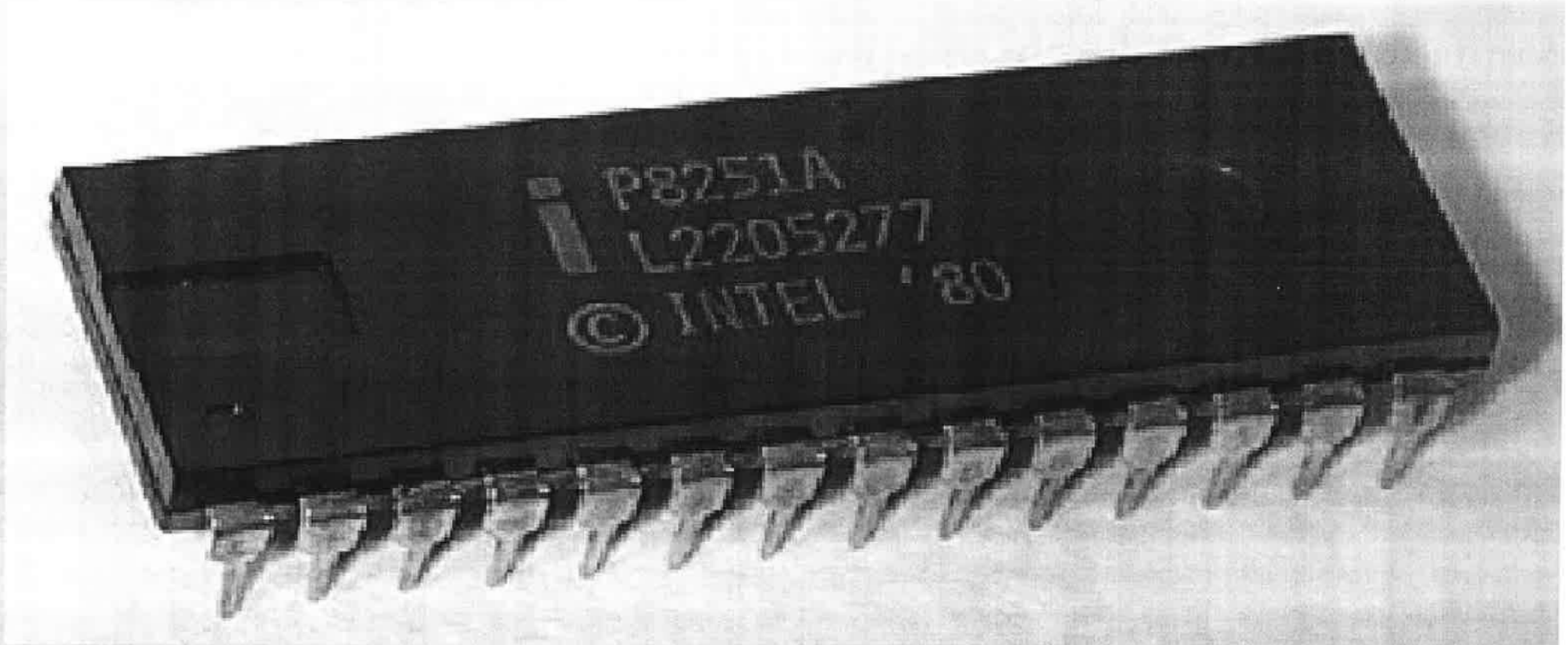
Receiver



Serial communication interface

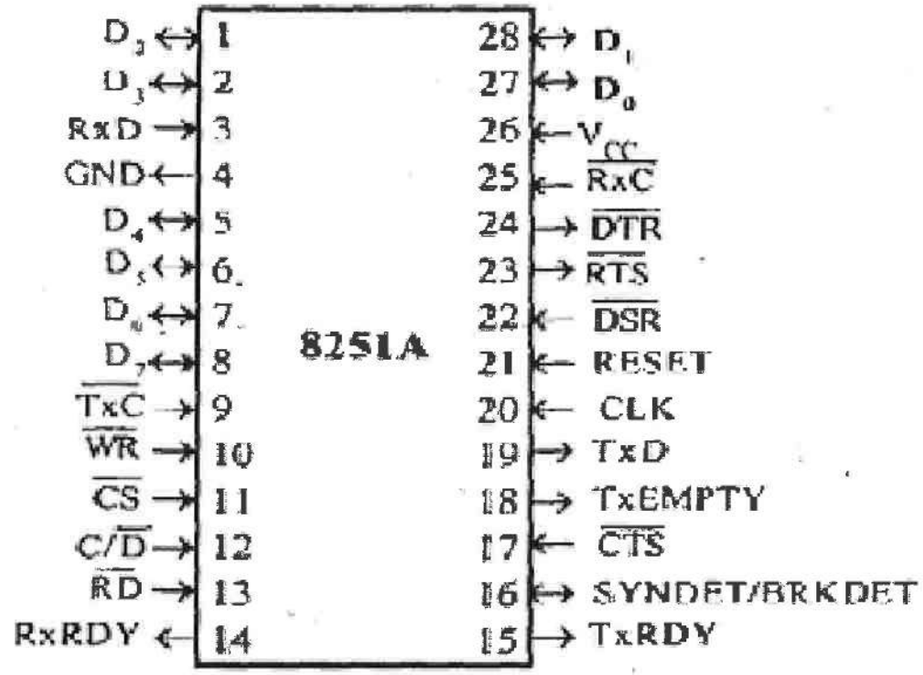
Important

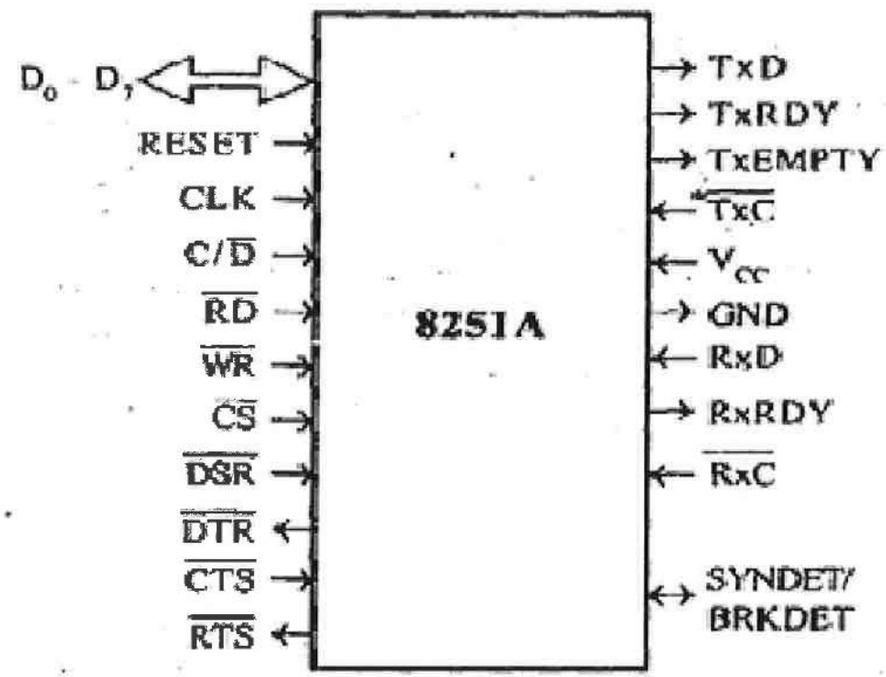
INTEL 8251 USART



UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (USART)

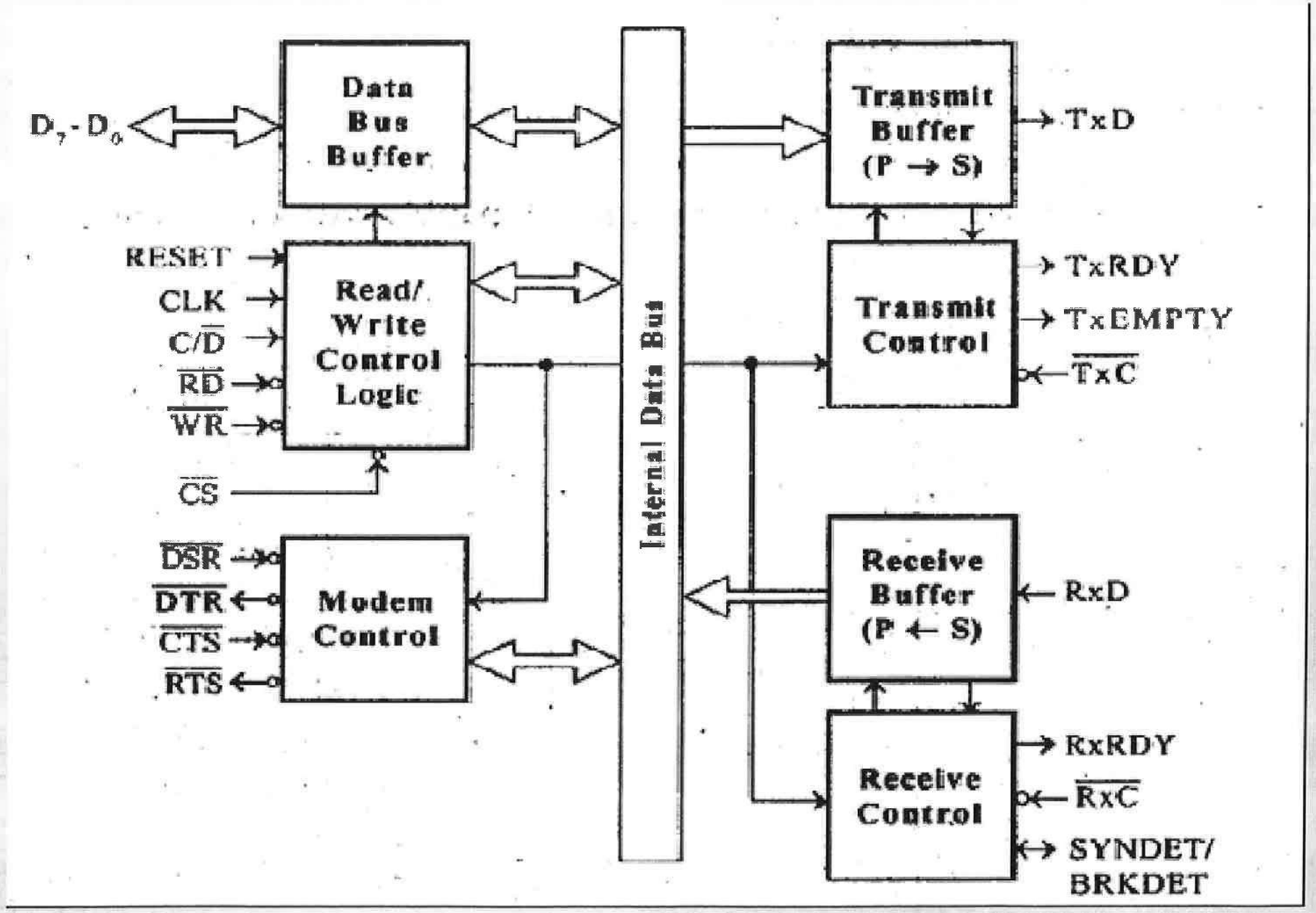
- Programmable chip designed for synchronous and asynchronous serial data transmission
- 28 pin DIP
- Coverts the parallel data into a serial stream of bits suitable for **serial transmission.**
- Receives a serial stream of bits and convert it into parallel data bytes to be read by a microprocessor.





Pin	Description
D_0-D_7	Parallel data
C/$\overline{D}$	Control register or Data buffer select
$\overline{RD}$	Read control
$\overline{WR}$	Write control
$\overline{CS}$	Chip Select
CLK	Clock pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready
TxRDY	Transmitter Ready
$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET/ BRKDET	Synchronous Detect / Break Detect
$\overline{RTS}$	Request To Send Data
$\overline{CTS}$	Clear To Send Data
TxEMPTY	Transmitter Empty
V_{cc}	Supply (+5V)
GND	Ground (0 V)

BLOCK DIAGRAM



Five Sections

- Read/Write Control Logic
  - Interfaces the chip with MPU
  - Determine the functions according to the control word
  - Monitors data flow
- Transmitter
  - Converts parallel word received from MPU into serial bits
  - Transmits serial bits over TXD line to a peripheral.
- Receiver
  - Receives serial bits from peripheral
  - Converts serial bits into parallel word
  - Transfers the parallel word to the MPU
- Data Bus Buffer- 8 bit Bidirectional bus.
- Modem Controller
  - Used to establish data communication modems over telephone line

Input Signals

- $\overline{CS}$ – Chip Select
  - When this signal goes **low**, 8251 is selected by MPU for communication
- C/$\overline{D}$ – Control/Data
  - When this signal is **high**, the **control register** or status register is addressed
  - When it is **low**, the **data buffer** is addressed
  - Control and Status register is differentiated by $\overline{WR}$ and $\overline{RD}$ signals, respectively

- $\overline{WR}$ – Write
  - writes in the control register or sends outputs to the data buffer.
  - This connected to IOW or MEMW
- $\overline{RD}$ – Read
  - Either reads a status from status register or accepts data from the data buffer
  - This is connected to either IOR or MEMR
- RESET - Reset
- CLK - Clock
  - Connected to system clock
  - Necessary for communication with microprocessor.

$\overline{CS}$	$C/\overline{D}$	$\overline{RD}$	$\overline{WR}$	Function
0	1	1	0	MPU writes instruction in the control register
0	1	0	1	MPU reads status from the status register
0	0	1	0	MPU outputs the data to the Data Buffer
0	0	0	1	MPU accepts data from the Data Buffer
1	X	X	X	USART is not Selected

- Control Register
  - 16-bit register
  - This register can be accessed an output port when the C/D pin is high
- Status Register
  - Checks ready status of a peripheral
- Data Buffer

Transmitter Section

- Accepts parallel data and converts it into serial data
- Two registers
  - Buffer Register
    - To hold eight bits
  - Output Register
    - Converts eight bits into a stream of serial bits
  - Transmits data on TxD pin with appropriate framing bits(Start and Stop)

Signals Associated with Transmitter Section

- TxD – Transmit Data
  - Serial bits are transmitted on this line
- TxC – Transmitter Clock
  - Controls the rate at which bits are transmitted
- TxRDY – Transmitter Ready
  - Can be used either to interrupt the MPU or indicate the status
- TxE – Transmitter Empty
  - Logic 1 on this line indicate that the output register is empty

Receiver Section

- Accepts serial data from peripheral and converts it into parallel data
- The section has two registers
  - Input Register
  - Buffer Register

Signals Associated with Receiver Section

- RxD – Receive Data
  - Bits are received serially on this line and converted into parallel byte in the receiver input
- RxC – Receiver Clock
- RxRDY – Receiver Ready
  - It goes high when the USART has a character in the buffer register and is ready to transfer it to the MPU

Signals Associated with Modem Control

- DSR- Data Set Ready
  - Normally used to check if the Data Set is ready when communicating with a modem
- DTR – Data Terminal Ready
  - device is ready to accept data when the 8251 is communicating with a modem.
- RTS – Request to send Data
  - the receiver is ready to receive a data byte from modem
- CTS – Clear to Send

Control words

There are two types of control word.

1. Mode instruction (setting of function)

2. Command (setting of operation)

1) Mode Instruction

Mode instruction is used for setting the function of the 8251. Mode instruction will be in "wait for write" at either internal reset or external reset. That is, the writing of a control word after resetting will be recognized as a "mode instruction."

Items set by mode instruction are as follows:

- Synchronous/asynchronous mode
- Stop bit length (asynchronous mode)
- Character length
- Parity bit
- Baud rate factor (asynchronous mode)

- Internal/external synchronization (synchronous mode)

- Number of synchronous characters (Synchronous mode)

The bit configuration of mode instruction is shown in Figures 2 and 3. In the case of synchronous mode, it is necessary to write one-or two byte sync characters. If sync characters were written, a function will be set because the writing of sync characters constitutes part of mode instruction.

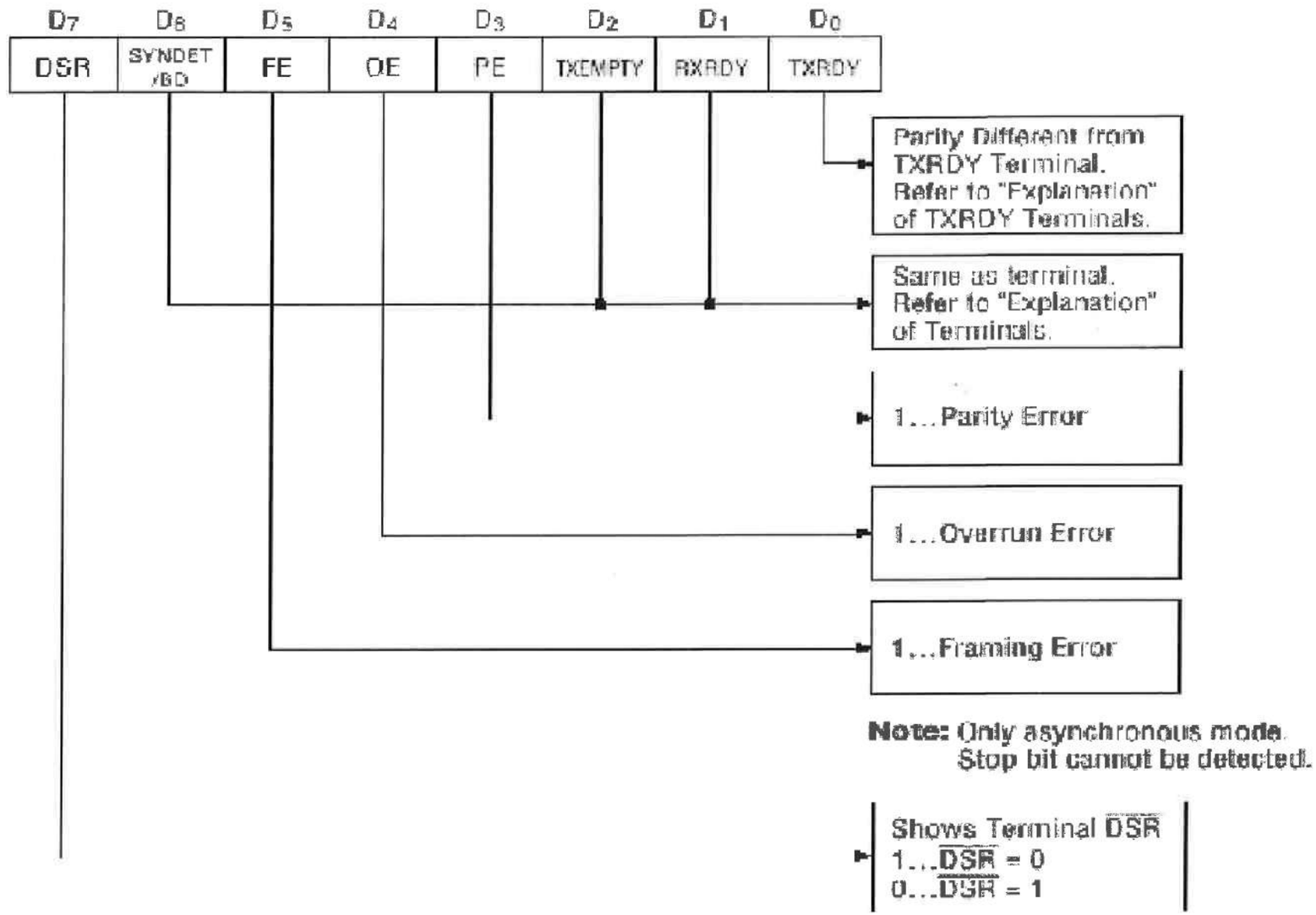


Fig. 5 Bit Configuration of Status Word

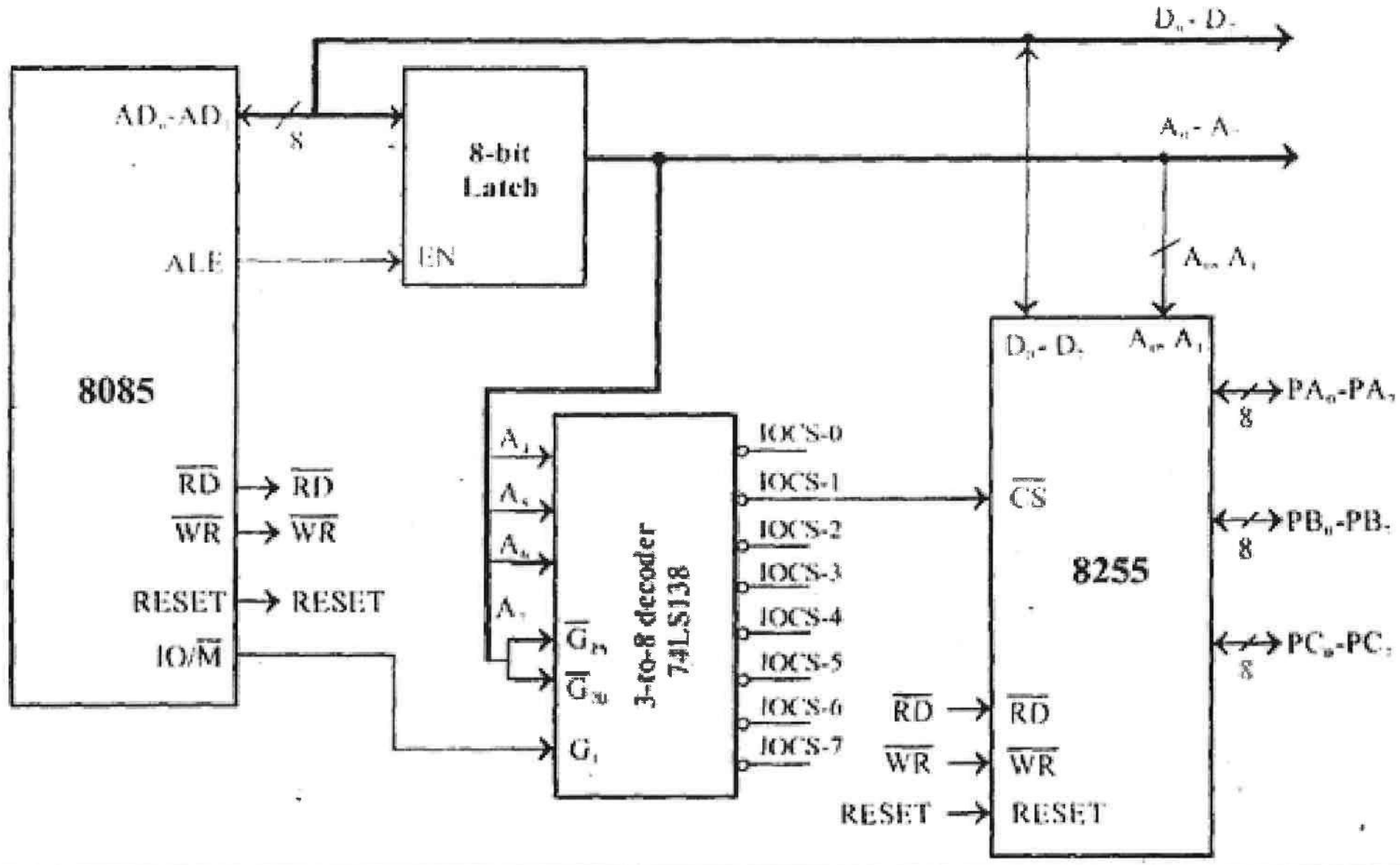
2) Command

Command is used for setting the operation of the 8251. It is possible to write a command whenever necessary after writing a mode instruction and sync characters.

Items to be set by command are as follows:

- Transmit Enable/Disable
- Receive Enable/Disable
- DTR, RTS Output of data.
- Resetting of error flag.
- Sending to break characters
- Internal resetting
- Hunt mode (synchronous mode)

Interfacing of 8255(PPI) with 8085 processor:

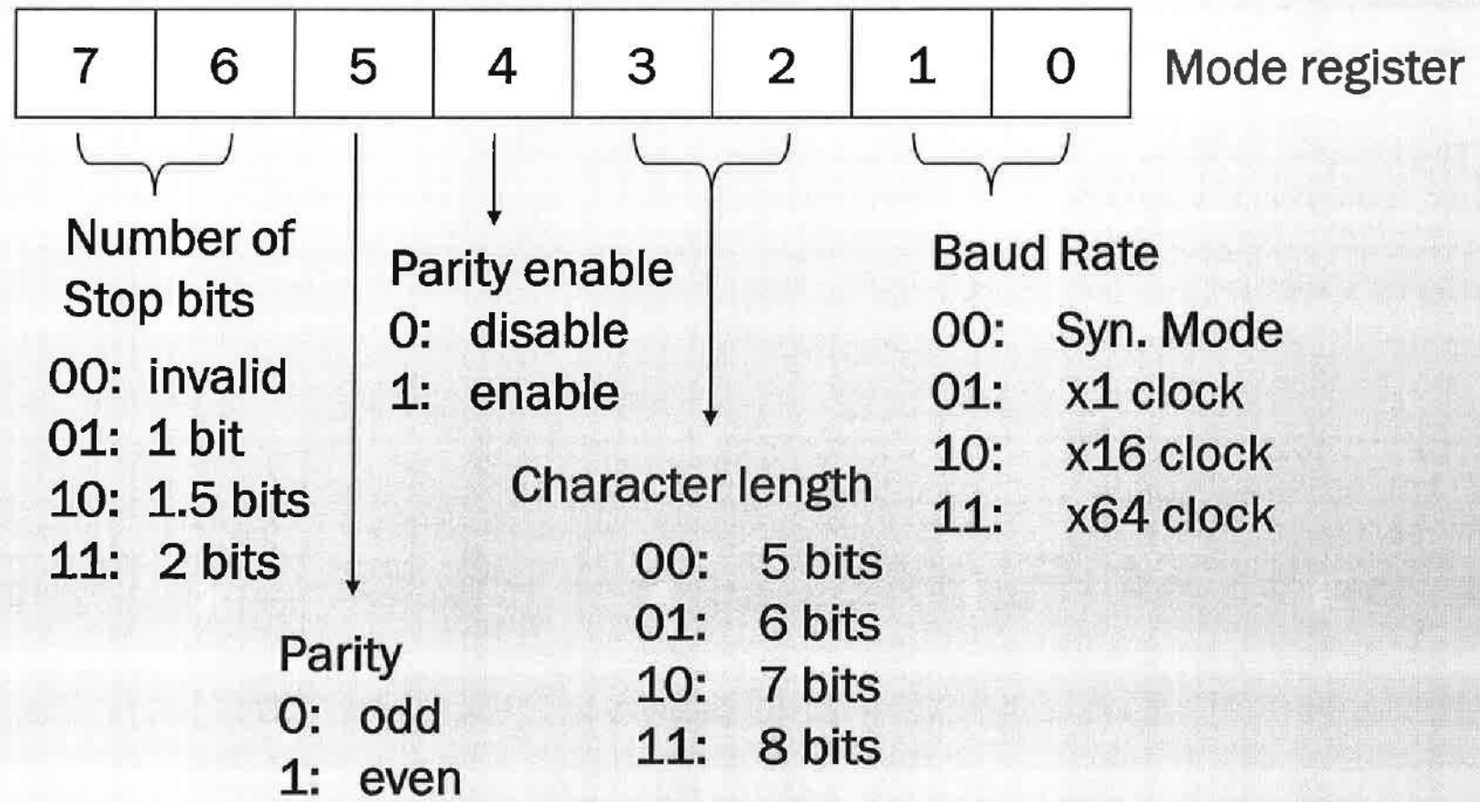


Internal Device	Binary Address								Hexa Address
	Decoder input and enable				Input to address pins of 8255				
	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Port-A	0	0	0	1	x	x	0	0	10
Port-B	0	0	0	1	x	x	0	1	11
Port-C	0	0	0	1	x	x	1	0	12
Control Register	0	0	0	1	x	x	1	1	13

Note : *Don't care "x" is considered as zero.*

Programming 8251

- 8251 mode register



❑ 8251 command register

EH	IR	RTS	ER	SBRK	RxE	DTR	TxE

command register

TxE: transmit enable

DTR: data terminal ready, $\overline{\text{DTR}}$ pin will be low

RxE: receiver enable

SBPRK: send break character, TxD pin will be low

ER: error reset

RTS: request to send, $\overline{\text{CTS}}$ pin will be low

IR: internal reset

EH: enter hunt mode (1=enable search for SYN character)

- 8251 status register

DSR	SYNDET	FE	OE	PE	TxEMPTY	RxRDY	TxRDY

status register

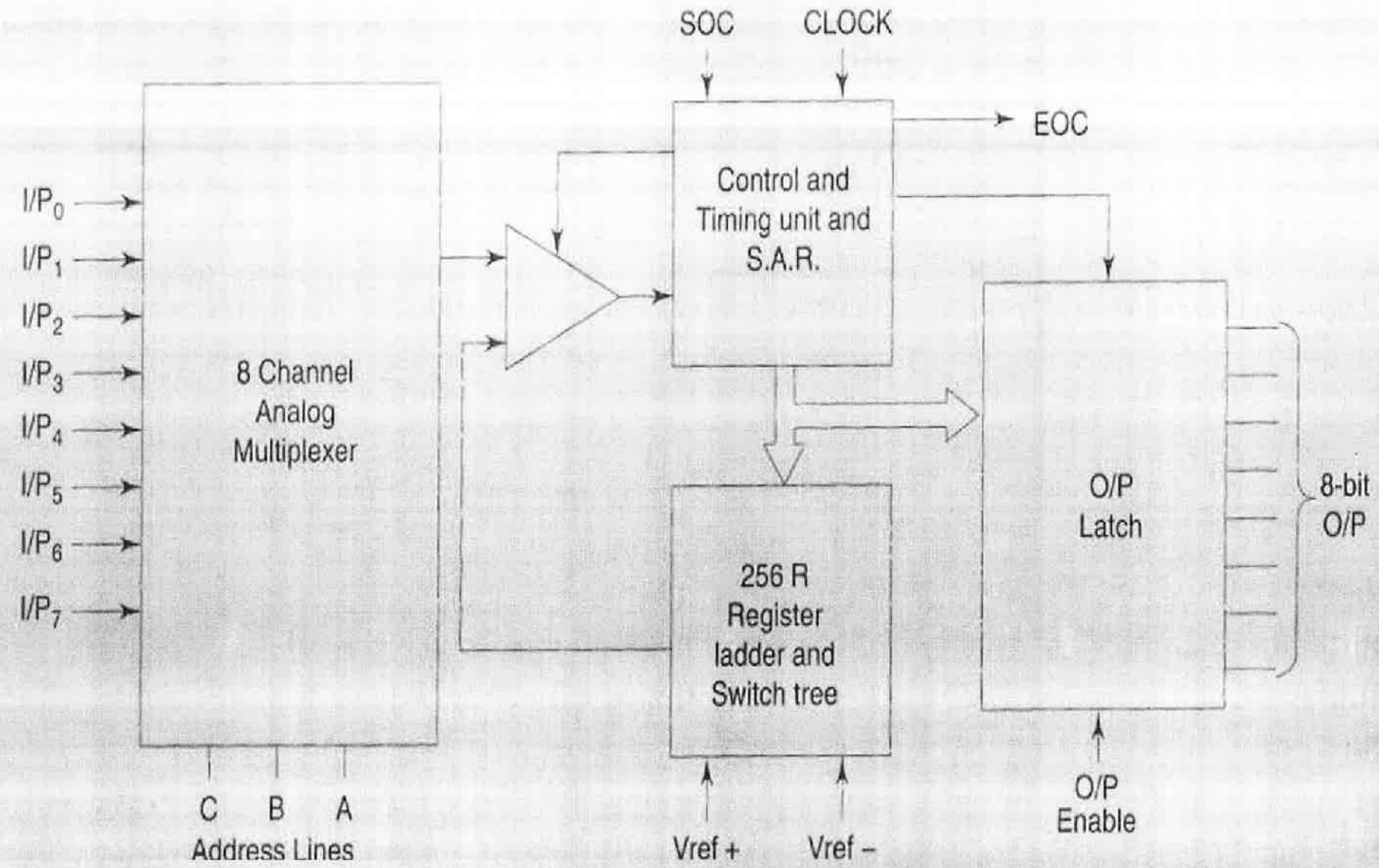
TxRDY: transmit ready
RxRDY: receiver ready
TxEMPTY: transmitter empty
PE: parity error
OE: overrun error
FE: framing error
SYNDET: sync. character detected
DSR: data set ready

ANALOG TO DIGITAL (A/D) INTERFACE

ADC 0808/0809

- The analog to digital converter chips 0808 and 0809 are 8-bit CMOS,*successive approximation converters.*
- ***Successive approximation technique*** is one of the fast techniques for analog to digital conversion. The conversion delay is 100 μs at a clock frequency of 640 kHz.

BLOCK DIAGRAM ADC 0808/0809



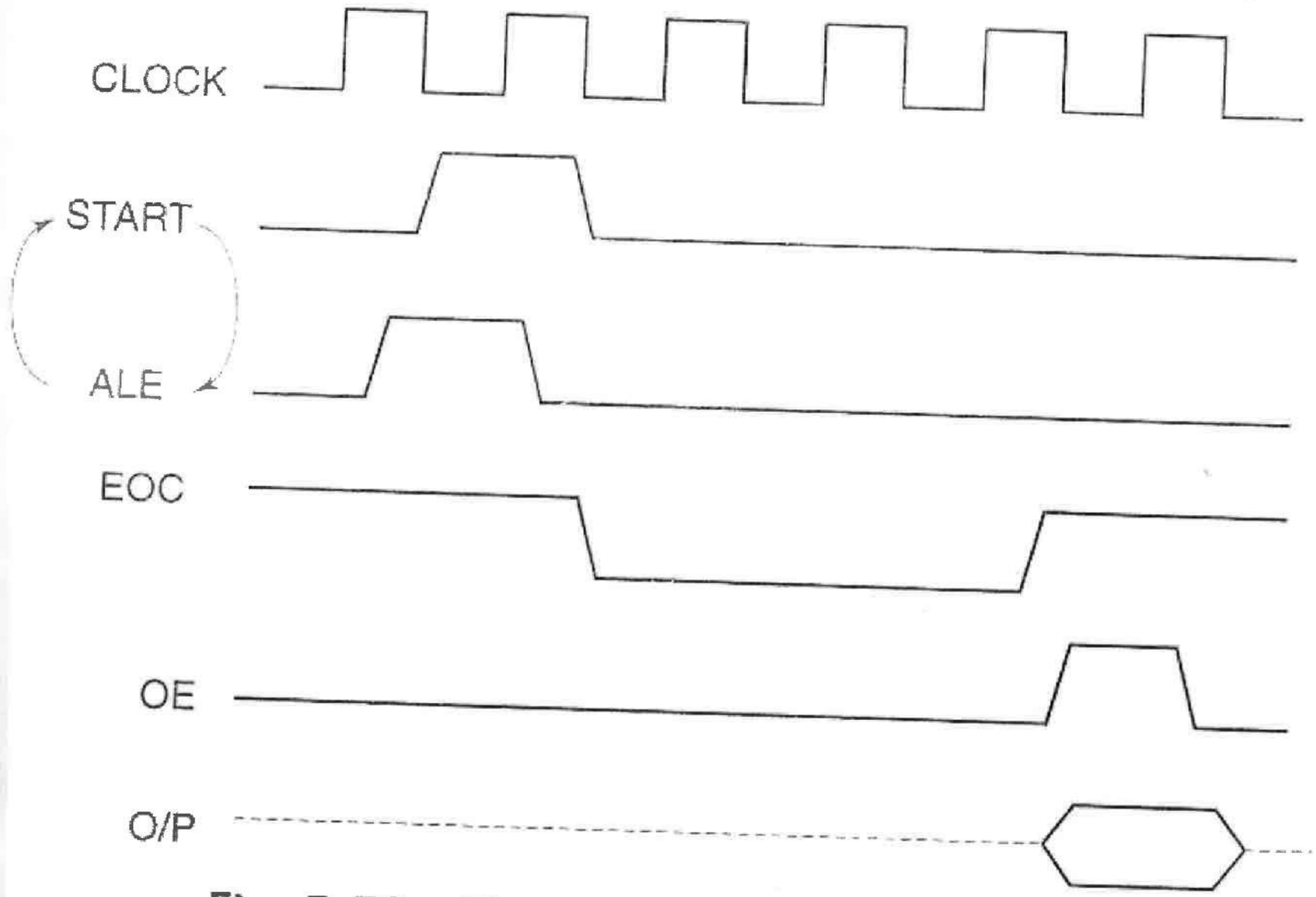
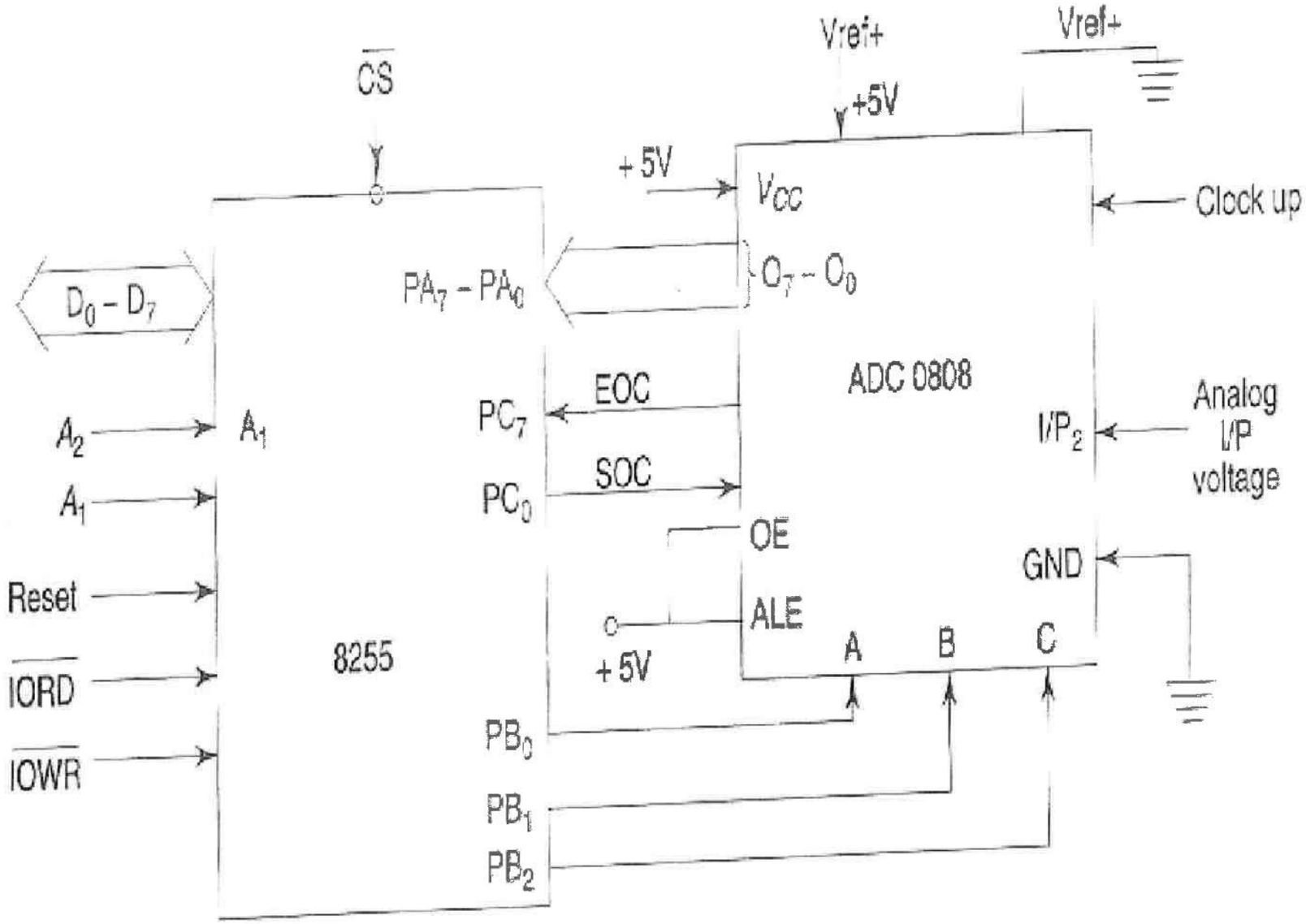


Fig. 5.38 *Timing Diagram of ADC 0808*

Interfacing ADC 0808 with 8086



```
        MOV AL, 98 H      ; Initialisation of 8255
        OUT CWR, AL       ; .
        MOV AL, 02 H      ; Select I/P 2 as analog
        OUT Port B, AL    ; input.
        MOV AL,00H        ; Give start of conversion
        OUT Port C,AL     ; pulse to the ADC
        MOV AL,01H
        OUT Port C,AL
Wait:   IN AL, PortC      ; Check for EOC by
        RCR               ; reading port C upper and rotate through carry
        JNC Wait
        IN AL, PortA      ; If EOC, read digital equivalent in AL
        HLT               ; Stop
```

DIGITAL TO ANALOG (D/A) INTERFACE

INTERFACING DIGITAL TO ANALOG ONVERTERS

The digital to analog converters convert binary numbers into their analog equivalent voltages or currents.

Techniques are employed for digital to analog conversion.

- i. Weighted resistor network
- ii. R-2R ladder network
- iii. Current output D/A converter

- The DAC find applications in areas like digitally controlled gains, motor speed control, programmable gain amplifiers, digital voltmeters, panel meters, etc.
- In a compact disk audio player for example a 14 or16-bit D/A converter is used to convert the binary data read off the disk by a laser to an analog audio signal.

Characteristics :

1. Resolution: It is a change in analog output for one LSB change in digital input.

It is given by(1/2^n)*Vref. If n=8 (i.e.8-bit DAC)

1/256*5V=39.06mV

2. Settling time: It is the time required for the DAC to settle for a full scale code change.

DAC 0800 8-bit Digital to Analog converter

Features:

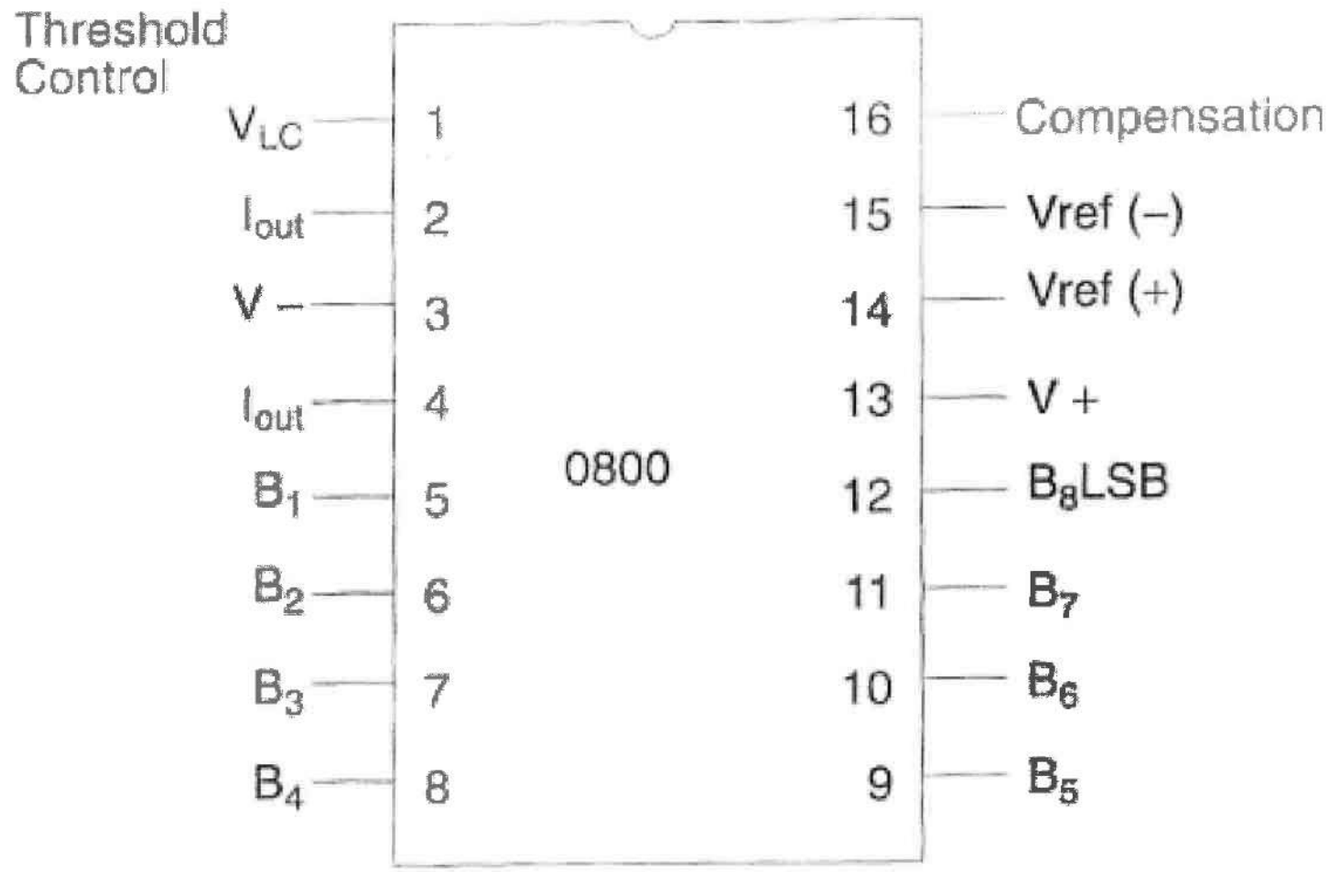
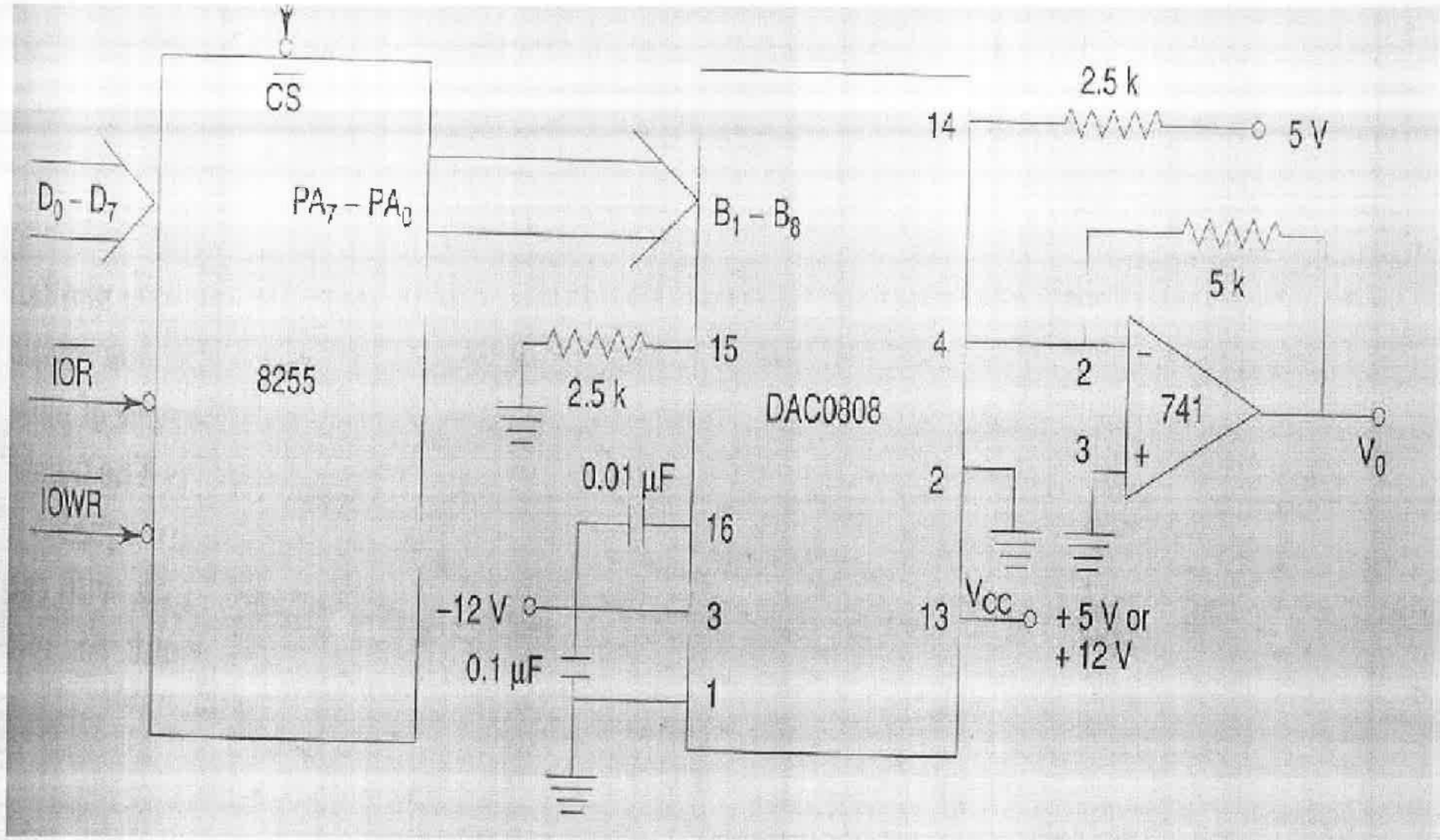
i. DAC0800 is a monolithic 8-bit DAC manufactured by National semiconductor.

ii. It has settling time around 100ms

iii. It can operate on a range of power supply voltage i.e. from 4.5V to +18V. Usually the supply V+ is 5V or +12V. The V- pin can be kept at a minimum of -12V.

iv. Resolution of the DAC is 39.06mV

Pin Diagram of DAC 0800



Interfacing of DAC0800 with 8086