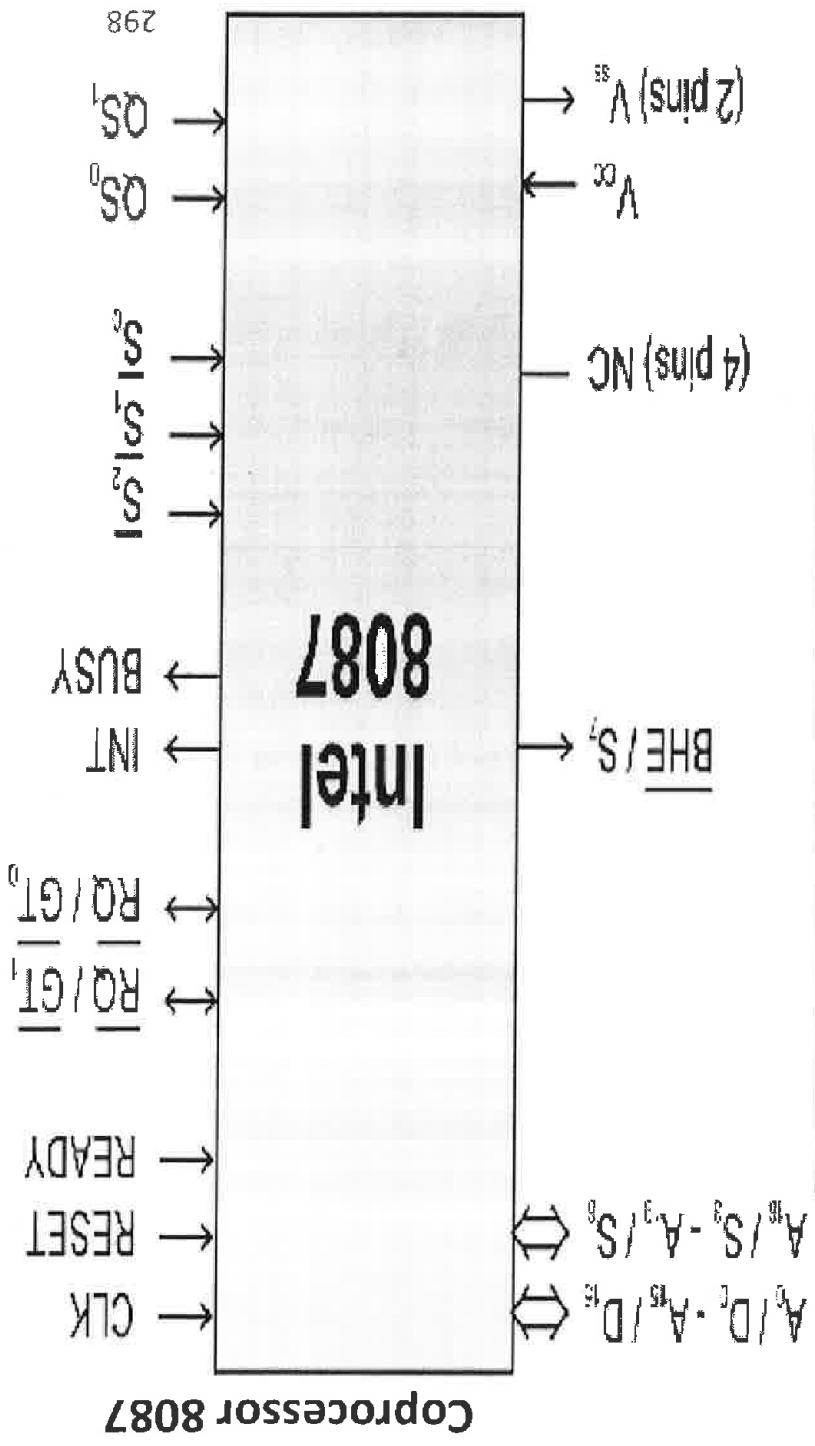


# MULTIPROCESSOR CONFIGURATIONS



**Multiprocessor configuration**

## Multiprocessor Configuration

- Multiprocessor Systems refer to the use of multiple processors that executes instructions simultaneously and communicate with each other using mail boxes and semaphores.

- Maximum mode of 8086 is designed to implement basic multiprocessor configurations:

1. Coprocessor (8087)
2. Closely coupled (8089)
3. Loosely coupled (Multibus)



- Coprocessors and Closely coupled configurations are similar in that both the 8086 and the external processor shares the:
  - Memory
  - I/O system
  - Bus & bus control logic
  - Clock generator

# Co-processor – Intel 8087

- 8087 keeps track for ESC instruction by monitoring  $S^2$  -  $S^0$  and  $AD^0$  -  $AD^{15}$  of
- 8087 keeps track for  $ESC$
- $8086$
- Also keeps track of  $QS^0$ .
- $QS^1$ .
- Q status 00; does nothing
- Q status 01; 8087 compares the five MSB bits with 11011
- If there is a match, then the ESC instruction is fetched and executed by 8087
- If there is an error during decoding an ESC an interrupt request an interrupt request sends instruction, 8087 sends an interrupt request

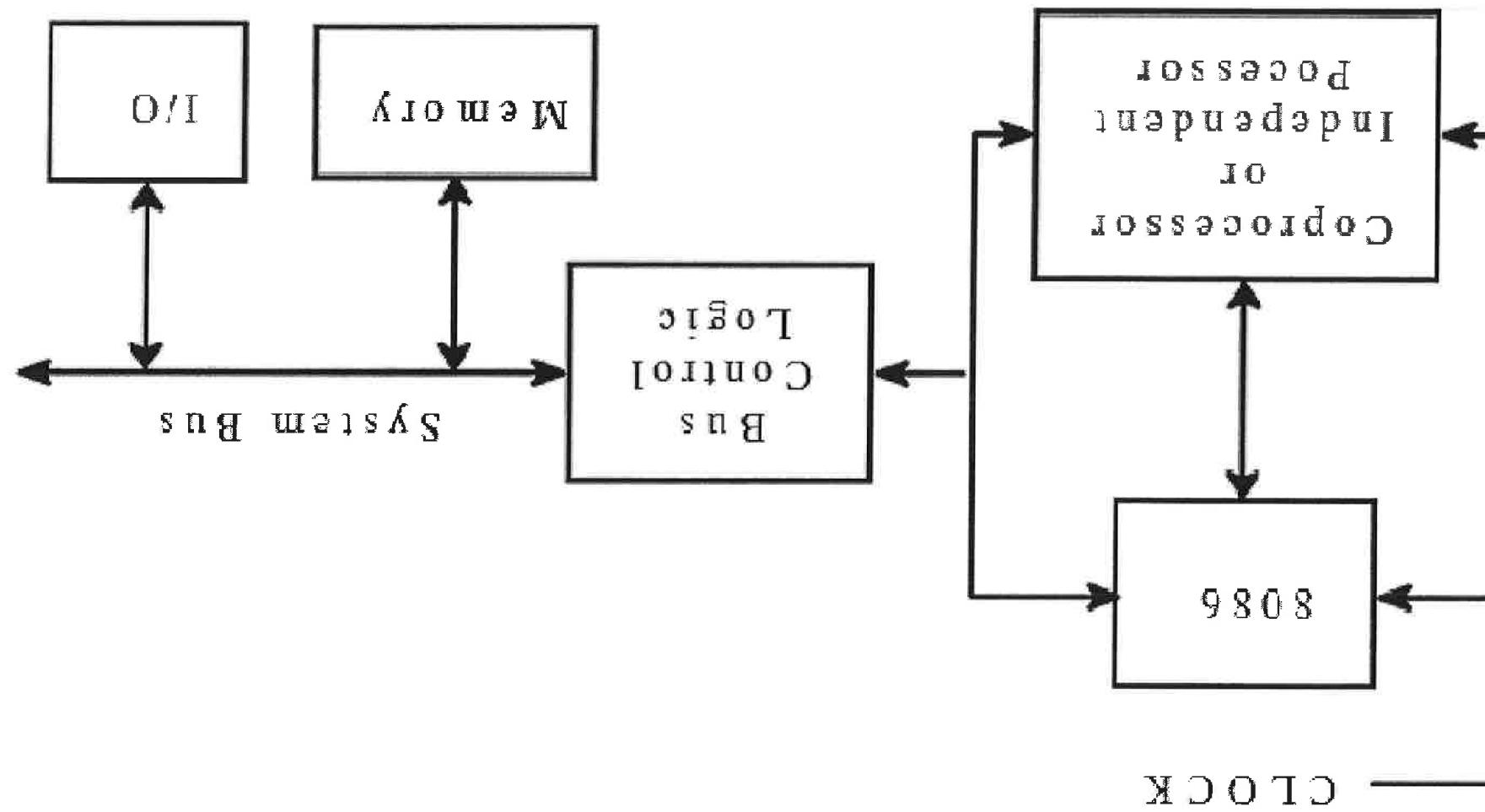


- 8087 instructions are inserted in the 8086 program
- 8086 and 8087 reads instruction bytes and puts them in the respective queues
- 8087 instructions are inserted in the 8086 program
- 8087 NOP
- 8087 instructions have 11011 as the MSB of their first code byte
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- Memory read/write
- Additional words : RD - GT<sub>0</sub>
- 8087 Busy pin high
- TEST
- WAIT



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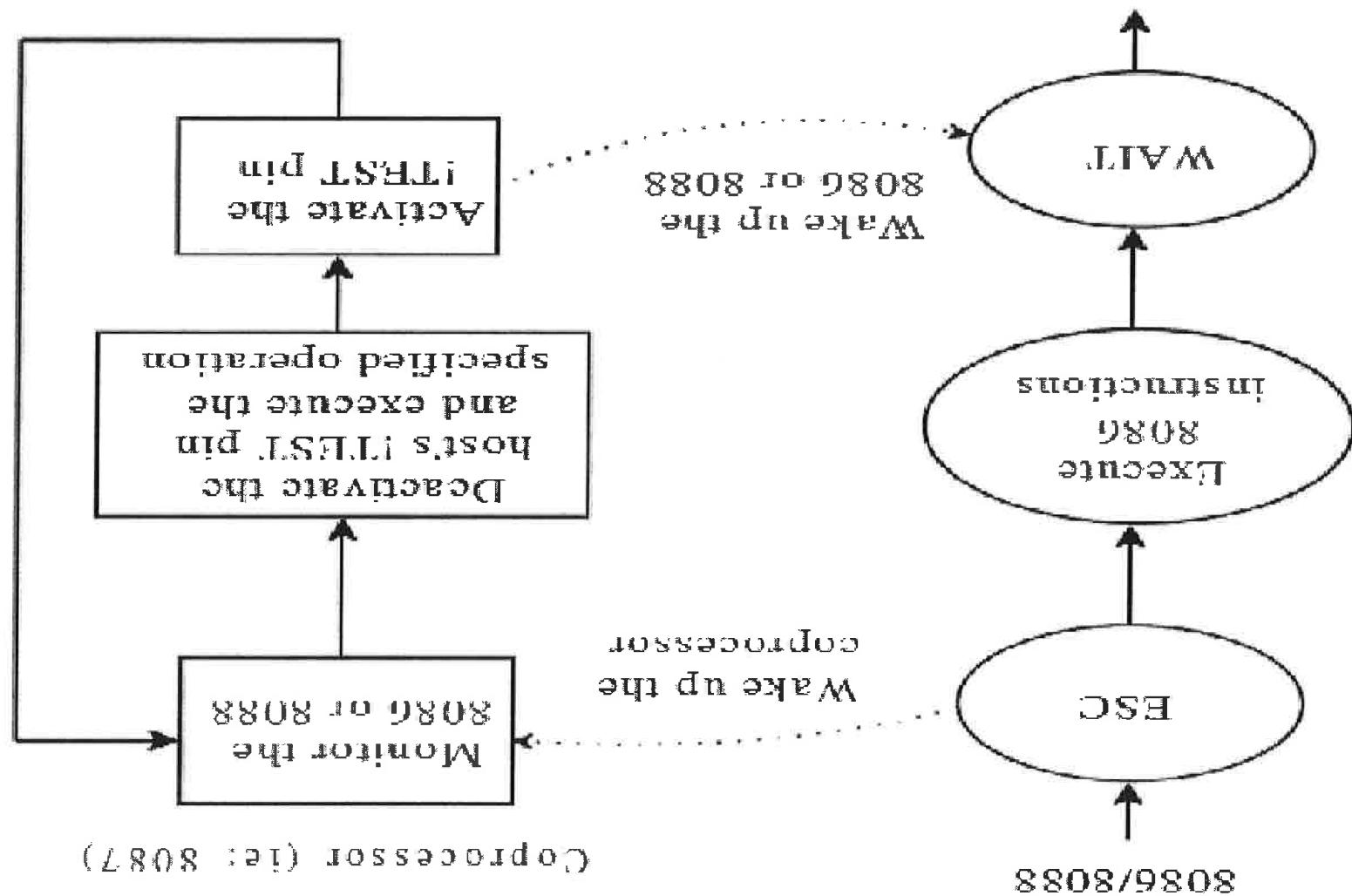




Coprocessor / Closely Coupled  
Configuration

- Used in conjunction with the WAIT instruction in multiprocessing environments.
- This is input from the 8087 coprocessor.
- During execution of a wait instruction, the CPU checks this signal.
  - If it is low, execution of the signal will continue; if not, it will stop executing.

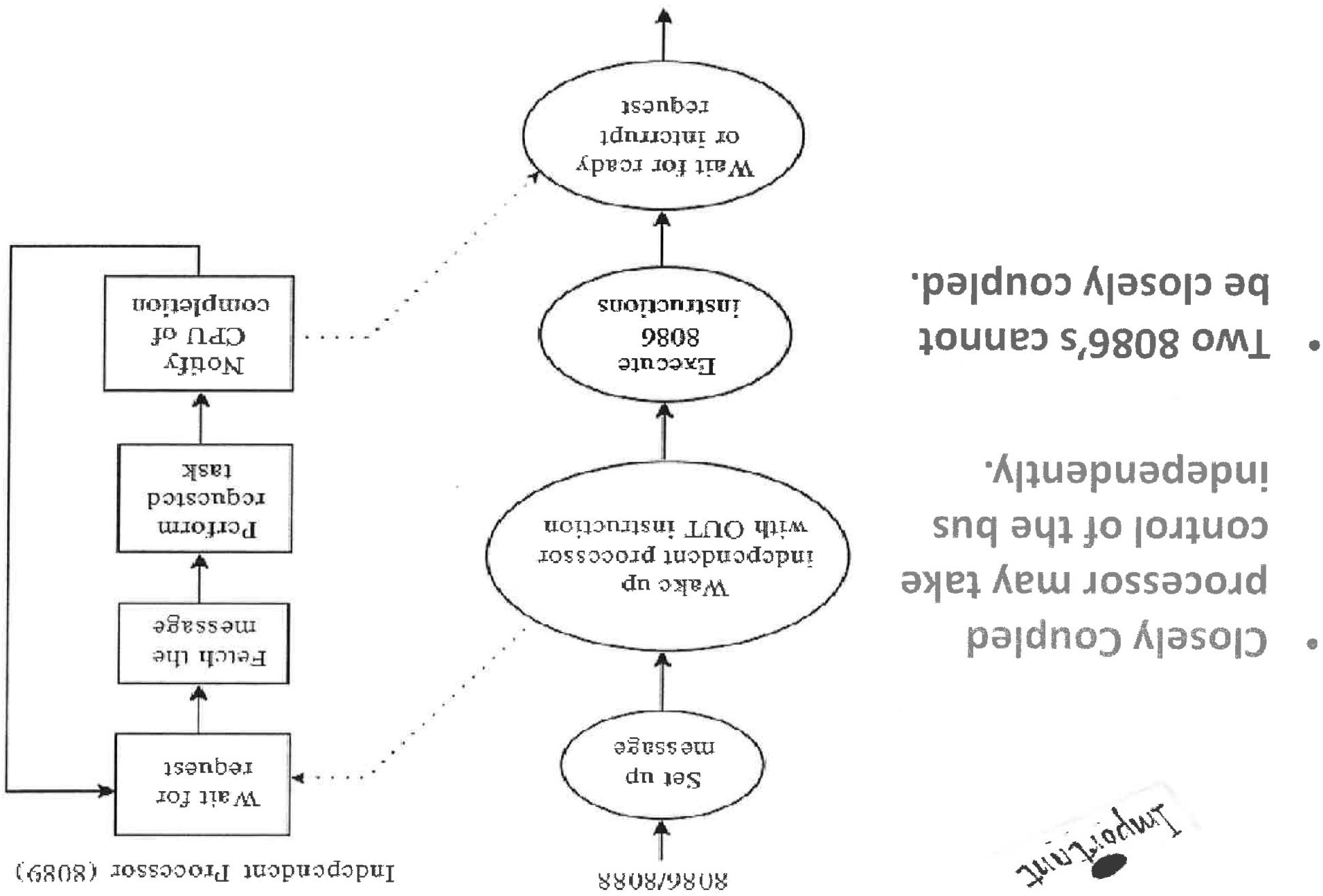
## TEST pin of 8086



Coprocessor cannot take control of the bus, it does everything through the CPU

## 1. Coprocessor Execution Example

## 2. Closely Coupled Execution Example

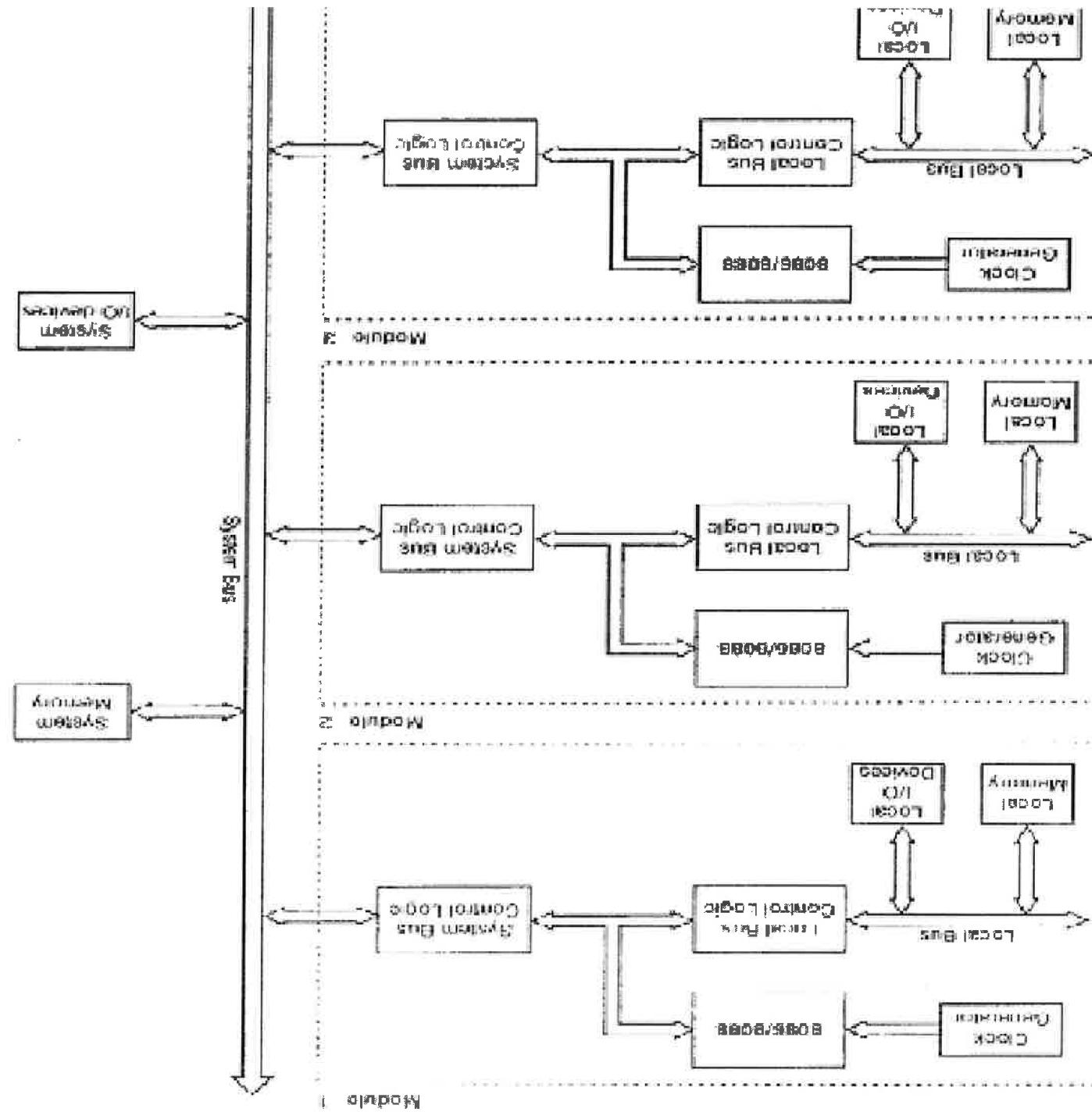


- Closely Coupled
- Processor may take control of the bus independently.
- Two 8086's cannot be closely coupled.

### 3. Loosely Coupled Configuration

- has shared system bus, system memory, and system *I/O*.
- each processor has its own clock as well as its own memory (in addition to access to the system resources).
- Used for medium to large multiprocessor systems.
- Each module is capable of being the bus master.
- Any module could be a processor capable of being a bus master, a coprocessor configuration or a closely coupled configuration.

Important



- Processor in their separate modules can simultaneously access their private subsystems through local instruction fetches independently. This results in busses, and perform their local data references and improved degree of concurrent processing.
- Excellent for real time applications, as separate modules can be assigned specialized tasks

## Loosely Coupled Configuration

# BUS ALLOCATION SCHEMES:

Three bus allocation schemes:

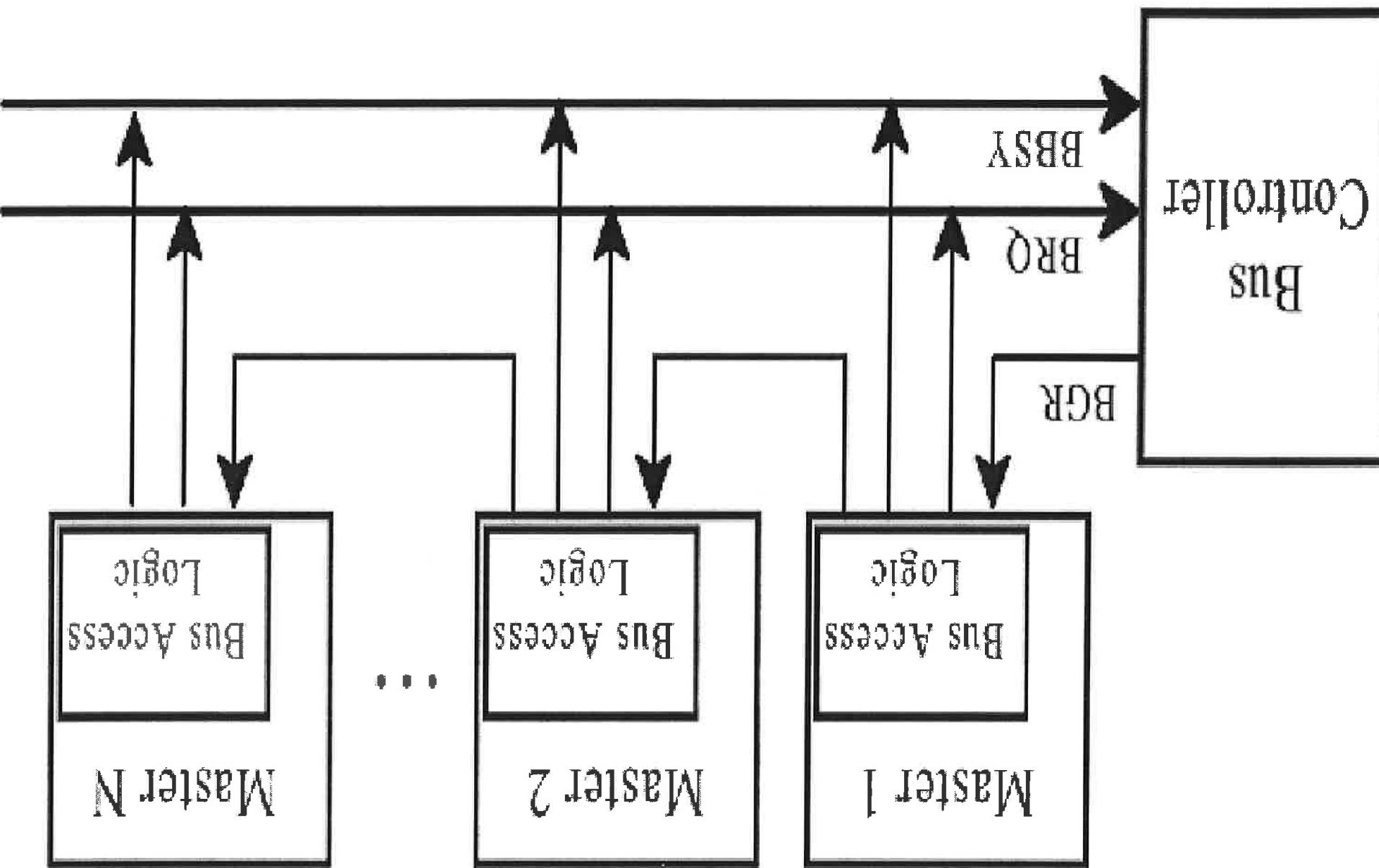
1. Daisy Chaining

2. Pooling

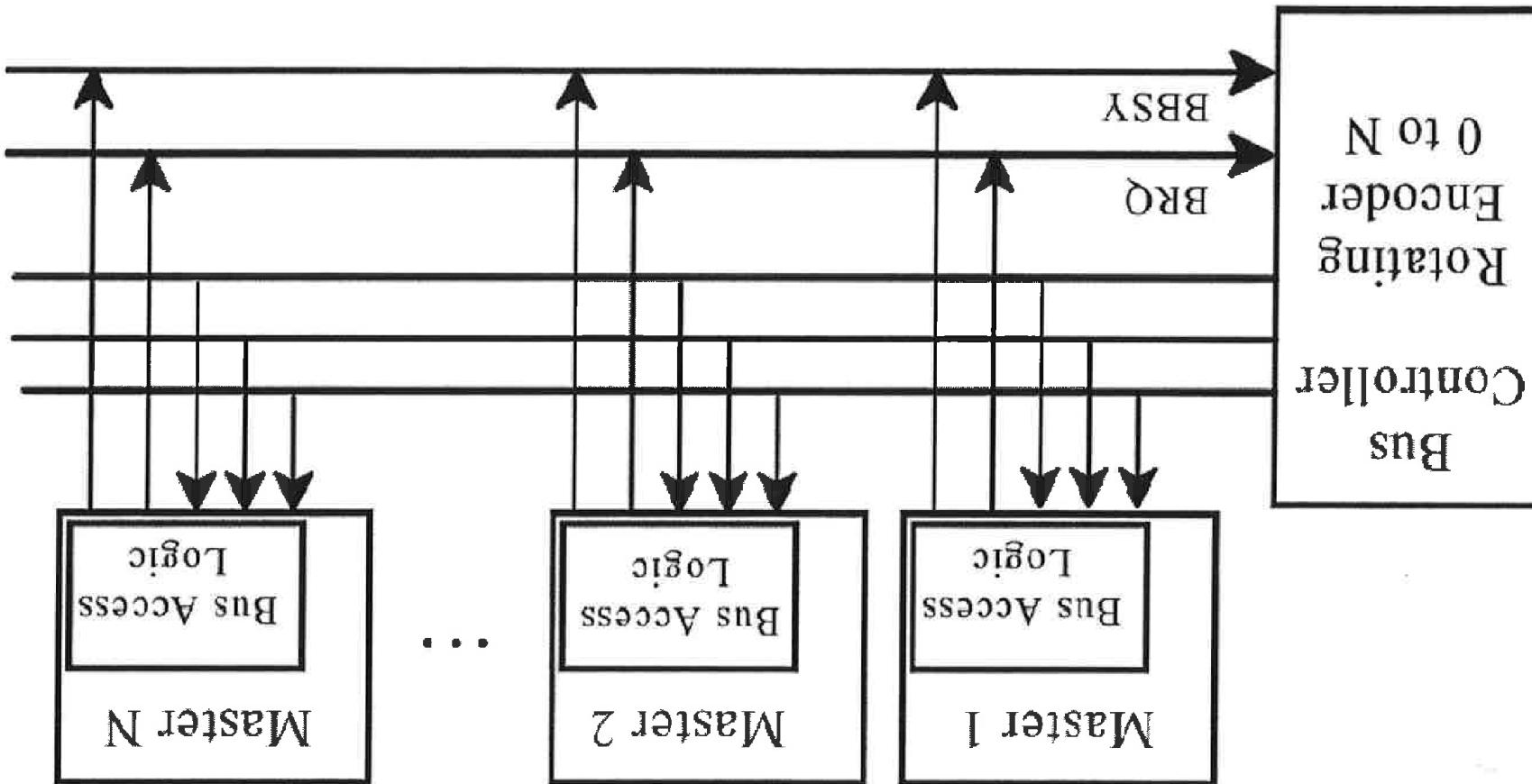
3. Independent

1. Daisy Chaining:

- Need a bus controller to monitor bus busy and bus request signals
- Sends a bus grant to a Master >> each Master either keeps the service or passes it on
- Controller synchronizes the clocks
- Master releases the Bus Busy signal when finished

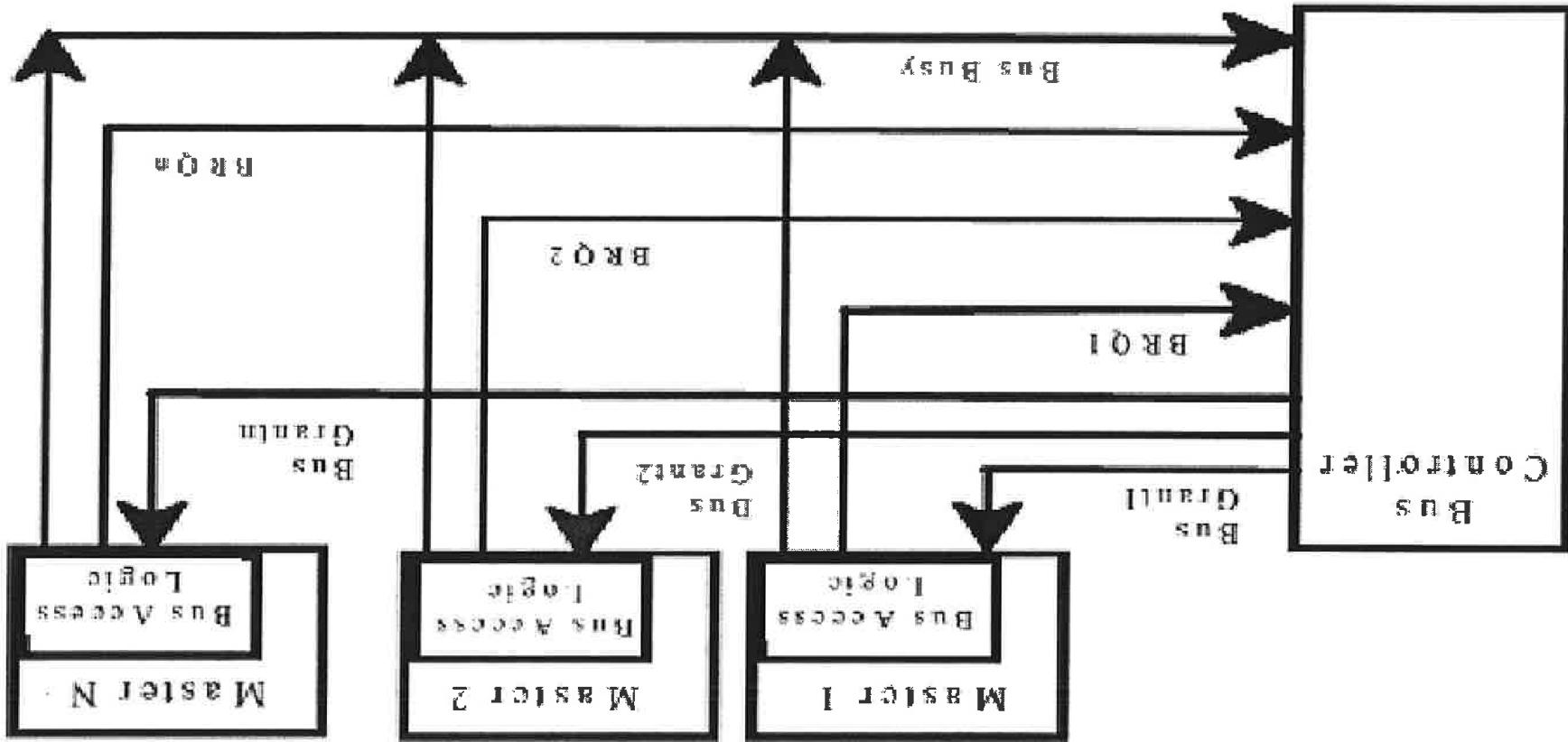


Daisy Chaining:



*Polling:*

- Controller sends address of device to grant bus access
- Can use priority resolution here:
  - memory = highest priority
  - Highest priority is granted first, if it does not respond, then a lower priority is granted, and so on until someone accepts
  - (ie: one request line, 3-bit grant line)



- Can accurately predict calculations (since memory is always the highest priority)

- Master will receive a common clock from one side and pass it to the controller which will derive a clock for transfer
- Each master has a request and grant line

## Independent

# Advantages of Multiprocessor Configuration

1. High system throughput can be achieved by having more than one CPU.
2. The system can be expanded in modular form.
3. A failure in one module normally does not affect the breakdown of the entire system and the faulty module can be easily detected and replaced
4. Each bus master has its own local bus to access dedicated memory or I/O devices. So a greater degree of parallel processing can be achieved.

# INTRODUCTION TO ADVANCED PROCESORS

Microprocessor	Address bus width	Data bus width	Memory size
80186	16	20	1M
80286	16	24	16M
80386 DX	32	32	4G
80486	32	32	4G
Pentium 4 & core 2	64	40	1T

Intel family of microprocessors, bus and memory sizes

» The total addressable memory size is 1MB.

vii. Programmable memory and peripheral chip-select logic

vi. Local bus controller

v. Programmable wait state generator

iv. Three programmable 16-bit timers

iii. Programmable interrupt controller

ii. Two independent high-speed DMA channels

i. Clock generator

80186 = 8086 + several additional chips

» The 80186 double the performance of 8086.

# 80186

- designed for multiuser and multitasking environments.
- addresses 16 M Byte of physical memory and 1G Bytes of virtual memory by using its memory-management system.
- operates in both the real and protected modes.
- In the real mode, the 80286 addresses a 1MByte memory space,
- In the protected mode, the 80286 addresses 16MBYTE memory space.

# 80286

- » Enhanced version of the 80286 microprocessor and includes a memory-management unit to provide memory paging.
- » Has a physical memory size of 4GB bytes that can be addressed as a virtual memory with up to 64TB bytes.
- » The 80386 has three processing modes:
  - 1. Protected Mode.
  - 2. Real-Address Mode.
  - 3. Virtual 8086 Mode.

# 80386