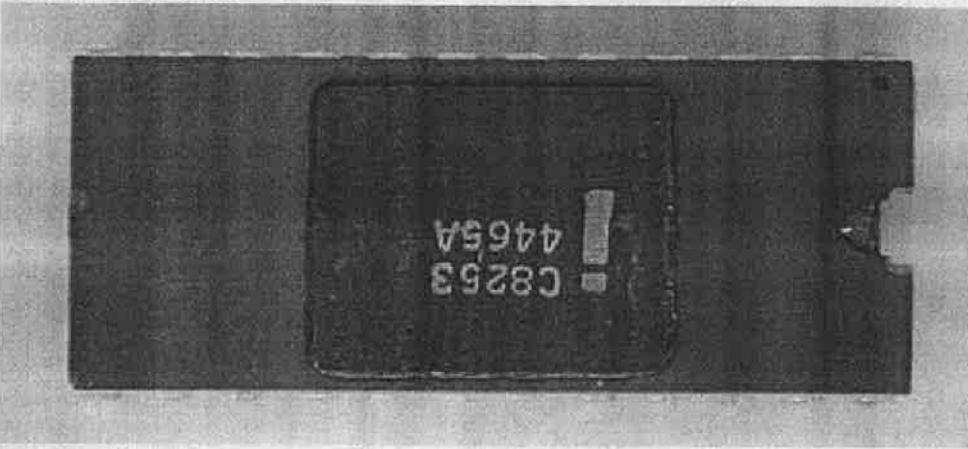
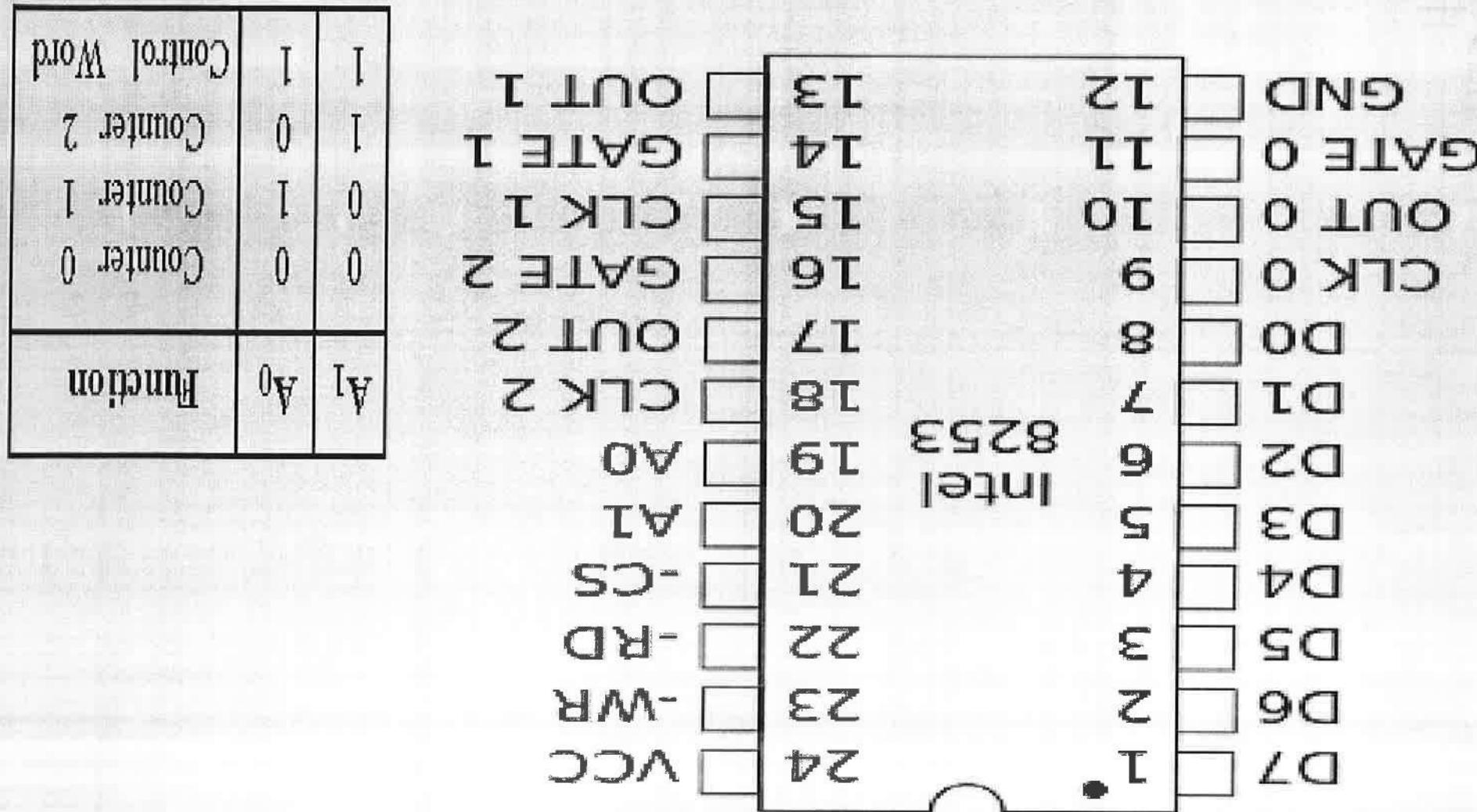


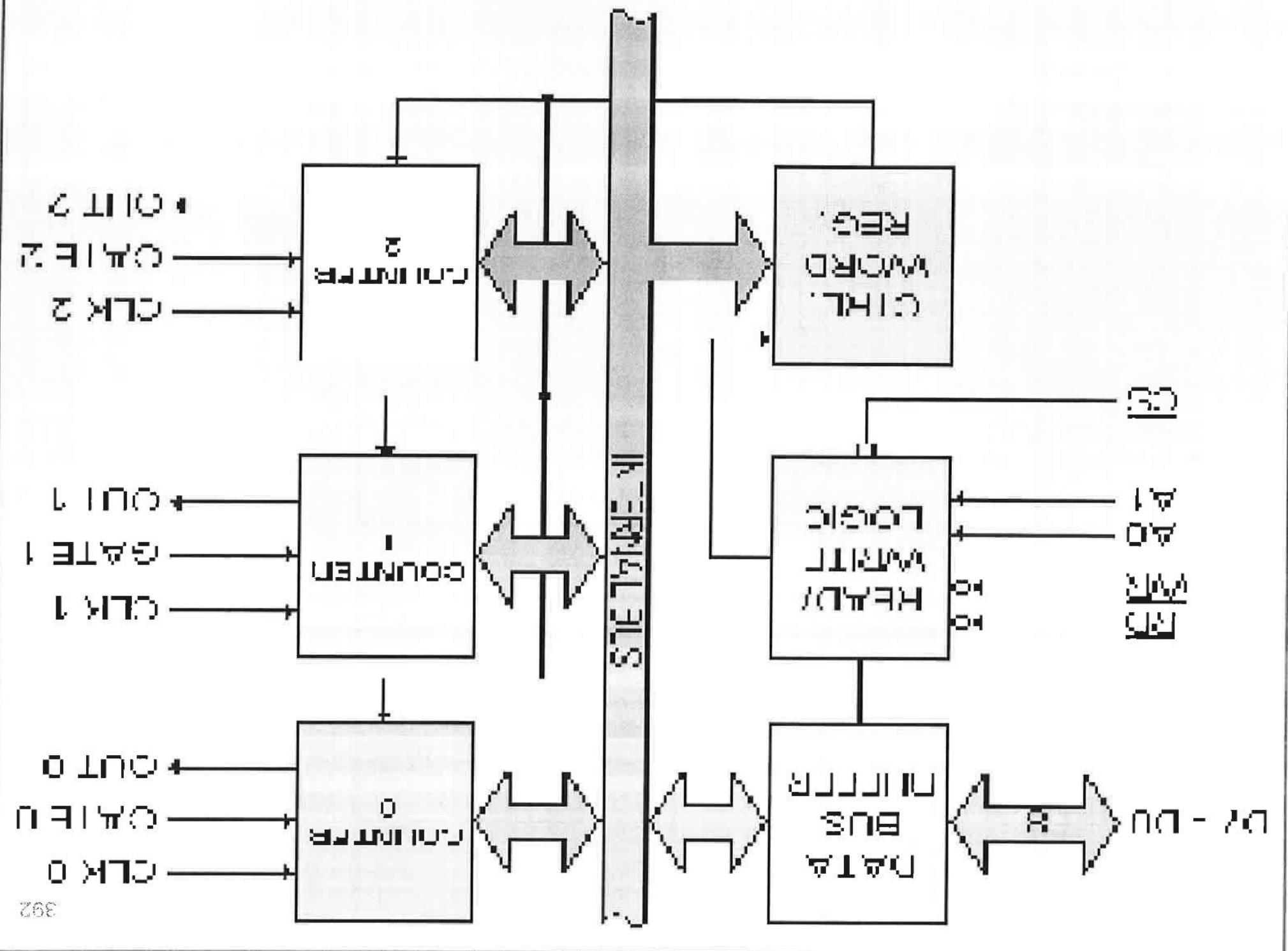
# INTTEL 8253/8254 TIMER/COUNTER





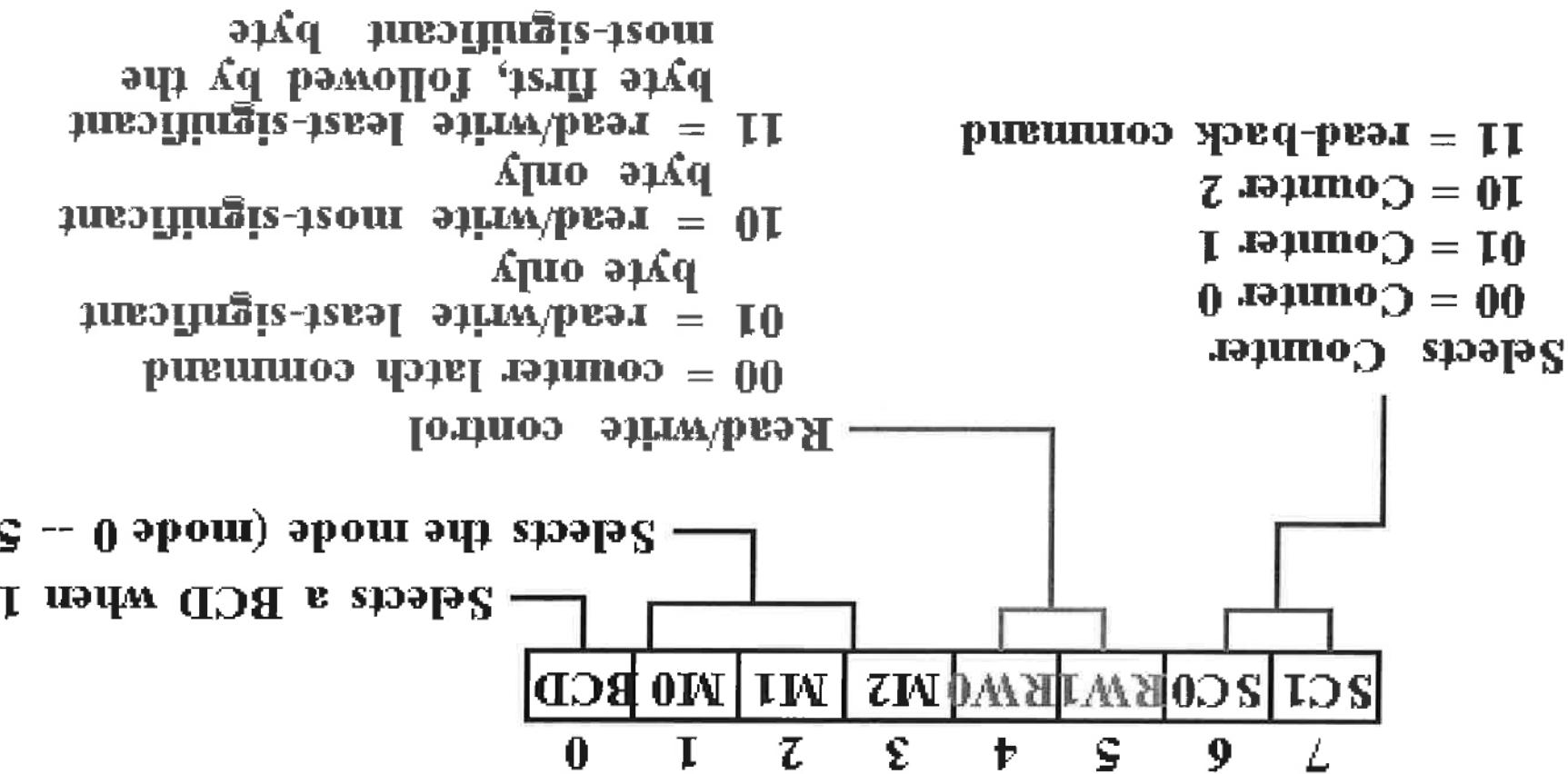
# Pin diagram

- \* **RD:** read signal
- \* **WR:** write signal
- \* **CS:** chip select signal
- \* **AO, A1:** address lines
- \* **Clock:** This is the clock input for the counter.
- The counter is 16 bits.
- \* **Out:** This single output line is the signal that is the final programmed output of the device.
- \* **Gate:** This input can act as a gate for the clock input line, or it can act as a start pulse,



**Control Word Register:** This internal register is used to write information

RD	WR	A0	A1	function
1	0	0	0	Load Counter 0
0	1	0	0	Read Counter 0
1	0	0	1	Load Counter 1
0	1	0	1	Read Counter 1
1	0	0	1	Load Counter 2
0	1	1	0	Read Counter 2
1	0	1	1	Write mode word
0	1	0	1	Mode WORD or CONTROL WORD

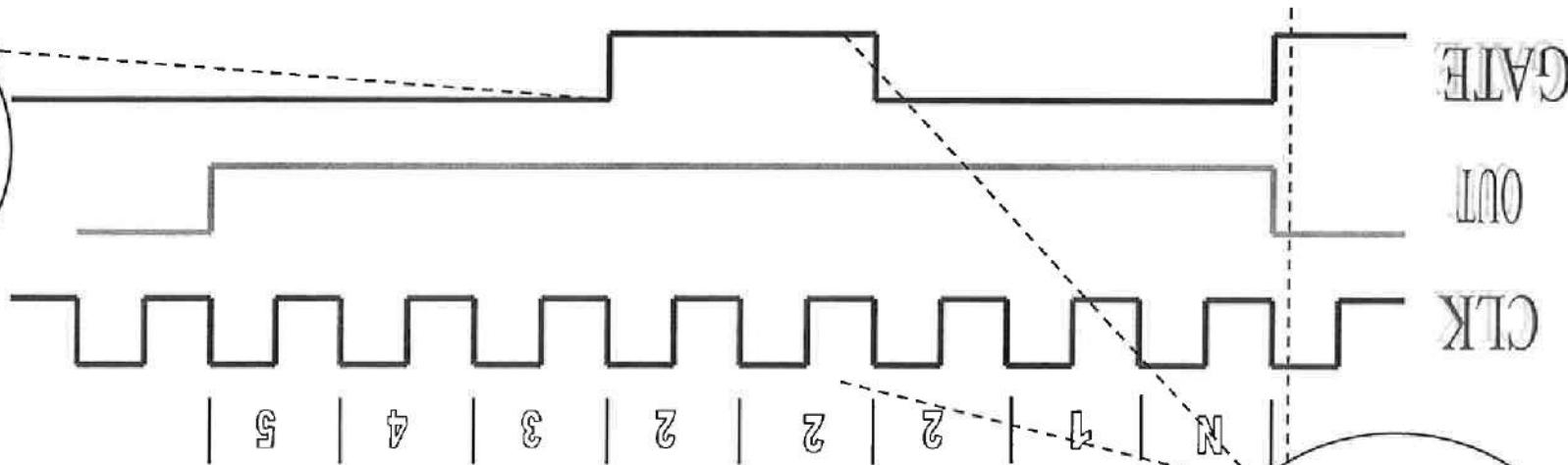


## 8254 Programming

## 8254 Modes

Mode 0: An events counter enabled with G.

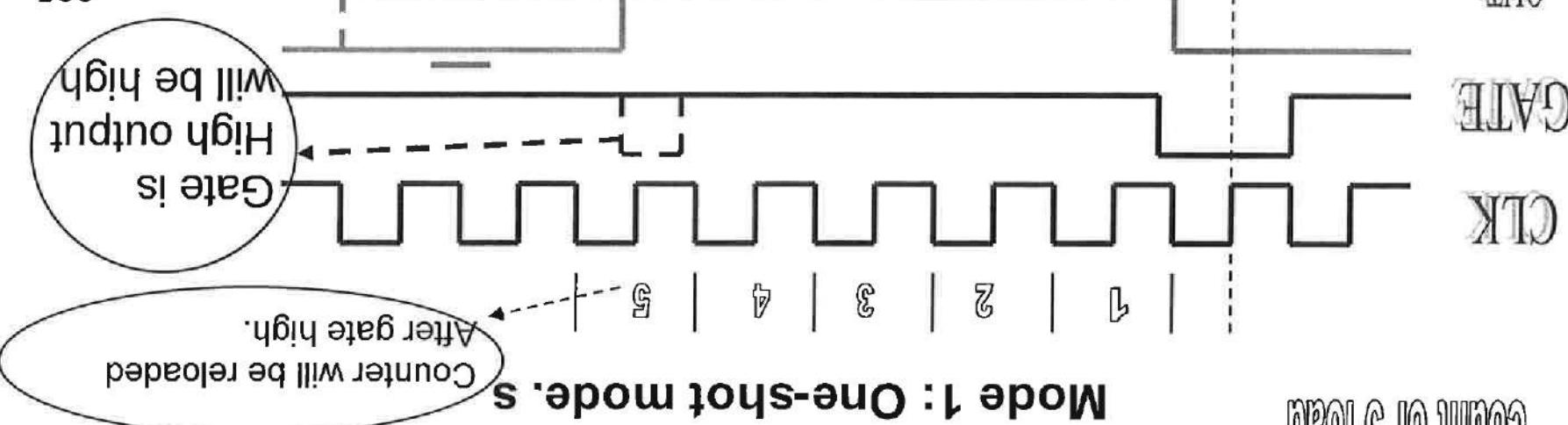
Gate is low the  
count will be  
paused



Mode 1: One-shot mode. s

Count of 5 load

Counter will be reloaded  
After gate high.



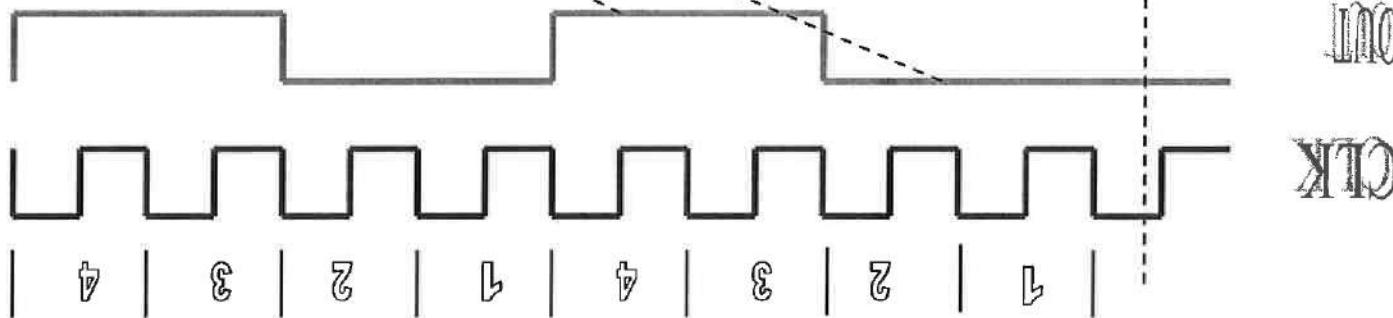
trigger with Count of 5

395

Gate is high  
will be high

If count is even, 50% duty cycle  
otherwise OUT is high 1 cycle  
longer

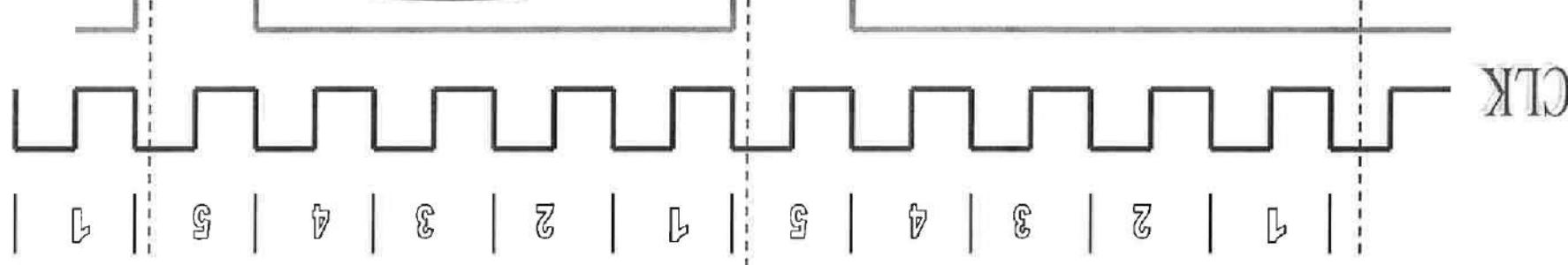
Count of 6 loaded



**Mode 3: Generates a continuous square-wave with G set to 1**

cycle is repeated until  
reprogrammed or G pin  
set to 0

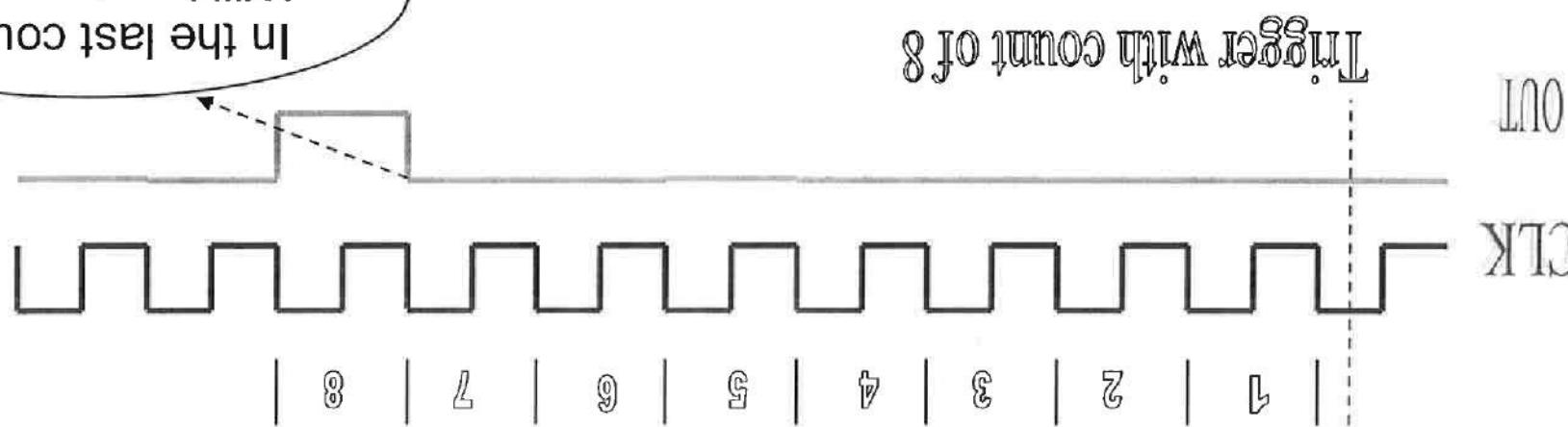
Count of 5 loaded



pulse wide

**Mode 2: Counter generates a series of pulses 1 clock**

#### Mode 4: Software triggered one-shot.

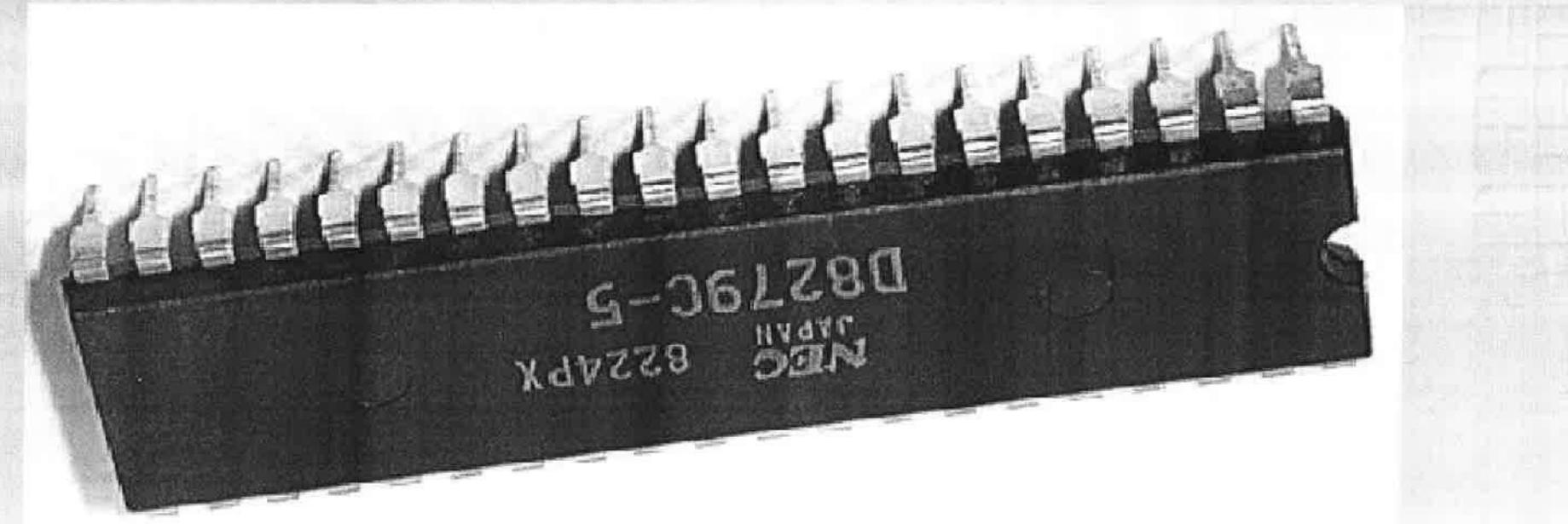


**Mode 5: Hardware triggered one-shot. G controls similar to Mode 1.**



INTEL 8279  
Controller  
Keyboard/Display

Important



The Intel 8279 is specially developed for interfacing keyboard and display devices to 8085/8086 microprocessor based system

## Introduction

- Simultaneous keyboard and display operations
- Scanned keyboard mode
- Scanned sensor mode
- 8-character keyboard FIFO
- 16-character display

## Features of 8279

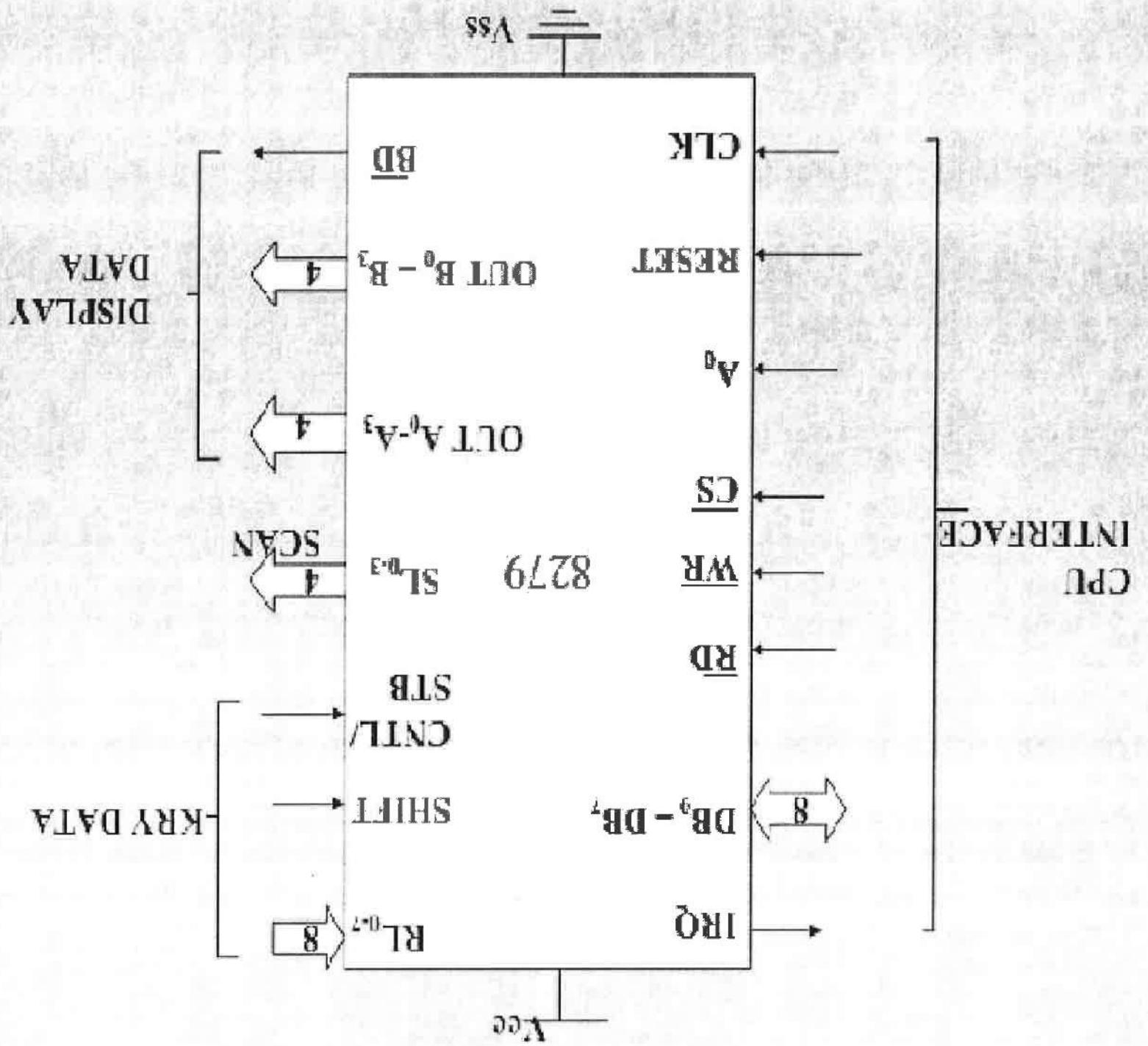
## 8279 Pin Configuration

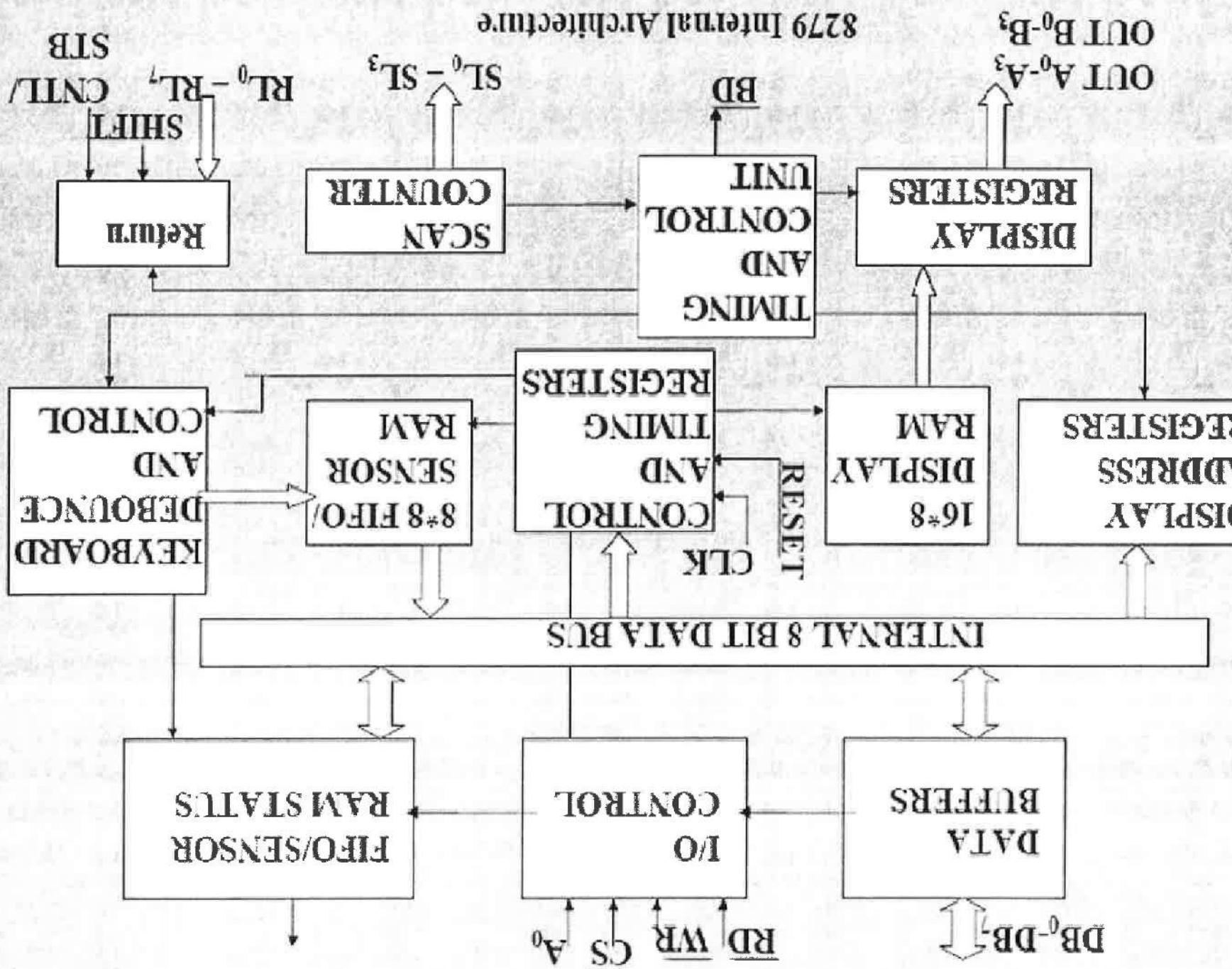
40	Vee	1	KL <sub>1</sub>	RI <sub>1</sub>	RI <sub>2</sub>	RI <sub>3</sub>	RI <sub>4</sub>	RI <sub>5</sub>	RI <sub>6</sub>	RI <sub>7</sub>	RL <sub>1</sub>	RL <sub>2</sub>	RL <sub>3</sub>	SL <sub>1</sub>	SL <sub>2</sub>	SL <sub>3</sub>	SL <sub>4</sub>	SL <sub>5</sub>	SL <sub>6</sub>	SL <sub>7</sub>	WR	RD	RESET	31	OUT B <sub>0</sub>	OUT B <sub>1</sub>	OUT B <sub>2</sub>	OUT B <sub>3</sub>	OUT B <sub>4</sub>	OUT B <sub>5</sub>	OUT B <sub>6</sub>	OUT B <sub>7</sub>	OUT A <sub>0</sub>	OUT A <sub>1</sub>	OUT A <sub>2</sub>	OUT A <sub>3</sub>	OUT A <sub>4</sub>	OUT A <sub>5</sub>	DB <sub>0</sub>	DB <sub>1</sub>	DB <sub>2</sub>	DB <sub>3</sub>	DB <sub>4</sub>	DB <sub>5</sub>	DB <sub>6</sub>	DB <sub>7</sub>	VSS	A <sub>0</sub>																									
39	RL <sub>1</sub>	2	KL <sub>2</sub>	CIK	IRO	37	CNTL/SIUS	36	SHIFT	35	SL <sub>3</sub>	SL <sub>4</sub>	SL <sub>5</sub>	SL <sub>6</sub>	SL <sub>7</sub>	34	SL <sub>1</sub>	SL <sub>2</sub>	SL <sub>3</sub>	SL <sub>4</sub>	SL <sub>5</sub>	SL <sub>6</sub>	SL <sub>7</sub>	8	RL <sub>7</sub>	RI <sub>1</sub>	RI <sub>2</sub>	RI <sub>3</sub>	RI <sub>4</sub>	RI <sub>5</sub>	RI <sub>6</sub>	RI <sub>7</sub>	WR	RD	RESET	10	OUT B <sub>0</sub>	OUT B <sub>1</sub>	OUT B <sub>2</sub>	OUT B <sub>3</sub>	OUT B <sub>4</sub>	OUT B <sub>5</sub>	OUT B <sub>6</sub>	OUT B <sub>7</sub>	OUT A <sub>0</sub>	OUT A <sub>1</sub>	OUT A <sub>2</sub>	OUT A <sub>3</sub>	OUT A <sub>4</sub>	OUT A <sub>5</sub>	DB <sub>0</sub>	DB <sub>1</sub>	DB <sub>2</sub>	DB <sub>3</sub>	DB <sub>4</sub>	DB <sub>5</sub>	DB <sub>6</sub>	DB <sub>7</sub>	VSS	A <sub>0</sub>													
38	RL <sub>2</sub>	3	IRO	34	37	CNTL/SIUS	36	SHIFT	35	SL <sub>3</sub>	SL <sub>4</sub>	SL <sub>5</sub>	SL <sub>6</sub>	SL <sub>7</sub>	34	SL <sub>1</sub>	SL <sub>2</sub>	SL <sub>3</sub>	SL <sub>4</sub>	SL <sub>5</sub>	SL <sub>6</sub>	SL <sub>7</sub>	7	RL <sub>6</sub>	RI <sub>1</sub>	RI <sub>2</sub>	RI <sub>3</sub>	RI <sub>4</sub>	RI <sub>5</sub>	RI <sub>6</sub>	RI <sub>7</sub>	WR	RD	RESET	11	OUT B <sub>0</sub>	OUT B <sub>1</sub>	OUT B <sub>2</sub>	OUT B <sub>3</sub>	OUT B <sub>4</sub>	OUT B <sub>5</sub>	OUT B <sub>6</sub>	OUT B <sub>7</sub>	OUT A <sub>0</sub>	OUT A <sub>1</sub>	OUT A <sub>2</sub>	OUT A <sub>3</sub>	OUT A <sub>4</sub>	OUT A <sub>5</sub>	DB <sub>0</sub>	DB <sub>1</sub>	DB <sub>2</sub>	DB <sub>3</sub>	DB <sub>4</sub>	DB <sub>5</sub>	DB <sub>6</sub>	DB <sub>7</sub>	VSS	A <sub>0</sub>														
39	RL <sub>3</sub>	4	IRO	34	37	CNTL/SIUS	36	SHIFT	35	SL <sub>3</sub>	SL <sub>4</sub>	SL <sub>5</sub>	SL <sub>6</sub>	SL <sub>7</sub>	34	SL <sub>1</sub>	SL <sub>2</sub>	SL <sub>3</sub>	SL <sub>4</sub>	SL <sub>5</sub>	SL <sub>6</sub>	SL <sub>7</sub>	6	RL <sub>5</sub>	RI <sub>1</sub>	RI <sub>2</sub>	RI <sub>3</sub>	RI <sub>4</sub>	RI <sub>5</sub>	RI <sub>6</sub>	RI <sub>7</sub>	WR	RD	RESET	12	OUT B <sub>0</sub>	OUT B <sub>1</sub>	OUT B <sub>2</sub>	OUT B <sub>3</sub>	OUT B <sub>4</sub>	OUT B <sub>5</sub>	OUT B <sub>6</sub>	OUT B <sub>7</sub>	OUT A <sub>0</sub>	OUT A <sub>1</sub>	OUT A <sub>2</sub>	OUT A <sub>3</sub>	OUT A <sub>4</sub>	OUT A <sub>5</sub>	DB <sub>0</sub>	DB <sub>1</sub>	DB <sub>2</sub>	DB <sub>3</sub>	DB <sub>4</sub>	DB <sub>5</sub>	DB <sub>6</sub>	DB <sub>7</sub>	VSS	A <sub>0</sub>														
40	Vee	1	KL <sub>1</sub>	RI <sub>1</sub>	RI <sub>2</sub>	RI <sub>3</sub>	RI <sub>4</sub>	RI <sub>5</sub>	RI <sub>6</sub>	RI <sub>7</sub>	RL <sub>1</sub>	RL <sub>2</sub>	RL <sub>3</sub>	SL <sub>1</sub>	SL <sub>2</sub>	SL <sub>3</sub>	SL <sub>4</sub>	SL <sub>5</sub>	SL <sub>6</sub>	SL <sub>7</sub>	32	SL <sub>0</sub>	31	OUT B <sub>0</sub>	OUT B <sub>1</sub>	OUT B <sub>2</sub>	OUT B <sub>3</sub>	OUT B <sub>4</sub>	OUT B <sub>5</sub>	OUT B <sub>6</sub>	OUT B <sub>7</sub>	OUT A <sub>0</sub>	OUT A <sub>1</sub>	OUT A <sub>2</sub>	OUT A <sub>3</sub>	OUT A <sub>4</sub>	OUT A <sub>5</sub>	DB <sub>0</sub>	DB <sub>1</sub>	DB <sub>2</sub>	DB <sub>3</sub>	DB <sub>4</sub>	DB <sub>5</sub>	DB <sub>6</sub>	DB <sub>7</sub>	WR	RD	RESET	10	OUT B <sub>0</sub>	OUT B <sub>1</sub>	OUT B <sub>2</sub>	OUT B <sub>3</sub>	OUT B <sub>4</sub>	OUT B <sub>5</sub>	OUT B <sub>6</sub>	OUT B <sub>7</sub>	OUT A <sub>0</sub>	OUT A <sub>1</sub>	OUT A <sub>2</sub>	OUT A <sub>3</sub>	OUT A <sub>4</sub>	OUT A <sub>5</sub>	DB <sub>0</sub>	DB <sub>1</sub>	DB <sub>2</sub>	DB <sub>3</sub>	DB <sub>4</sub>	DB <sub>5</sub>	DB <sub>6</sub>	DB <sub>7</sub>	VSS	A <sub>0</sub>

Pin Diagram

# 4 sections

- \* CPU interface section
- \* Scan section
- \* Display section
- \* Keyboard section





- \* The keyboard section consists of 8 return lines R<sub>0</sub> - R<sub>7</sub> that can be used to form the columns of a keyboard matrix.
- \* It has two additional input : shift and control/strobe. The keys are automatically debounced.
- \* The two operating modes of keyboard section are 2-key lockout and N-key rollover.

## Keyboard section

- In the 2-key lockout mode, if two keys are pressed simultaneously, only the first key is recognized.
- In the N-key rollover mode simultaneous keys are recognized and their codes are stored in FIFO.
- The keyboard section also have an 8 x 8 FIFO (First In First Out) RAM.
- The FIFO can store eight key codes in the scan control key are also stored along with key code. The keyboard mode. The status of the shift key and 8279 generate an interrupt signal (IRQ) when there is an entry in FIFO.

- \* The display section has eight output lines divided into two groups A0-A3 and B0-B3.
- \* The output lines can be used either as a single group of eight lines or as two groups of four lines, in conjunction with the scan lines for a multiplexed display.
- \* The output lines are connected to the anodes through driver transistor in case of common cathode 7-segment LEDs.

## Display section

- any location of the display RAM.
- RAM. The CPU can read from or write into
- \* The display section consists of  $16 \times 8$  display
- \* The display can be blanked by BD (low) line.
- The cathodes are connected to scan lines through driver transistors.

- \* The scan section has a scan counter and four scan lines, SLO to SL3.
- \* The scan section has a scan counter and four scan lines, SLO to SL3.
  - \* In decoded scan mode, the output of scan lines will be similar to a 2-to-4 decoder.
  - \* In encoded scan mode, the output of scan lines will be similar to a 2-to-4 decoder.
- \* In decoded scan mode, the output of scan lines will be binary count, and so an external decoder should be used to convert the binary count to decoded output.
- \* The scan lines are common for keyboard and display.

## Scan section

- The CPU interface section takes care of data transfer between 8279 and the processor.
- This section has eight bidirectional data lines DB0 to DB7 for data transfer between 8279 and CPU.
- It requires two internal address A = 0 for 8279 and CPU.
- It requires two internal address A = 1 for selecting 8279 and CPU.
- Control register of 8279.

## CPU interface section

- \* The control signals WR (low), RD (low), CS (low) and AO are used for read/write to 8279.

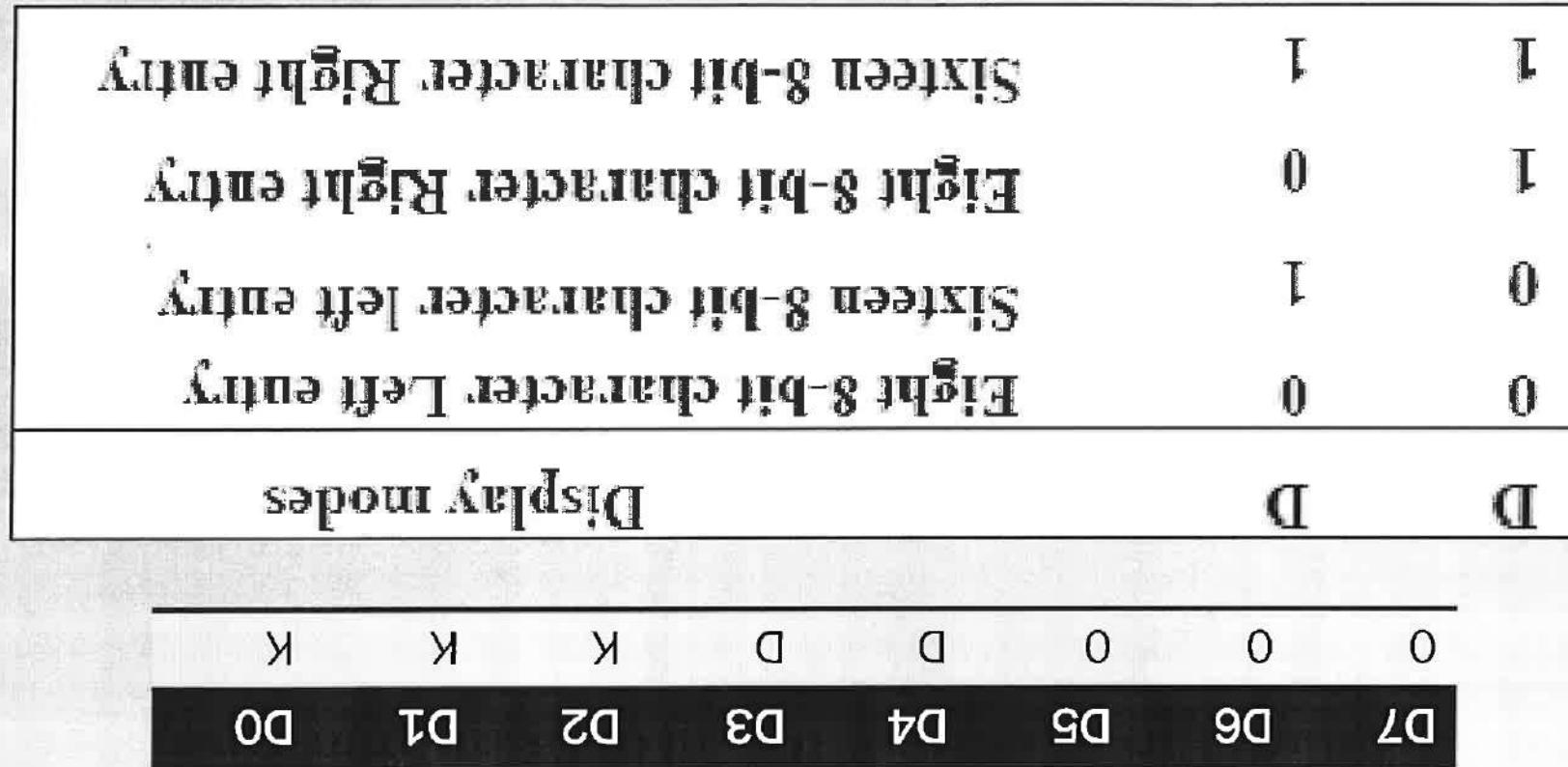
- \* It has an interrupt request line IRQ, for interrupt driven data transfer with processor.
- \* The 8279 require an internal clock frequency of 100 KHz. This can be obtained by dividing the input clock by an internal prescaler.

Command Words of 8279

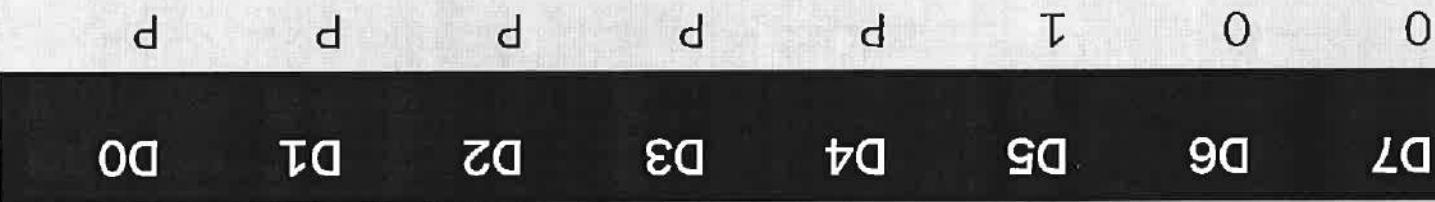
All the command words or status words are written or read with  $\text{AO} = 1$  and  $\text{CS} = 0$  to or from 8279.

**Keyboard Display Mode Set :** The format of the command word to select different

modes of operation of 8279 is given below with its bit definitions.



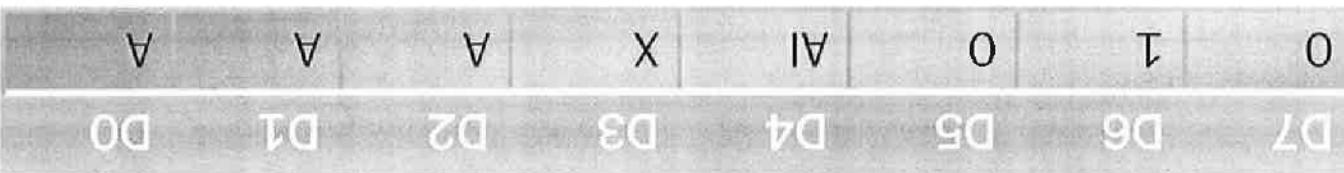
Keyboard modes	K	K	K	Shobed Input Decoded Scan	1	1	1
Encoded Scan, 2 key lockout (Default after reset)	0	0	0	Encoded Scan, 2 key lockout	0	0	0
Encoded Scan, 2 key lockout	0	0	1	Encoded Scan, 2 key lockout	0	1	0
Encoded Scan, N-key Roll over	0	1	1	Encoded Scan, N-key Roll over	0	0	0
Encoded Scan, N-key Roll over	0	1	0	Encoded Scan, N-key Roll over	0	0	1
Decoded Scan, SENSOR MATRIX	1	0	1	Decoded Scan, SENSOR MATRIX	1	0	1
Decoded Scan	1	1	0	Shobed Input Decoded Scan	1	1	0
Shobed Input Decoded Scan	1	1	1	Shobed Input Decoded Scan	1	1	1



- The clock for operation of 8279 is obtained by dividing the external clock input signal by a programmable constant called prescaler.
  - PPPPP is a 5-bit binary constant.
  - The input frequency is divided by a decimal constant ranging from 2 to 31, decided by the bits of an internal prescaler, PPPPP.
- b) Programmable clock :

- ✓ This word is written to set up 8279 for reading FIFO/ sensor RAM.
- ✓ In scanned keyboard mode, AI and AAA bits are of no use. The 8279 will automatically drive data bus for each subsequent read, in the same sequence, in which the data was entered.
- ✓ In sensor matrix mode, the bits AAA select one of the 8 rows of the sensor matrix, in which each successive read will be from the subsequent RAM.
- X- Don't care

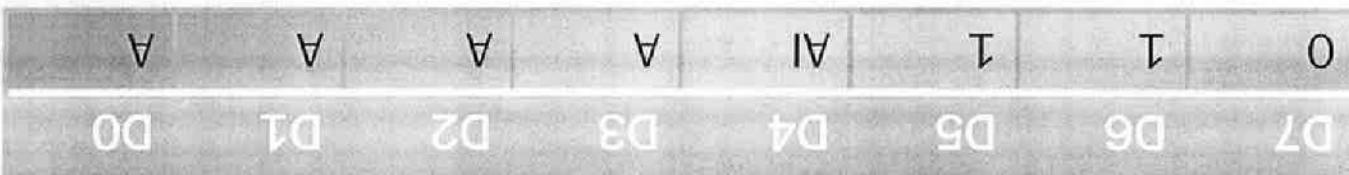
AAA - Address pointer to 8 bit FIFO RAM  
AI - Auto increment Flag



below.

c) **Read FIFO / Sensor RAM :** The format of this command is given below.

- ❖ The CPU writes this command word to 8279 to prepare it for display RAM read operation.
- ❖ AI is auto increment flag and AAA, the 4-bit address points to the 16-byte display RAM that is to be read.
- ❖ If AI=1, the address will be automatically, incremented after each read or write to the Display RAM.
- ❖ The same address counter is used for reading and writing.



d) **Read Display RAM :**  
This command enables a programmer to read the display RAM data.

BL - blank display bit flags

IW - inhibit write flag

1	0	1	X	IW	BL	BL
D7	D6	D5	D4	D3	D2	D1

e) Display Write inhibit/Blanking :

written.

AAA - 4 bit address for 16-bit display RAM to be

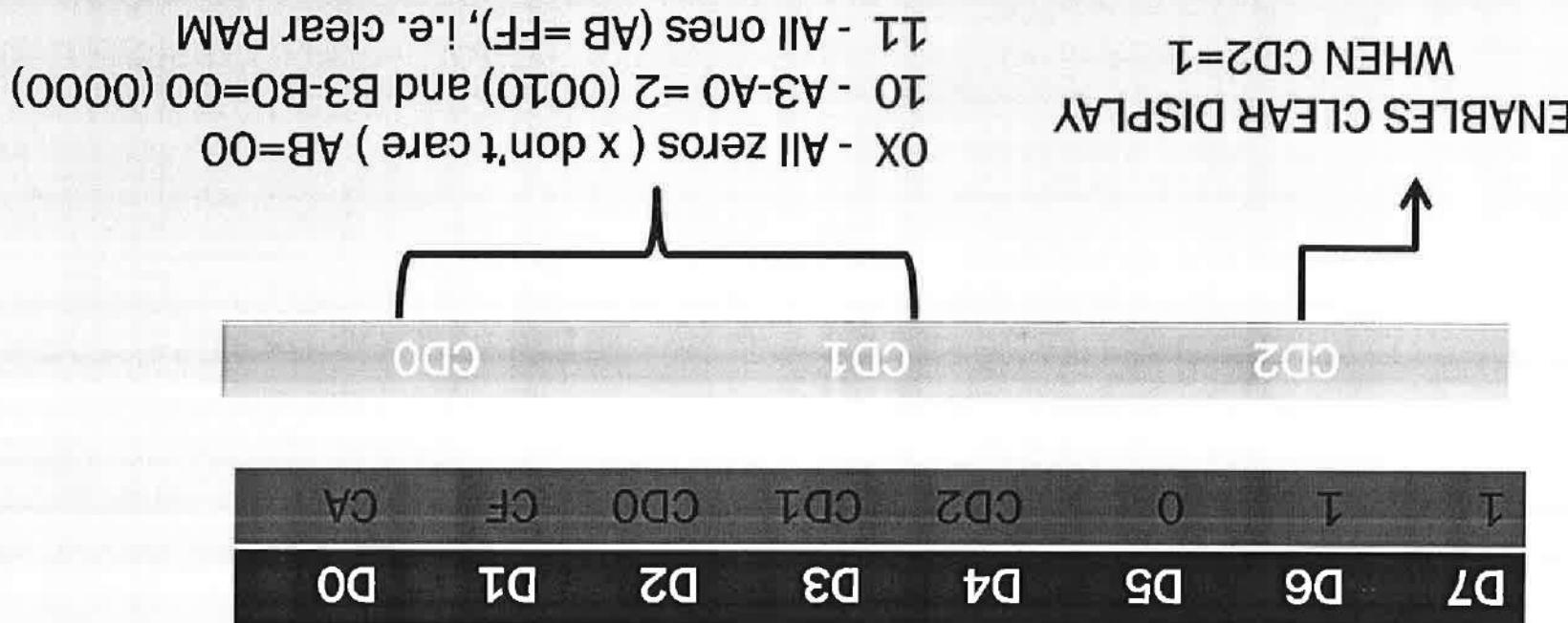
AI - Auto increment Flag.

1	0	0	AI	A	A	A
D7	D6	D5	D4	D3	D2	D1

This command enables a programmer to write the display RAM data.

d) Write Display RAM :

- If CA=1, this combines the effect of CD and CF bits.
- If CF(CLEAR FIFO RAM STATUS) =1, FIFO status is cleared and IRQ line is pulled down and the sensor RAM pointer is set to row 0.
- If CD2 = 0, the clear display command is invoked by setting CA(CLEAR ALL) =1 and maintaining CD1, CDO bits exactly same as above.
- CD2 must be 1 for enabling the clear display command.



g) Clear Display RAM :

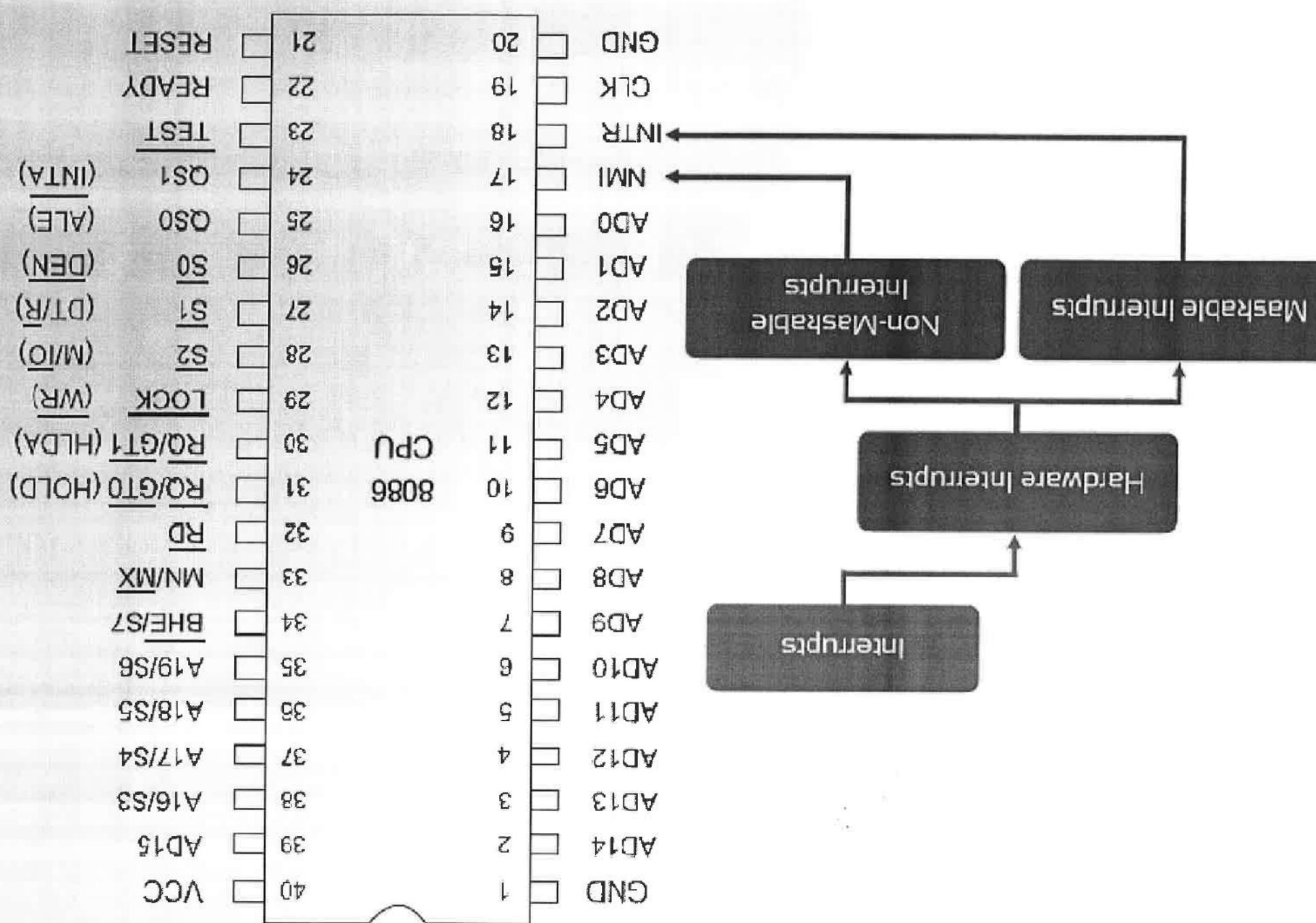
- be „1“, the 8279 operates in special Error mode
- » For N-Key roll over mode, if the E bit is programmed to goes high that inhibits writing in the sensor RAM.
- » Otherwise, if a change in sensor value is detected, IRQ line and enables further writing into the RAM.
- » For the sensor matrix mode, this command lowers the IRQ line and enables further writing into the RAM.

X - don't care  
E - Error mode

1	1	1	E	X	X	X	1
D7	D6	D5	D4	D3	D2	D1	D0

h) End interrupt / Error mode Set :

**INTEGRUP  
CONTROLLER  
INTEL 8259**



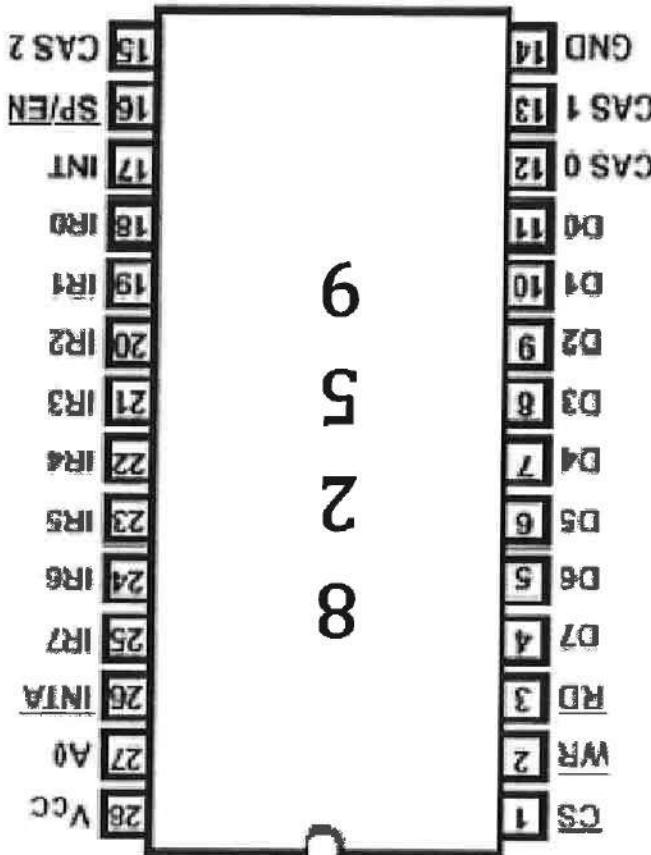
8086 CPU

## 8259 Programmable Interrupt Controller (PIC)

1. This IC is designed to simplify the implementation of the interrupt interface in the 8088 and 8086 based microcomputer systems.
2. This device is known as a 'Programmable Interrupt Controller' or PIC.
3. It is manufactured using the NMOS technology and it is available in 28-pin DIP.
4. The operation of the PIC is programmable under software control (Programmable) and it can be configured for a wide variety of applications.
5. 8259A is treated as peripheral in a microcomputer system.
6. 8259A PIC adds eight vectored priority encoded interrupts to the microprocessor.
7. This controller can be expanded without additional hardware to accept up to 64 interrupt request inputs. This expansion required a master 8259A and eight 8259A slaves.
8. Some of its programmable features are:

- Its ability to be configured to implement a wide variety of priority schemes.
- The ability to be easily cascaded to expand from 8 to 64 interrupt-inputs.
- The ability to accept level-triggered or edge-triggered inputs.

DESCRIPTION	PIN	
Data Bus (Bidirectional)	D7 - D0	
Read Input	RD	
Write Input	WR	
Command Select Address	A0	
Chip Select	CS	
Cascade Lines	CAS 2 · CAS 0	
Slave Program Input Enable	SP/EN	
Interrupt Output	INT	
Interrupt Acknowledge Input	INTA	
Interrupt Request Inputs	IRQ - IRT	

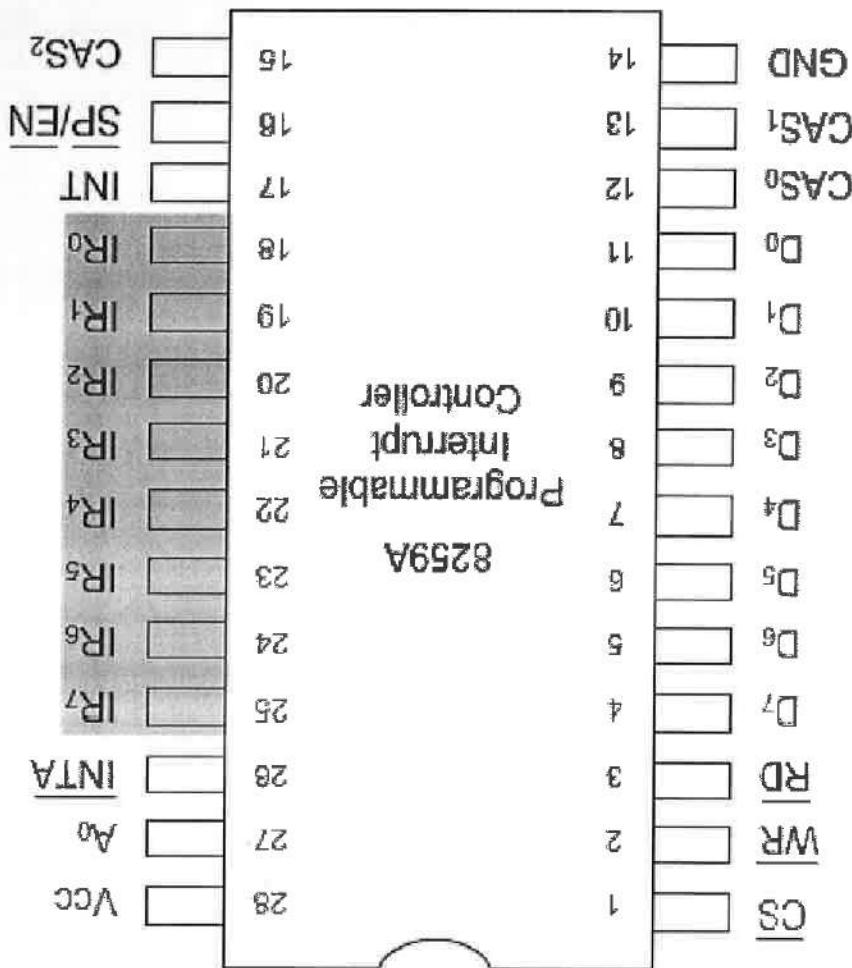


62C59A (PDI/P, CERD/P, SOIC)  
TOP VIEW

# 8259A PIC- PIN DIGRAM

The processor is interrupted whenever the interrupting device delivers a signal to the 8259.

Up to eight hardware interrupting devices are supported.

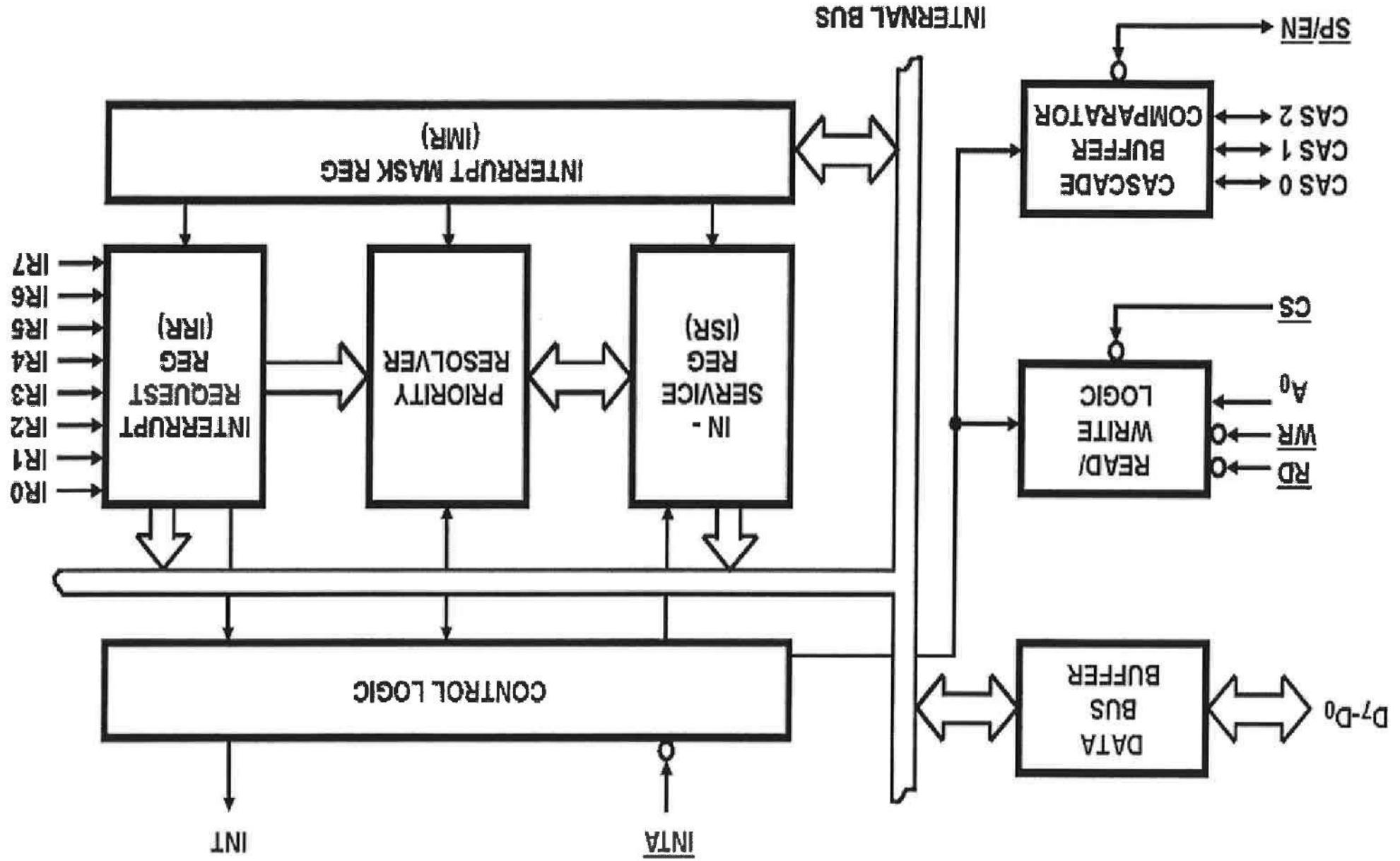


8259 PIC

1. D<sub>7</sub>-D<sub>0</sub> is connected to microprocessor data bus D<sub>7</sub>-D<sub>0</sub> (AD<sub>7</sub>-AD<sub>0</sub>).  
in a system with multiple 8259As.
2. IR<sub>7</sub>-IR<sub>0</sub>, Interrupt Request inputs are used to request an interrupt and to connect to a slave
3. WR - the write input connects to write strobe signal of microprocessor.  
in a system with multiple 8259As.
4. RD - the read input connects to the IORC signal.
5. INT - the interrupt output connects to the INTR pin on the microprocessor from the master,  
and is connected to a master IR pin on a slave.
6. INTA - the interrupt acknowledge is an input that connects to the INTA signal on the system.
7. AO - this address input selects different command words within the 8259A.  
In a system with a master and slaves, only the master INTA signal is connected.
8. CS - chip select enables the 8259A for programming and control.
9. SP/EN - Slave Program/Enable Buffer is a dual-function pin.

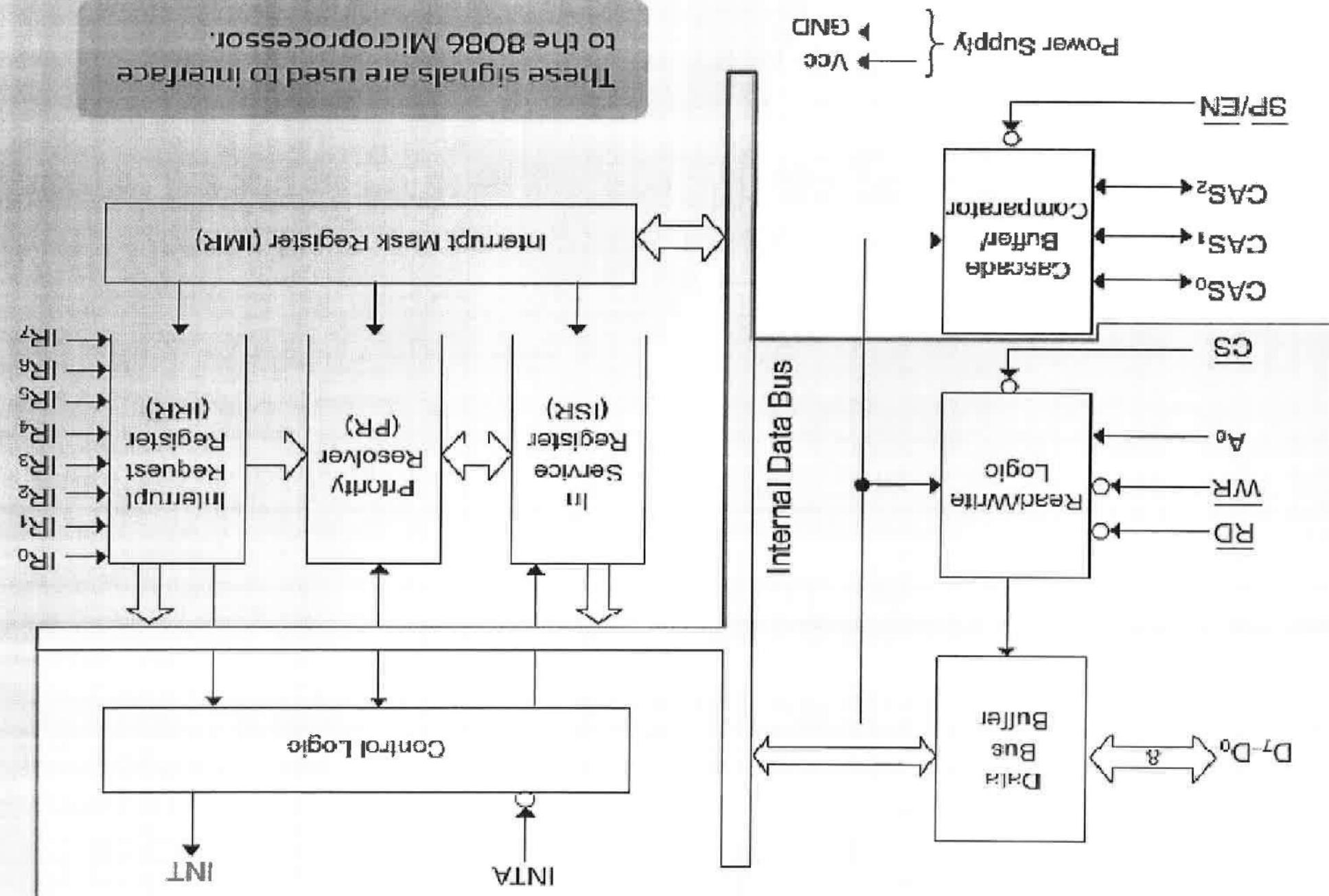
## ASSIGNMENT OF SIGNALS FOR 8259:

- ❖ When the 8259A is in buffered mode, this pin is an output that controls the data bus transceivers in a large microprocessor-based system.
- ❖ When the 8259A is in buffered mode, this pin is an output that controls the data bus transceivers in a large microprocessor-based system.
- ❖ When the 8259A is not in buffered mode, this pin programs the device as a master (1) or a slave (0).
- ❖ CAS2-CAS0, the cascade lines are used as outputs from the master to the slaves for cascading multiple 8259As in a system.

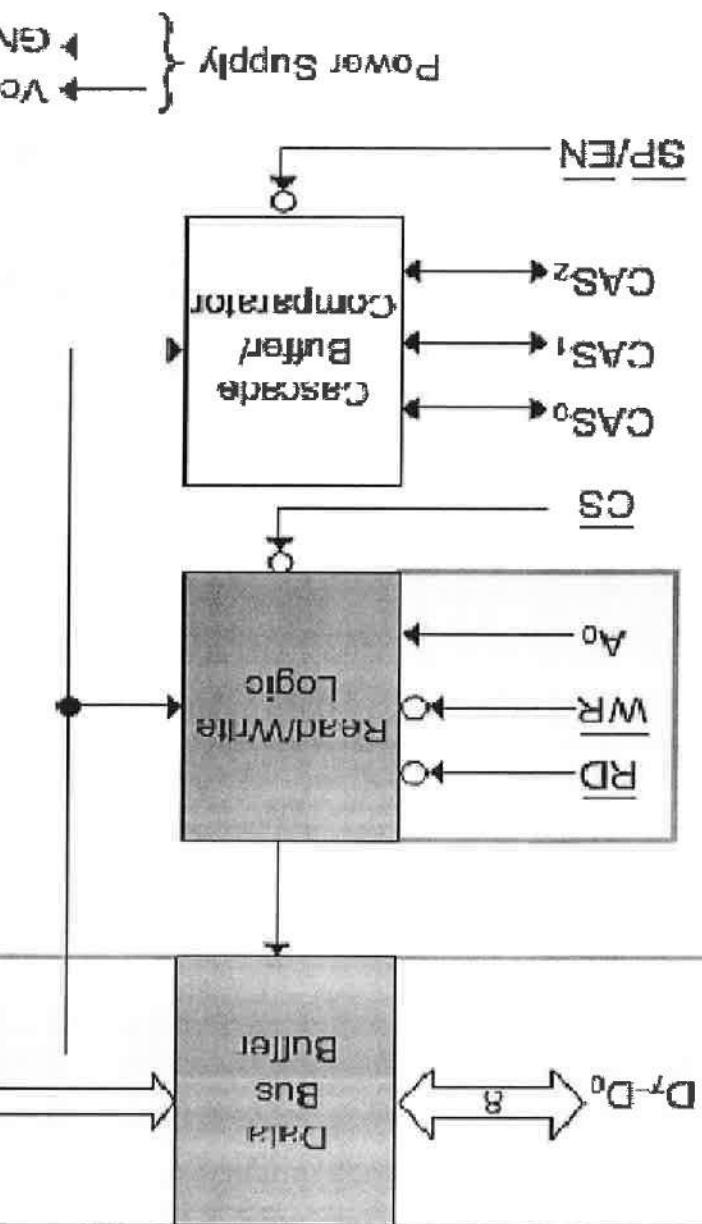
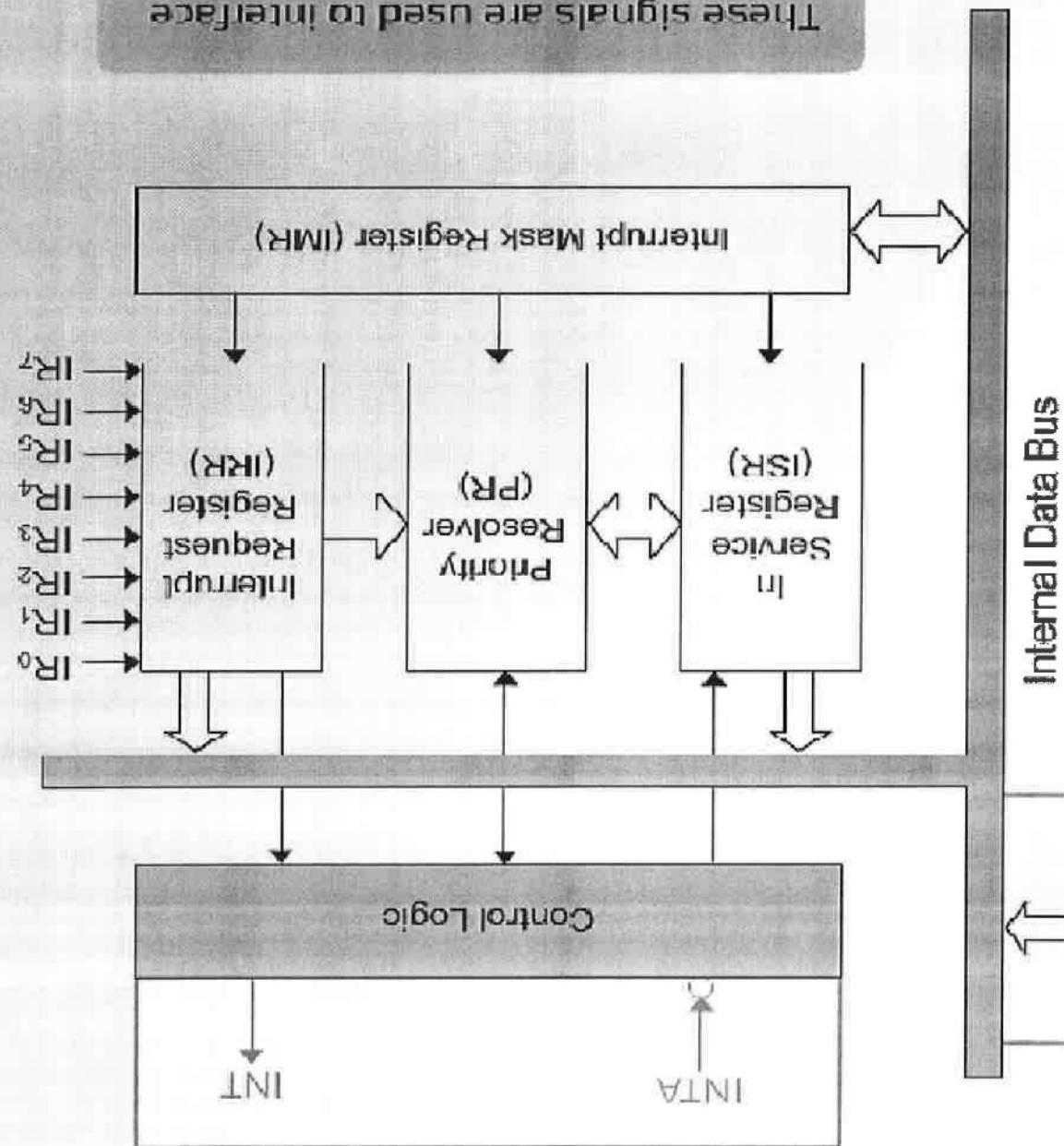


8259A PIC - BLOCK DIAGRAM

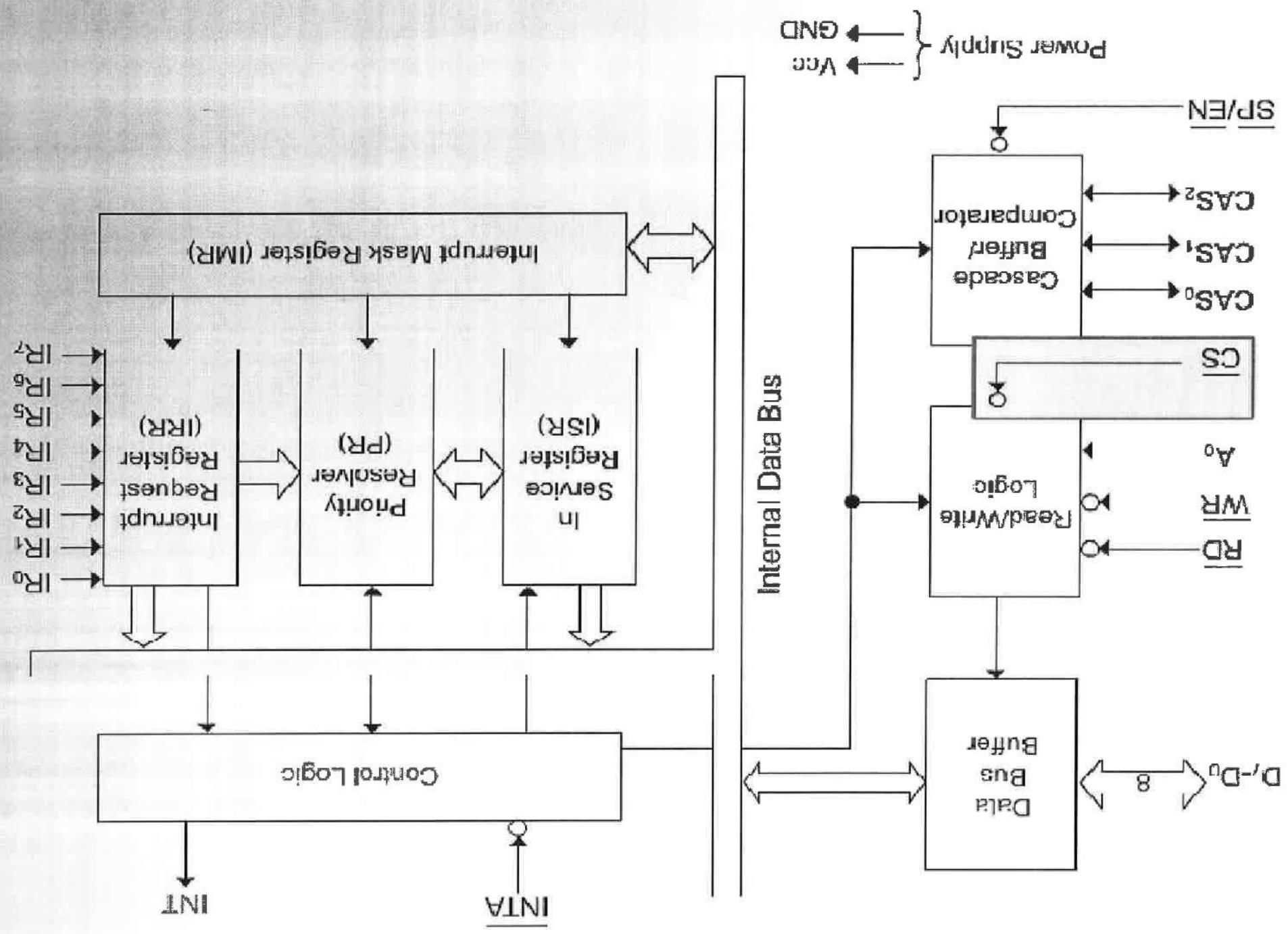
## The Internals of 8259



These signals are used to interface to the 8086 Microprocessor.

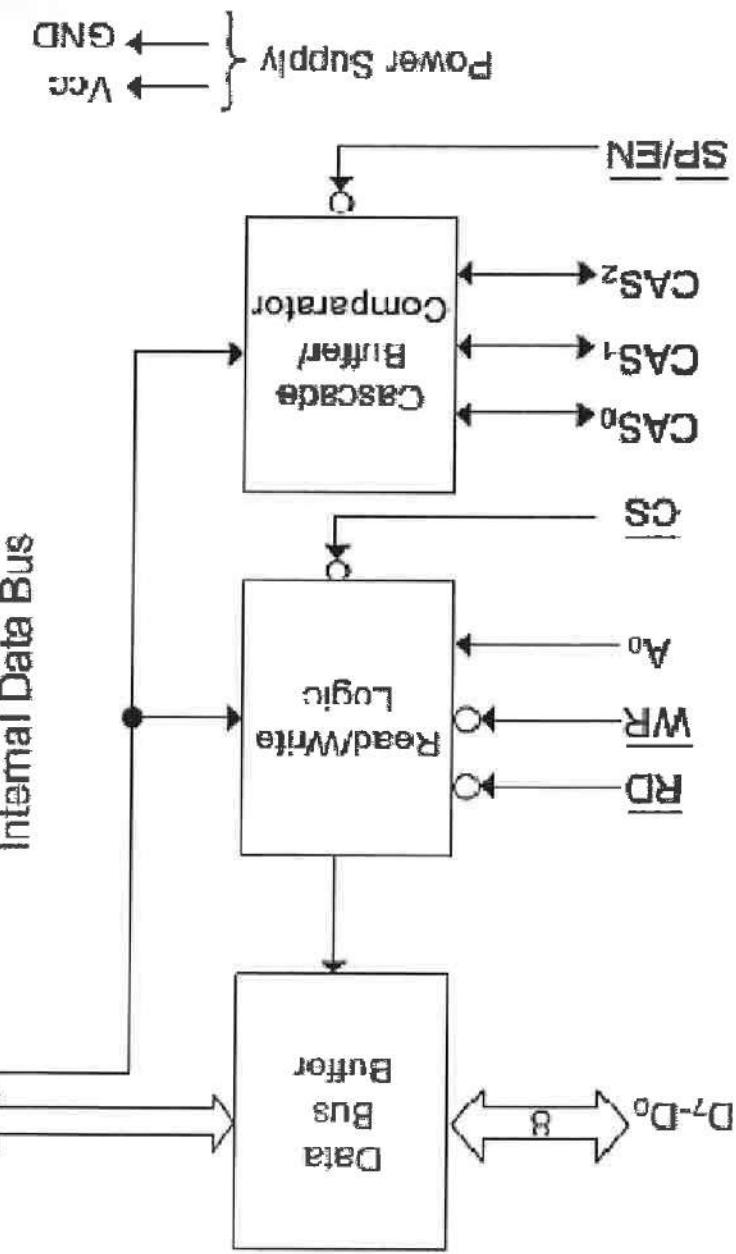
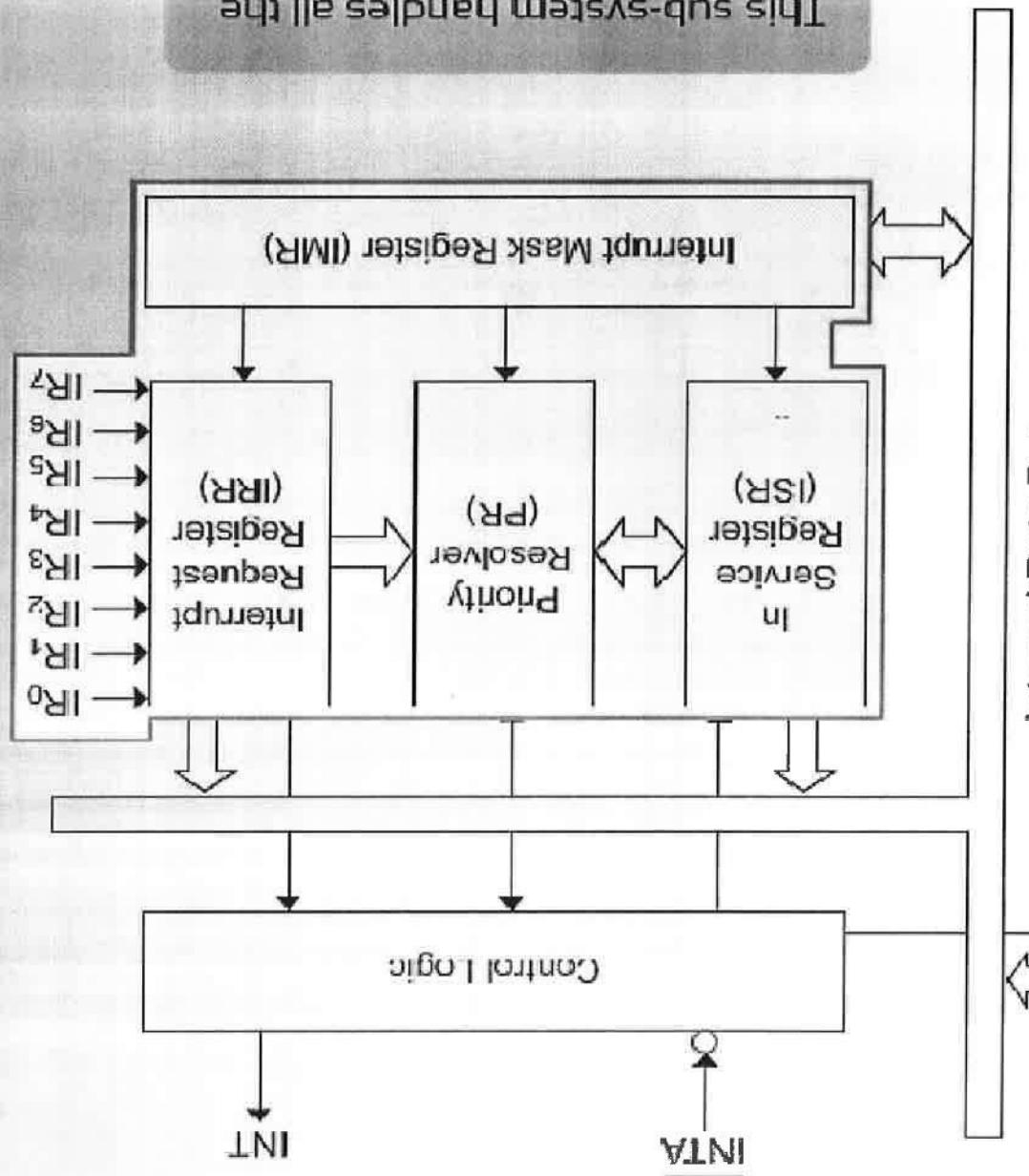


The Internals of 8259

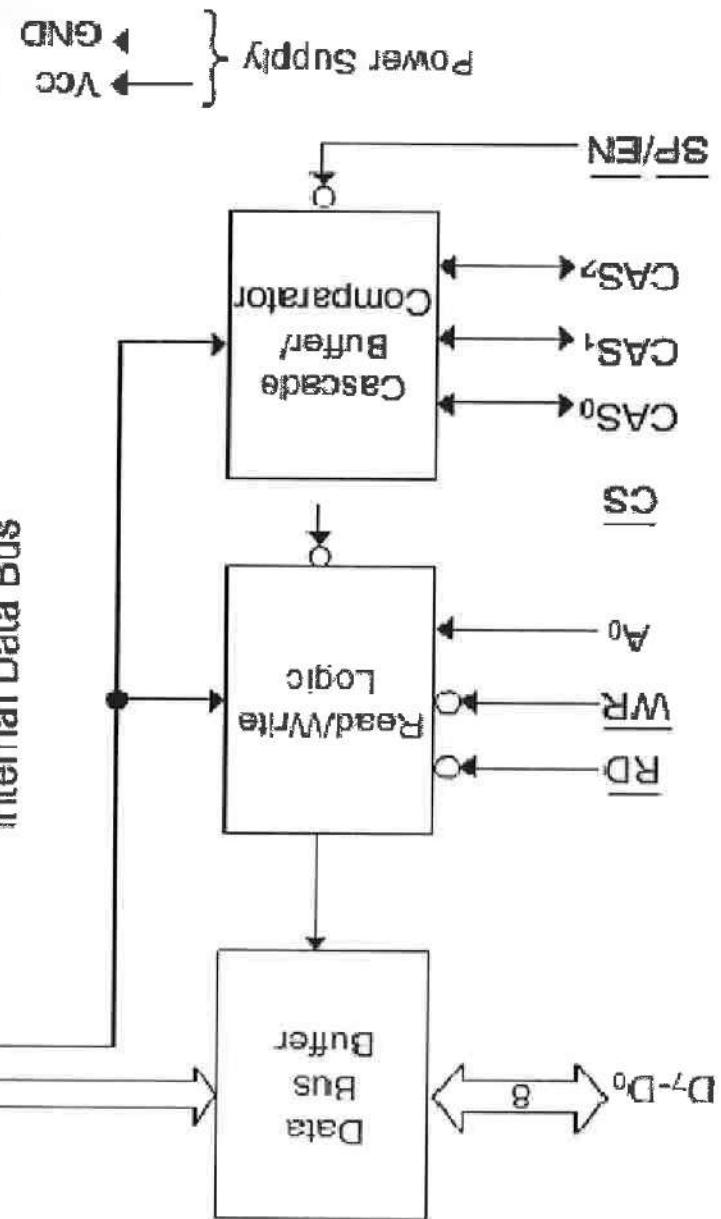
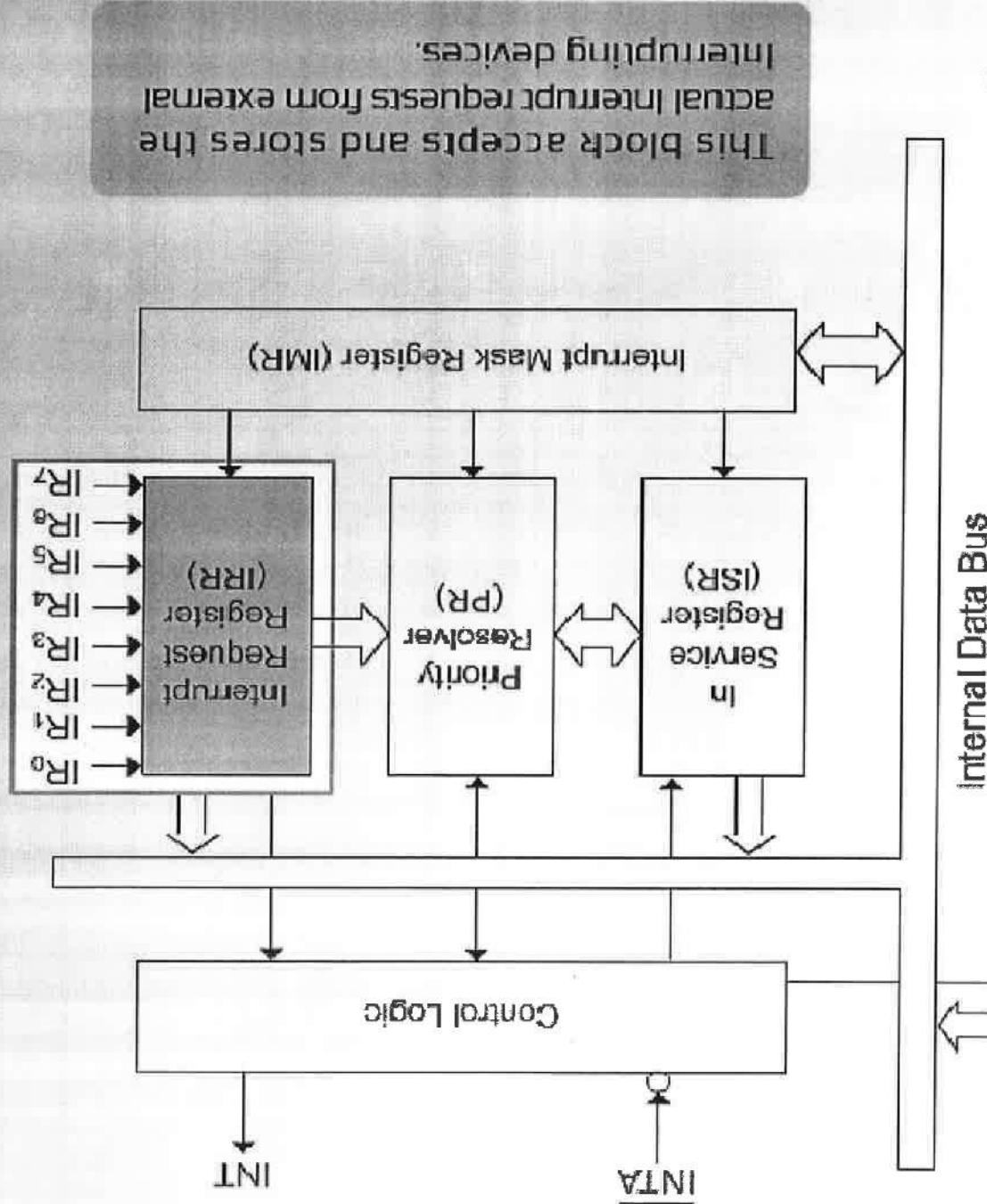


The Internals of 8259

This sub-system handles all the external interrupt requests.



The Internals of 8259

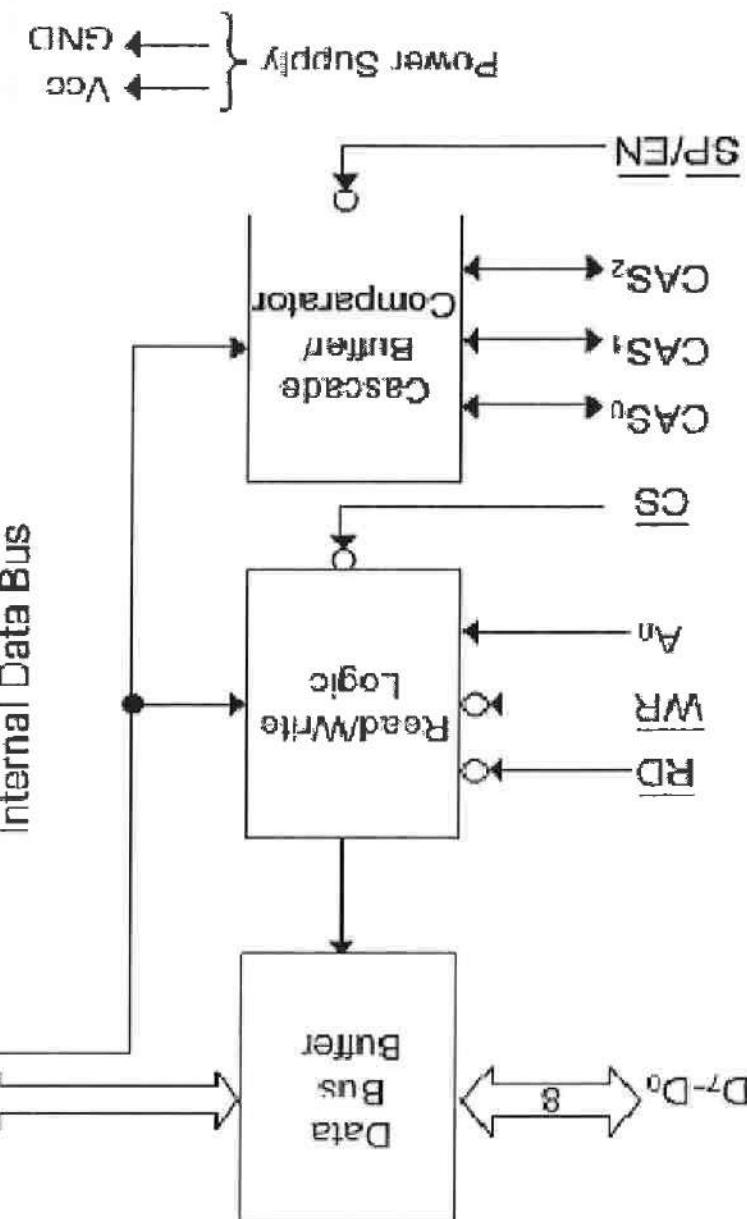
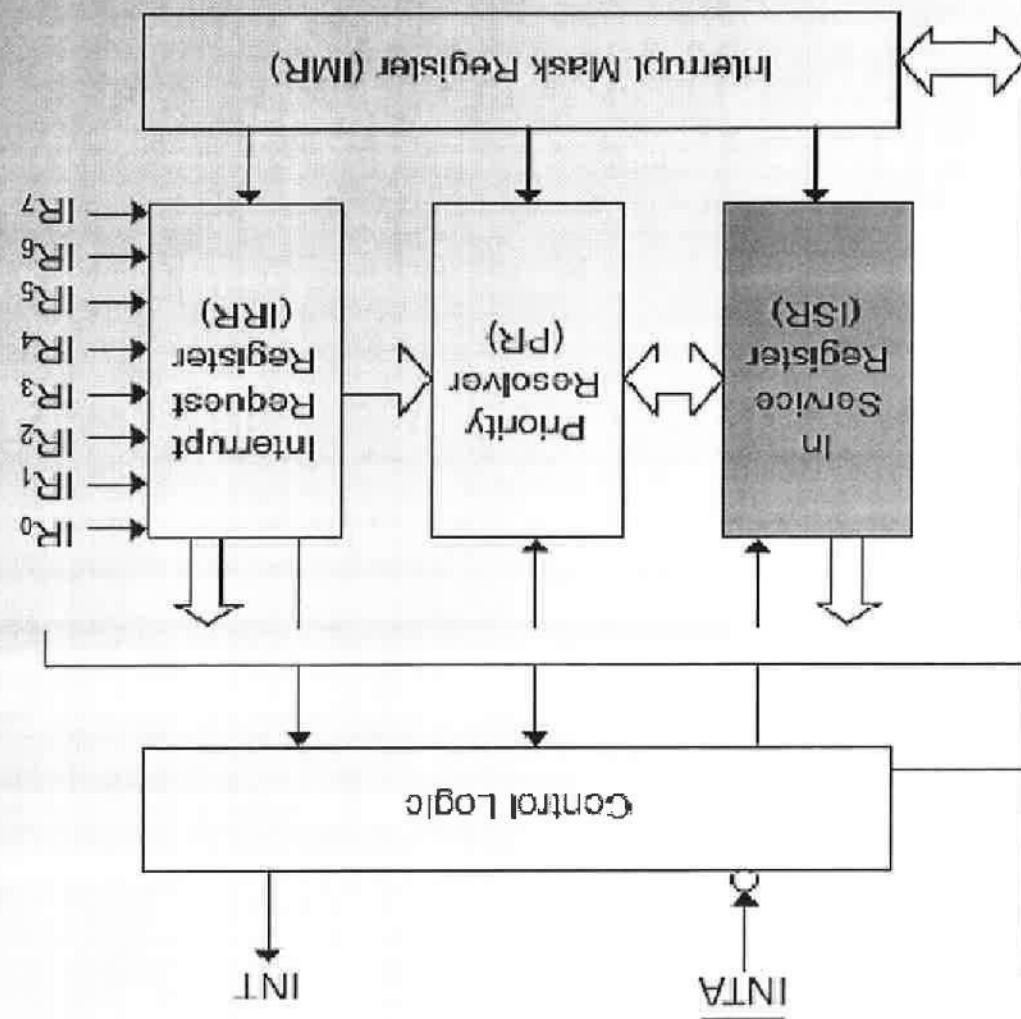


The Internals of 8259

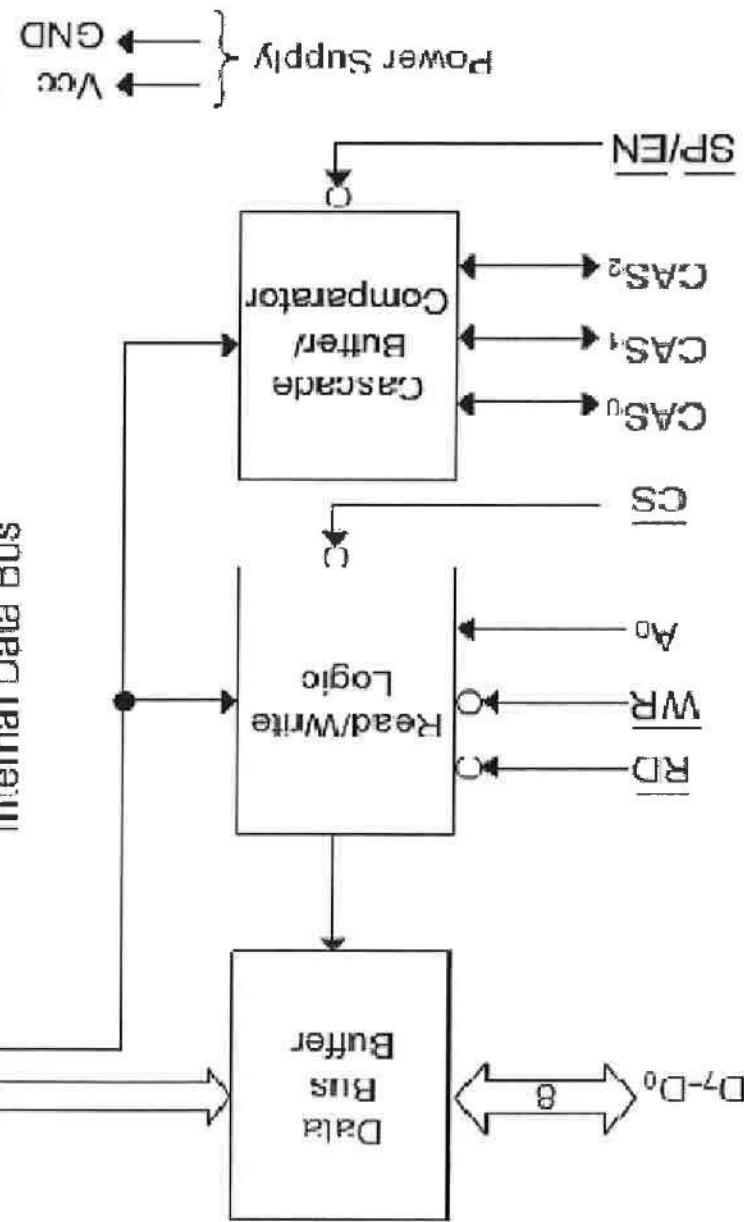
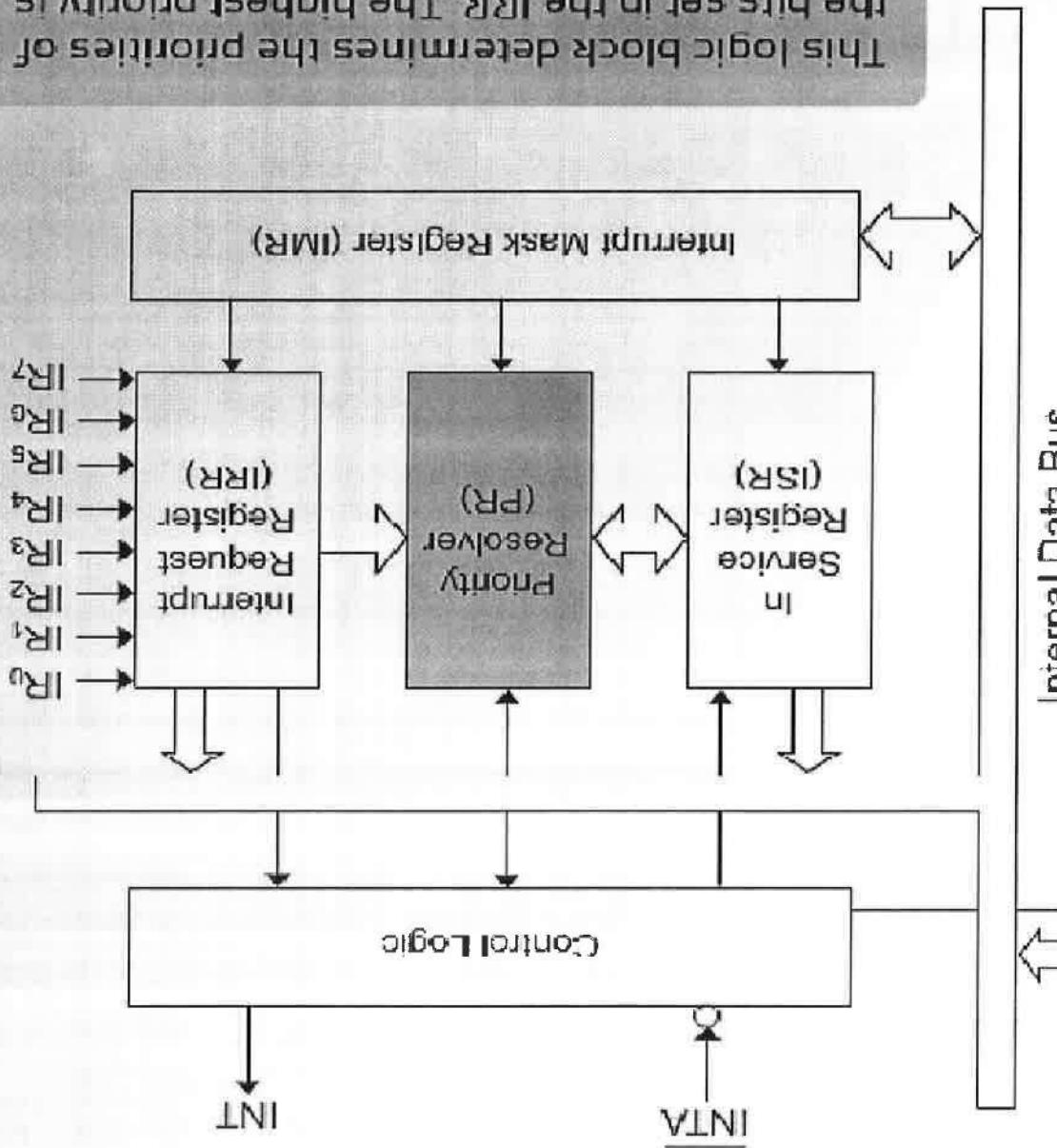
## The Internals of 8259

This block identifies all the current interrupts that are serviced by the processor.

The ISR acts as a buffer between the interrupt requests and the 8086.

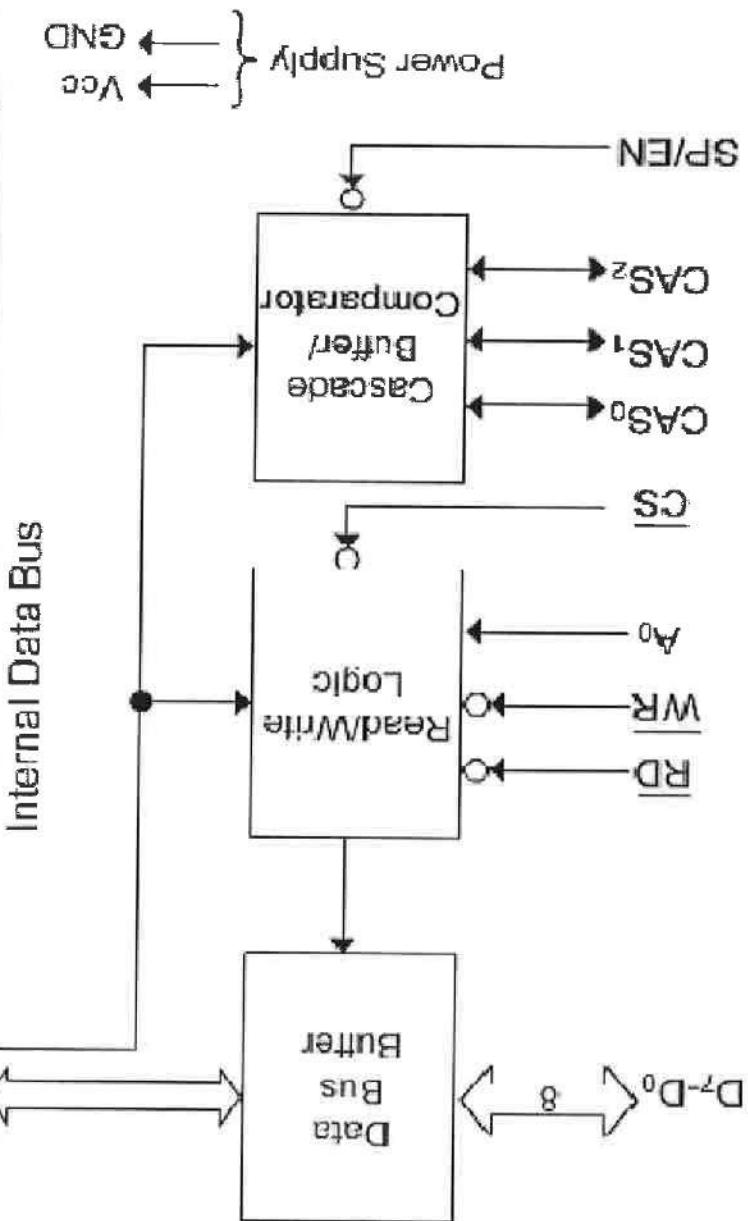
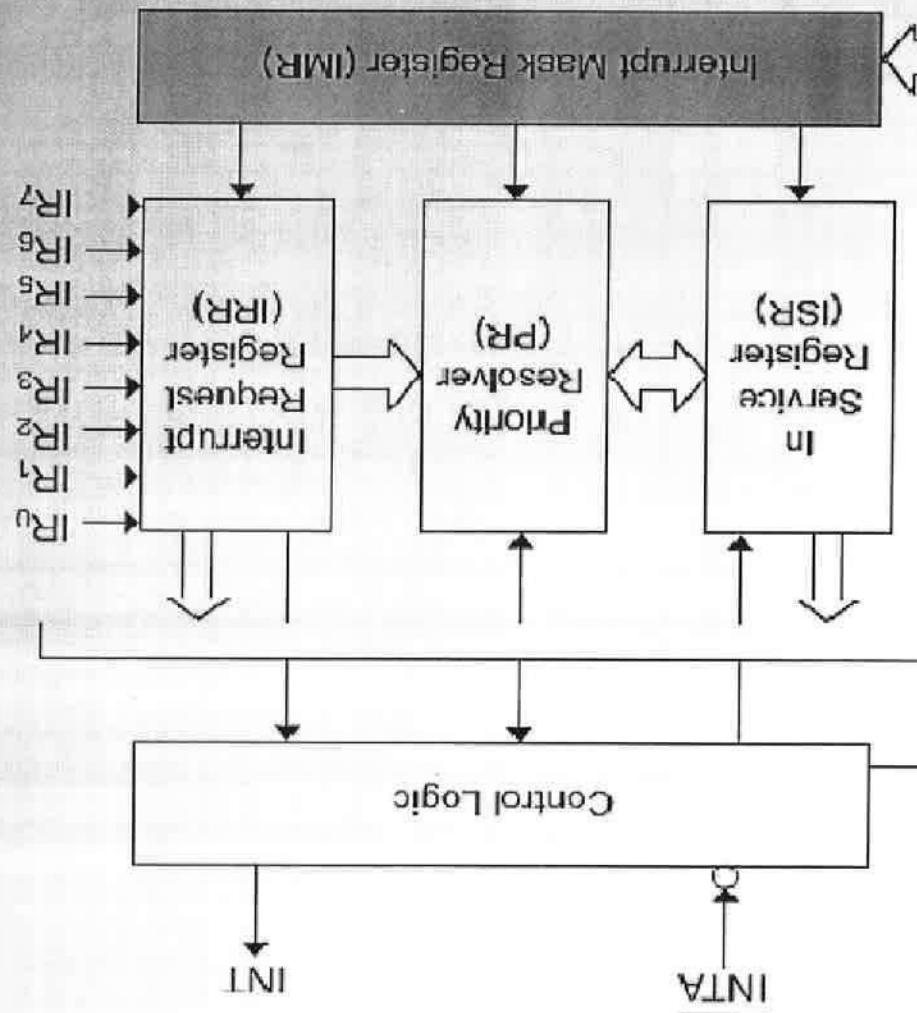


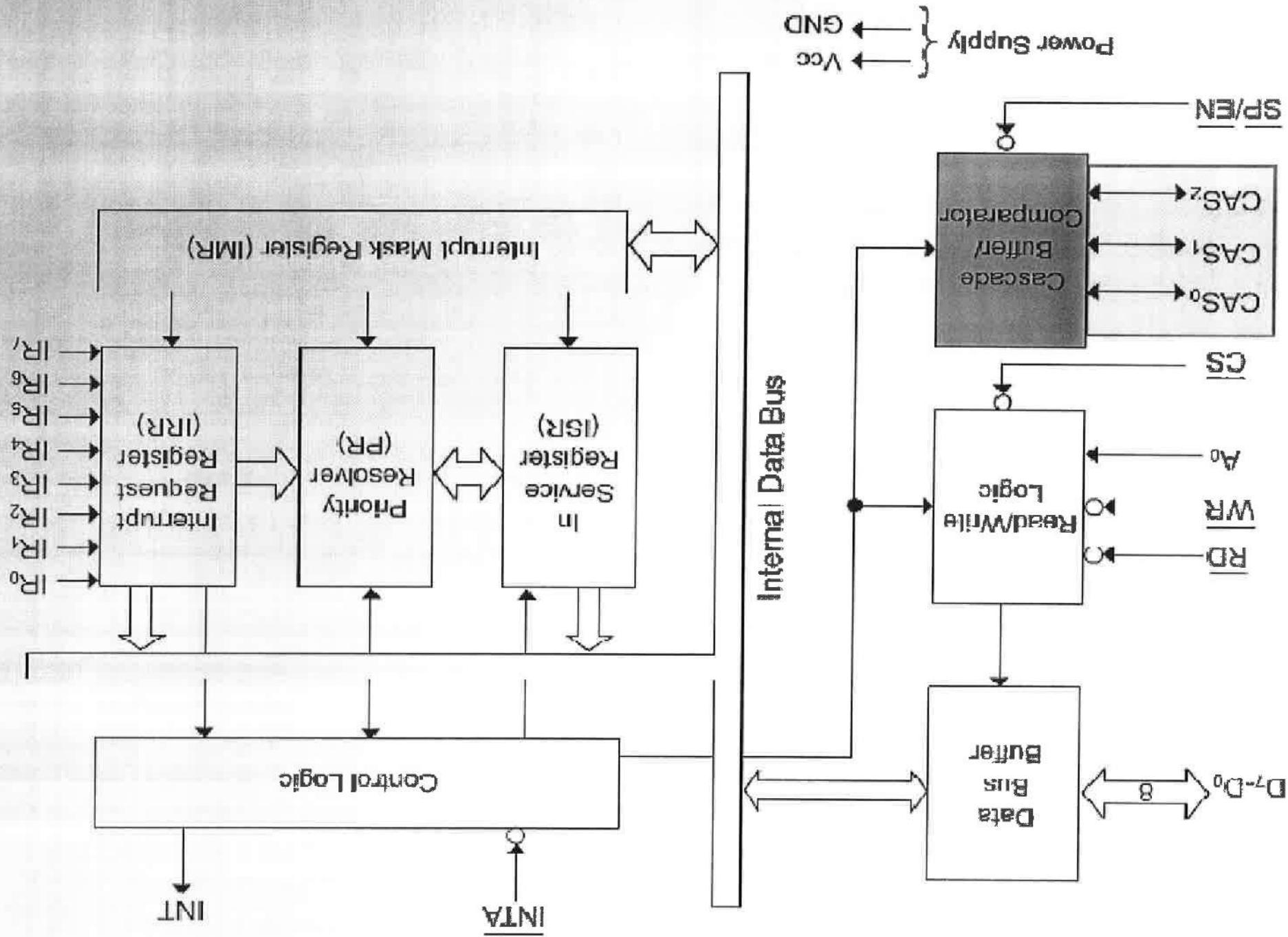
This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during INTA Pulse.



## The Internals of 8259

This logic block masks interrupt lines based on programming by the processor. It prevents masked interrupt lines from interrupting the processor.



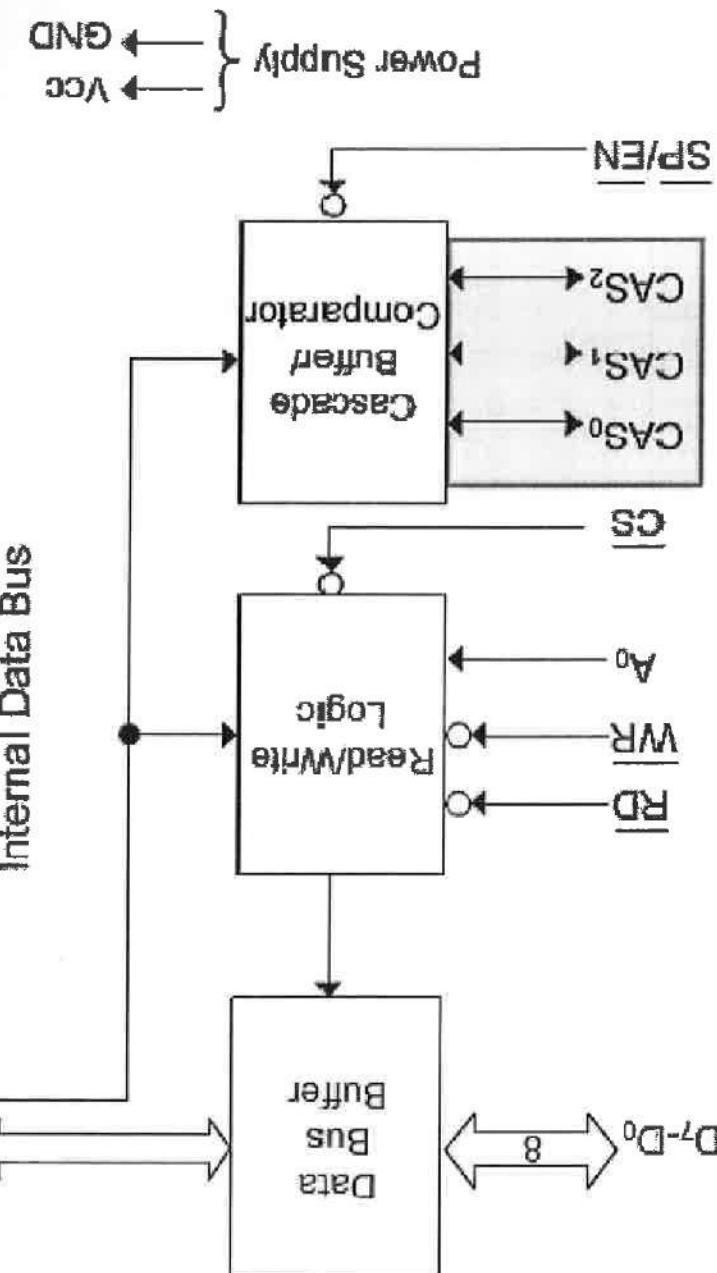
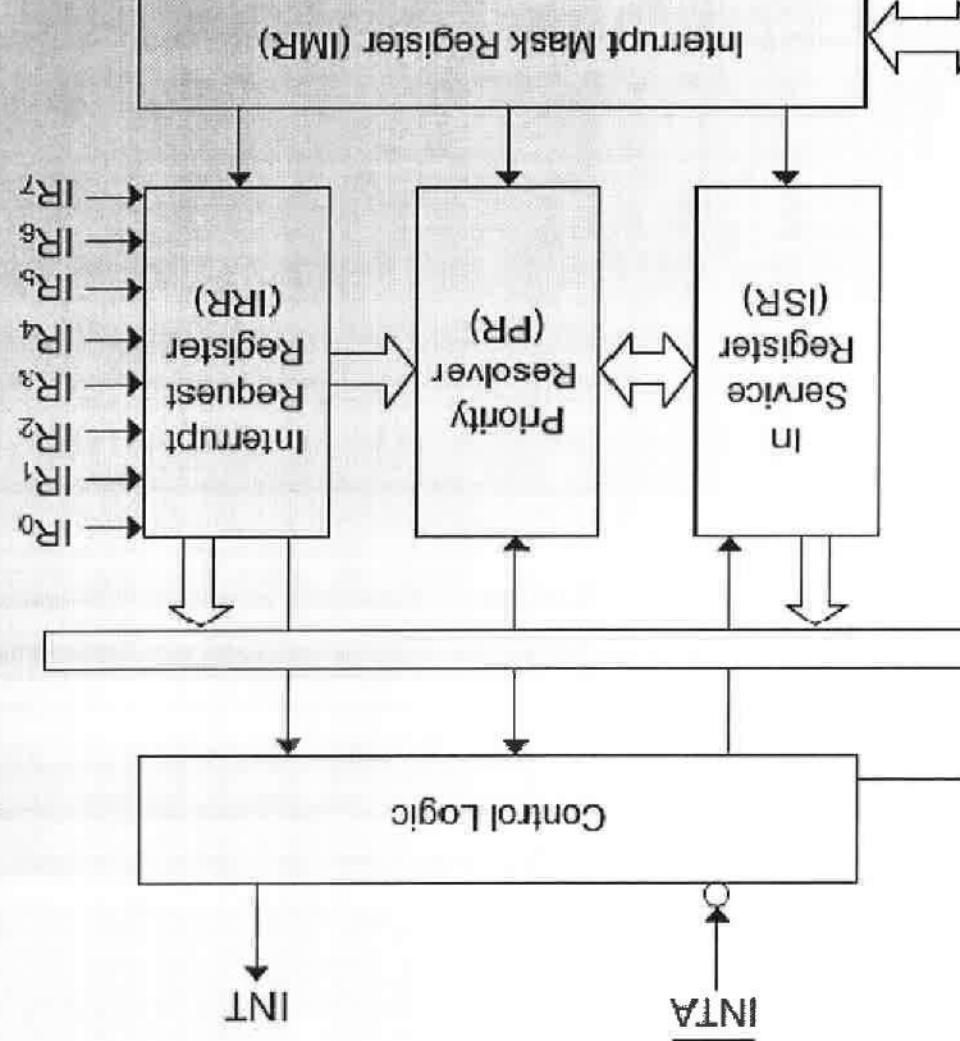


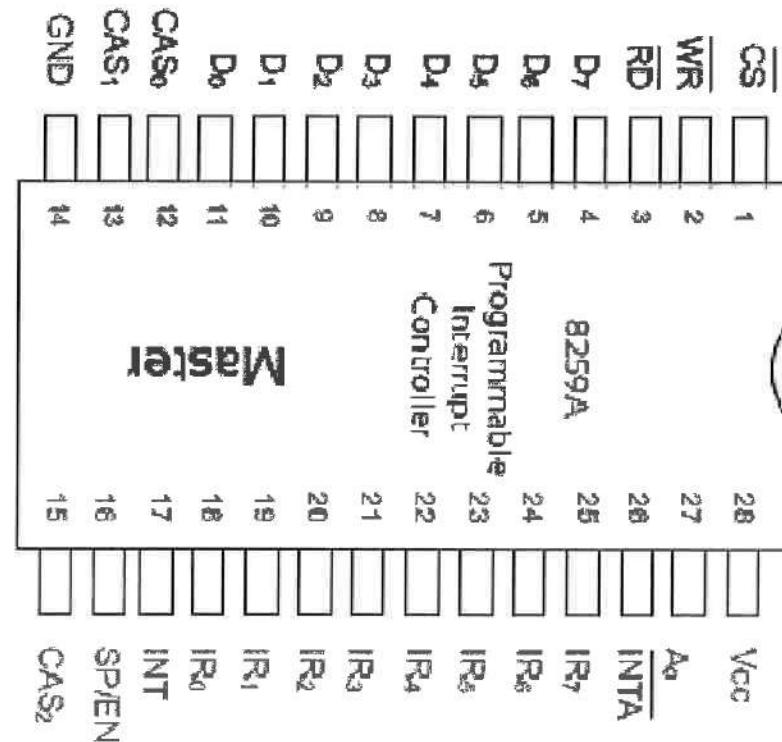
The Internals of 8259

## The Internals of 8259

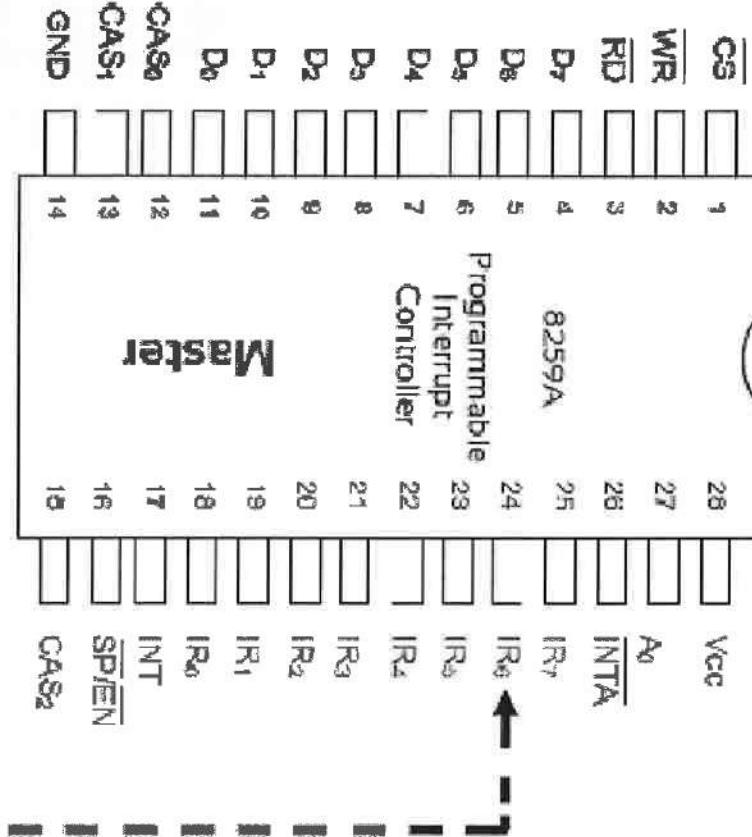
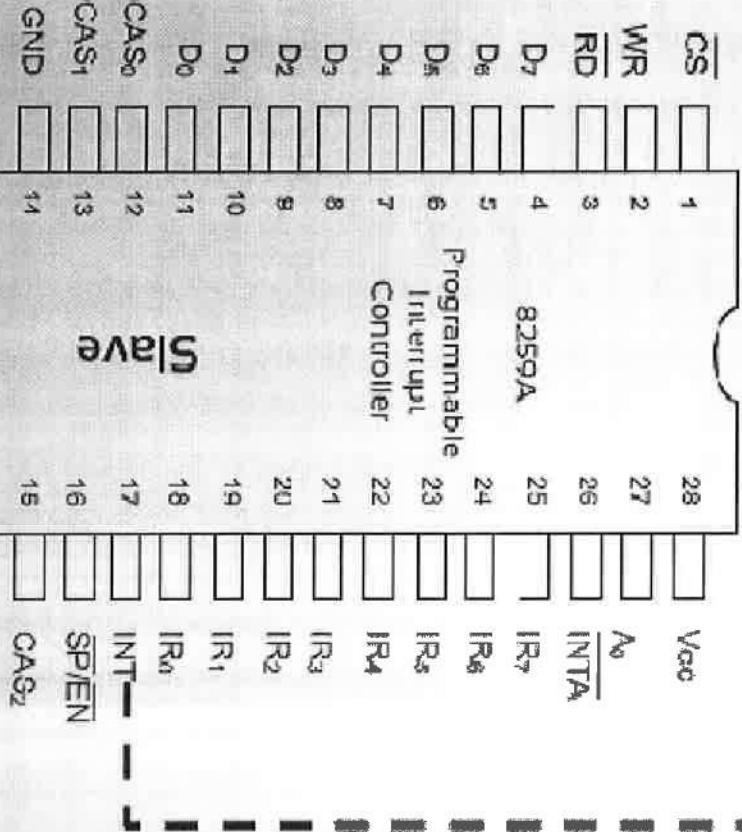
This logic allows for cascading multiple 8259 controllers in a Master-Slave configuration.

8259

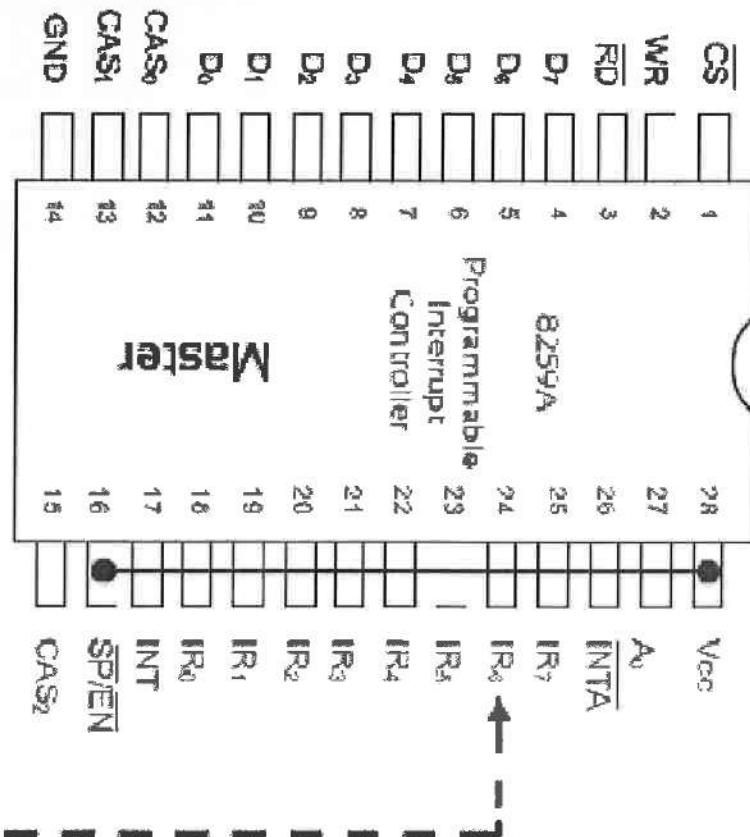
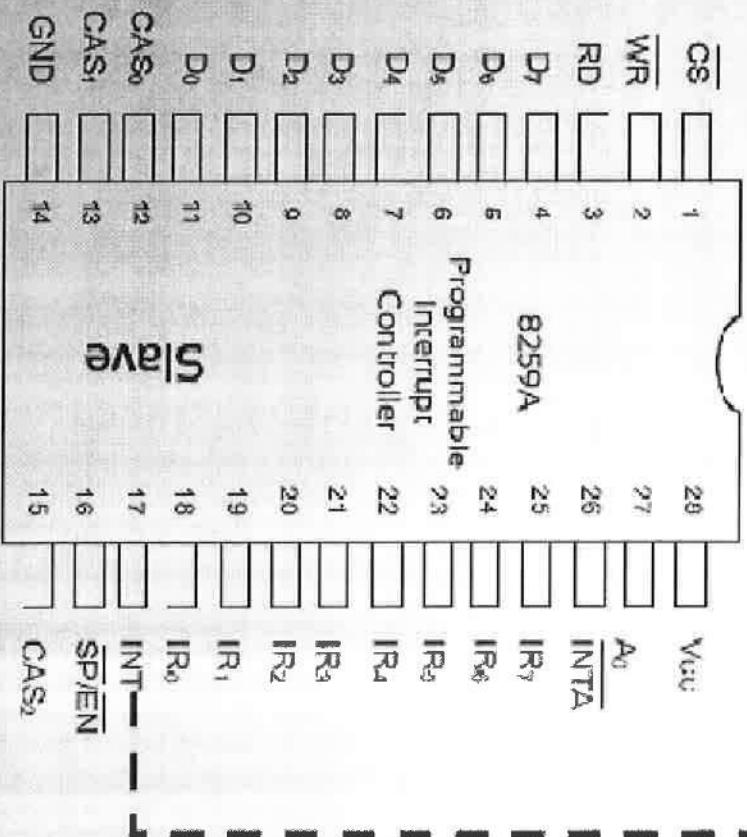




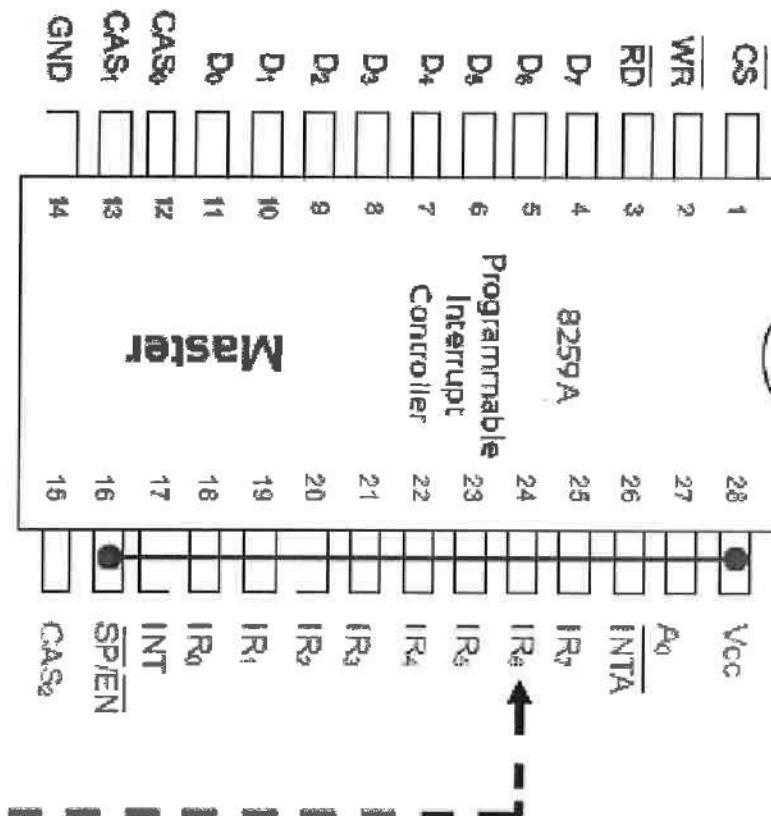
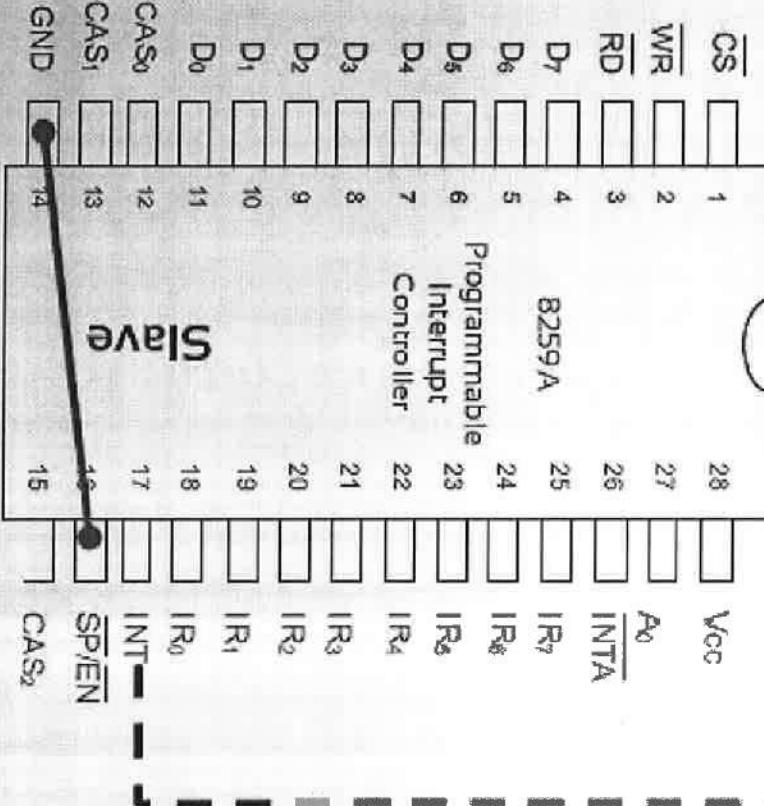
Master-Slave Concept in 8259



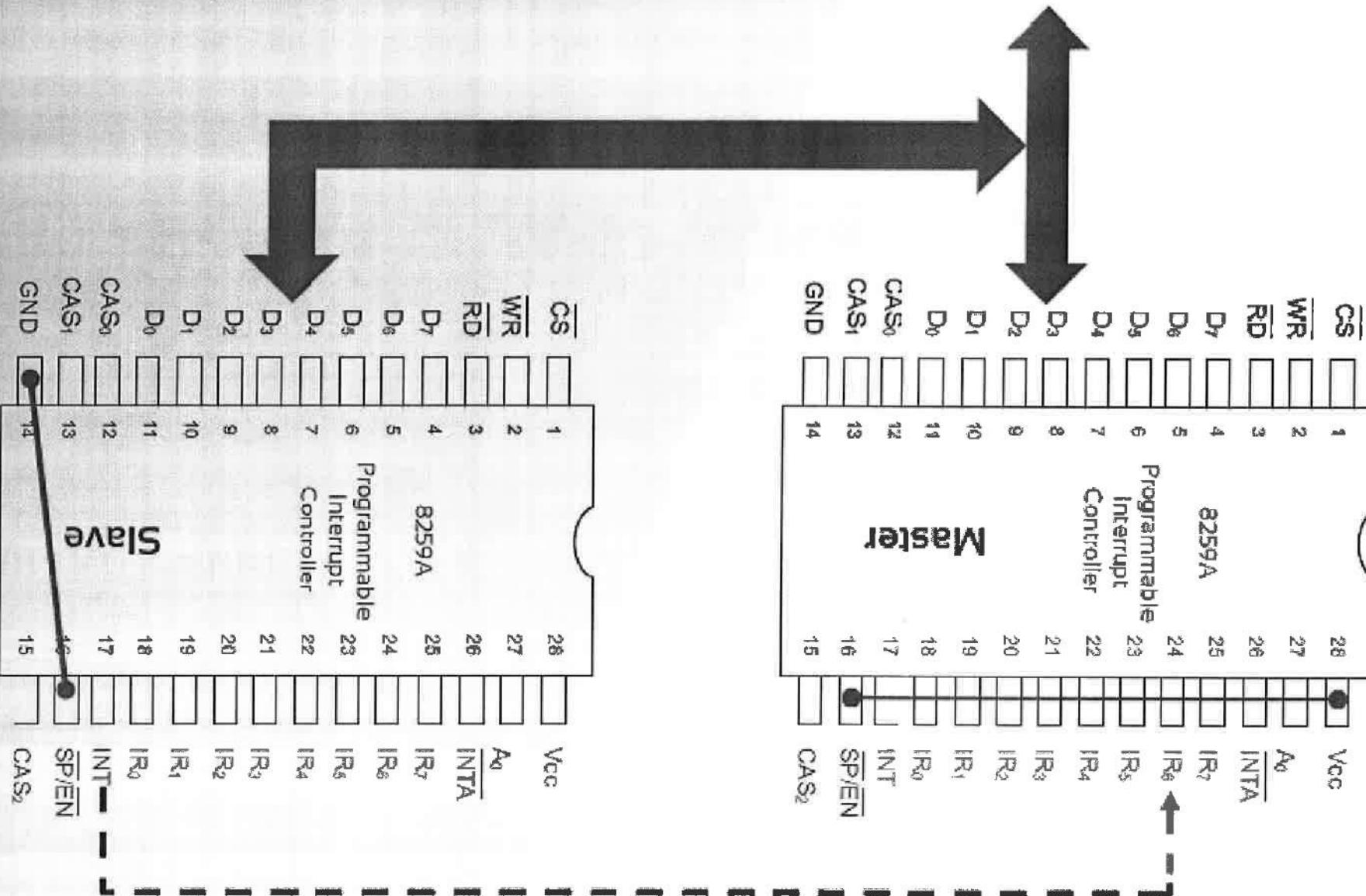
Master-Slave Concept in 8259



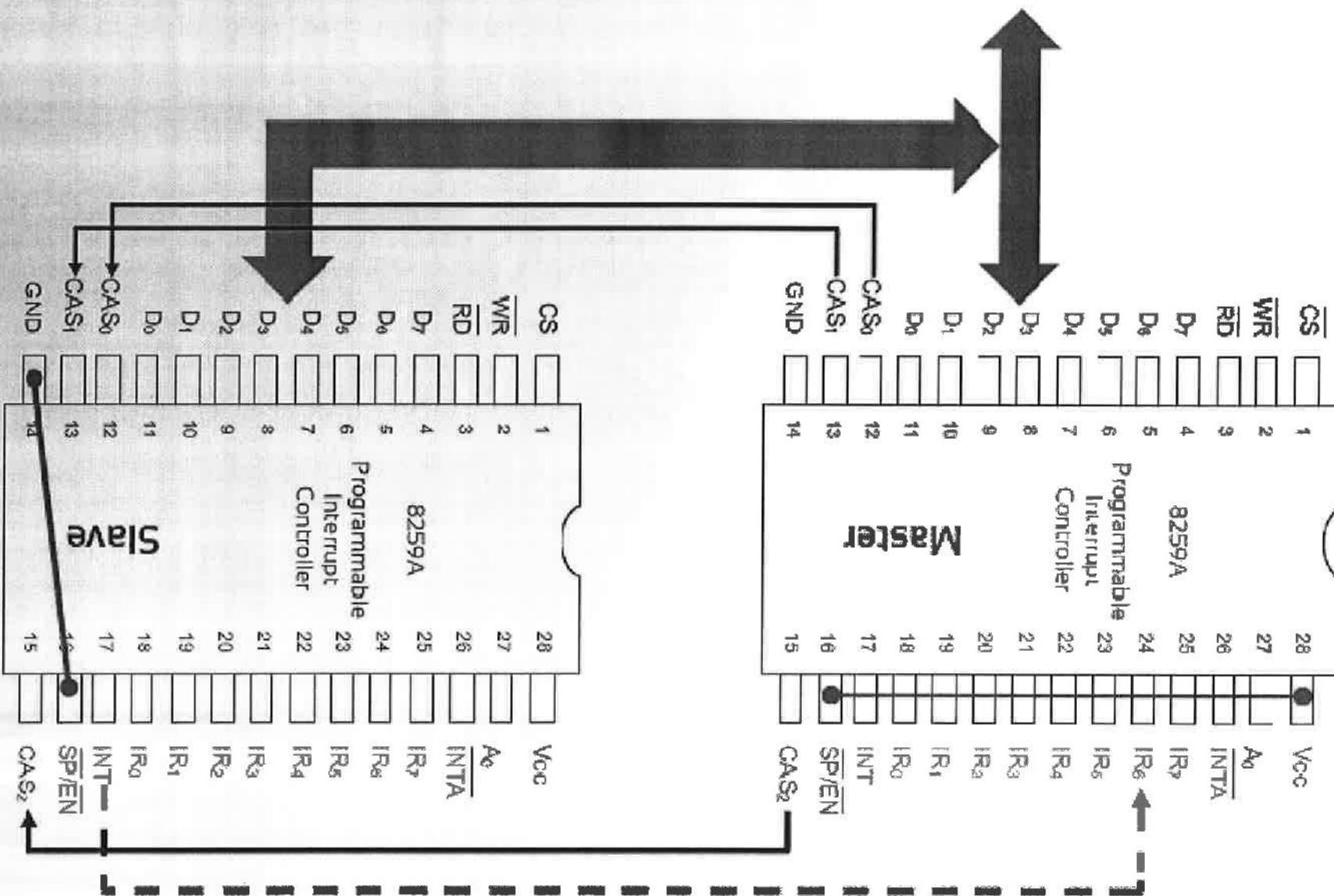
Master-Slave Concept in 8259



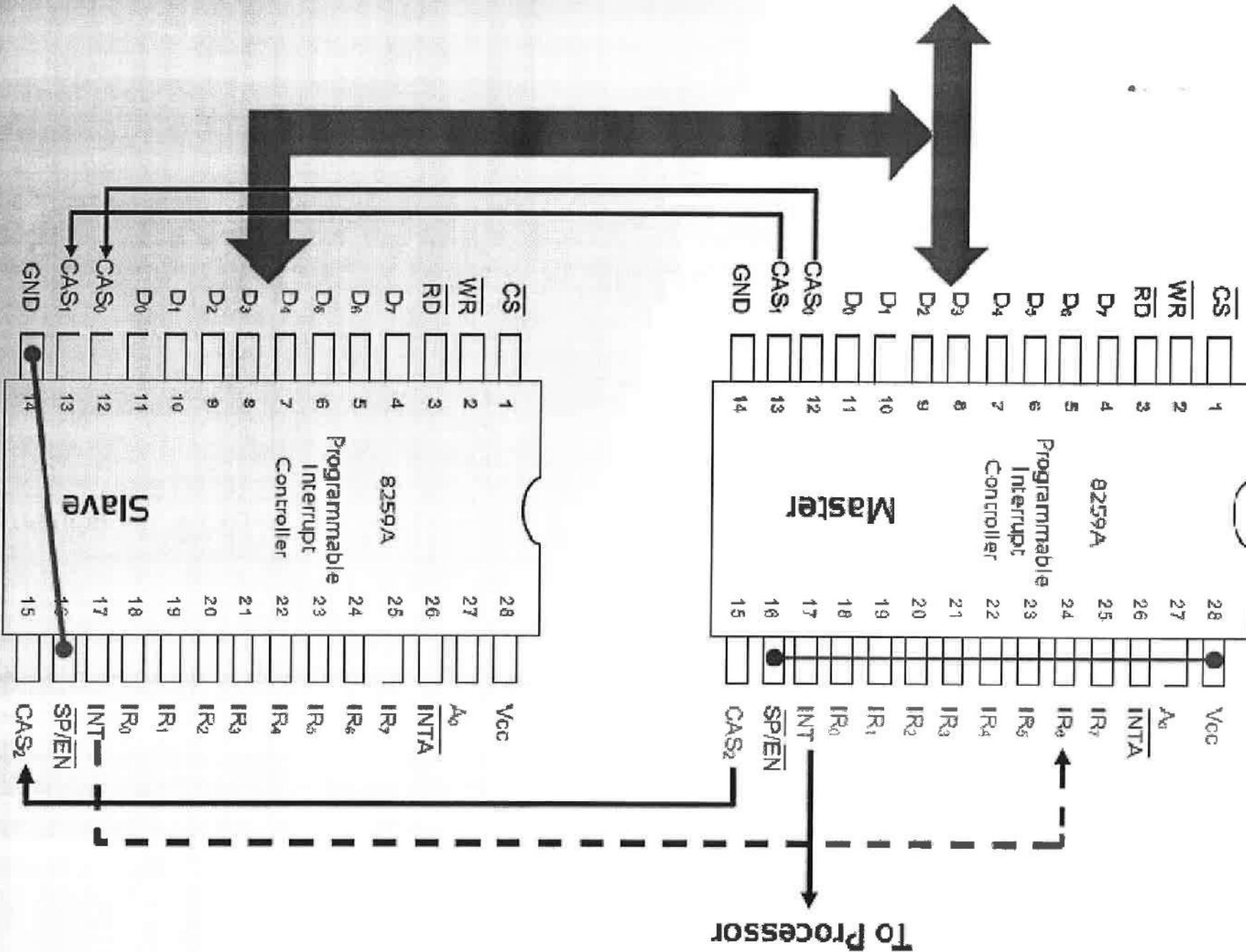
Master-Slave Concept in 8259



Master-Slave Concept in 8259



Master-Slave Concept in 8259



Master-Slave Concept in 8259

## **Programming the 8259A:-**

The 8259A accepts two types of command words generated by the CPU:

1. Initialization Command Words (ICWs):

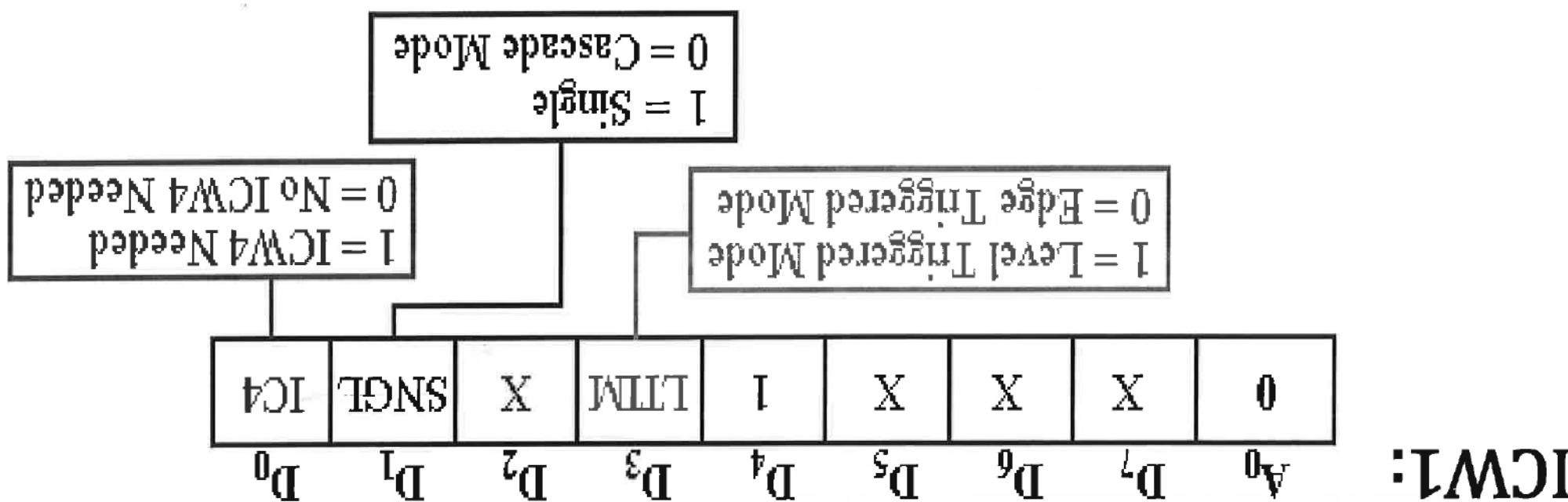
Before normal operation can begin, each 8259A in the system must be brought to a starting point - by a sequence of 2 to 4 bytes timed by WR pulses.

These are the command words which command the 8259A to operate in various interrupt modes. Among these modes are:

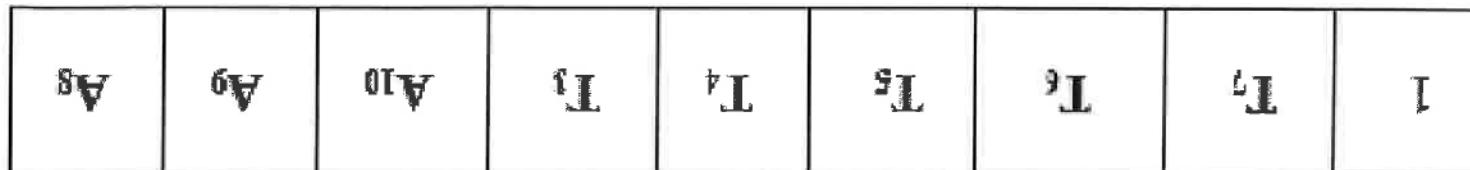
- a. Fully nested mode.
- b. Rotating priority mode.
- c. Special mask mode.
- d. Poll mode.

The OCWs can be written into the 8259A anytime after initialization.

- ❖ To program this ICW for 8086 we place a logic 1 in bit IC4.
- ❖ Bits D7, D6 , D5 and D2 are don't care for microprocessor operation and only
- ❖ This ICW selects single or cascade operation by programming the SNGL bit. If apply to the 8259A when used with an 8-bit 8085 microprocessor.
- ❖ This ICW selects single or cascade operation by programming the SNGL bit. If cascade operation is selected, we must also program ICW3.
- ❖ The LTM bit determines whether the interrupt request inputs are positive edge triggered or level-triggered.

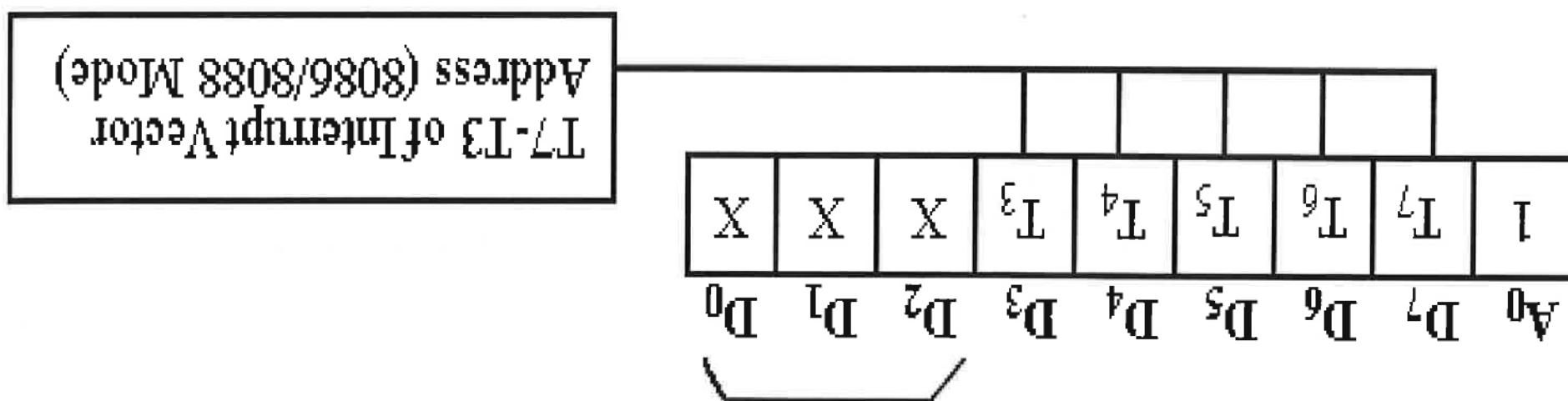


- $A_0 = 1$  selects ICW<sub>2</sub>.
- They are not the address lines of Microprocessor.
- $A_{10} - A_8$  – Selected according to interrupt request level.
- $T_7 - T_3$  are  $A_3 - A_0$  of interrupt address



$70H$  in this ICW.  $A_0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0$

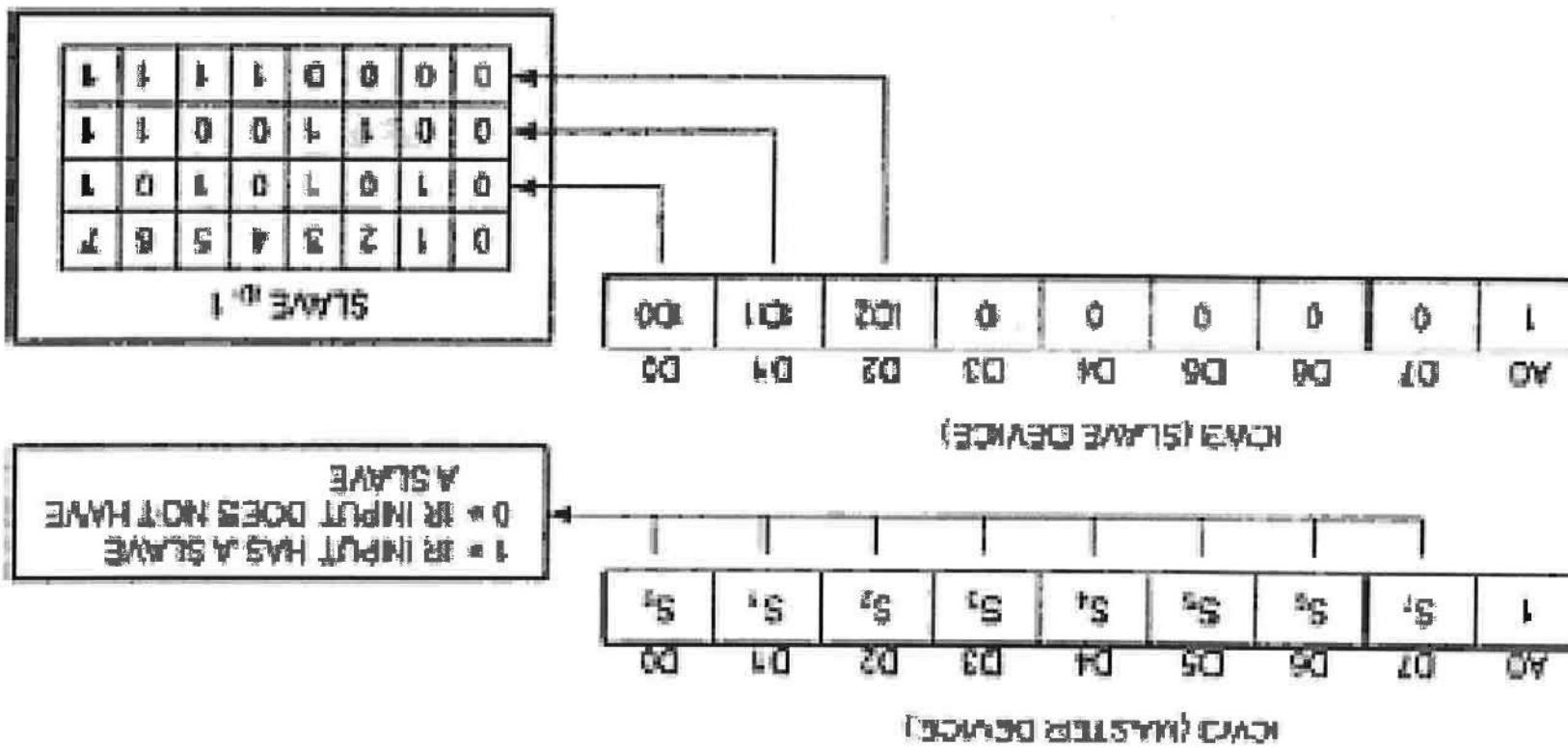
- ❖ Likewise, if we decide to program the 8259A for vectors  $70H - 77H$ , we place a locations  $08H - 0FH$ , we place a  $08H$  into this command word.
- ❖ For example, if we decide to program the 8259A so that it functions at vector
- ❖ Selects the vector number used with the interrupt request inputs.



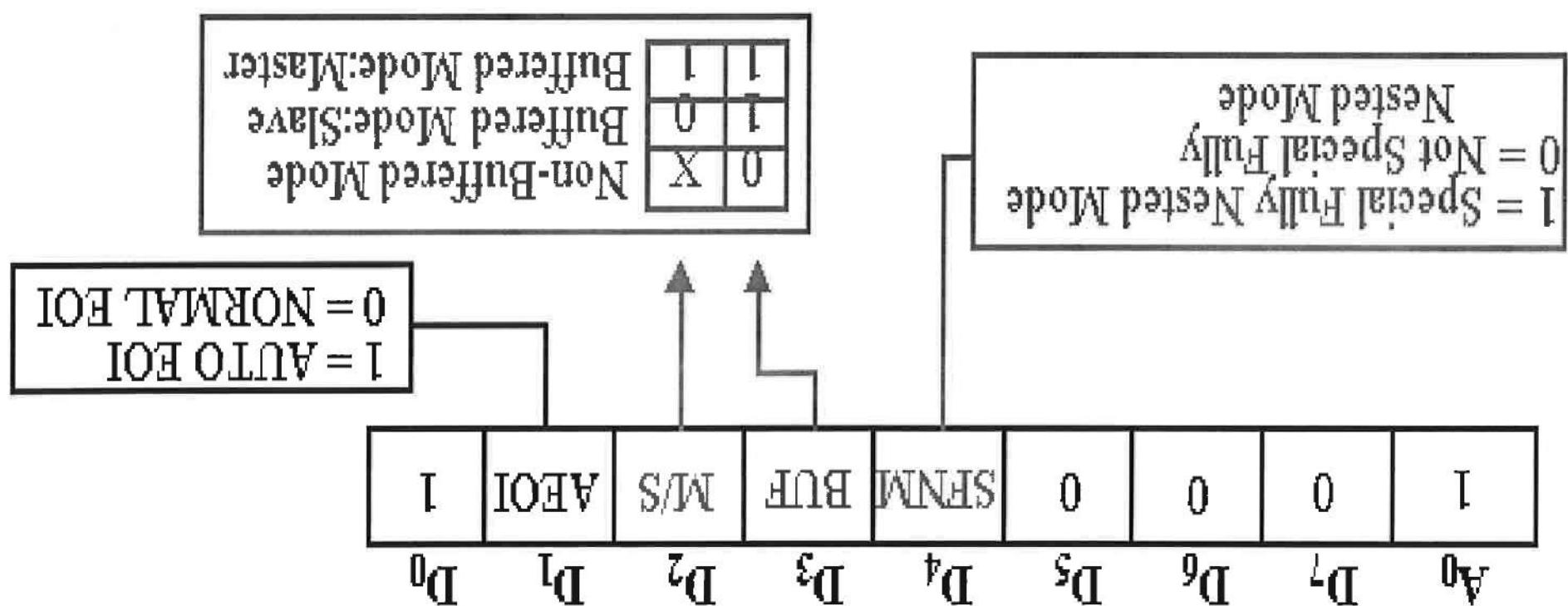
ICW2:

## ICW3:

- ❖ Suppose we have two slaves connected to a master using IR0 and IR1. The master is programmed with an ICW3 of 03H; one slave is programmed with an ICW3 of 01H and the other with an ICW3 of 02H.
- ❖ If we place a 04H in ICW3, connection, in both master and slave, we place a 04H in ICW3.
- ❖ For example, if we connected a slave to IR2, then to program ICW3 for this connection, this ICW indicates where the slave is connected to the master.
- ❖ Is used only when ICW1 indicates that the system is operated in cascade mode.



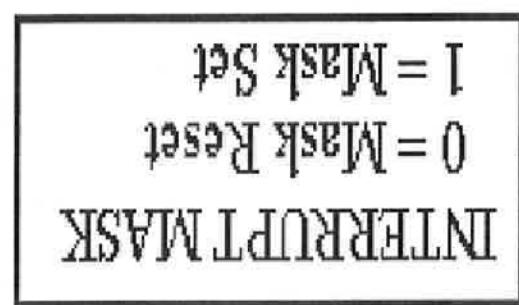
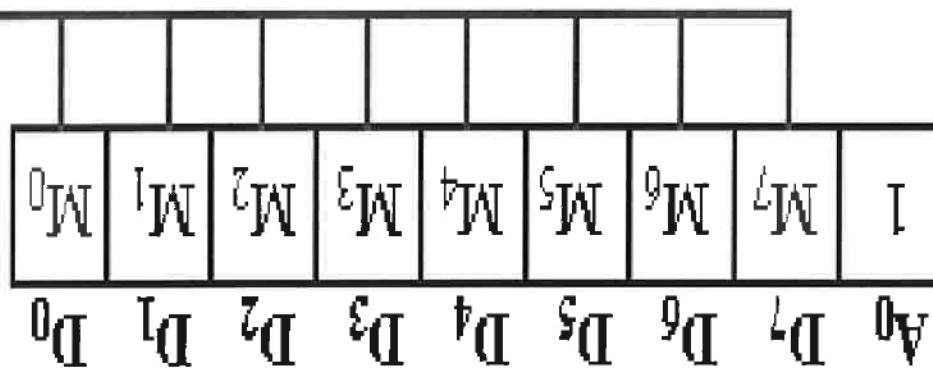
- ❖ Is programmed for use with the 8088/8086. This ICW
- ❖ is not programmed in a system that functions with the 8085 microprocessors.
- ❖ The rightmost bit must be logic 1 to select operation with the 8086 microprocessor, and the remaining bits are programmed as follows:



ICW4:

# Operation Command Words

OCW1:

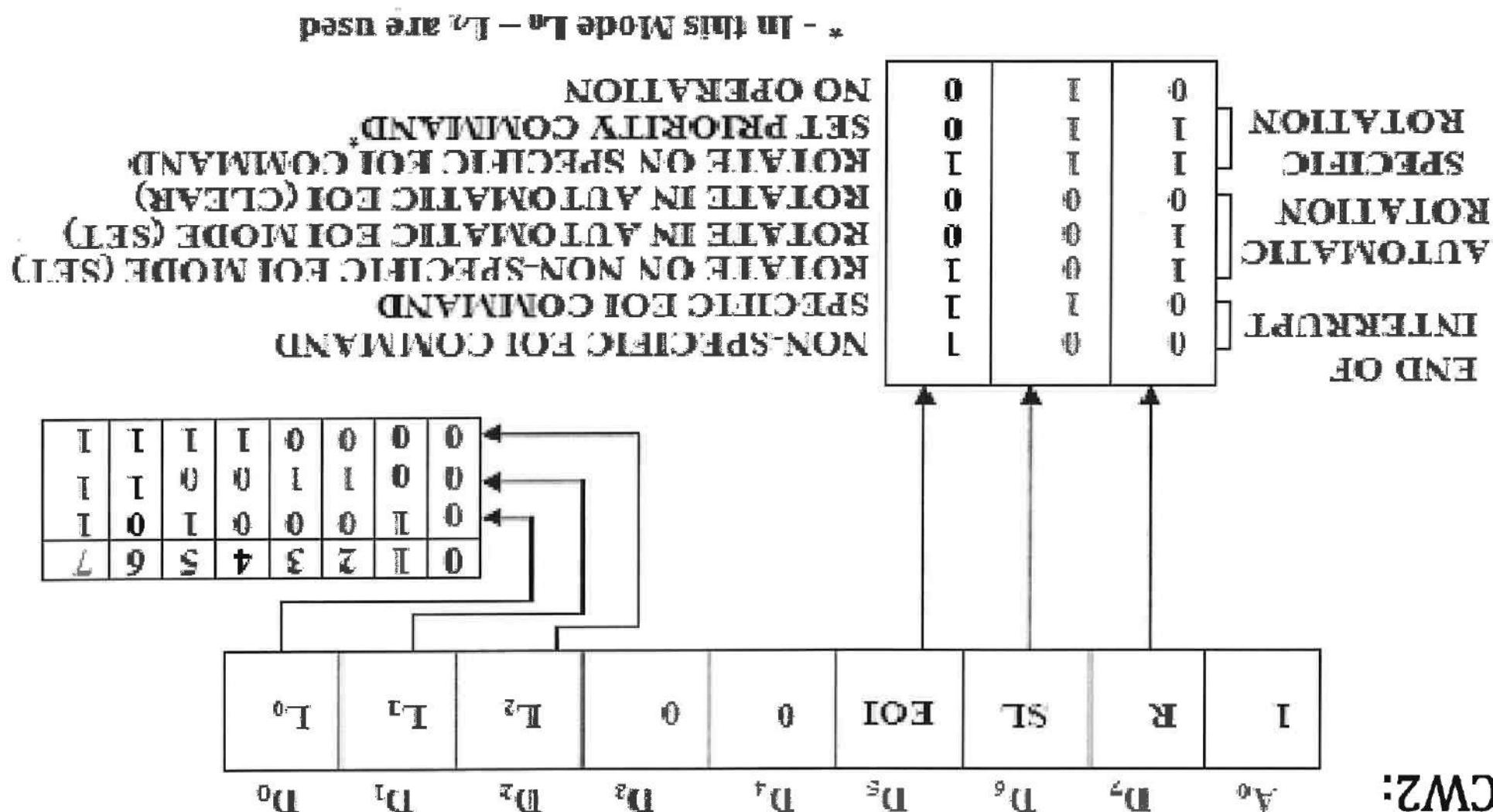


first initialized, OCW1 must be programmed after programming

- ❖ Because the state of the mask bits is known when the 8259A is interrupt input. The mask register is read when OCW1 is read.
- ❖ When a mask bit is set, it will turn off (mask) the corresponding interrupt input.
- ❖ Is used to set and read the interrupt mask register.

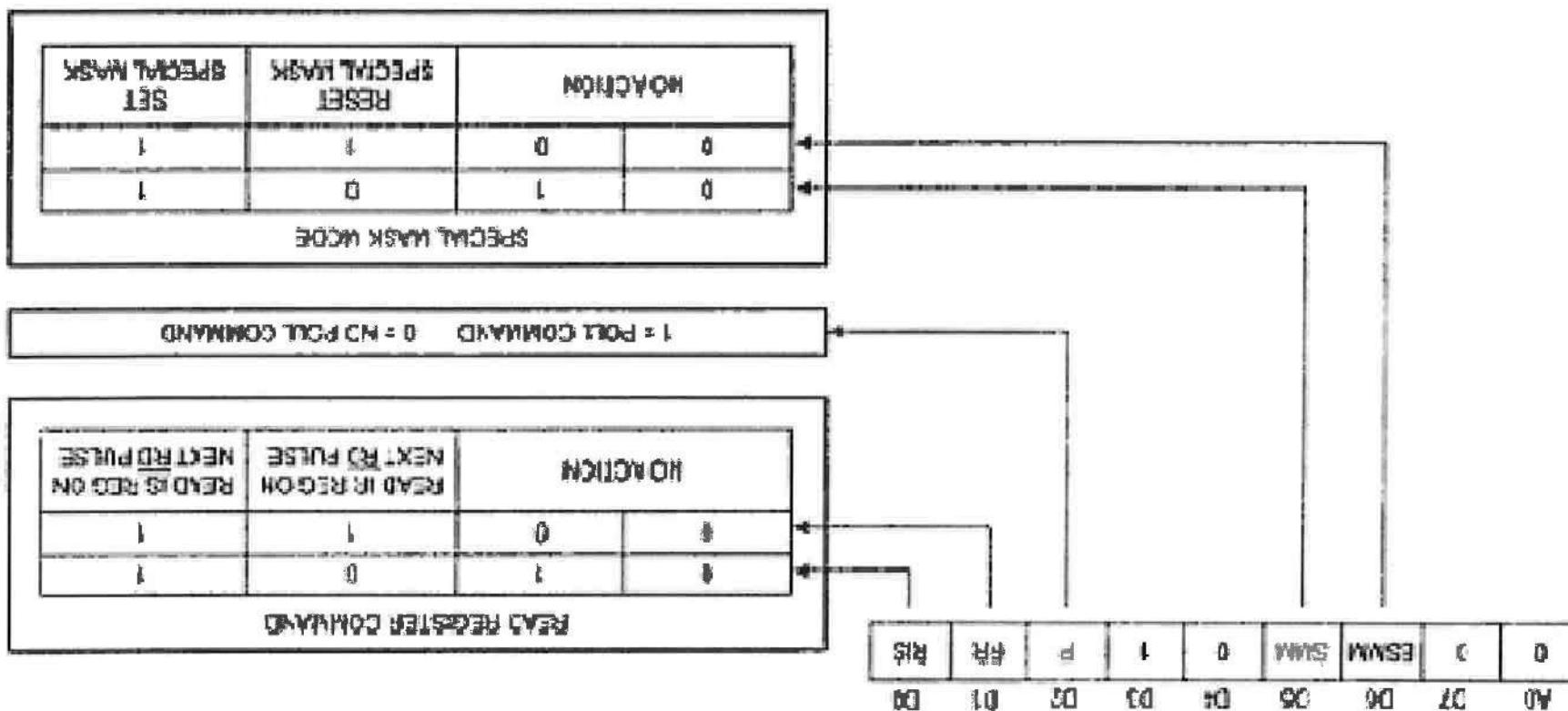
the ICW upon initialization.

- ❖ Is programmed only when the AEOI mod is not selected for the 8259A.
  - ❖ In this case, this OCW selects how the 8259A responds to an interrupt.
  - ❖ The modes are listed as follows in next slide:



to determine whether the rightmost three bits contain valid information.

- ▷ The leftmost bit indicates whether there is an interrupt, and must be checked poll word indicate the active interrupt request with the highest priority.
- ▷ next read operation would read the poll word. The rightmost three bits of the next read operation would be set and then output to the 8259A. The poll command.
- ▷ If polling is selected, the P-bit must be set and then output to the 8259A. The
- ▷ Selects the register to be read, the operation of the special mask register, and the poll command.



OCW3: