

# 8237DMA CONTROLLER

Important

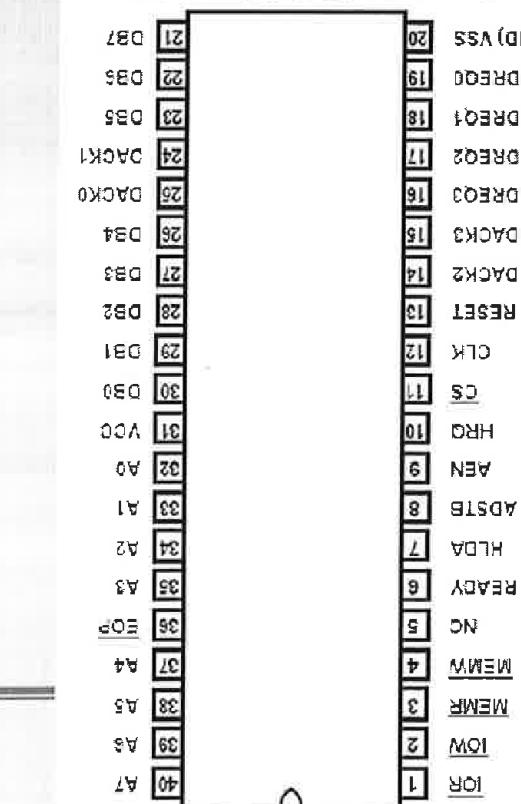
## Introduction:

- Direct Memory Access (DMA) is a method of allowing data to be moved from one location to another in a computer without intervention from the central processor (CPU). It is also a fast way of transferring data within (and sometimes between) computer.
- The DMA I/O technique provides direct access to the memory while the microprocessor is temporarily disabled.
- The DMA controller temporarily borrows the address bus, data bus and control bus from the microprocessor and transfers the data directly from the external devices to a series of memory locations (and vice versa).

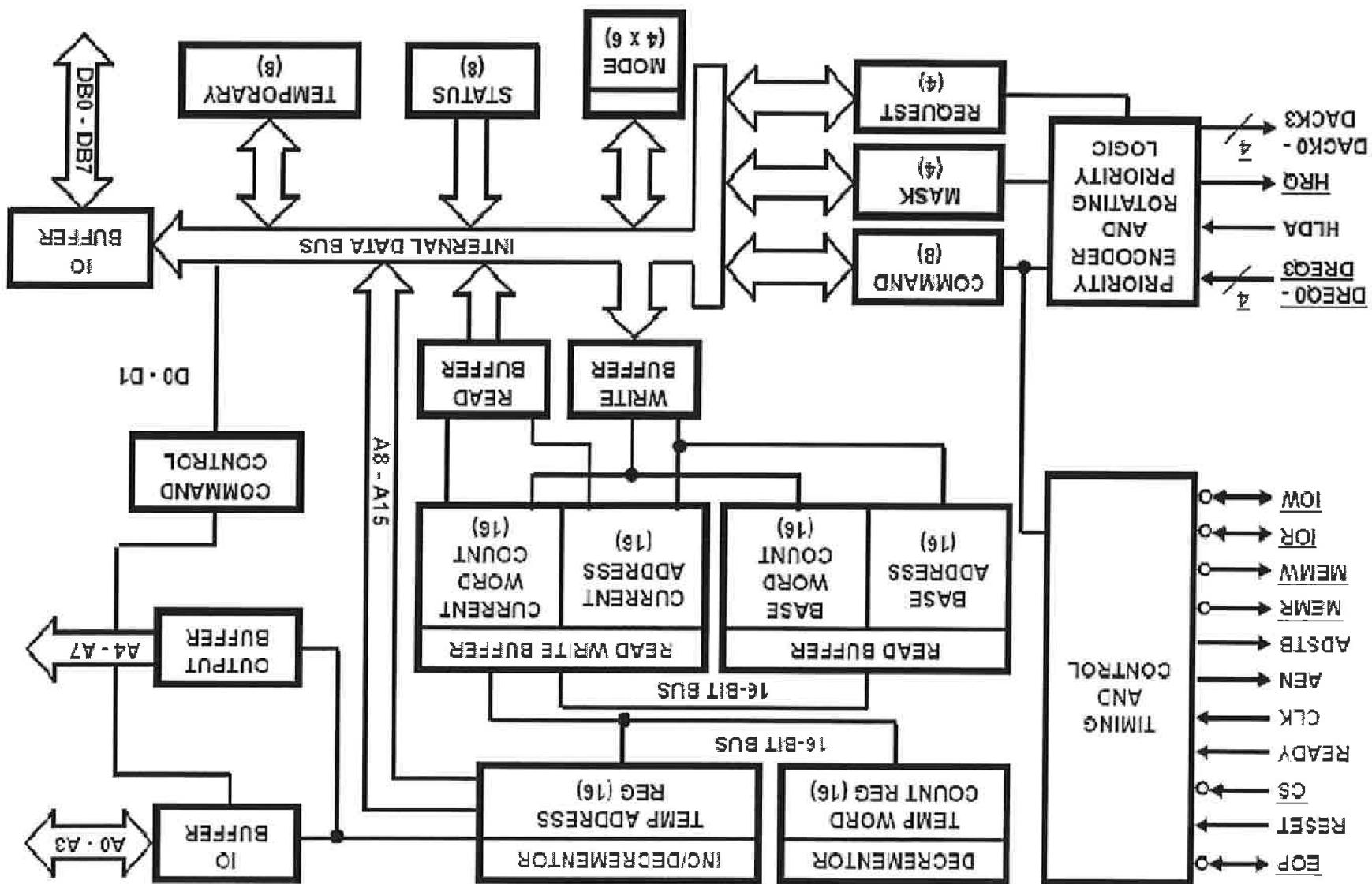
## The 8237 DMA controller

- Supplies memory and I/O with control signals and addresses during DMA transfer
  - 0: DRAM refresh
  - 1: Free
  - 2: Floppy disk controller
  - 3: Free
- 4-channels (expandable)
- 1.6MB/sec transfer rate
- 64 KByte section of memory address capability with single programming
- “Fly-by” controller (data does not pass through the DMA-only memory to I/O)
- Initialization involves writing into each channel:
  - i) The address of the first byte of the block of data that must be transferred (called the base address).
  - ii) The number of bytes to be transferred (called the word count).

# 8237 pins



- CLK: System clock
- CS: Chip select (decoder output)
- READY: 0 for inserting wait states
- HLDA: Signals that the chip has relinquished buses
- DREQ3 - DREQ0: DMA request input for each channel
- DB7-DB0: Data bus pins
- IOR: Bidirectional pin used during programming
- IOW: Bidirectional pin used during programming
- EO<sub>P</sub>: End of process is a bidirectional signal used as input to terminate a DMA process or as output to signal the end of the DMA transfer
- A<sub>3</sub>-A<sub>0</sub>: Address pins for selecting internal registers
- A<sub>7</sub>-A<sub>4</sub>: Outputs that provide part of the DMA transfer address
- HREQ: DMA request output
- DACK3-DACK0: DMA acknowledge for each channel.
- AEN: Address enable signal
- ADSTB: Address strobe
- MEMR: Memory read output used in DMA read cycle
- MEMW: Memory write output used in DMA write cycle



8237 block diagram

# Block Diagram Description

- It contains Five main Blocks.
  - 1. Data bus buffer
  - 2. Read/Control logic
  - 3. Control logic block
  - 4. Priority resolver
  - 5. DMA channels.

## DATA BUS BUFFER:

- It contain tri-state, 8 bit bi-directional buffer.
- Slave mode , it transfer data between microprocessor and internal data bus.
- Master mode , the outputs A8-A15 bits of memory address on data lines
- (Unidirectional).

## READ/CONTROL LOGIC:

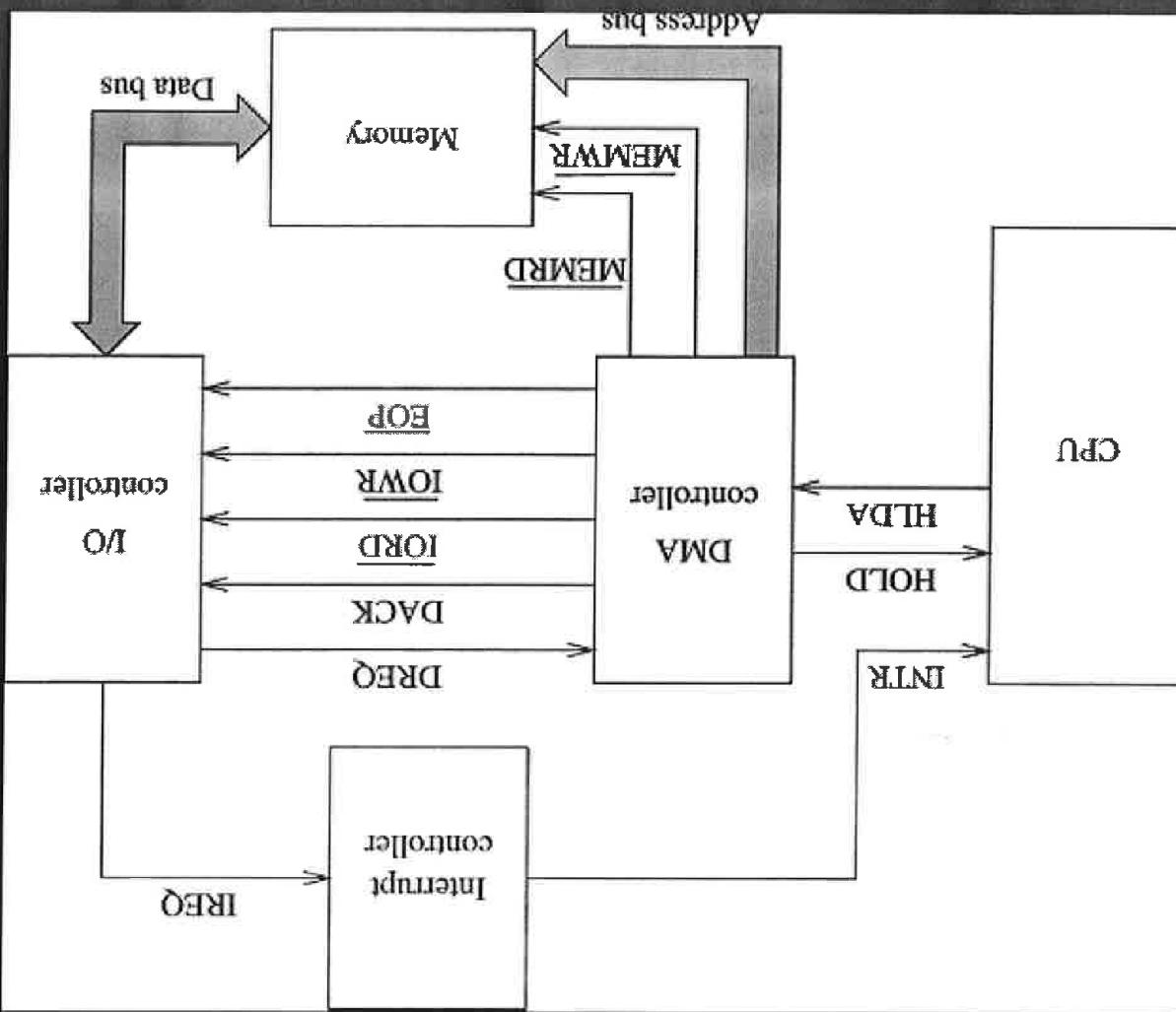
- It control all internal Read/Write operation.
- Slave mode , it accepts address bits and control signal from microprocessor.
- Master mode , it generate address bits and control signal.

## Control logic block

- It contains ,  
1. Control logic  
2. Mode set register and  
3. Status Register.

## CONTROL LOGIC:

- Master mode ,It control the sequence of DMA operation during all DMA cycles.
- It generates address and control signals.
- It increments 16 bit address and decrement 14 bit counter registers.
- It activate a HRC signal on DMA channel Request.
- Slave ,mode it is disabled.



## DMA controller details

Programmig and  
Applications Case  
Studies

- 1.Traffic Light control
- 2.LED display
- 3.LCD display
- 4.Keyboard display interface
- 5.Alarm Controller

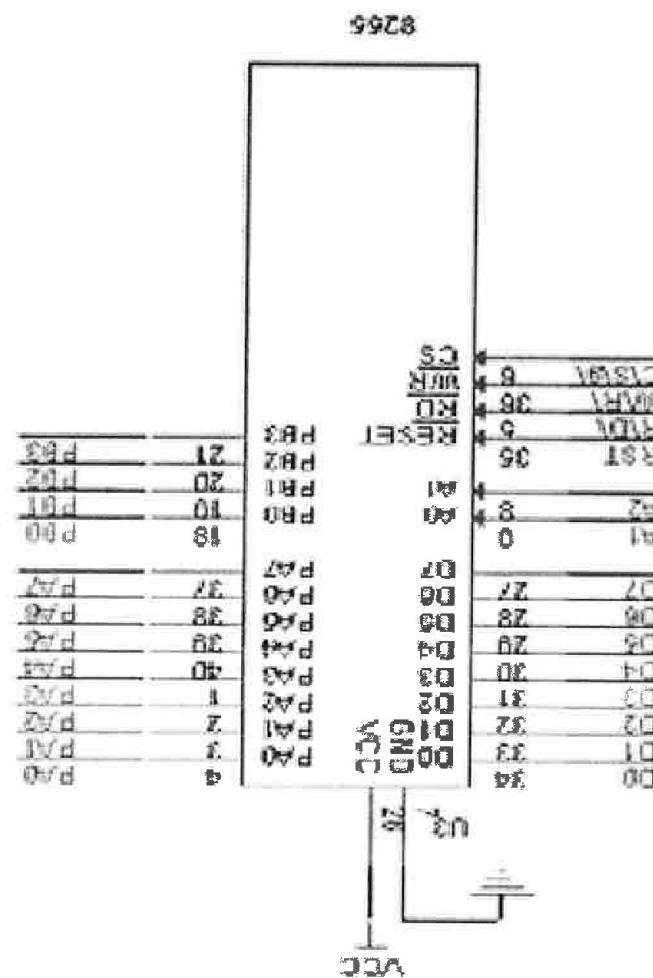
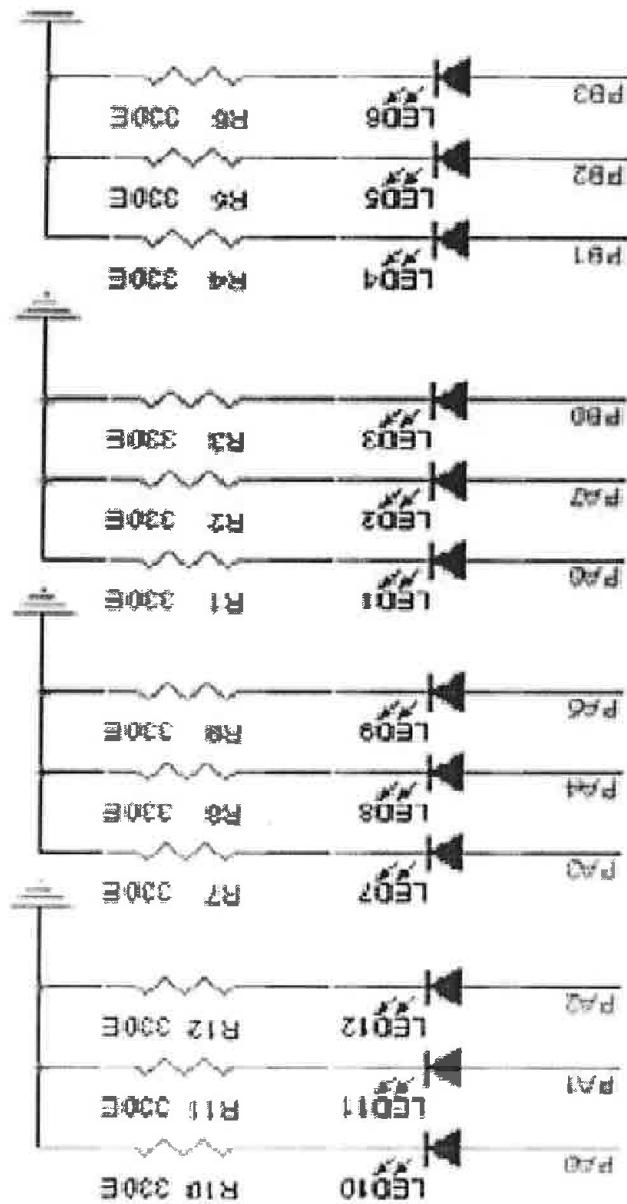
# CONTROL LEGHT L. TRAFFIC

Lumportum

- Traffic lights, which may also be known as stoplights, traffic lamps, traffic signals, signal lights, robots or semaphore, are signaling devices positioned at road intersections, pedestrian crossings and other locations to control competing flows of traffic.
- INTERFACING TRAFFIC LIGHT WITH 8086

The Traffic light controller section consists of 12 Nos. point Led's arranged by 4 Lanes in Traffic light interface card. Each Lane has Go(Green), Listen(Yellow) and Stop(Red) LED is being placed.

MODULES	8086 LINES	LAN Direction	SOUTH	EAST	NORTH	WEST	PWR
GO	PA.0	PA.1	LISTEN	PA.2	STOP	PA.3	PB.0
GO	PA.1	PA.4	LISTEN	PA.5	STOP	PA.6	PB.1
GO	PA.3	PA.4	LISTEN	PA.5	STOP	PA.6	PB.2
GO	PA.6	PA.7	LISTEN	PA.7	STOP	PB.3	PB.3
LISTEN	PA.0	PA.0	LISTEN	PA.0	STOP	PB.16	No Connection
LISTEN	PA.1	PA.1	LISTEN	PA.1	STOP	17,189	Supply from
microcontroller	PA.2	PA.2	LISTEN	PA.2	STOP	18,20	



CIRCUIT DIAGRAM TO INTERFACE TRAFFIC LIGHT WITH 8086

# 8086 ALP:

1100: START: MOV BX, 1200H  
MOV CX, 0008H  
MOV AL,[BX]  
MOV DX, CONTROL PORT  
OUT DX, AL  
INC BX  
MOV AL,[BX]  
MOV DX, CONTROL PORT  
OUT DX, AL  
INC BX  
NEXT:  
MOV AL,[BX]  
MOV DX, PORT A  
INC BX  
CALL DELAY  
LOOP NEXT  
JMP START  
PUSH CX  
MOV CX, 0005H  
MOV DX, OFFEEH  
DEC DX  
JNZ LOOP2  
LOOP REPEAT  
POP CX  
RET

REPEAT:  
DELAY:  
LOOP2:  
REPEAT:

## Lookup Table

- 1200 80H
- 1201 21H,09H,10H,00H (SOUTH WAY)
- 1205 0CH,09H,80H,00H (EAST WAY)
- 1209 64H,08H,00H,04H (NORTH WAY)
- 120D 24H,03H,02H,00H (WEST WAY)
- 1211 END

## 2. LED DISPLAY

**L**ight Emitting Diodes (LED) is the most commonly used components, usually for displaying pins digital states.

Typical uses of LEDs include alarm devices, timers and

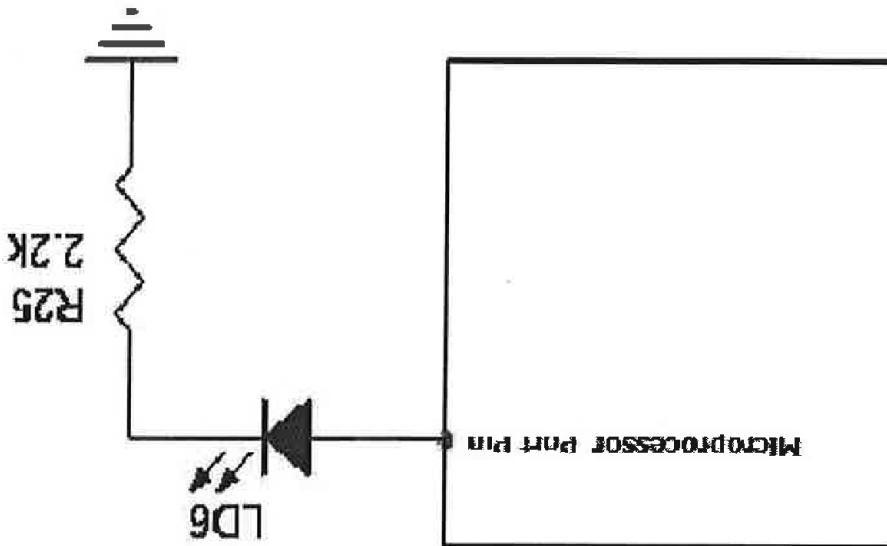
confirmation of user input such as a mouse click or keystroke.

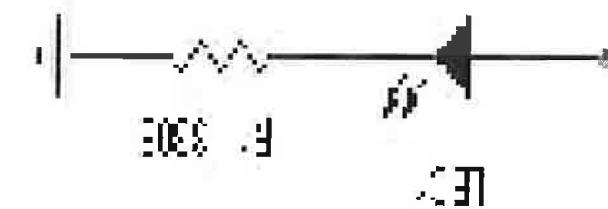
## INTERFACING LED

Anode is connected through a resistor to GND & the

Cathode is connected to the **Microprocessor pin**. So when the Port Pin is HIGH the LED is OFF & when the Port Pin is LOW

the LED is turned ON.





WAKE FA HIGH - LED ON  
WAKE FA LOW - LED OFF

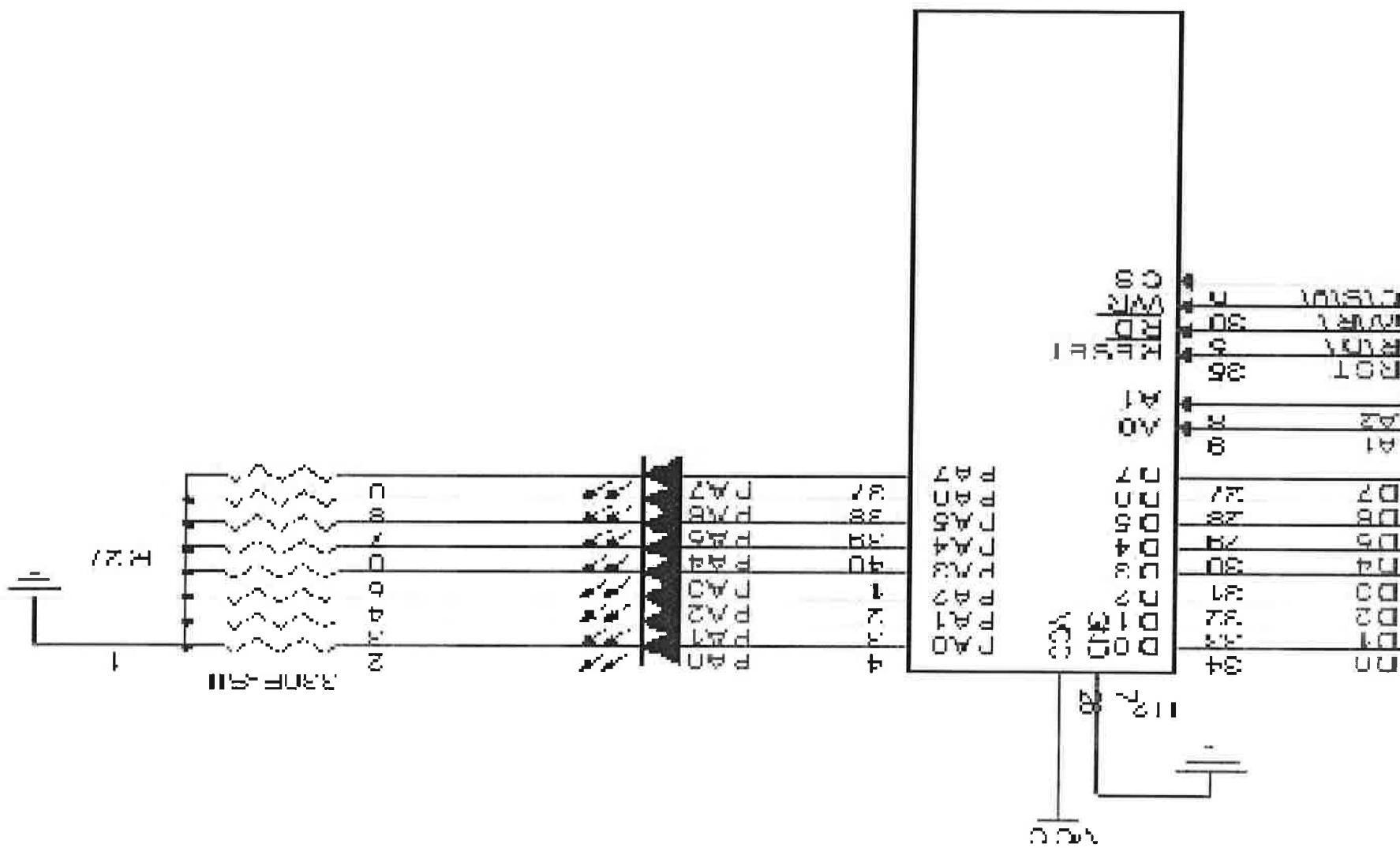
P01 LEDs      P255 LEDs      LED Selection

DIGITAL	OUTPUTS
P01	L01 PA.0
P02	L02 PA.1
P03	L03 PA.2
P04	L04 PA.3
P05	L05 PA.4
P06	L06 PA.5
P07	L07 PA.6
P08	L08 PA.7

## PIN ASSIGNMENT WITH 8086

472

8255



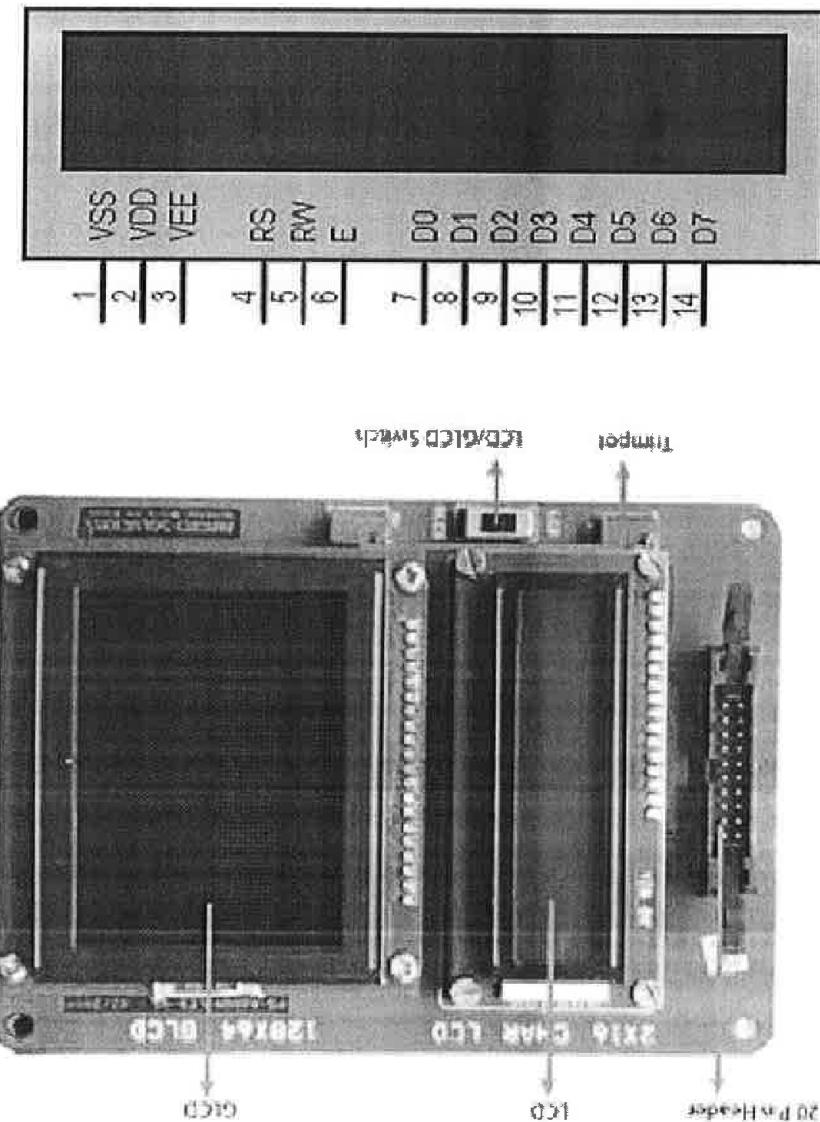
# INTERFACE LED WITH 8255

```
1100: START: MOV AL, 80
        MOV DX, FF36
        OUT DX, AL
        BEGIN: MOV AL, 00
        MOV DX, FF30
        OUT DX, AL
        CALL DELAY
        MOV AL, FE
        OUT DX, AL
        CALL DELAY
        JMP BEGIN
        OUT DX, AL
        CALL DELAY
        MOV CX, FFFF
        PO: DEC CX
        JNE PO
        RET
```

## 8086 ALP LED interface

### 3. LCD DISPLAY

COMMAND TO LCD INSTRUCTION REGISTER	CODE(HEX)
Clear display SCREET	0x01
Return home	0x02
Decrement cursor, shift cursor to left	0x04
Increment cursor, shift cursor to right	0x06
Shift display right	0x05
Shift display left	0x07
Display off, cursor off	0x0C
Display off, cursor on	0x0A
Display off, cursor on	0x0B
Display on, cursor off	0x0E
Display on, cursor off	0x0F
Display on, cursor on	0x0D
Display on, cursor on	0x0E
Display on, cursor on	0x0F
Display or, cursor blinking	0x0B
Display or, cursor blinking	0x0C
Display or, cursor blinking	0x0D
Display or, cursor blinking	0x0E
Display or, cursor blinking	0x0F
Display or, cursor blinking	0x0G
Shift cursor position to left	0x10
Shift cursor position to right	0x14
Shift the entire display to the left	0x18
Shift the entire display to the right	0x1C
Force cursor to beginning to 1st line	0x80
2 lines and 5x7 matrix	0x38



LCD   128x64 GLCD Selection		LCD   128x64 GLCD Selection		LCD - DATA LINES		CONTROL LINES	
20 PIN Conn	GLCD	PA.0	RS	PA.0	RS	PA.1	R/W
	GLCD	PA.0	RS	PA.4	C.S2	PA.5	RST
		PA.1	R/W	PA.3	C.S1	PA.0	DB0
		PA.2	E	PA.2	DB1	PA.1	DB2
		PA.3		PA.3	DB3	PA.4	DB4
		PA.4		PA.5	DB5	PA.5	DB6
		PA.5		PA.6	DB7	PA.7	DR7
		PA.6		PA.7	VCC	PA.7	VCC
		PA.7		PA.8	GND	PA.8	GND

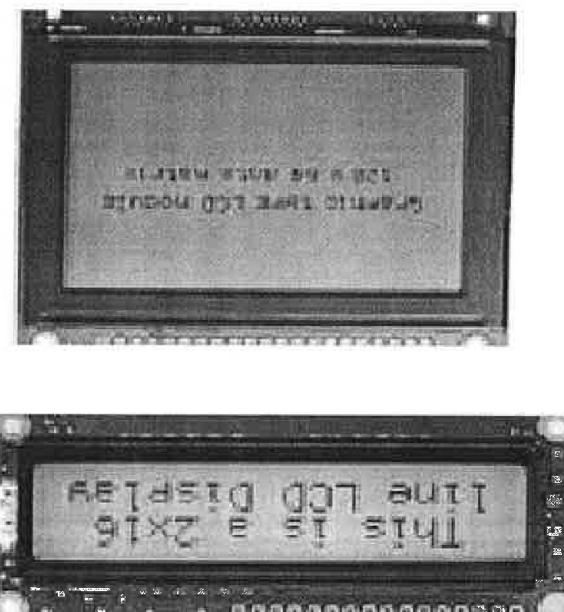
Supply drawn from MCU/MPU/FPGA

LCD

SW1

LCD

GLCD



HARDWARE CONFIGURATION OF LCD  
WITH 8051/8086/8085

# LCD INTERFACING WITH 8086

## TRAINER KIT

- **GPIO-1 (8255) J1 Connector**
  - PORTS                    ADDRESS : FF26
  - PORTA                    DATA : FF20
  - PORTB                    DATA : FF22
  - PORTC                    DATA : FF24
  - Control port            LOOK UP TABLE:
- **GPIO-1 (8255) J4 Connector**
  - PORTS                    ADDRESS : 1204
  - PORTA                    ADDRESS : 1206
  - PORTB                    ADDRESS : 1208
  - PORTC                    ADDRESS : 120C
  - Control port            (”PANTECH”)

478

CALL INT

INT RET

DEC CL

INC SI

CALL DEFLAY

CALL DATWT

REPFET: MOV AL,[SI]

MOV SI,1200

START: MOV CL,0B

CALL DELAY

CALL CMDWT

MOV AT,01

CALL DELAY

CALL CMDWT

MOV AL,06

CALL DELAY

CALL CMDWT

MOV AL,0E

CALL DELAY

CALL CMDWT

MOV AI,38

OUT DX,AL

MOV DX,BF26

MOV AL,00

MNEMONICS

IMP START

HII

CMDWT: MOV DX,BF26

OUT DX,AL

MOV AL,04

MOV DX,BF20

OUT DX,AL

MOV AL,00

MOV DX,BF20

OUT DX,AL

RET

DATWT: MOV DX,BF26

CHTDX,AL

MOV AI,05

MOV DX,BF20

OUT DX,AL

MOV AL,01

MOV DX,BF20

OUT DX,AL

RET

DEFLAY: MOV DX,BFEE

JNZ JUMP

JZ: DEC DX

RET

# LCD INTERFACING WITH 8051 TRAINER KIT

Used in UNIT 5 also

- **GPIO- I (8255) J1 Connector**

PORTS            ADDRESS

Control port     4003

PORT A            4000

PORT B            4001

PORT C            4002

## LOOK UP TABLE:

### DATA

= PORTD

= PORTA

( "PANTECH" )

00H, 01H, 02H, 03H

45H, 46H, 47H, 52H

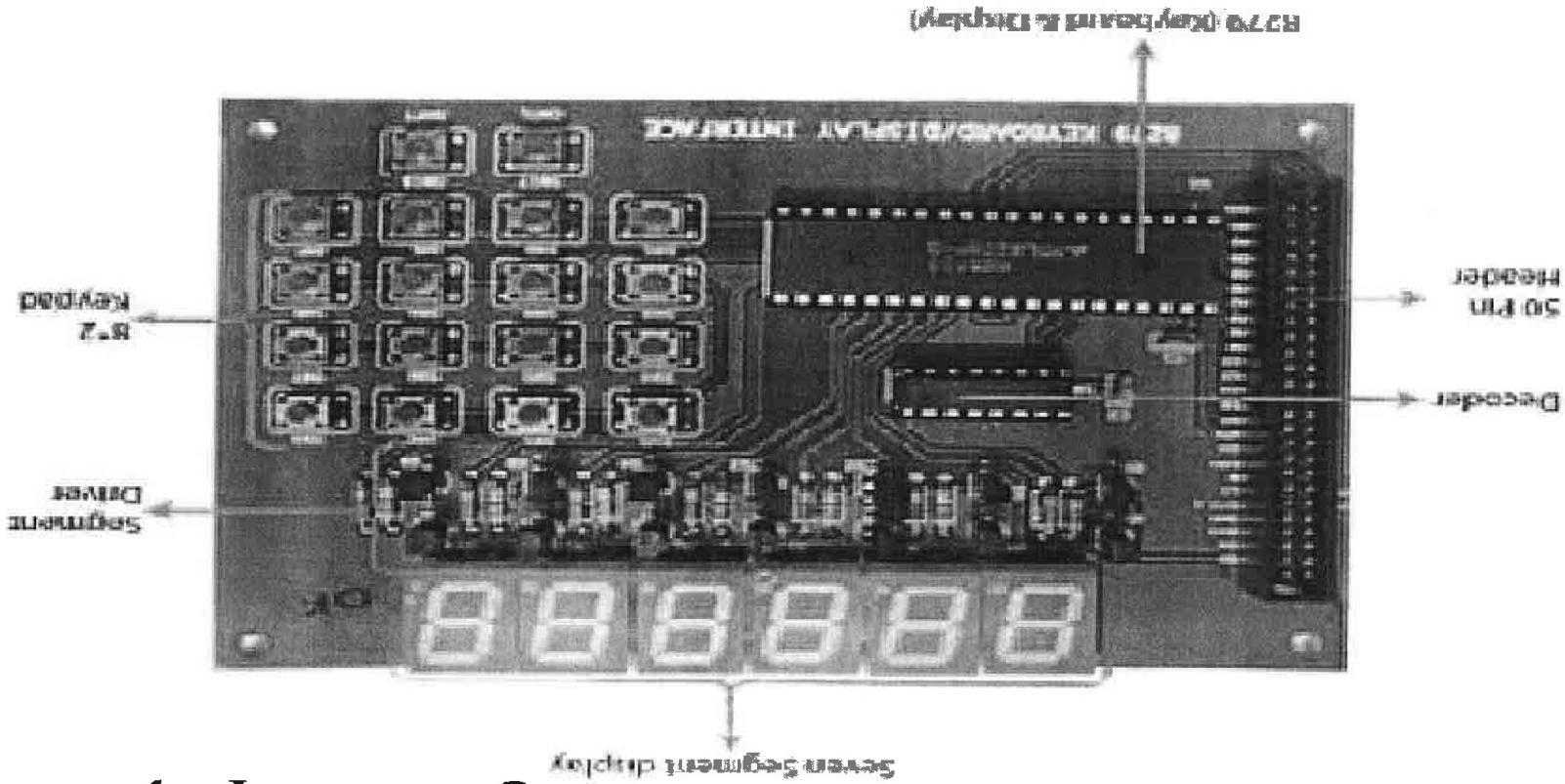
50H, 51H, 52H, 54H

55H, 56H, 57H, 59H

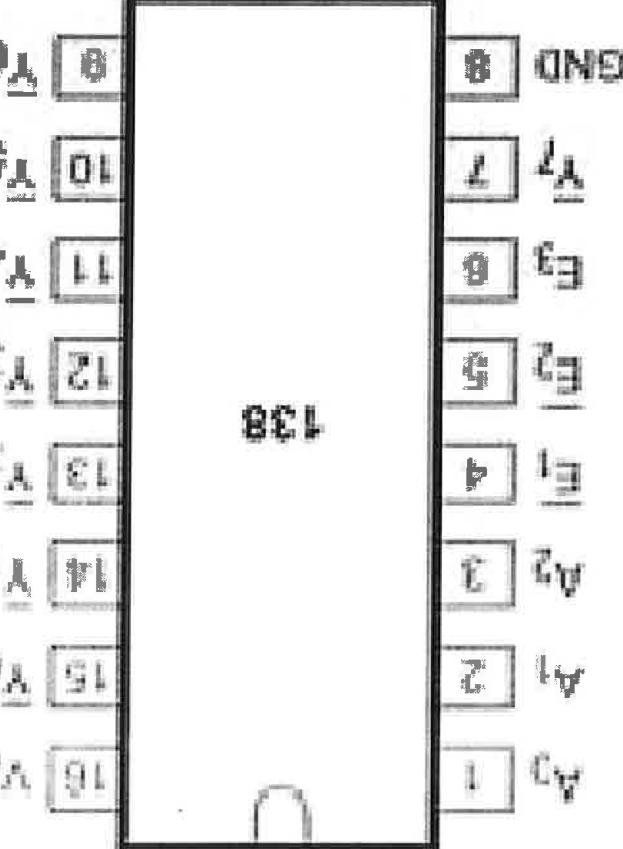
479

MOV A.#00	LCALL DELAY
MOV DPTR,A	MOV DPTR,#4000
MOV A.#04	LCALL CMDWT
MOV DPTR,A	MOV A,#00
MOV A.#00	LCALL DELAY
MOV A.#00	MV A,A#00
MOV DPTR,A	LCALL CMDWT
MOV A.#04	MV A,A#00
MOV DPTR,A	LCALL DELAY
MOV A.#00	MV A,A#00
MOV DPTR,A	LCALL CMDWT
MOV A.#04	MV A,A#00
MOV DPTR,A	LCALL DELAY
MOV A.#00	MV A,A#00
MOV DPTR,A	LCALL CMDWT
MOV A.#04	MV A,A#00
MOV DPTR,A	LCALL DELAY
MOV A.#00	MV A,A#00
MOV DPTR,A	LCALL CMDWT
MOV A.#00	MV A,A#00
MOV DPTR,A	LCALL DELAY
MOV A.#00	MV A,A#00
MOV DPTR,A	LCALL CMDWT
MOV A.#04	MV A,A#00
MOV DPTR,A	LCALL DELAY
MOV A.#00	MV A,A#00
MOV DPTR,A	LCALL CMDWT
MOV A.#04	MV A,A#00
MOV DPTR,A	LCALL DELAY
MOV A.#00	MV A,A#00
RET	
CMDWTR: MOV DPTR,#4001	MV A,A#33
MOV A.#00	LCALL CMDWT
MOV DPTR,A	MV A,A#00
MOV DPTR,A	LCALL DELAY
MOV A.#00	MV A,A#00
MOV DPTR,A	LCALL CMDWT
MOV A.#00	MV A,A#00
MOV DPTR,A	LCALL DELAY
MOV A.#00	MV A,A#00
MOV DPTR,A	LCALL CMDWT
MOV A.#00	MV A,A#00
MOV DPTR,A	LCALL DELAY
MOV A.#00	MV A,A#00
MOV DPTR,A	LCALL CMDWT
MOV A.#00	MV A,A#00
MOV DPTR,A	LCALL DELAY
MOV A.#00	MV A,A#00
RET	
CMDWTR: MOV DPTR,#4002	MV A,A#33
MOV A.#00	LCALL CMDWT
MOV DPTR,A	MV A,A#00
MOV DPTR,A	LCALL DELAY
MOV A.#00	MV A,A#00
MOV DPTR,A	LCALL CMDWT
MOV A.#00	MV A,A#00
MOV DPTR,A	LCALL DELAY
MOV A.#00	MV A,A#00
RET	
DINZ R11,LOOF	MV A,DINZ
LCALL DELAY	MV A,A#00

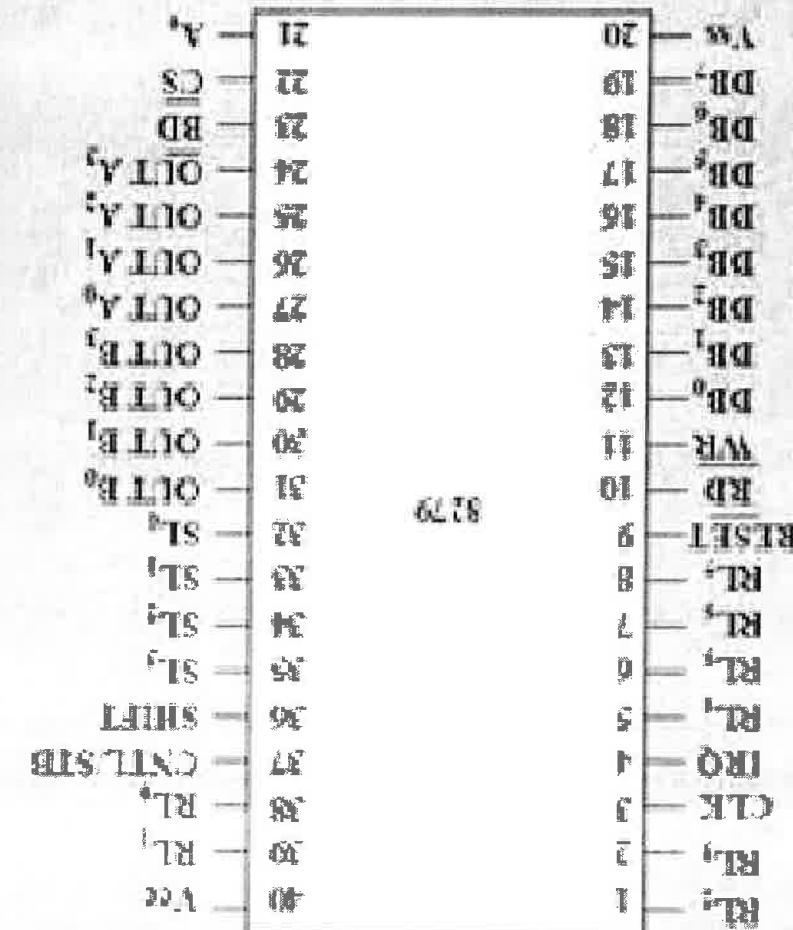
## 4. Keyboard display interface



Keyboard and display is configured in the encoded mode. In the encoded mode, a binary count sequence is put on the scan lines S<sub>LO</sub>-S<sub>L3</sub>. These lines must be externally decoded to provide the scan lines for keyboard and display. A 3 to 8 decoder 74LS138 is provided for this purpose. The S<sub>0</sub>-S<sub>1</sub> output lines of this decoder are connected to the two rows of the keyboard. And Q<sub>0</sub> to Q<sub>7</sub> is connected to 7 Segment Display.

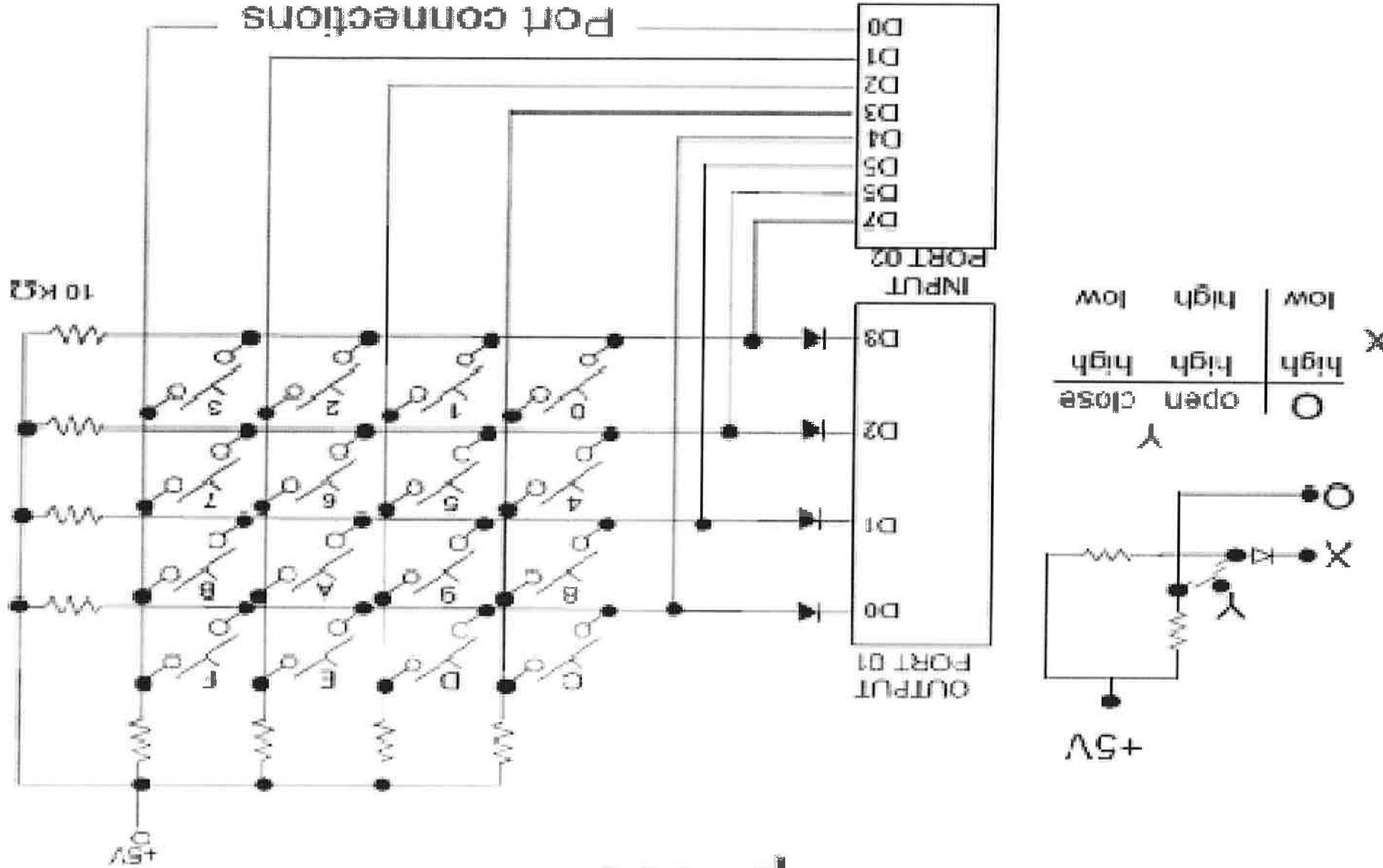


PIN DIAGRAM OF 74LS138



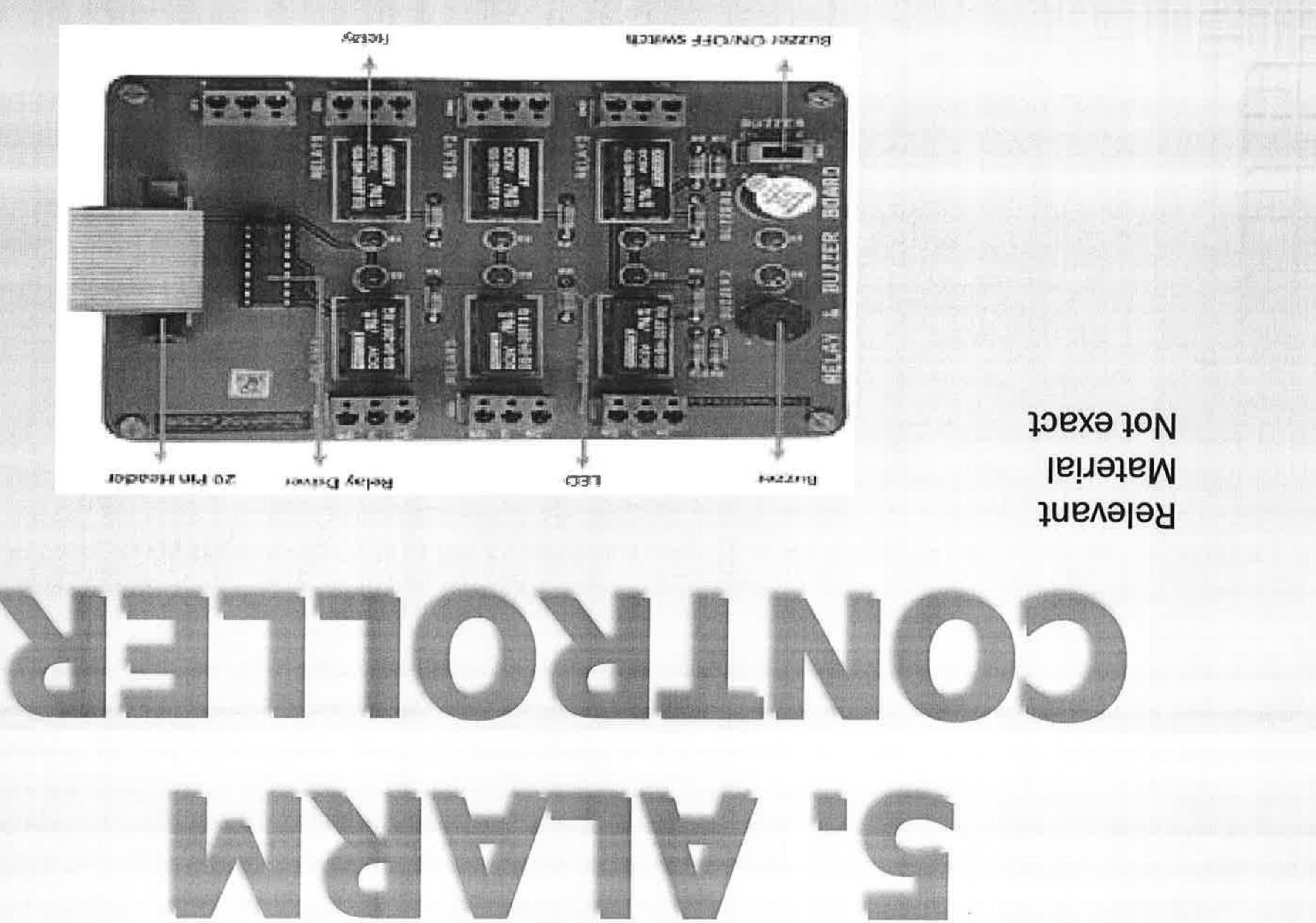
PIN DIAGRAM OF 8279

# detecting a Matrix Keyboard key press



OUTPUT	CONNECTIONS	8279	HEADER	50 PIN
				DATA LINES
			D0	RSI
			D1	RST
			D2	CS
			D3	WR
			D4	RD
			D5	From Decoder
			D6	WR
			D7	Interlace card and cable to PS - 8279
			D8	Segment or Memory
			D9	displayed on Seven
			D10	Segments
			D11	Interlace card and
			D12	trainee kit
			D13	addresses specified in the
			D14	Program(D0 to D7)
			D15	
			D16	
			D17	
			VCC	
			GND	
				Supply draw from MCU/MPU
				Pin number 24 to 31 is connected to 7 segments,
				SL0 SL2 is connected to decoder and SL3 is no
				connect RLO RLO is connected to keypad

Initiate keyboard/display in encoded scan keyboard 2 key lockout mode	MVI A, 00h	OUT 81H	MVI A, 34H	OUT 81H	MVI A, 0BH	OUT 81H	MVI A, 40h	OUT 81H	MVI H, 62H	MOV L, A	OUT 81H	MVI A, 80h	INITIALIZE 8279 IN WRITE FIFO RAM MODE
Initiate prescaler count	MVI A, 0BH	OUT 81H	MVI A, 0BH	OUT 81H	MVI A, 40h	OUT 81H	MVI A, 62H	MOV L, A	INITIALIZE MEMORY POINTER TO POINT	7-SEGMENT CODE	INITIALIZE 8279 IN WRITE DISPLAY RAM MODE	MVI A, 80h	INITIALIZE 8279 IN WRITE DISPLAY RAM MODE
Load mask pattern to enable RST 7.5	MVI A, 0BH	OUT 81H	MVI A, 34H	OUT 81H	MVI A, 0BH	OUT 81H	MVI A, 40h	OUT 81H	MVI H, 62H	MOV L, A	INITIALIZE MEMORY POINTER TO POINT	7-SEGMENT CODE	INITIALIZE 8279 IN WRITE DISPLAY RAM MODE
Mask other interrupts	SI M		EI										INTERRUPT SERVICE ROUTINE
Enable Interrupt			HERE: JMP HERE										INTERRUPT SERVICE ROUTINE
Wait for the interrupt													
Initialize 8279 in read FIFO RAM mode	IN 80h	OUT 81H	MVI A, 40h	OUT 81H	MVI H, 62H	MOV L, A	INITIALIZE 8279 IN WRITE DISPLAY RAM MODE	INITIALIZE 8279 IN WRITE DISPLAY RAM MODE	MVI A, 80h	MOV L, A	OUT 81H	MVI A, 80h	INITIALIZE 8279 IN WRITE DISPLAY RAM MODE
Get keycode													
Initialize memory pointer to point													
7-Segment code													
7-Segment code													
Initialize memory pointer to point													
INITIALIZE 8279 IN WRITE DISPLAY RAM MODE													
Get keycode													
INITIALIZE 8279 IN WRITE DISPLAY RAM MODE													
INITIALIZE 8279 IN WRITE DISPLAY RAM MODE													
INITIALIZE 8279 IN WRITE DISPLAY RAM MODE													
RET													
: Return to main program													



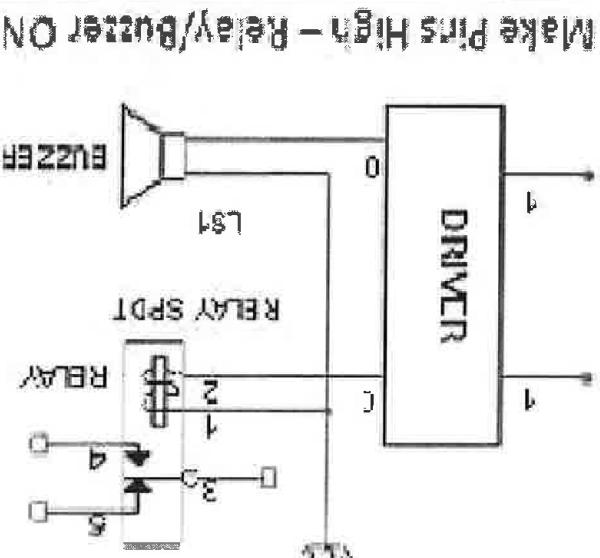
# COUNTERROLLER

## 5. ALARM

# HARDWARE DESCRIPTION OF RELAY & BUZZER INTERFACE

488

20PIN CONNECTOR	MODULES	RELAY & BUZZER CARD
	RELAY1	VCC
	RELAY2	4
	RELAY3	4
	RELAY4	4
	RELAYS	5
	RELAY6	6
	RELAY7	7
	BUZZER1	8
	BUZZER2	8
	NC	9-16
PWR	Vcc	17,19
	Gnd	18,20
	Supply from MCU/MPU/EFGA ICs	



\* **GPIO-1 J1 Connector**  
 ADDRESS PORTS  
 Control port FF26  
 PORT A FF20  
 PORT B FF22  
 PORT C FF24  
 ADDRESS PORTS  
 Control port FF26  
 PORT A FF30  
 PORT B FF32  
 PORT C FF34  
 FF36  
 ADDRESS PORTS  
 Control port FF36  
 PORT A FF30  
 PORT B FF32  
 PORT C FF34  
 FF36

**To Interface Relay and Buzzer with 8086 Timer Kit**  
 and To ON/OFF Relay and Buzzer card

# Microprocessor & Microcontroller Basics