TECHNOLOGICAL UNIVERSITY OF THE PHILIPPINES

ELECTRONICS ENGINEERING DEPARTMENT

ASSIGNMENT NO. 3

CPET11 – BET-CPET-3A / 7:00 AM – 10:00 AM W

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FIGURE 4 Given Requirements:

- Iomax ≈ 750 mA
- Vripple = 0.10Vp
- Maximum center-tap Vm = 12*2 = 24V
- Using LM317A voltage regulator

Parameters	**Computed**
Vm	24 V (Given)
Vmp	33.94 V
Vk1	0.7 V
Vk2	0.7 V
Vk3	0.7 V
Vk4	0.7 V
Vdc	20.70 V
Vripple	0.10 V (Given)
Vin (LM317)	3V-40V , so Vdc = 20.70V is check
RL (ideal)	27.6 Ω
RL (actual)	45.25 Ω
PD RL (ideal)	15.525 W
PD RL(actual)	25.455 w
VR1	1.25v
IR1	5.21 mA
VR2min	0.00 V
IR2min	0.00 A
VR2max	16.446 V

IR2max	5.21mA
C1	62,500 μF
C2	1 μF
Vomin (pureDC)	1.25 V
Vomax (pureDC)	17.70 V
Iomin (pureDC)	45.30 mA
Iomax (pureDC)	0.75 A or 750mA
FI	60 Hz
FO	120 Hz

Parameters	**Solutions and Justifications**
Vm	24 V **(Given)**
Vmp	$Vmp=Vm\sqrt{2}= 24\sqrt{2}=$**33.94 V**
Vk1	0.7 V (diode voltage drop) This value is dependent on the diode's material, typically 0.6-0.7V for silicon diodes
Vk2	0.7 V (diode voltage drop) This value is dependent on the diode's material, typically 0.6-0.7V for silicon diodes
Vk3	0.7 V (diode voltage drop) This value is dependent on the diode's material, typically 0.6-0.7V for silicon diodes

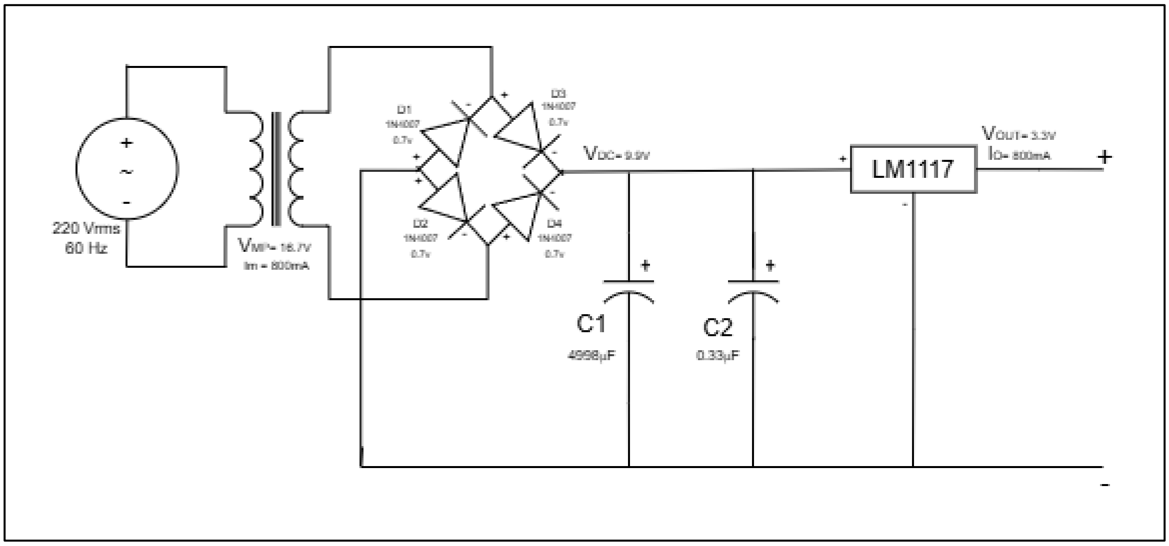
Vk4	0.7 V (diode voltage drop) This value is dependent on the diode's material, typically 0.6-0.7V for silicon diodes
Vdc	Vdc= 0.636(Vmp-2Vk)= 0.636 [33.94 - (2*0.7)]= **20.70 V**
Vripple	0.10 V **(Given)**
Vin (LM317)	According to datasheet: **3V-40V** , so **Vdc = 20.70V is check**
RL (ideal)	RL=Vdc /Io= 20.70 / 0 .750 = **27.6 Ω**
RL (actual)	RL=Vmp /Io= 33.94 / 0.750 = **45.25 Ω**
PD RL (ideal)	PD = IVdc = (0 .750 *20.70) = **15.525 W**
PD RL(actual)	PD = IVmp = (0 .750 *33.94) = **25.455 w**
VR1	LM317A has a built-in reference voltage (Vref) of about 1.25 V between its output pin and adjust pin.
IR1	Vref / R1 = 1.25v / 240 ohms = 0.0052083333 = **5.21 mA**
VR2min	Minimum LM317 output = Vref (≈1.25 V). If output set to Vref, across R2 there is 0 V so R2 current is 0 (ignoring Iadj).

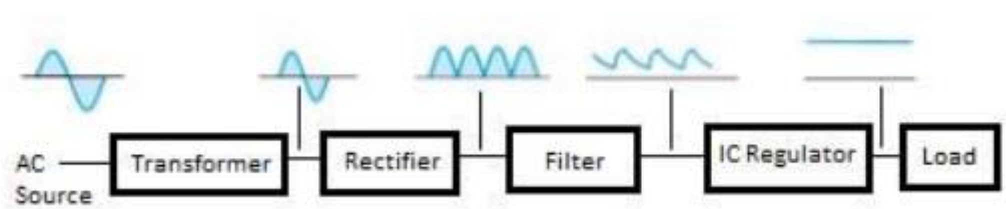
IR2min	Practically zero; tiny Iadj exists but negligible here
VR2max	VR2max= Vomax - Vref = 17.70−1.25= **16.45V**
IR2max	VR2max / R2 = 16.45V / 3157.66 ohms = 0.00520833 A = **5.21 mA**
C1	C1 = I * T / ΔV • Compute T = 1/120 = 0.008333333333 s • T = 1/120 = 0.008333333333 s • I * T = 0.750 A x 0.008333333333 s = 0.00625 • Divide by ΔV (0.10 V): C= 0.00625 ÷ 0.10 = 0.0625 F • Convert to µF: 0.0625 F = 62,500 µF • Result: C1 = **62,500 µF**
C2	LM317 datasheet and module recommend a small bypass on the adjust or output (typical values 1 µF for adjust bypass to improve ripple rejection). Also an input bypass ~0.1 µF near regulator recommended. • Result (practical): C2 = **1 µF** (adjust/output bypass) and 0.1–0.33 µF (input bypass) as per datasheet practice.
Vomin (pureDC)	LM317 minimum output is Vref (≈ 1.25 V) when R2 = 0.

Vomax (pureDC)	LM317 requires headroom; approximate Vomax ≈ Vdc − Vdropout. Using assumed dropout ≈ 3.0 V • Vdc = 20.70 V • Vomax=20.70V −3.0v =17.696 V • Rounded result: Vomax ≈ **17.70V**
Iomin (pureDC)	Vomin / RL (ideal) = 1.25v / 27.60 ohms = 0.045289 A = **45.30 mA**
Iomax (pureDC)	**0.750 A or 750mA** – given design or requirement
FI	**60 Hz** - standard frequency used (here in Philippines)
FO	2 × FI = **120 Hz**

2. In reference to your previous proposed IPO/block model in Modules 1 and 2, design the appropriate power supply system. Present the following requirements:

- Schematic circuit design
- Computational solution/s for each electronic component, including justification if necessary





A Direct Current (DC) voltage regulator takes in an analog voltage signal and converts it into a stable, regulated, DC voltage. This is achieved through various components: The transformer that steps down (or steps up depending on the engineer) a given Alternating Current (AC) voltage to a much lower voltage peak. The rectifier that converts the stepped down voltage into pulsating DC. A Filter which is usually in the form of a capacitor is then utilized to try and smoothen out the rectified DC signal. Lastly, an IC Regulator that would stabilize the filtered pulsating DC into a pure and stable DC ouptut. For this circuit, a step down transformer with a 12 V_{AC} secondary winding would be utilized. The transformer type to be used is a center—tapped, (6-0-6) transformer. The IC Regulator to be utilized is Texas Instruments' LM1117, 800mA that would output 3.3v. From the revised proposed IPO Model with respect to the tasks from Module 1 and 2, the load would be Espressif System's ESP32-WROOM-32UE.

3.3V Regulated DC Fixed Power Supply	
Step 1: Transformer -> Rectifier	
Transformer Peak Voltage	**Peak Voltage Formula:** $V_{MP} = Vm\sqrt{2}$ **Solution:** $V_{MP} = 12.0 \times 1.41421356$ $V_{MP=}$ 16.97V
Calculate V_{DC}	**V_{DC} Formula:** $V_{DC} = 0.636 \times (Vmp - 2Vk)$ **Solution:** $V_{DC} = 0.636 \times (16.97 - 1.4)$ $V_{DC} = 9.9V$ **Justification:** $V_{DC} = 9.9V$ gives enough headroom for the LM1117 to regulate voltage to 3.3v. According to the Texas Instrument LM1117, 800mA data sheet, the dropout voltage is 1.2v at $V_{TYPICAL}$ and 1.3v at V_{MAX}.
Transformer Current Rating	**Transformer Current** = 800mA

	Justification: According to the Espressif Systems ESP32-WROOM-32UE data sheet, the recommended current delivered by an external power supply to the ESP32 module is 500mA at minimum with the typical and maximum to be desired by the engineer. Since this is the case, an additional 300mA increase would be ample headroom in the case of sudden power draws. Furthermore, the IC to be utilized is rated at 800mA.
Step 2: Bridge Rectifier	
Bridge Rectifier Details	The Rectifier would host a bridge-type system composing of 4 silicon diodes with 0.7v of voltage drop each. The silicon diode model to be utilized is the 1N4007. **Justification:** The aforementioned diode model would be utlized since the diode can survive reverse voltage of up to 1000v.
Step 3: Filter Capacitor	
Calculate the Capacitor Value (Capacitance)	**Filter Capacitance Formula:** C= (IT)/V Where in: T= 8.33ms (Full Wave) V= 0.5V_{pp}

	Solution: C= (0.3 x 0.00833)/0.5 C= 0.004998F C= 4998 µF **Justification:** A 25V electrolytic capacitor for safety as the filter should be higher or equal to the $V_{DC.}$
Step 4: Input Decoupling After Filter Capacitor	
0.33µF Film/Ceramic Capacitor	**Justification:** This functions as a small high frequency component that by passes the ground to remove HF spikes that large electrolytics miss. The voltage rating for this capacitor is also equal to C3 which is 25V electrolytic.
Step 5: IC Voltage Regulator	
LM1117 Details$_o$	According to Texas Instruments' LM1117, 800mA Data Sheet, the LM1117 is a voltage regulator that steps down and regulates a pulsating DC voltage into a stable 3.3V. It's input voltage max is 20v and a dropout voltage of 1.2V at $V_{TYPICAL}$ and 1.3v at V_{MAX}. Furthermore, it is rated at 800mA.

	Justification: Since the load requires a voltage input of 3.3v and also has a current draw of 800mA, the LM1117 serves as the best voltage regulator component that fits the requirements needed to properly run the load.
Step 6: Load	
Espressif Systems ESP32-WROOM-32UE	From the revised proposed IPO Model with respect to the tasks from Module 1 and 2, the load would be Espressif System's ESP32-WROOM-32UE. This microcontroller would be utilized for the proposed Room-Level Fire Prediction System that would utilized various components for room fire prediction. According to the Espressif System's ESP32-WROOM-32UE Data Sheet, the recommended operating conditions of the microcontroller are the following: V_{MIN}= 3V $V_{TYPICAL}$= 3.3V V_{MAX}= 3.6V I_{MIN}= 500mA From these operating conditions alone, the following computations and components utilized for the 3.3v Regulated Power Supply are justified. With this, the 3.3V Regulated DC Fixed Power Supply has the following output. **V_o**= *3.3V*

	I_o= *800mA*

References:

- Espressif Systems. (2021). *ESP32-D0WD-V3 Datasheet*. ALLDATASHEET.COM. https://www.alldatasheet.com/datasheet-pdf/pdf/1242996/ESPRESSIF/ESP32-D0WD-V3.html
- Texas Instruments. (2023, January). TI.com. https://www.ti.com/lit/ds/symlink/lm1117.pdf?ts=1759082277413&ref_url=https%253A%252F%252Fwww.mouser.in%252F

3. Specify the percentage contribution of each group member (100% total). Each member should sign to confirm the breakdown of contribution.

Contributions of each group member:

ARENAS, JOSEPH 20%

ESTRADA, CYRUS 20%

GUTIERREZ, GEO KENTZER 20%

PACIS, LIAN GIL 20%

RECAÑA, JORDAN 20%

TOTAL 100%

Signature of each group member:

ARENAS, JOSEPH

ESTRADA, CYRUZ

GUTIERREZ, GEO KENTZER

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