TECHNOLOGICAL UNIVERSITY OF THE PHILIPPINES

Ayala Blvd. cor San Marcelino St. Ermita, Manila

CPET7L Hands On Activity 3

CPET – 2A

Tuesday 4:00PM to 7:00 PM

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INTRODUCTION TO HDL

Task Assessment:

An ABCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d, e, f, and g) select the corresponding segments in the display, as shown on Figure 1. The numeric display chosen to represent the decimal digit is shown in Table No.1. Using a truth table and Karnaugh maps, design the BCD-to-seven-segment using a minimum number of gates (except NOT gate).

Here is the following step to solve the given combinational logic design:

1. **Specification**, you must know the following specification in a circuit. Assume the inputs are W, X, Y and Z.

   where:

   - Variable W is the most significant bit (MSB)
   - Variable Z is the least significant bit (LSB)

   WXYZ = 4 variables

   2 ^ 4 = 16 rows / lines

   As shown in figure 1, the output segment labelled a, b, c, d, e, f and g.

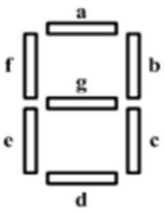
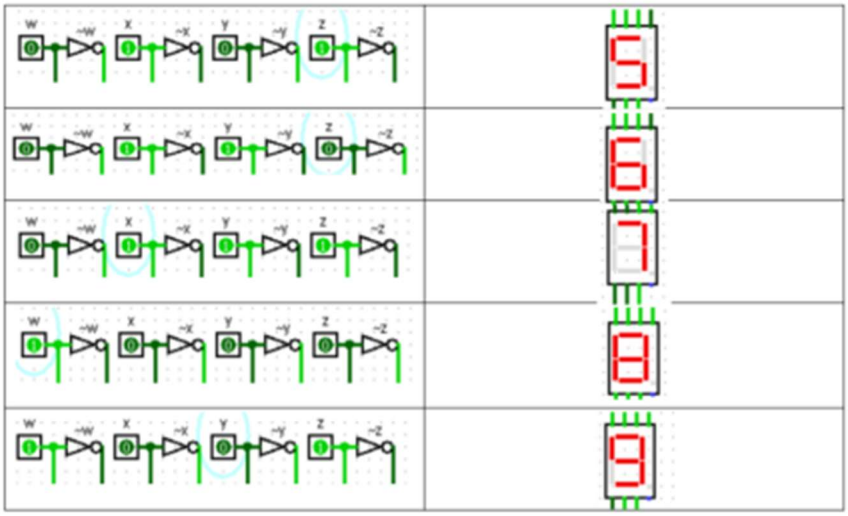


Figure 1: Seven (7) Segment Display



2. **Formulation** – you need to convert the specifications into a variety of forms. The form is to construct a Truth table. The table below shows the conversion of binary number to decimal number.

Table 1: Truth Table for BCD

	Input Variables				Output Variables							Decimal Number
	Binary Number				7-Segement Display							
	W	X	Y	Z	a	b	c	d	e	f	g	
0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	1	0	1	1	0	0	0	0	1
2	0	0	1	0	1	1	0	1	1	0	1	2
3	0	0	1	1	1	1	1	1	0	0	1	3
4	0	1	0	0	0	1	1	0	0	1	1	4
5	0	1	0	1	1	0	1	1	0	1	1	5
6	0	1	1	0	1	0	1	1	1	1	1	6
7	0	1	1	1	1	1	0	1	1	0	1	7
8	1	0	0	0	1	1	1	1	1	1	1	8
9	1	0	0	1	1	1	1	0	1	1	1	9
10	1	0	1	0	0	0	0	0	0	0	0	No Light
11	1	0	1	1	0	0	0	0	0	0	0	No Light
12	1	1	0	0	0	0	0	0	0	0	0	No Light
13	1	1	0	1	0	0	0	0	0	0	0	No Light
14	1	1	1	0	0	0	0	0	0	0	0	No Light
15	1	1	1	1	0	0	0	0	0	0	0	No Light

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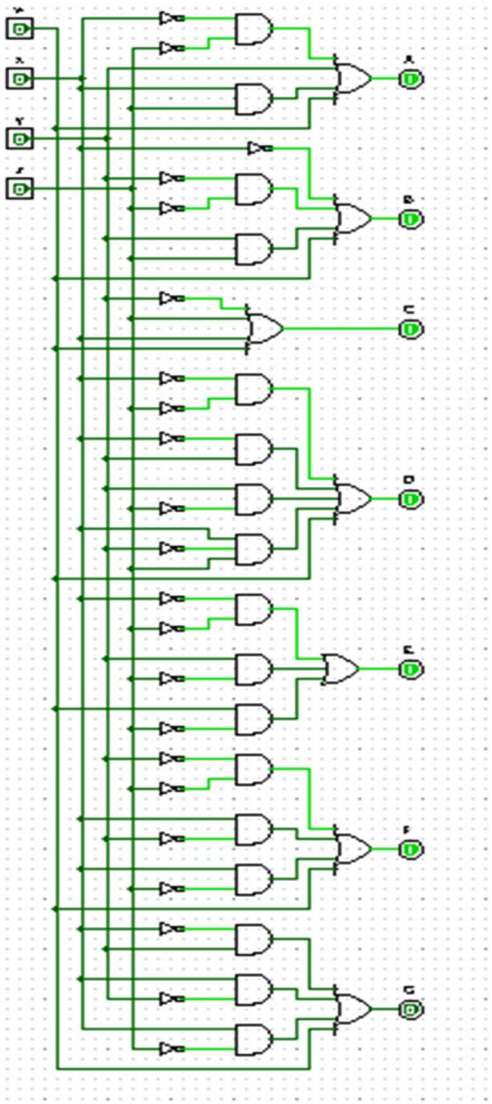
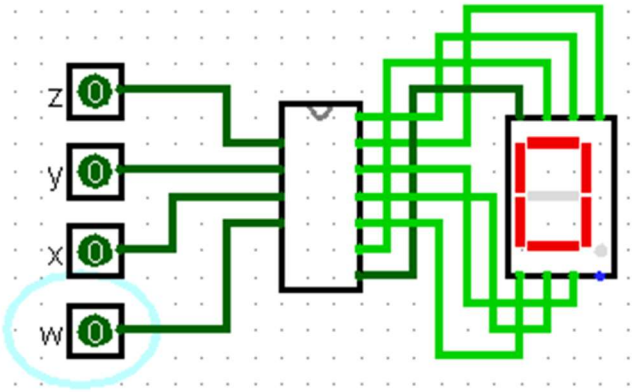
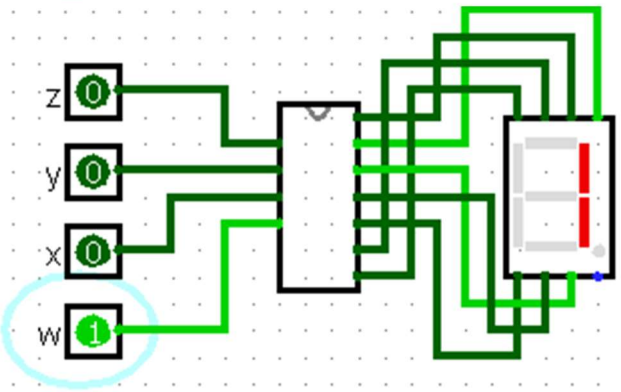
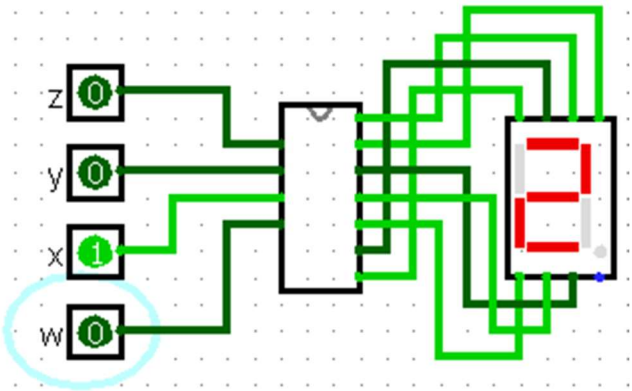
Documentation and Answers

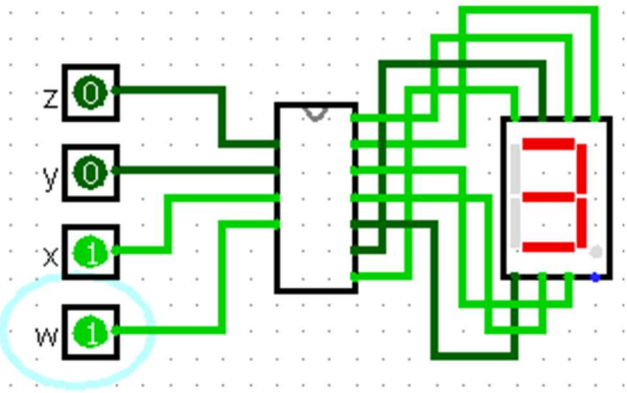
The following images illustrate a BCD to 7-segment display circuit that counts from 0 to 9 using an integrated circuit (IC). This circuit consists of four input switches (w, x, y, z) that provide a 4-bit binary-coded decimal (BCD) value to the decoder IC. The IC then converts this binary input into a corresponding decimal digit and controls the 7-segment display by lighting up the appropriate segments.

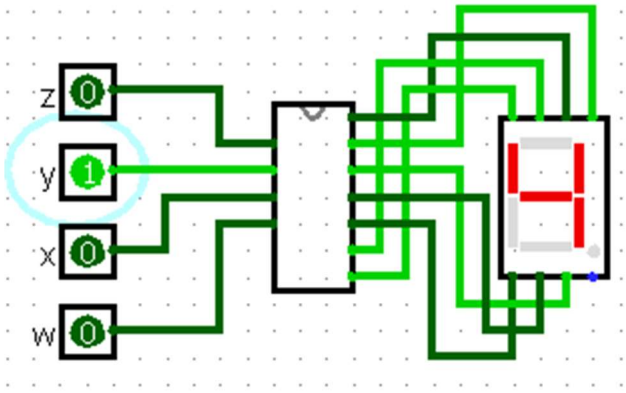


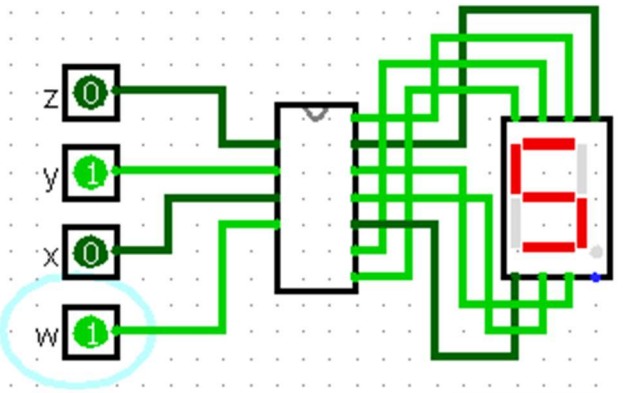


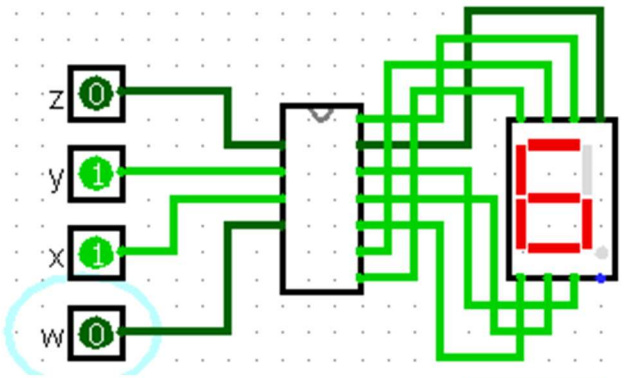


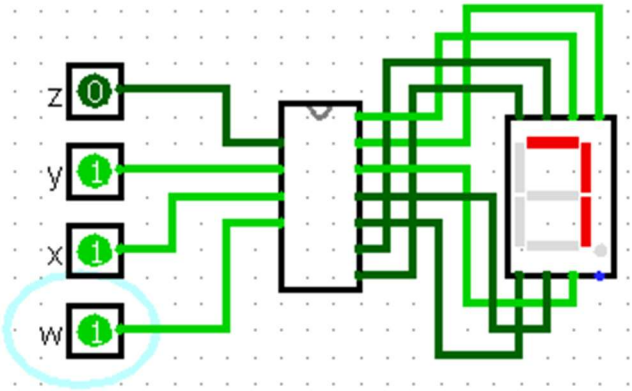


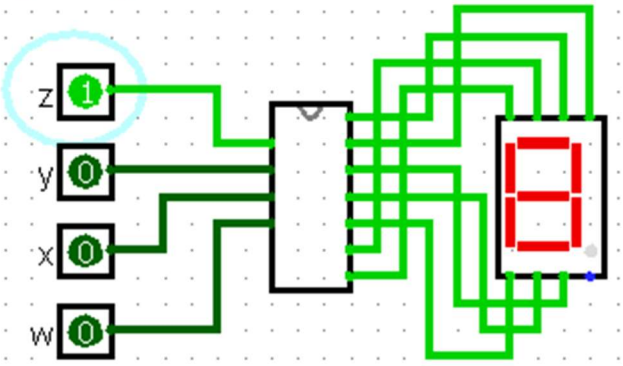

z 0
y 0
x 1
w 1

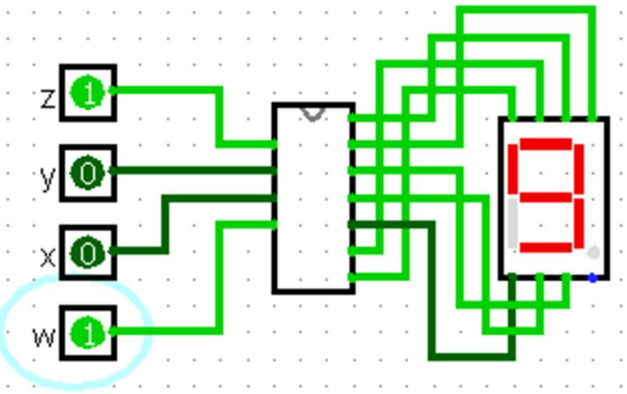

z 0
y 1
x 0
w 0


z 0
y 1
x 0
w 1


z 0
y 1
x 1
w 0


z 0
y 1
x 1
w 1


z 1
y 0
x 0
w 0


z 1
y 0
x 0
w 1

INTRODUCTION TO HDL

For the formulation of the truth table using the Behavioral Method in Verilog programming, the group created a program that implements this approach. Below is the Verilog program along with its corresponding output.

Source Code:

```
module handson3 (w,x,y,z,decimal);
        input w,x,y,z;
        output reg [6:0] decimal;
        always @(*) begin
                decimal[6] = ~x&~z | y | z&x | w;
                decimal[5] = ~x | ~y&~z | y&z | w;
                decimal[4] = ~y | z | x | w;
                decimal[3] = ~x&~z | ~x&y | y&~z | x&~y&z | w;
                decimal[2] = ~x&~z | y&~z | w&~z;
                decimal[1] = ~y&~z | x&~y | x&~z | w;
                decimal[0] = ~x&y | x&~y | x&~z | w;
                end
endmodule


module testbench;
        reg w,x,y,z;
        wire [6:0] decimal;
        initial begin
                $display("w x y z | A B C D E F G");
                w = 1'b0; x = 1'b0; y = 1'b0; z = 1'b0;
                #16 $finish;
        end
        always #8 w = ~w;
        always #4 x = ~x;
        always #2 y = ~y;
        always #1 z = ~z;
```

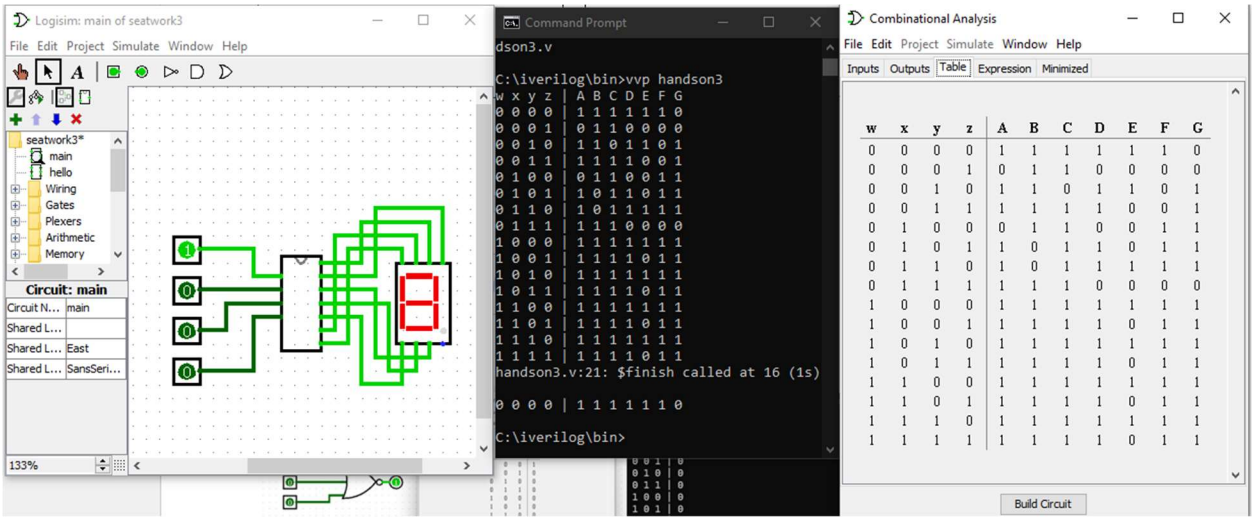
```
handson3 U1(w,x,y,z,decimal);

initial

$monitor("%b %b %b %b | %b %b %b %b %b %b %b", w, x, y, z, decimal[6], decimal[5], decimal[4], decimal[3], decimal[2], decimal[1], decimal[0]);

endmodule
```

Output:



Conclusion:

Through the implementation of Verilog programming using the Behavioral Method, the group successfully formulated a truth table that aids in understanding digital logic operations. Additionally, the BCD to 7-segment display circuit effectively demonstrates the conversion of a 4-bit binary-coded decimal (BCD) input into a corresponding decimal output.