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April 2013

FDMQ86530L

GreenBridgeTM Series of High-Efficiency Bridge Rectifiers N-Channel PowerTrench[®] MOSFET 60 V, 8 A, 17.5 m Ω

Features

- Max $r_{DS(on)}$ = 17.5 m Ω at V_{GS} = 10 V, I_D = 8 A
- Max $r_{DS(on)} = 23 \text{ m}\Omega$ at $V_{GS} = 6 \text{ V}$, $I_D = 7 \text{ A}$
- Max $r_{DS(on)}$ = 25 m Ω at V_{GS} = 4.5 V, I_D = 6.5 A
- Substantial efficiency benefit in PD solutions
- RoHS Compliant

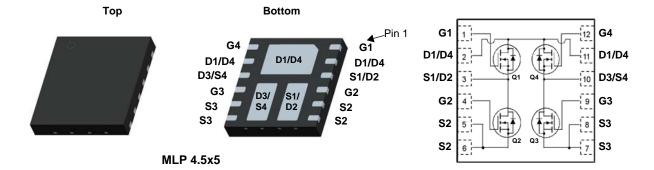


General Description

This Quad MOSFET solution provides ten-fold improvement in power dissipation over diode bridge.

Applications

- Active bridge
- Diode Bridge replacement in 24V & 48V AC systems



MOSFET Maximum Ratings TA = 25 °C unless otherwise noted

Symbol	Paramete		Ratings	Units	
V _{DS}	Drain to Source Voltage			60	V
V_{GS}	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T _C = 25 °C		8	
I _D	-Continuous	T _A = 25 °C	(Note 1a)	8	Α
	-Pulsed			50	
D	Power Dissipation	T _C = 25 °C		22	W
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	1.9	VV
T _J , T _{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	65	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	135	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMQ86530L	FDMQ86530L	MLP 4.5x5	13 " 12 mm		3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu A$, referenced to 25 °C		27		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 48 V, V _{GS} = 0 V			1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		-6		mV/°C
		$V_{GS} = 10 \text{ V}, I_D = 8 \text{ A}$		12	17.5	mΩ
_	Static Drain to Source On Resistance	$V_{GS} = 6 \text{ V}, I_D = 7 \text{ A}$		15	23	
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 6.5 \text{ A}$		20	25	
		$V_{GS} = 10 \text{ V}, I_D = 8 \text{ A}, T_J = 125 ^{\circ}\text{C}$		18	26	
9 _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 8 A		28		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 20 V V 0 V	1725	2295	pF
C _{oss}	Output Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	299	400	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1/11/12	10	15	pF

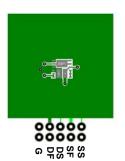
Switching Characteristics

t _{d(on)}	Turn-On Delay Time		8.8	18	ns
t _r	Rise Time	V _{DD} = 30 V, I _D = 8 A,	3.8	10	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	22	35	ns
t _f	Fall Time		2.8	10	ns
Q_g	Total Gate Charge	V _{GS} = 0 V to 10 V	23	33	nC
Q_{g}	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V}$ $V_{DD} = 30 \text{ V},$	11	16	nC
Q_{gs}	Gate to Source Charge	I _D = 8 A	5.1		nC
Q_{gd}	Gate to Drain "Miller" Charge		2.3		nC

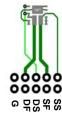
Drain-Source Diode Characteristics

Ven Source to Drain Diode Forward Voltage	Source to Drain Diode, Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 8 \text{ A}$ (Note 2)		0.8	1.3	V
	$V_{GS} = 0 \text{ V}, I_S = 1.6 \text{ A}$ (Note 2)		0.7	1.2	V	
t _{rr}	Reverse Recovery Time	I - 9 A di/dt - 100 A/v.o		27	43	ns
Q _{rr}	Reverse Recovery Charge	I _F = 8 A, di/dt = 100 A/μs		12	22	nC

^{1.} $R_{\theta,M}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta,JC}$ is guaranteed by design while $R_{\theta,CA}$ is determined by the user's board design.



a. 65 °C/W when mounted on a 1 in 2 pad of 2 oz copper. the board designed Q1+Q3 or Q2+Q4.



b. 135 °C/W when mounted on a minimum pad of 2 oz copper. the board designed Q1+Q3 or Q2+Q4.

^{2.} Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.

Typical Characteristics T_J = 25 °C unless otherwise noted

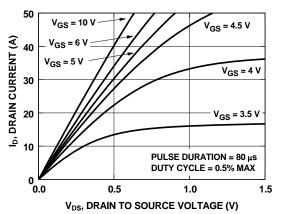


Figure 1. On-Region Characteristics

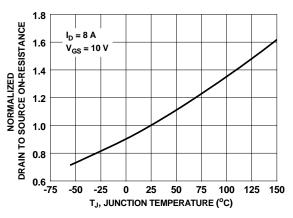


Figure 3. Normalized On-Resistance vs Junction Temperature

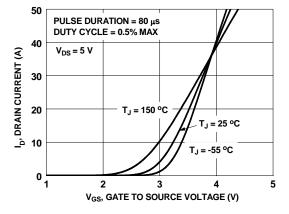


Figure 5. Transfer Characteristics

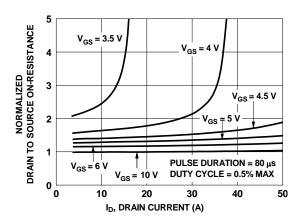


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

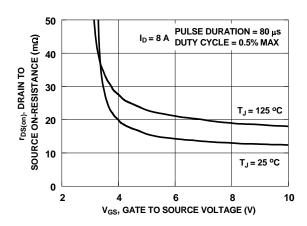


Figure 4. On-Resistance vs Gate to Source Voltage

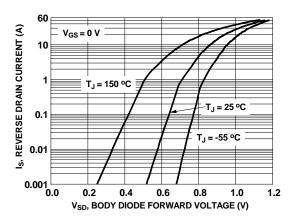


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

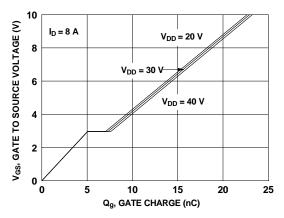


Figure 7. Gate Charge Characteristics

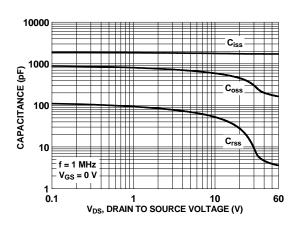


Figure 8. Capacitance vs Drain to Source Voltage

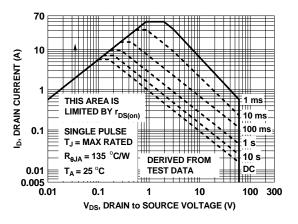


Figure 9. Forward Bias Safe Operating Area

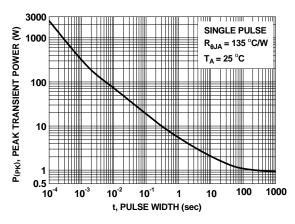


Figure 10. Single Pulse Maximum Power Dissipation

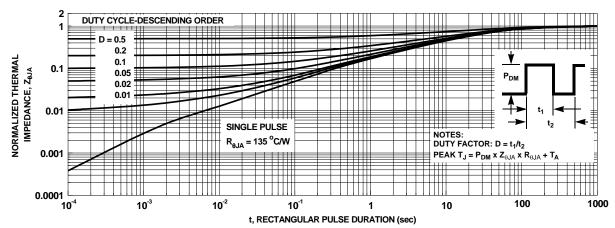
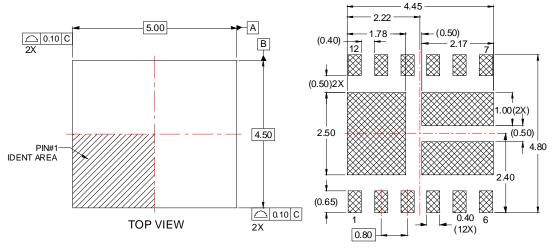
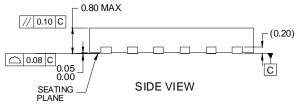
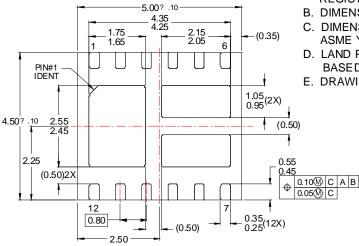


Figure 11. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout







BOTTOM VIEW

RECOMMENDED LAND PATTERN

NOTES:

- (A) THIS MKT. DWG. DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
- E. DRAWING FILENAME: MKT-MLP12FRev1.





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