SYNOPSYS®

ModelSim

Advanced Simulation and Debugging

数字集成电路设计课程设计

第 6 组

高性能FFT芯片设计

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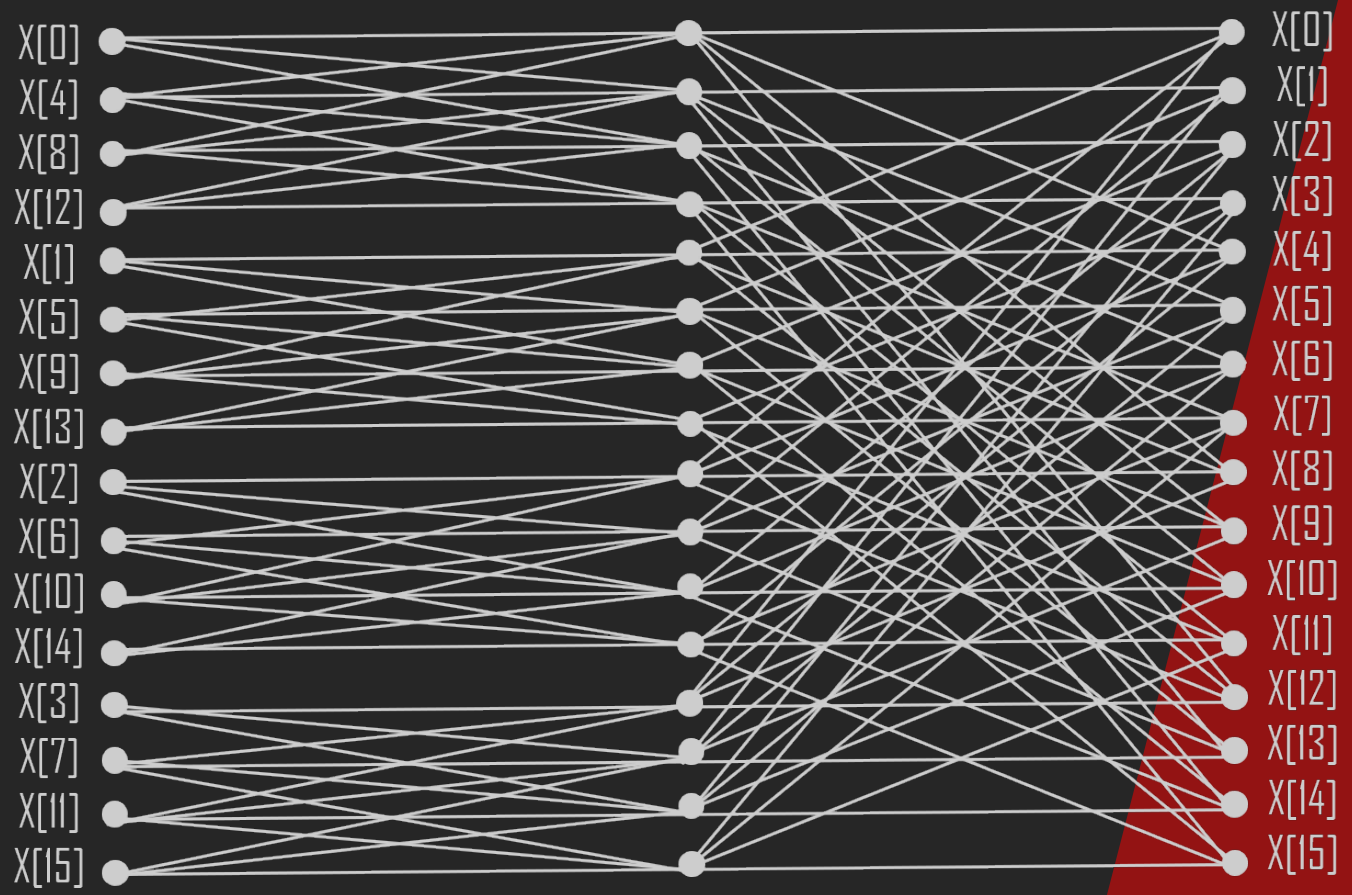
https://github.com/VenciFreeman/FFT_ChipDesign

TOC

设计规范简介

Introduction to Design Specification

功能描述Function Description



16点 基-4 FFT运算

功能描述Function Description

运算数据的实部虚部均为17 bit

而旋转因子的实部与虚部为8 bit

时序过程 Timing Process

各模块																											
时钟周期	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
输入	第N组输入数据到REG1																第N+1组输入数据到REG1												
计算	两级蝶形运算																两级蝶形运算												
输出	第N-1组从REG3输出数据					第N-1组从REG3输出数据																第N组从REG3输出数据							
REGISTER																													
0	第N组输入																第N+1组输入												
1	蝶形运算中间值																蝶形运算中间值												
2	第N-2组输出					第N-1组输出																第N组输出							

性能描述 Performance Description

135 MHz

工作频率

41988

次/(mm^2·mW·s)

面积单位功耗时间

FFT操作数

5.25×10^{-6} mJ

单次FFT能耗

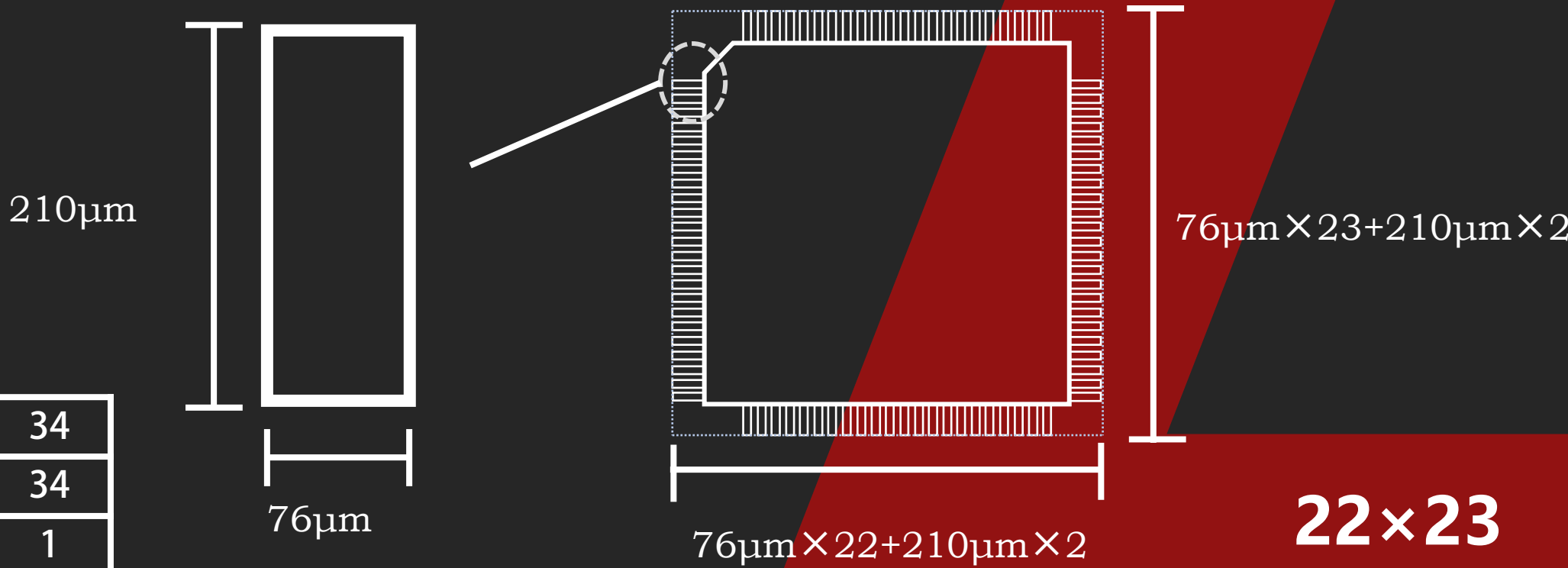
4.535456 mm^2

面积开销

性能分析与结构设计

Performance & Structure

面积估算 Area Estimation



输入管脚	34
输出管脚	34
时钟信号	1
使能信号	1
管脚供电	8
内核供电	12

$$2.168\ mm \times 2.092\ mm = 4.535456\ mm^2$$

0.18 μm工艺

22×23

管脚数量

性能估算 Performance Estimation

$$\frac{1\ s}{16 \times 7.4\ ns} = 8.445946 \times 10^6$$

每秒FFT运算次数

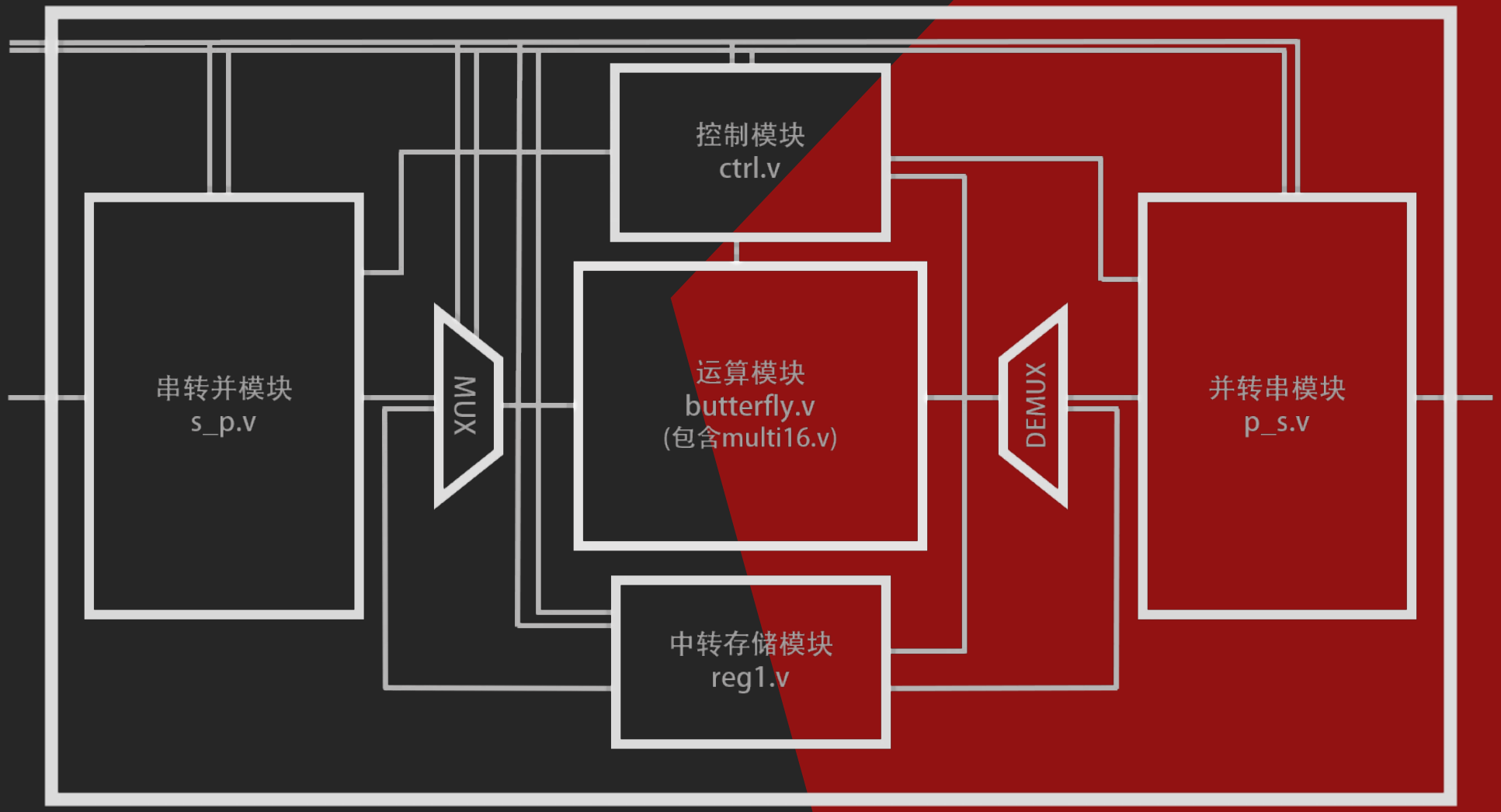
$$135\ MHz \times \frac{34\ bits}{9} = 510.51 MB/s$$

平均带宽

$$\frac{1\ s}{16 \times 7.4\ ns} \times 16 \times (17 + 17) = 4.5946 \times 10^9\ bps$$

流水吞吐率

硬件结构Hardware Structure



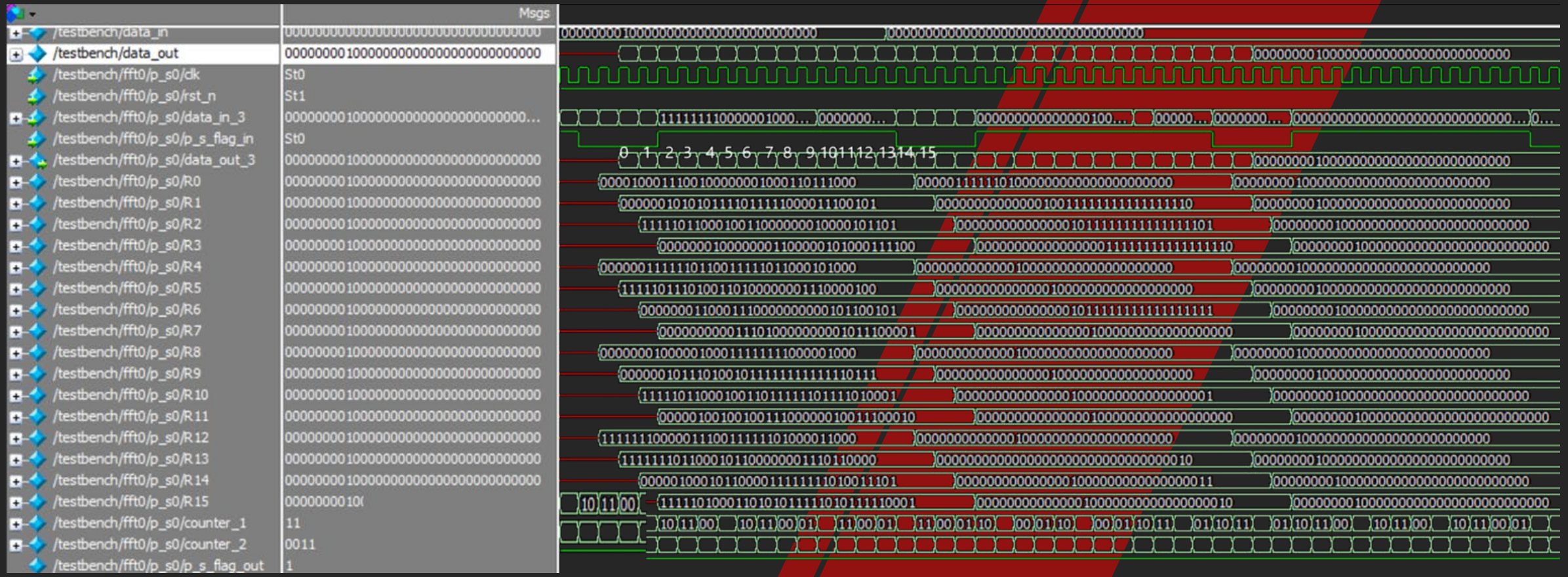
RTL模型与仿真验证

RTL Model & Simulation Verification

运算结果验证 Operation results Verification

Out	Standard Real Part	Our Real Part	Standard Imaginary Part	Our Imaginary Part
0	0 00010010 00000000	0 00010010 11001000	0 00010010 0000000	0 00010001 10111000
1	0 00000101 01101110	0 00000101 01011110	1 11110000 10111010	1 11110000 11100101
2	1 11110110 00101011	1 11110110 00100110	0 00000100 00111110	0 00000100 00101101
3	0 00000010 00001101	0 00000010 00000011	0 00001010 01011100	0 00001010 00111100
4	0 00001000 00000000	0 00000111 11101100	1 11110110 00000000	1 11110110 00101000
5	1 11110111 00110000	1 11110111 01001101	0 00000011 10010000	0 00000011 10000100
6	0 00000011 00101011	0 00000011 00011100	0 00000001 01100101	0 00000001 01100101
7	0 00000000 01101101	0 00000000 01110100	0 00000001 01101010	0 00000010 11100001
8	0 00000010 00000000	0 00000010 00001000	1 11111110 00000000	1 11111110 00001000
9	0 00000101 11100001	0 00000101 11010010	1 11111111 11110101	1 11111111 11110111
10	1 11110110 00000000	1 11110110 00100110	1 11111011 11000001	1 11111011 11010001
11	0 00001001 01000010	0 00001001 00100111	0 00000100 11100000	0 00000100 11100010
12	1 11111100 00000000	1 11111100 00011100	1 11111010 00000000	1 11111010 00011000
13	1 11111101 01111111	1 11111101 10001011	0 00000011 10111111	0 00000011 10110000
14	0 00001000 11010100	0 00001000 10110000	1 11111110 10010101	1 11111110 10011101
15	1 11110100 01000010	1 11110100 011010100	1 11110101 11001111	1 11110101 11110001

流水线验证 Pipeline Verification

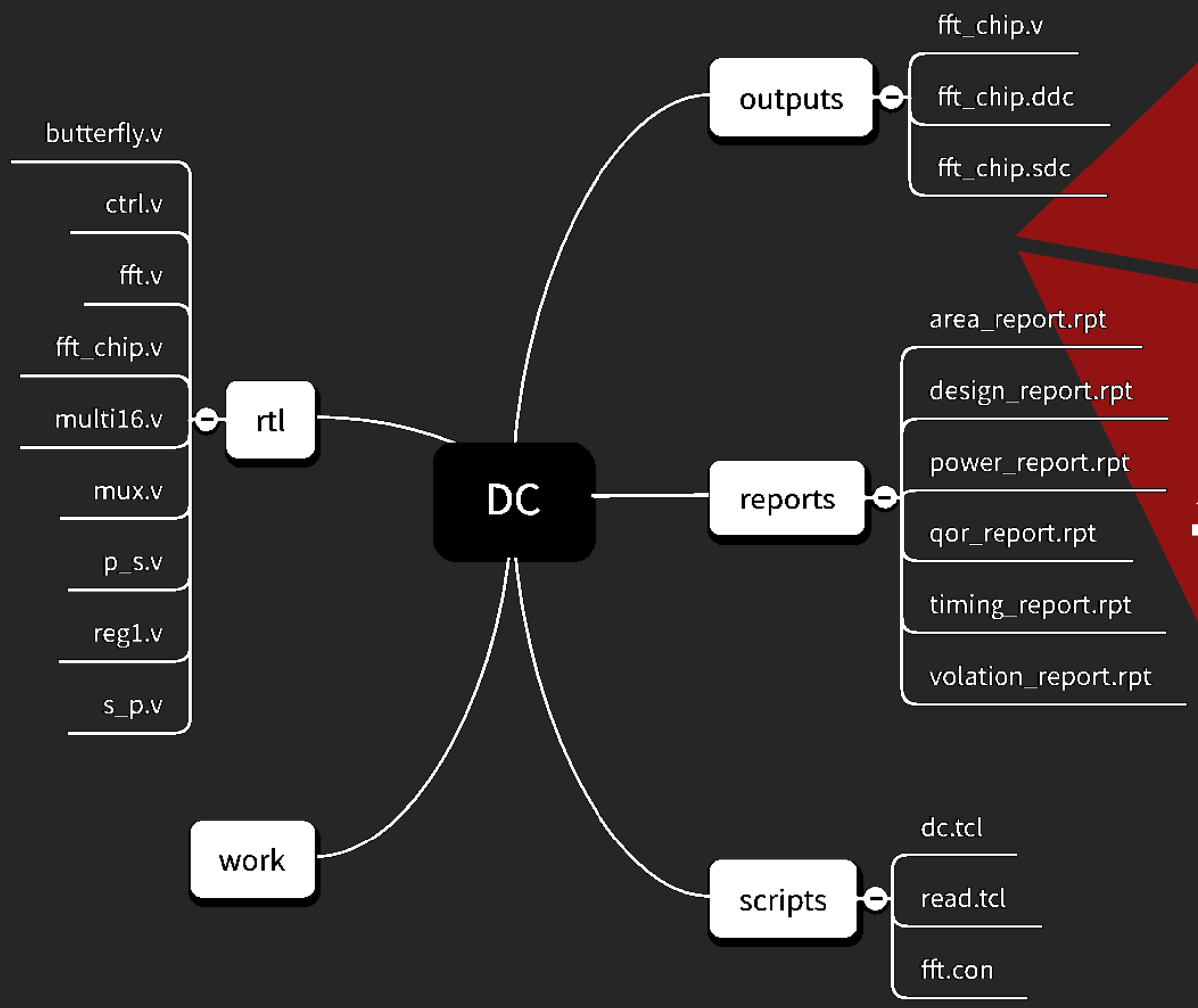


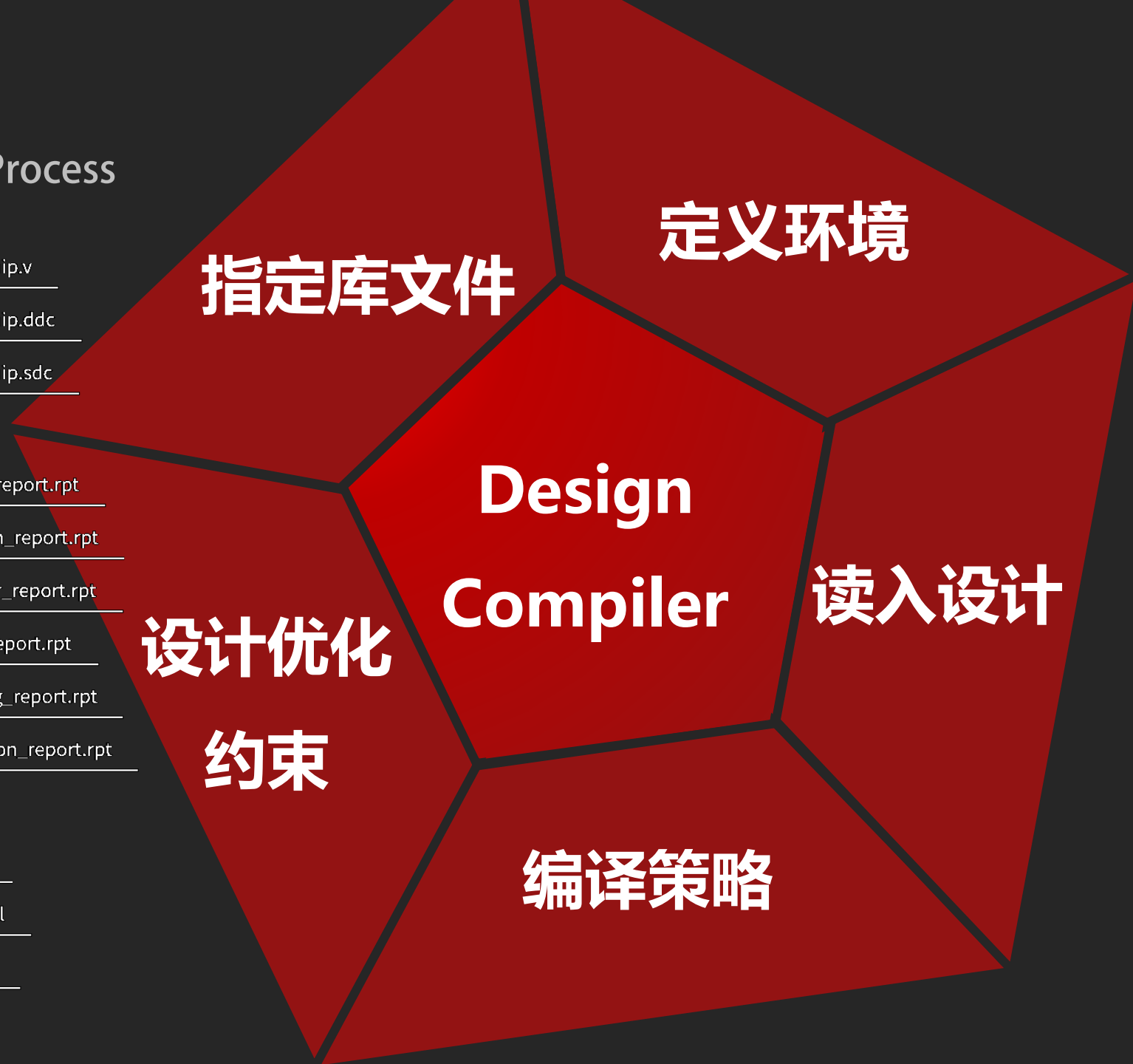
单次运算结果和流水运算结果均正确

逻辑综合策略与结果

Logic Synthesis Strategy & Result

逻辑综合流程DC Process





参数设置与结果 Parameters setup & DC results

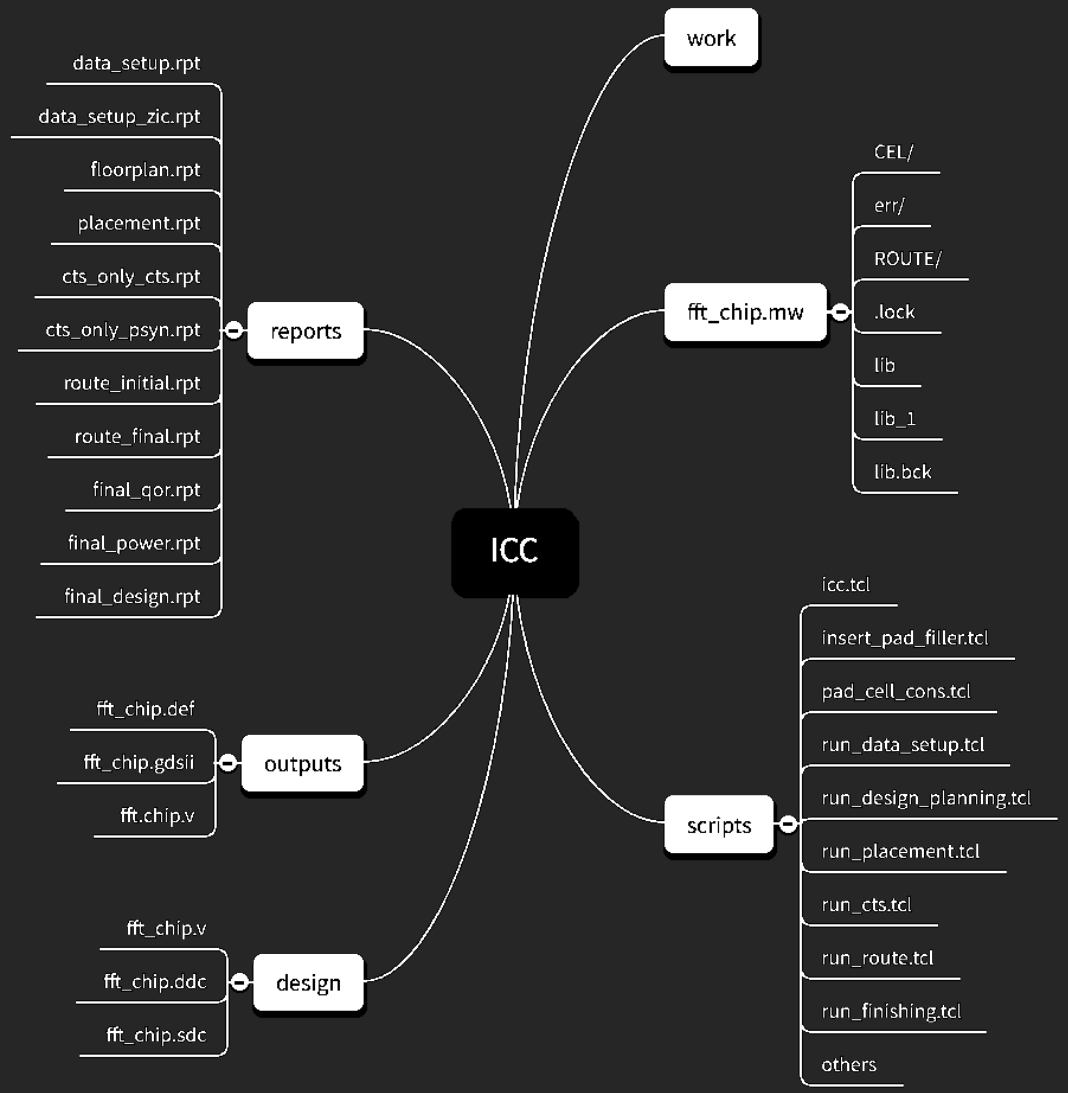
设计工艺	时钟周期	I/O延时	时钟延时	不确定时钟	过渡时钟	最大过渡	工作电压	运行温度
0.18 um	7.4 ns	3.7 ns	4.3 ns	0.5 ns	0.2 ns	3 ns	1.62 V	125 ℃

clk max slack	0.00 ns (MET)
Total Area	3726936.833315 um^2
Net Switching Power	1.1317 W
Violation	0
Leaf Cell	16473
Total Number of Nets	18037

物理实现与结果分析

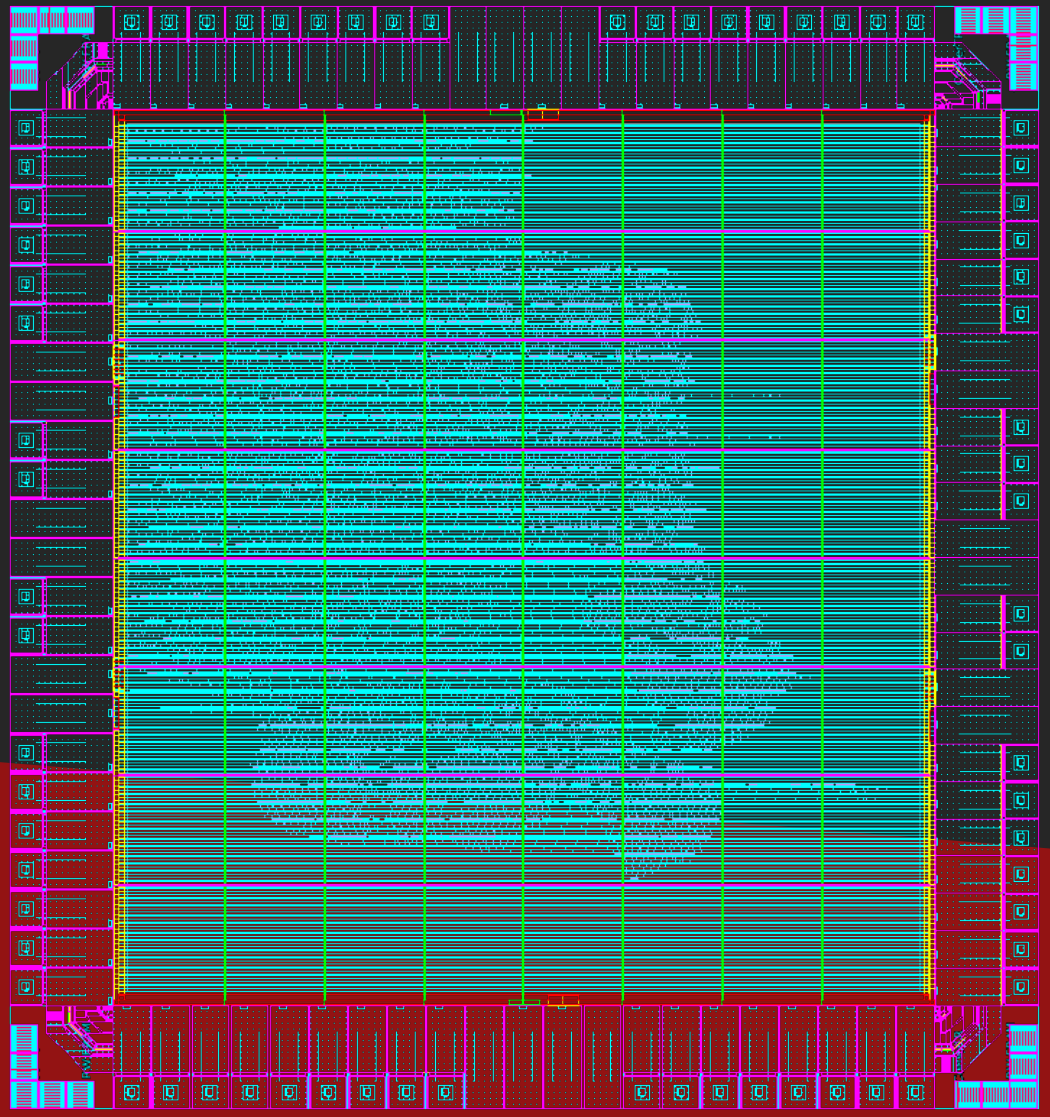
Physical Realization & Result

ICC设计步骤ICC Process

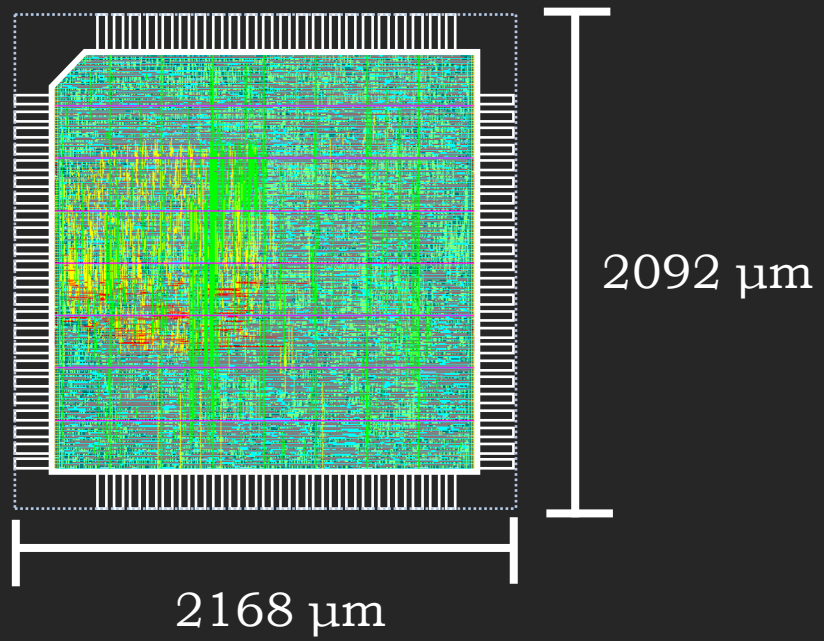


芯片概览与slack Chip Overview & slack

Slack	input (ns)	output (ns)	clk (ns)
data_setup	—	—	0.48
data_setup_zic	1.43	0.48	1.19
floorplan	0.95	-1.02	-1.39
placement	1.01	0.59	0.19
cts_only_psyn	1.26	0.82	0.62
cts_only_cts	1.26	0.83	0.36
route_initial	1.35	0.88	0.65
route_final	1.35	0.85	0.01

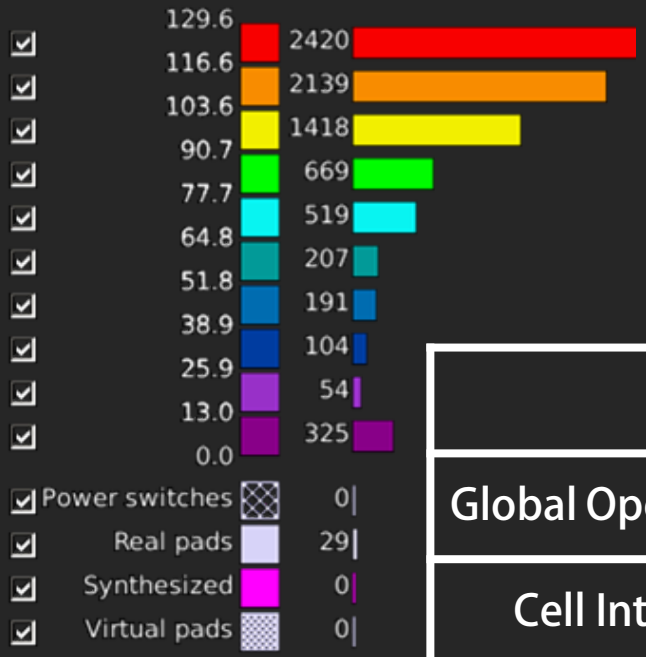


面积Area

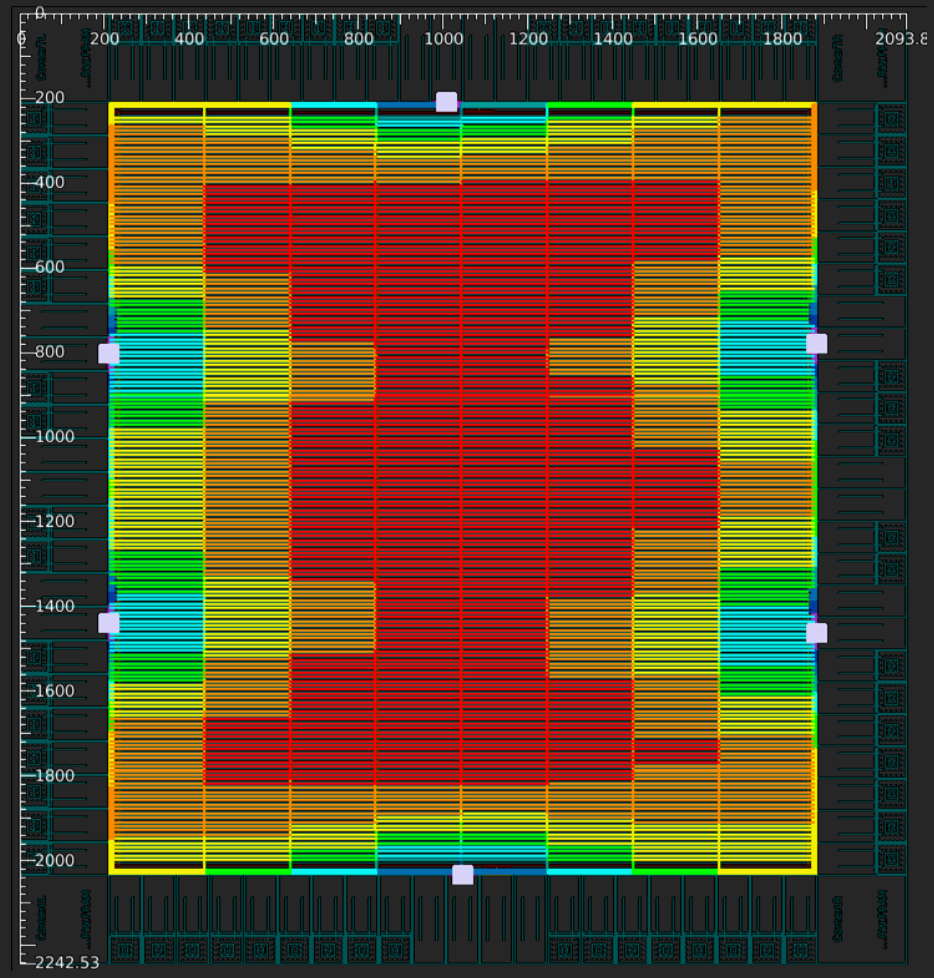


项目	面积或长度
Combinational Area	1477888.208778 um^2
Non-combinational Area	154248.498180 um^2
Net Area	0.000000 um^2
Net X Length	620954.62 nm^2
Net Y Length	666869.44 nm
Cell Area	1632136.706958 um^2
Design Area	1632136.706958 um^2
Net Length	1287824.00 nm
Total Area	4695300.72 um^2

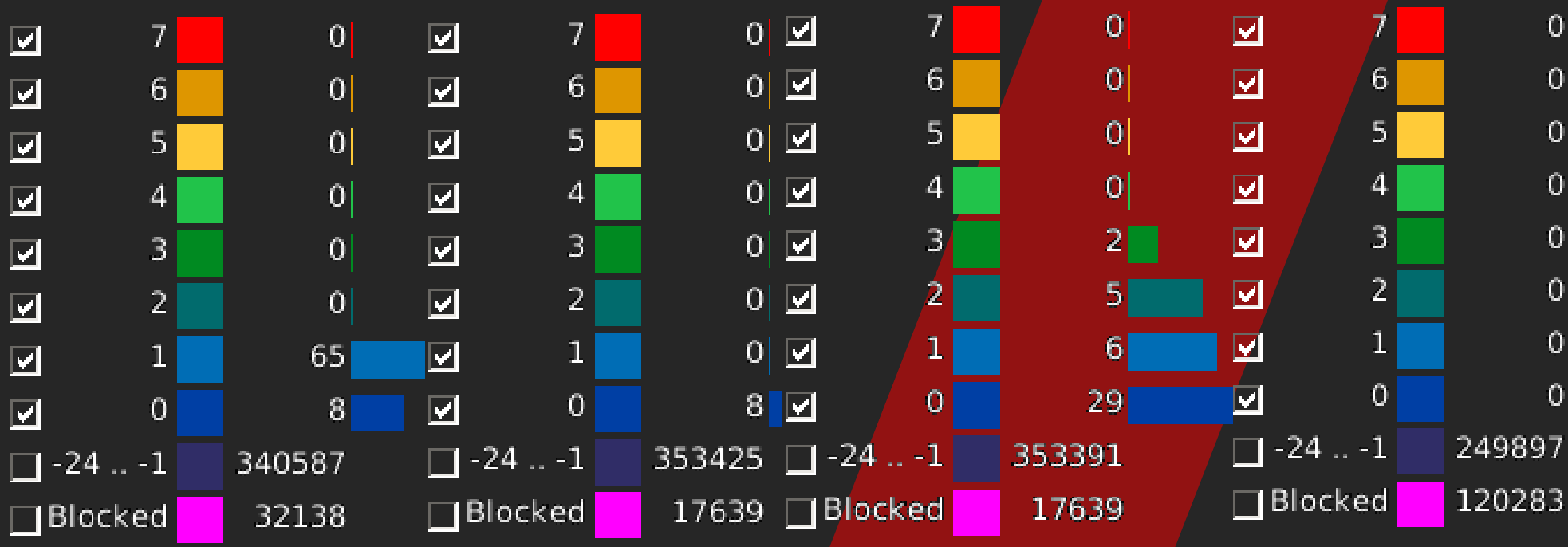
电压降与功耗Voltage Drop and Power



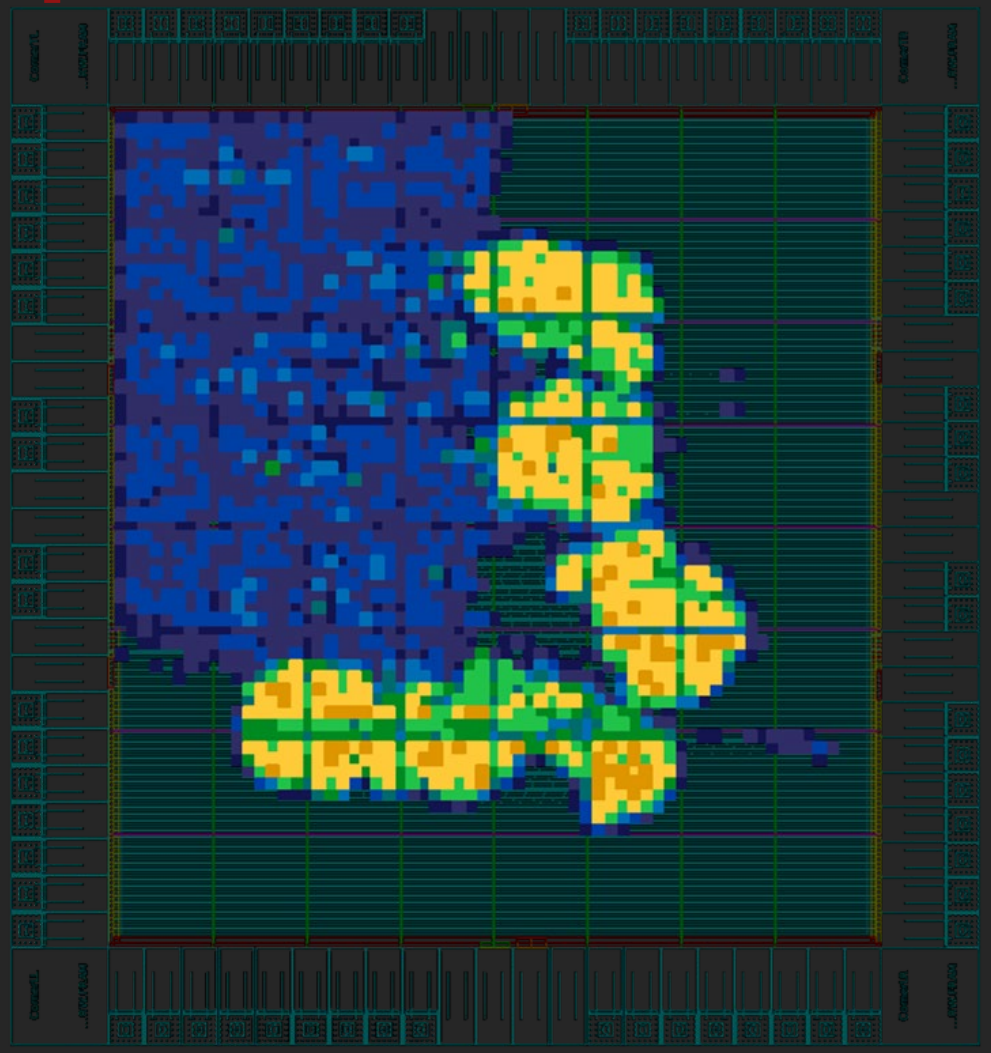
项目	电压或功耗
Global Operating Voltage	1.62 V
Cell Internal Power	33.6445 mW
Net Switching Power	12.7067 mW
Total Dynamic Power	44.3512 mW
Cell Leakage Power	26.0446 uW



拥塞 Congestion



资源使用 Utilization



项目	数量或利用率
Module Cells	16240
Pins	91614
IO Pad Cells	90
IO Pins	70
Nets	18151
Average Pins Per Net	3.0535
Total Std Cell Area	514936.70 um^2
Total Pad Cell Area	1612800.00 um^2
Std cells utilization	18.10%
Cell/Core Ratio	18.10%
Cell/Chip Ratio	45.32%
Number of Cell Rows	350

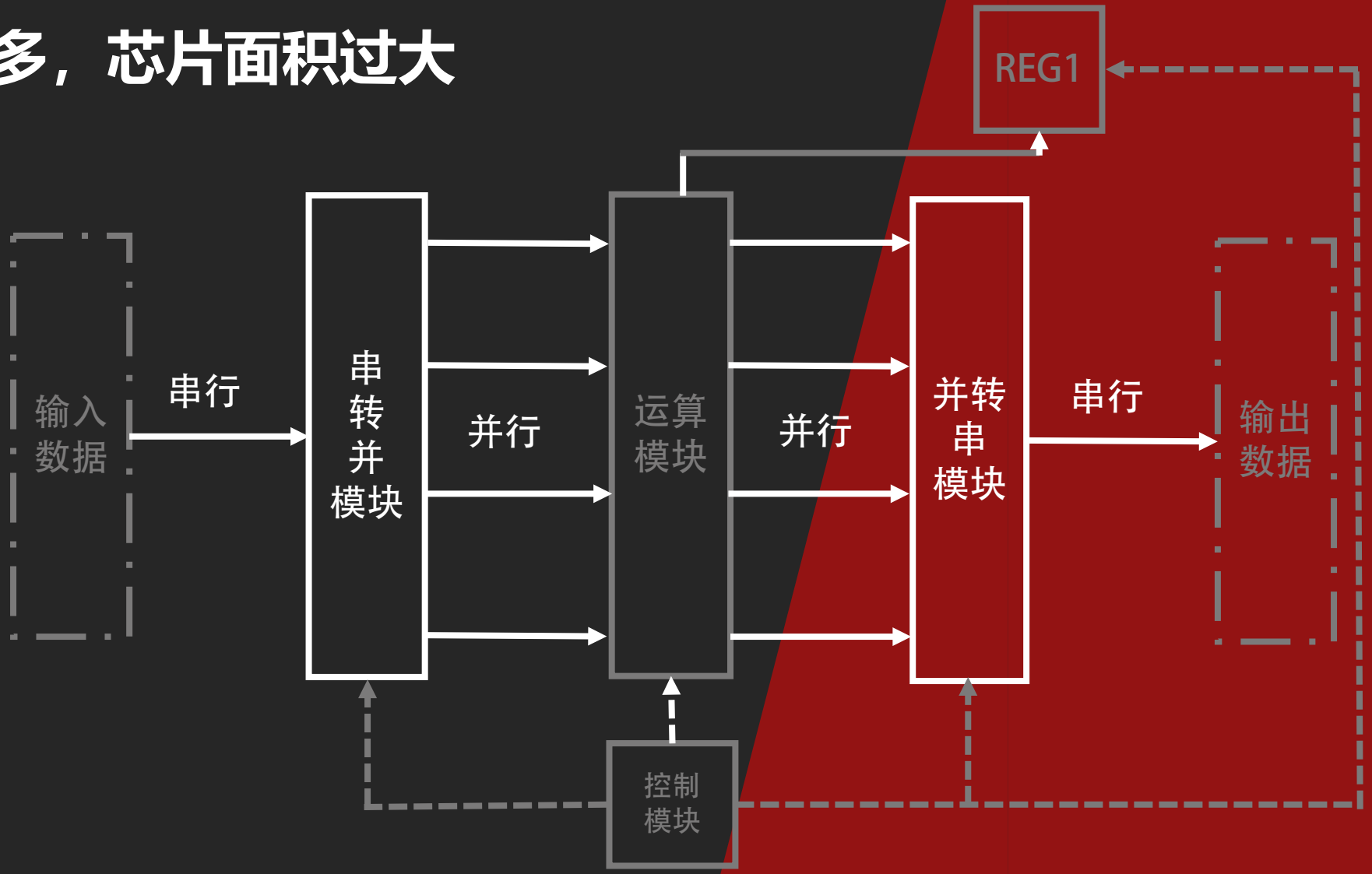
设计总结与任务分工

Summary & Work Division

遇到的问题及解决方案 Problems & Solutions

管脚数量过多，芯片面积过大

串并转换



遇到的问题及解决方案 Problems & Solutions

! 计算结果不正确

代码Debug

蝶形运算

乘法器

串并转换

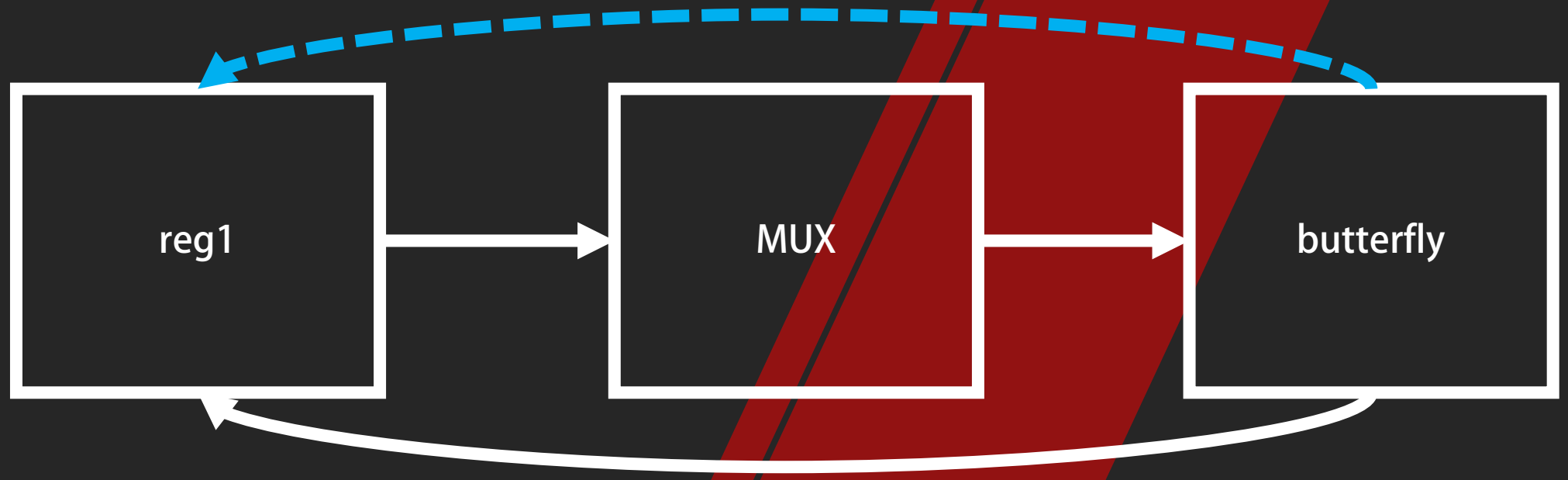
控制模块

testbench

… …

遇到的问题及解决方案 Problems & Solutions

- 时序模块数据传输不同步，拖慢运算速度
- 添加一条组合逻辑路径传输数据



遇到的问题及解决方案 Problems & Solutions

芯片工作频率过低 (DC slack为负)

```
set_flatten true
compile -map high
```

乘法计算 → 组合逻辑状态机移位乘法

```
assign mul = in_17bit[16:0] * in_8bit[7:0];
```

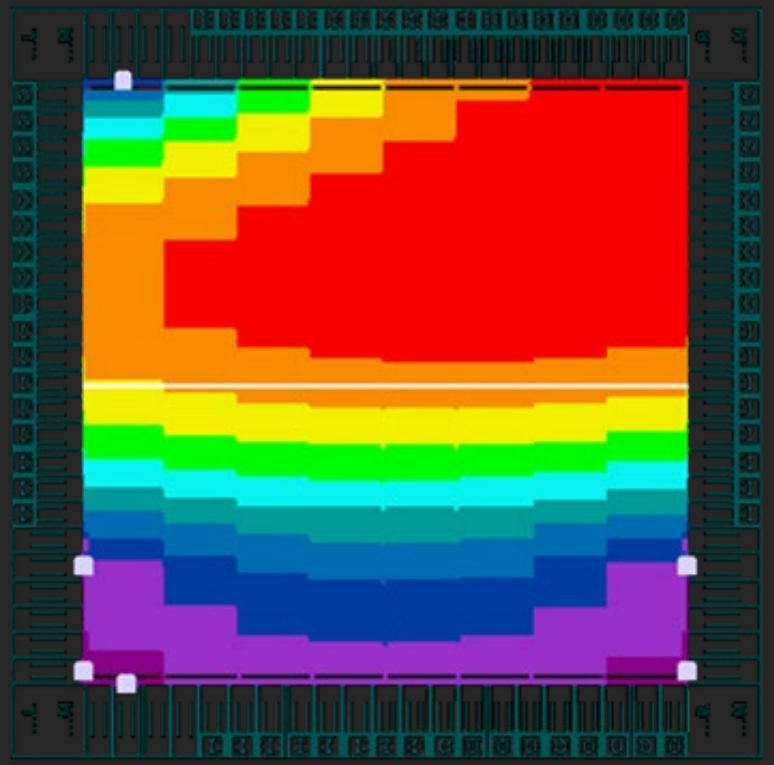
→

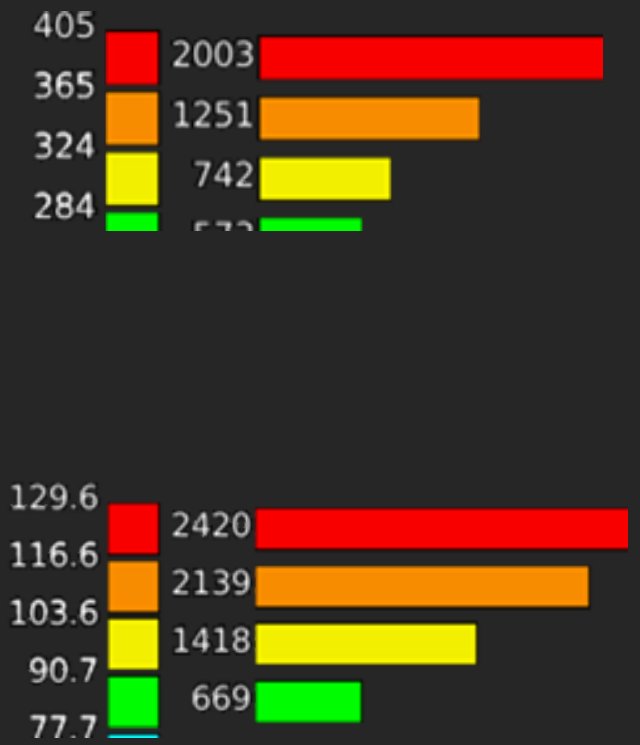
```
always @ ( in_17bit or in_8bit ) begin
  case ( in_8bit )
    8'b00000000: neg_mul = 25'b0;
    8'b01111111: neg_mul = ( in_17bit << 7 );
    ... ...
  endcase
end
```

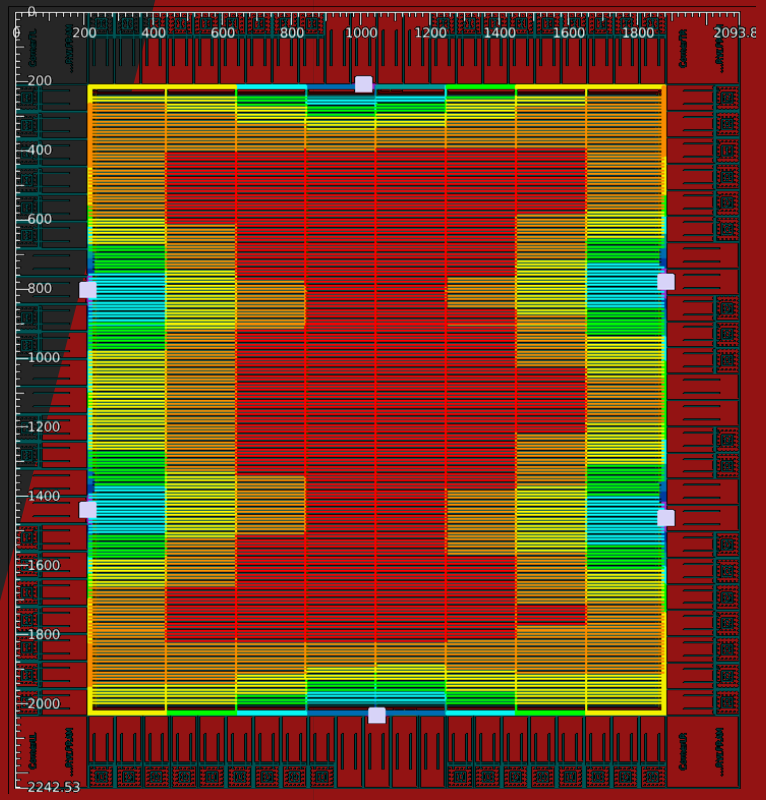
遇到的问题及解决方案 Problems & Solutions

芯片电压降问题

添加供电管脚并调整位置







任务分工 Work Division

组员	代码编写	逻辑综合	物理实现	其他工作
罗恬	串并转换模块 中间存储模块 明确运算逻辑 Debug	相关文件debug 实现135 MHz	相关文件debug 实现135 MHz	撰写报告
齐奕翔	乘法器 运算模块 测试模块 运算模块 Debug	编写相关文件 实现82 MHz	编写相关文件 实现82 MHz	撰写报告
杨文曦	运算模块 乘法器 整合代码 Debug	相关文件debug 实现135 MHz	相关文件debug 实现135 MHz	撰写报告 组织团队协作 准备展示材料
*未列出的部分，入架构设计、测试向量的准备等均为团队共同合作完成。				

参考资料References

[1] Siva Kumar Palaniappan, et al. Design of 16-point Radix-4 Fast Fourier Transform in 0.18μm CMOS Technology [J]. American Journal of Applied Sciences 4(8): 570-575, 2007

[2] N. Weste, M. Bickerstaff, et al. A 50MHz 16-point FFT processor for WLAN application: IEEE 1997 Custom Integrated Circuits Conference: 457-460, 1997

[3] 丁晓磊等. 16点基4-FFT芯片设计技术研究[J]. 信息技术. 64-71, 2007(1)

```
Processing module butterfly_DW01_add_158
Processing module butterfly_DW01_sub_115
Processing module butterfly_DW01_add_141
Processing module butterfly_DW01_add_151
Processing module butterfly_DW01_sub_104
Processing module butterfly_DW01_sub_96
Processing module butterfly_DW01_sub_101
Processing module butterfly_DW01_add_129
Processing module butterfly_DW01_add_185
Processing module butterfly_DW01_sub_124
Processing module butterfly_DW01_add_184
Processing module butterfly_DW01_sub_123
Processing module butterfly_DW01_sub_121
Processing module butterfly_DW01_add_170
Processing module butterfly_DW01_add_164
Processing module butterfly_DW01_sub_118
Processing module butterfly
Processing module mux
Processing module s_p
Processing module ctrl
Processing module fft
Processing module fft_chip
Elapsed =    0:00:01, CPU =    0:00:00
Write verilog completed successfully.
1
icc_shell> close_mw_c
Removing physical des        hip'
1
icc_shell> close_mw_lib
1
icc_shell> exit
Updating preference file: /home/student/.synopsys_icc_prefs.tcl

Memory usage for main task 540 Mbytes.
Memory usage for this session 540 Mbytes.
CPU usage for this session 593 seconds ( 0.16 hours ).

Thank you...
Exit IC Compiler!
[student@Student work]$
```

上海交通大學

SHANGHAI JIAO TONG UNIVERSITY

Thanks for watching.

Slides designed by Venci Freeman

Sunday, May 10, 2020

https://github.com/VenciFreeman/FFT_ChipDesign