Assignment : 3

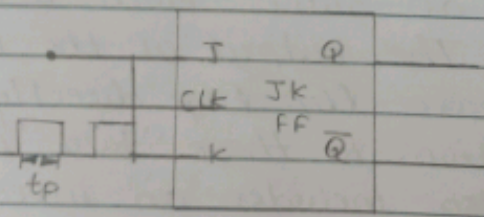
Page No.
Date

Que 1 Can a Flip Flop be used as a memory? if so how many bits can be stored by R-S Flip Flop?

⇒ - yes a Flip Flop can be used as a memory.
- It has two stable states namely logic 1 State & logic 0 state. We can design it either using NOR gates and or NAND Gates.
- it can store 1-bit of digital information.

Que 2 What is race around condition? How does it gets eliminated in master slave Jk ff? Explain.

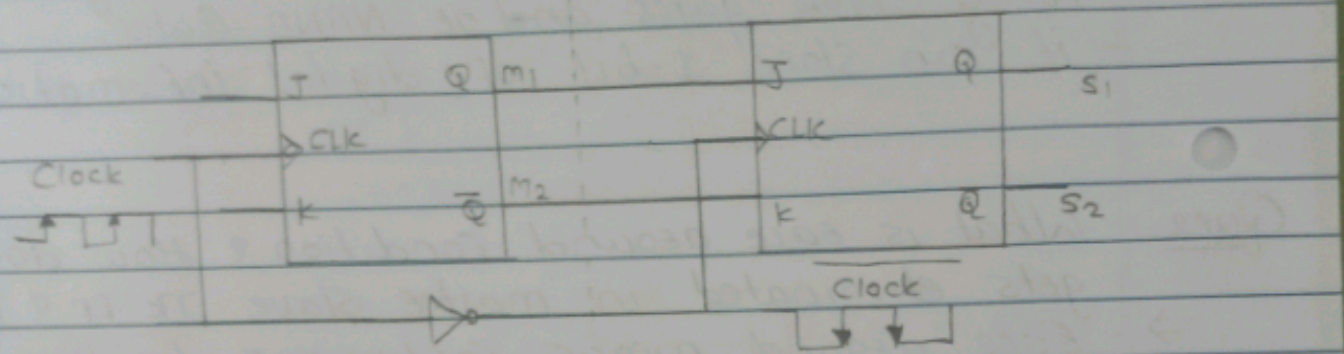
⇒ - Race around means continuous toggling.
- It is phenomenon which occues in a level triggered Jk Flip-Flop when both input terminals (J & K) are at 1, and the clock is active



(Jk Flip Flop in toggle mode)

- The toggle mode for Jk Flip-Flop is obtained when J=K=1 & CLK=1
- Many times this mode is used as an application, for example in counters.
- But, if J=K=1 & CLK=1 for a long time, then Q output will toggle as long as CLK is high, which makes the output of the Flip Flop

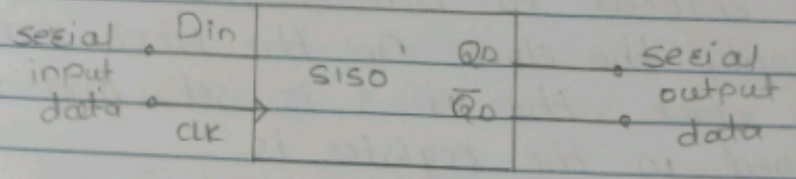
unstable or uncertain. This problem is called as race around condition in JK flip-flop.
- Using Master slave JK Flip-Flop, the race around condition can be avoided, it is



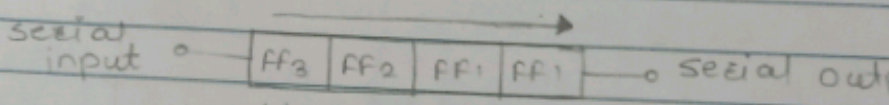
- the master slave Flip-Flop is constructed using two JK Flip Flops. The first Flip Flop is called as master Flip-Flop and the 2nd is called as slave. Both are positive edge triggered. The output of the master is connected to the slave Flip-Flop directly.
- In addition to these two Flip Flops, the circuit also includes an inverter. The inverter is connected to the clock pulse in such a way that the inverted clock pulse is given to the slave Flip-Flop. In other words if CP=1 for a master then CP=0 for a slave and if CP=0 for a master then CP=1 for a slave
- This makes the arrangement such that when master then is active that time slave is not active.

Que 3 with a neat diagram explain the operation of 4-bit SISO Register. Draw the timing diagramand give its truth table.

⇒ (I) logic symbol and Input-output flow diagram.

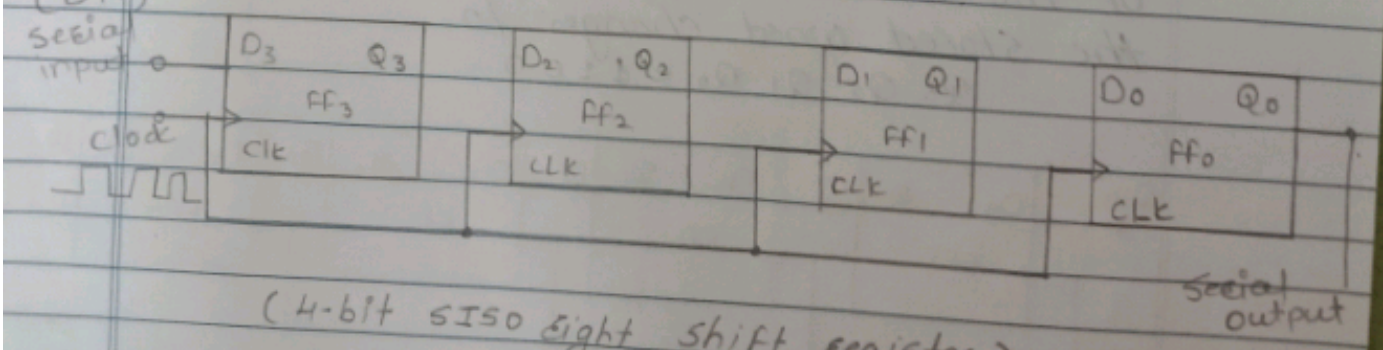


(a) logic symbol



(b) Flow diagram.

- As the name suggests the data enters into the shift register serially (one by one) and the output is also obtained serially.
- Number of FFs depending upon how many bits we want to store. As FF can store only one bit of information to store 4-bits, need 4 FFs, or to store 3 bits. uses 3 FFs & so on.

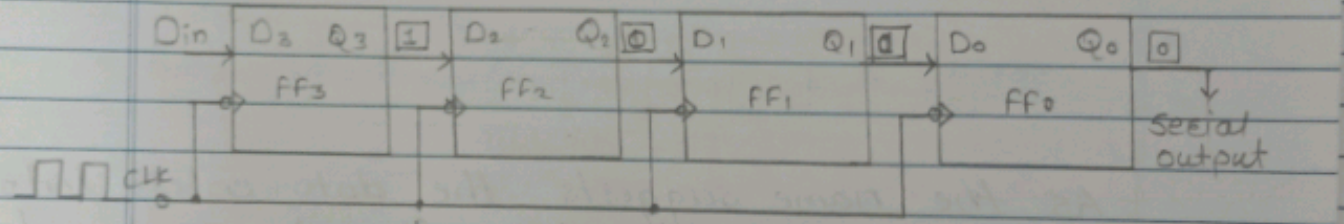


(4-bit SISO Right shift register)

- This operation contains of two parts
1) loading the data
2) shifting the data.

i) - Before application of clock signal let $Q_3Q_2Q_1Q_0 = 0000$ and apply LSB bit to the number to be entered to Din so $Din = D_3 = 1$
- Apply the clock. On the first falling edge of clock, the FF-3 is set, and the stored word in the register is,

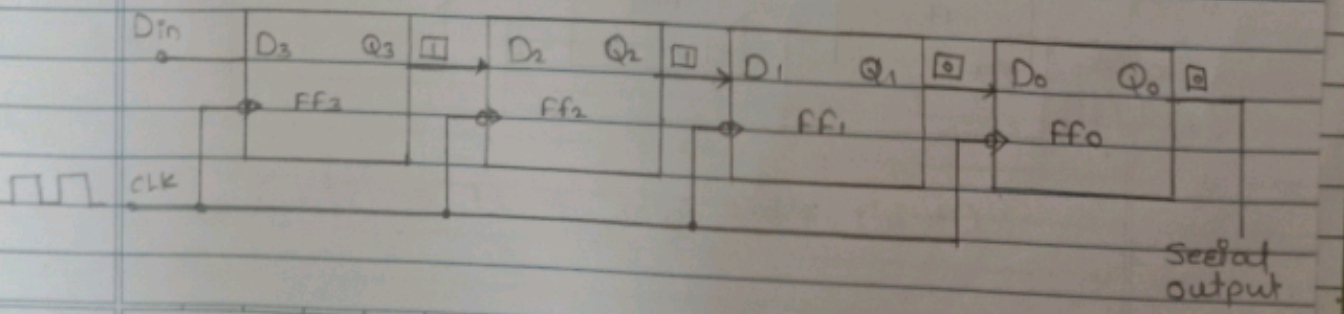
$Q_3\ Q_2\ Q_1\ Q_0 = 1000$



- The shift register after the application of the first clock pulse is as shown in fig.
- Apply the next bit to Din. So $Din = 1$.

ii) As soon as the next negative edge of the clock is applied, FF-2 will set and the stored word changes to,

$Q_3\ Q_2\ Q_1\ Q_0 = 1100$



- Apply the next bit to be stored. 1 to Din.
- Apply the clock pulse. As soon as the third negative clock edge gets applied, FF-1 will be set and the output get modified to.

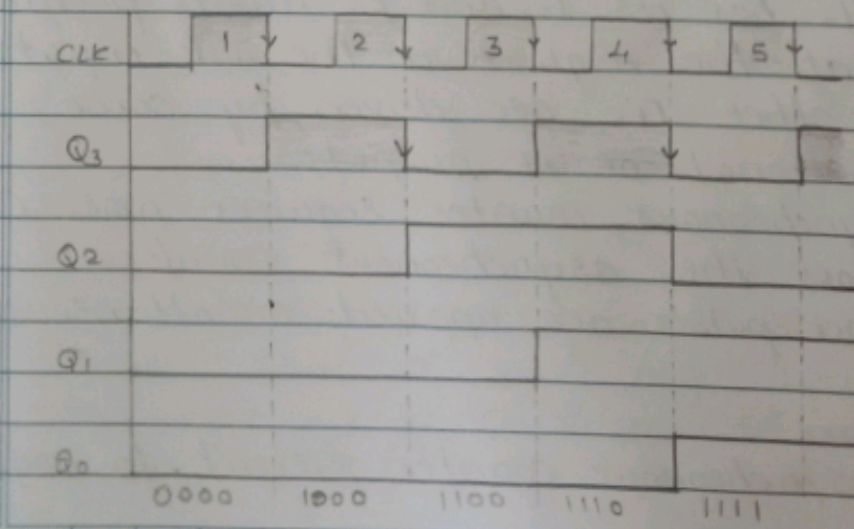
$Q_3\ Q_2\ Q_1\ Q_0 = 1110$

- Similarly with Din = 1 and with the fourth -ve clock edge arriving, the stored word in the register is

$Q_3\ Q_2\ Q_1\ Q_0 = 1111$

	CLK	$D_{in} = D_3$	$Q_3 = D_2$	$Q_2 = D_1$	$Q_1 = D_0$	Q_0
Initially			0	0	0	0
1st	↓	1	1	0	0	0
2nd	↓	1	1	1	0	0
3rd	↓	1	1	1	1	0
4th	↓	1	1	1	1	1

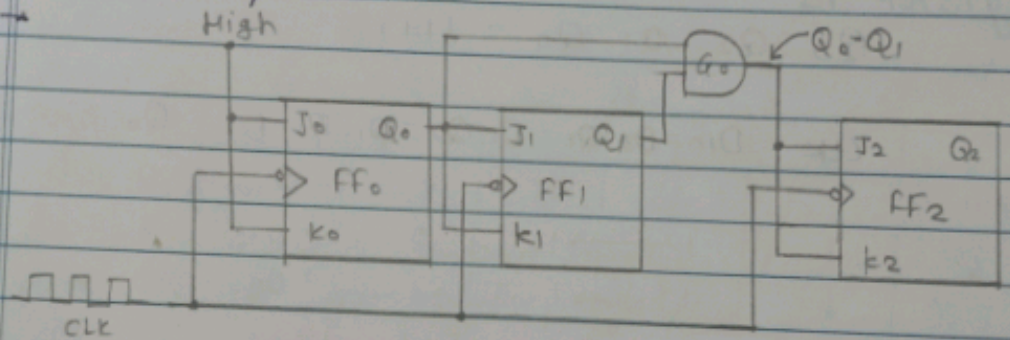
Timing diagram.



Que4 Write a note on MOD-8 Synchronous up-counter using TFF.

⇒ - 4 bit counter the number of states are $N = 2^n = 2^3 = 8$. So it is MOD-8 Counter. The three bit Counter requires 3 FFs.

- The counting sequence in a 3-bit up counter is 0, 1, 2, 3, 4, 5, 6, 0 .... That is counter repeats after 8 clock pelets.



- The clk inputs of all of the FFs are connected together so that the input clock signal is applied to each FF simultaneously.
- Only, FF_0, has its J_0 and K_0 inputs permanently at the High level. The J,K inputs of the other FFs are driven by some Combinational of FF outputs.
- The Synchronous counter requires more circuitry than does the asynchronous counter.
- The clock pulses are applied simultaneously to all FFs.

• operation

- 3 bit Synchronous counter circuit, to count

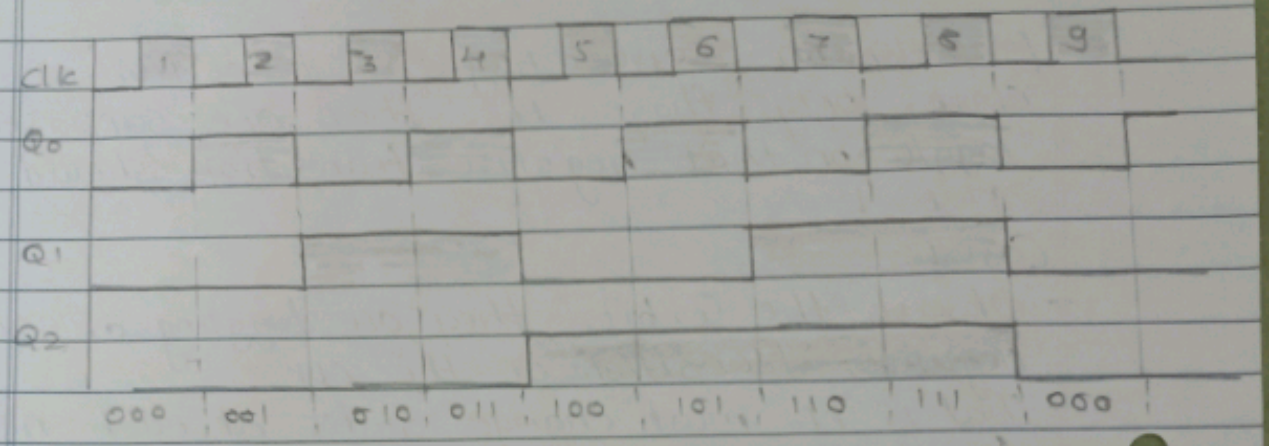
Page No.
Date:

properly on a given negative transition of the clock, only those FFs that are supposed to toggle on that negative transition should have $J = K = 1$

Case 1.
- Observe the Q_0 bits, they are toggling at each negative transition of the CLK.
- That is FF_0 must change states at each negative transition of CLK. For this reason, its J_0 & K_0 inputs are permanently HIGH(1) so that it will toggle on each negative transition of CLK

Case 2.
- The counting sequence shows that FF1 must change states on each negative transition of CLK that occurs while $Q_0 = 1$
- This operation is accomplished by connecting output Q_0 to the J_1 & K_1 inputs of FF_1 so that $J_1 = K_1 = 1$ only when $Q_0 = 1$

Case 3.
- The counting sequence shows that FF_2 must change states on each negative transition of CLK that occurs while $Q_0 = Q_1 = 1$
- By connecting logic signal $Q_0 \cdot Q_1$ to FF_2 J_2 & K_2 inputs, this FF_2 will toggle only when $Q_0 = Q_1 = 1$ The logic signal $Q_0 \cdot Q_1$ is obtained by ~~AND~~ adding 2 inputs Q_0 & Q_1 using AND gate (4).



Ques Compare Moore & Mealy Circuits.

Moore Model	Mealy model.
i) it is sequential circuit. Its output depends on the present state of the Flip-Flops $z(t) = g[s(t)]$	i) It is a sequential circuit Its output depends on the present state of the Flip Flop and also the external I/P $z(t) = g[s(t), x(t)]$
ii) Changes in the input do not affect the output	ii) Input changes may affect the output of the circuit.
iii) it requires more no of States for implementing the same function.	iii) it requires less no of States for implementing same function
iv) They require more circuitry to decide the output	iv) These machines react faster to input There is no delay.