REPORT

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1. 16-line to 4-line 우선순위 인코더를 설계하려고 한다.
(Active-HIGH Input, Active-HIGH output)

① 진리표 (Truth Table)

A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	O_3	O_2	O_1	O_0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
X	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
X	X	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
X	X	X	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
X	X	X	X	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
X	X	X	X	X	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1
X	X	X	X	X	X	1	0	0	0	0	0	0	0	0	0	0	1	1	0
X	X	X	X	X	X	X	1	0	0	0	0	0	0	0	0	0	1	1	1
X	X	X	X	X	X	X	X	1	0	0	0	0	0	0	0	1	0	0	0
X	X	X	X	X	X	X	X	X	1	0	0	0	0	0	0	1	0	0	1
X	X	X	X	X	X	X	X	X	X	1	0	0	0	0	0	1	0	1	0
X	X	X	X	X	X	X	X	X	X	X	1	0	0	0	0	1	0	1	1
X	X	X	X	X	X	X	X	X	X	X	X	1	0	0	0	1	1	0	0
X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	0	1	1	0	1
X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	1	1	1	0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1	1	1

② 각 출력의 간략화한 대수식

※ 방법: 각 output 마다 1이 되는 부분에서 A_i 가 인 부분 위의 0을 지우고 대수식을 구한다.

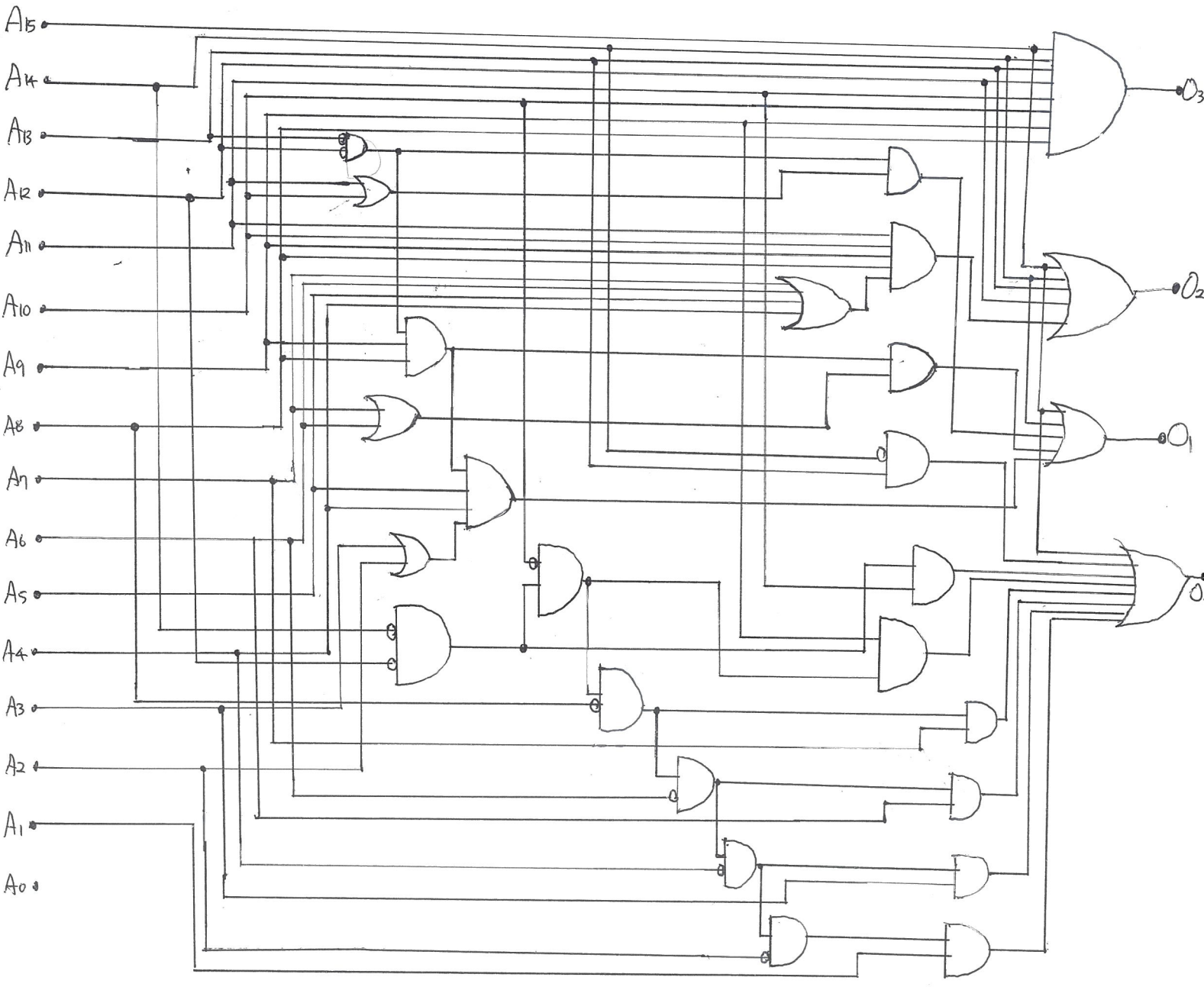
$$O_3 = A_{15} + A_{14} + A_{13} + A_{12} + A_{11} + A_{10} + A_9 + A_8$$

$$O_2 = A_{15} + A_{14} + A_{13} + A_{12} + (\overline{A_{11}} \cdot \overline{A_{10}} \cdot \overline{A_9} \cdot \overline{A_8})(A_7 + A_6 + A_5 + A_4)$$

$$O_1 = A_{15} + A_{14} + (\overline{A_{13}} \cdot \overline{A_{12}})(A_{11} + A_{10}) + (\overline{A_{13}} \cdot \overline{A_{12}} \cdot \overline{A_9} \cdot \overline{A_8})(A_7 + A_6) + (\overline{A_{13}} \cdot \overline{A_{12}} \cdot \overline{A_9} \cdot \overline{A_8} \cdot \overline{A_5} \cdot \overline{A_4})(A_3 + A_2)$$

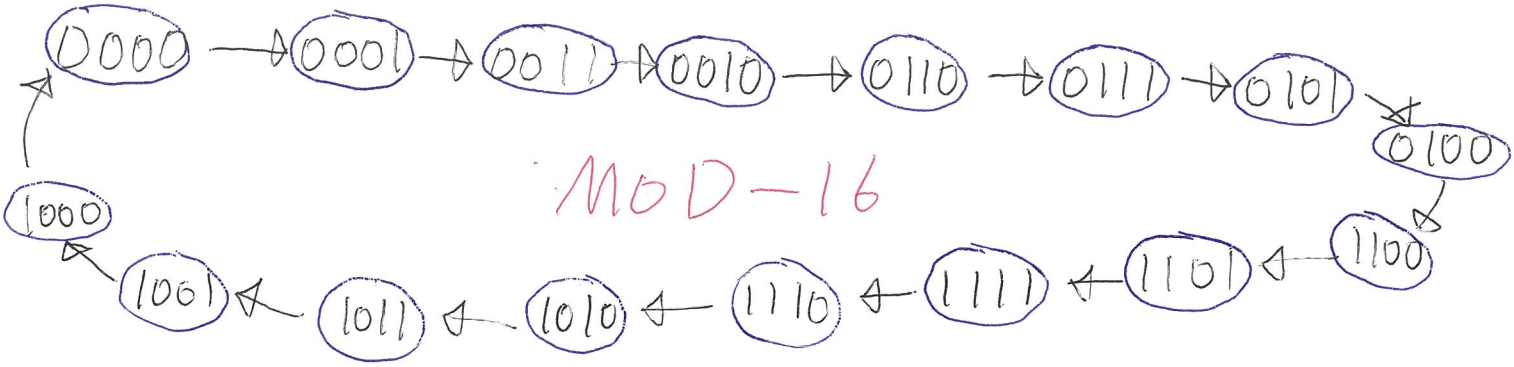
$$O_0 = A_{15} + \overline{A_{14}} \cdot A_{13} + \overline{A_{14}} \cdot \overline{A_{12}} \cdot A_{11} + \overline{A_{14}} \cdot \overline{A_{12}} \cdot \overline{A_{10}} \cdot A_9 + \overline{A_{14}} \cdot \overline{A_{12}} \cdot \overline{A_{10}} \cdot \overline{A_8} \cdot A_7 + \overline{A_{14}} \cdot \overline{A_{12}} \cdot \overline{A_{10}} \cdot \overline{A_8} \cdot \overline{A_6} \cdot A_5 + \overline{A_{14}} \cdot \overline{A_{12}} \cdot \overline{A_{10}} \cdot \overline{A_8} \cdot \overline{A_6} \cdot \overline{A_4} \cdot A_3 + \overline{A_{14}} \cdot \overline{A_{12}} \cdot \overline{A_{10}} \cdot \overline{A_8} \cdot \overline{A_6} \cdot \overline{A_4} \cdot \overline{A_2} \cdot A_1$$

③ 회로도



2. 4-bit Gray Code 순서를 순환하는 MOD16 동기식 카운터회로를 JK 플립플롭을 이용하여 설계하고자 한다.

① 상태변화도 (State Transition Diagram)



② Excitation Table을 포함한 현재상태/다음상태표

<현재> D	C	B	A	J_D	K_D	J_C	K_C	J_B	K_B	J_A	K_A	<다음> D	C	B	A
0	0	0	0	0	X	0	X	0	X	1	X	0	0	0	1
0	0	0	1	0	X	0	X	1	X	X	0	0	0	1	1
0	0	1	0	0	X	1	X	X	0	0	X	0	1	1	0
0	0	1	1	0	X	0	X	X	0	X	1	0	0	1	0
0	1	0	0	1	X	X	0	0	X	0	X	1	1	0	0
0	1	0	1	0	X	X	0	0	X	X	1	0	1	0	0
0	1	1	0	0	X	X	0	X	0	1	X	0	1	1	1
0	1	1	1	0	X	X	0	X	1	X	0	0	1	0	1
1	0	0	0	X	1	0	X	0	X	0	X	0	0	0	0
1	0	0	1	X	0	0	X	0	X	X	1	1	0	0	0
1	0	1	0	X	0	0	X	X	0	1	X	1	0	1	1
1	0	1	1	X	0	0	X	X	1	X	0	1	0	0	1
1	1	0	0	X	0	X	0	0	X	1	X	1	1	0	1
1	1	0	1	X	0	X	0	1	X	X	0	1	1	1	1
1	1	1	0	X	0	X	0	X	0	0	X	1	0	1	0
1	1	1	1	X	0	X	1	X	0	X	1	1	1	1	0

③ 각 제어입력의 간략화한 대수식

J_D

DC \ BA	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	X	X	X	X
10	X	X	X	X

$J_D = C\overline{B}\,\overline{A}$

K_D

DC \ BA	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	0	0	0
10	1	0	0	0

$K_D = \overline{C}\,\overline{B}\,\overline{A}$

J_C

DC \ BA	00	01	11	10
00	0	0	0	1
01	X	X	X	X
11	X	X	X	X
10	0	0	0	0

$J_C = \overline{D}\,B\overline{A}$

K_C

DC \ BA	00	01	11	10
00	X	X	X	X
01	0	0	0	0
11	0	0	0	1
10	X	X	X	X

$K_C = DB\overline{A}$

J_B

DC \ BA	00	01	11	10
00	0	1	X	X
01	0	0	X	X
11	0	1	X	X
10	0	0	X	X

$J_B = DC\overline{A} + \overline{D}\,\overline{C}A$
$= (D \oplus C)\cdot A$

K_B

DC \ BA	00	01	11	10
00	X	X	0	0
01	X	X	1	0
11	X	X	0	0
10	X	X	1	0

$K_B = \overline{D}CA + D\overline{C}A$
$= (D \oplus C)\cdot A$

J_A

DC \ BA	00	01	11	10
00	1	X	X	0
01	0	X	X	1
11	1	X	X	0
10	0	X	X	1

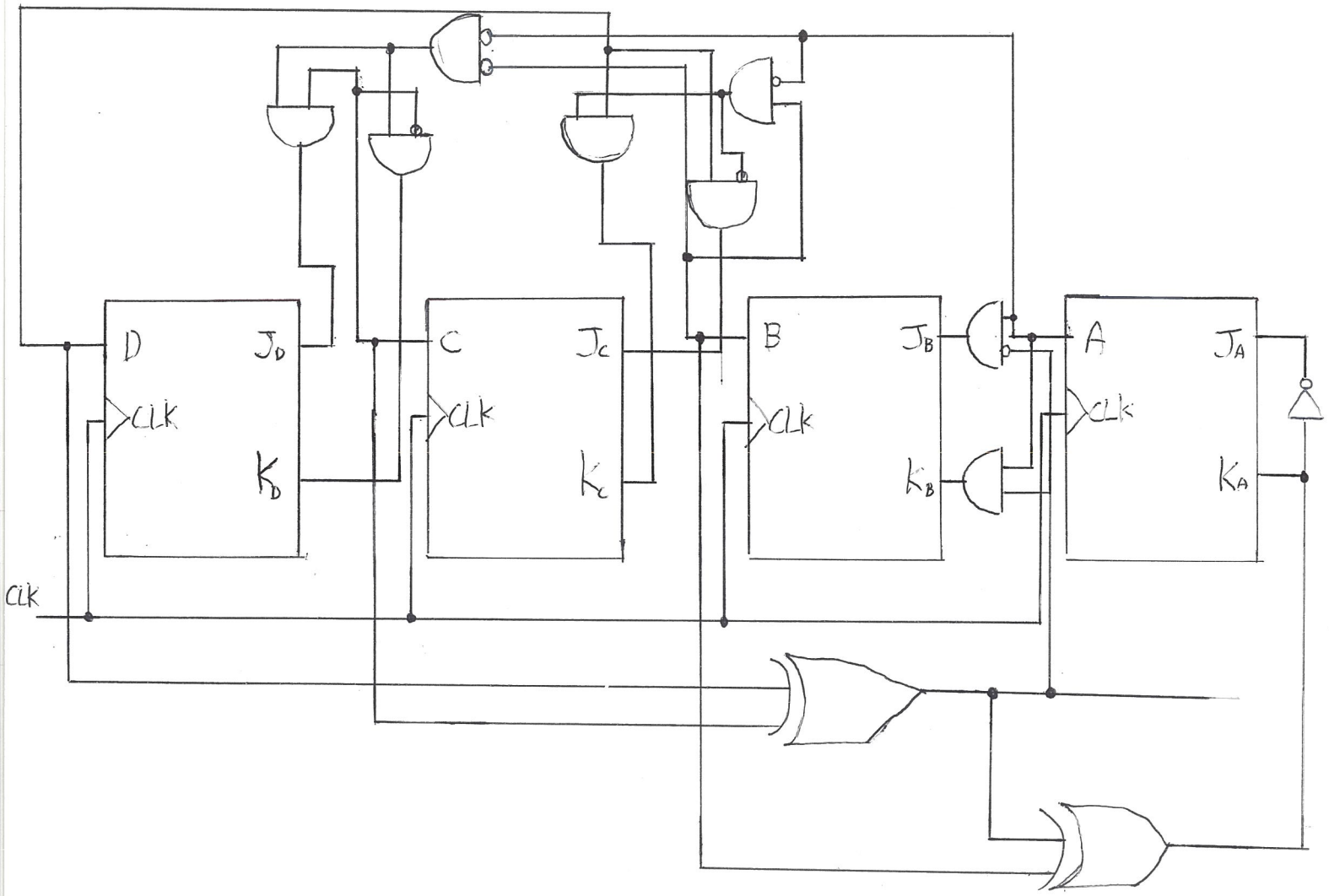
$J_A = \overline{D}\,\overline{C}B + \overline{D}CB + DC\overline{B} + D\overline{C}B$
$= (\overline{D \oplus C})\,\overline{B} + (D \oplus C)\,B$
$= \overline{(D \oplus C) \oplus B}$

K_A

DC \ BA	00	01	11	10
00	X	0	1	X
01	X	1	0	X
11	0	X	1	X
10	X	1	0	X

$K_A = \overline{D}\,\overline{C}B + \overline{D}\,C\overline{B} + DCB + D\overline{C}\,\overline{B}$
$= (\overline{D \oplus C})\cdot B + (D \oplus C)\cdot \overline{B}$
$= (D \oplus C) \oplus B$

④ 회로도



2. 해밍코드 인코딩/디코딩 회로를 설계하고자 한다. (7 bit ⟷ 11 bit)

*

	P_3	P_2	P_1	P_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1

*

I_1 I_2 I_3 I_4 I_5 I_6 I_7

(1) (2) 3 (4) 5 6 7 (8) 9 10 11

2^0 2^1 2^2 2^3

① 7 bit → 11 bit 해밍코드 인코더

1) 대수식

$O_1 = I_1 \oplus I_2 \oplus I_4 \oplus I_5$

$O_2 = I_1 \oplus I_3 \oplus I_4 \oplus I_6$

$O_3 = I_1$

$O_4 = I_2 \oplus I_3 \oplus I_4$

$O_5 = I_2$

$O_6 = I_3$

$O_7 = I_4$

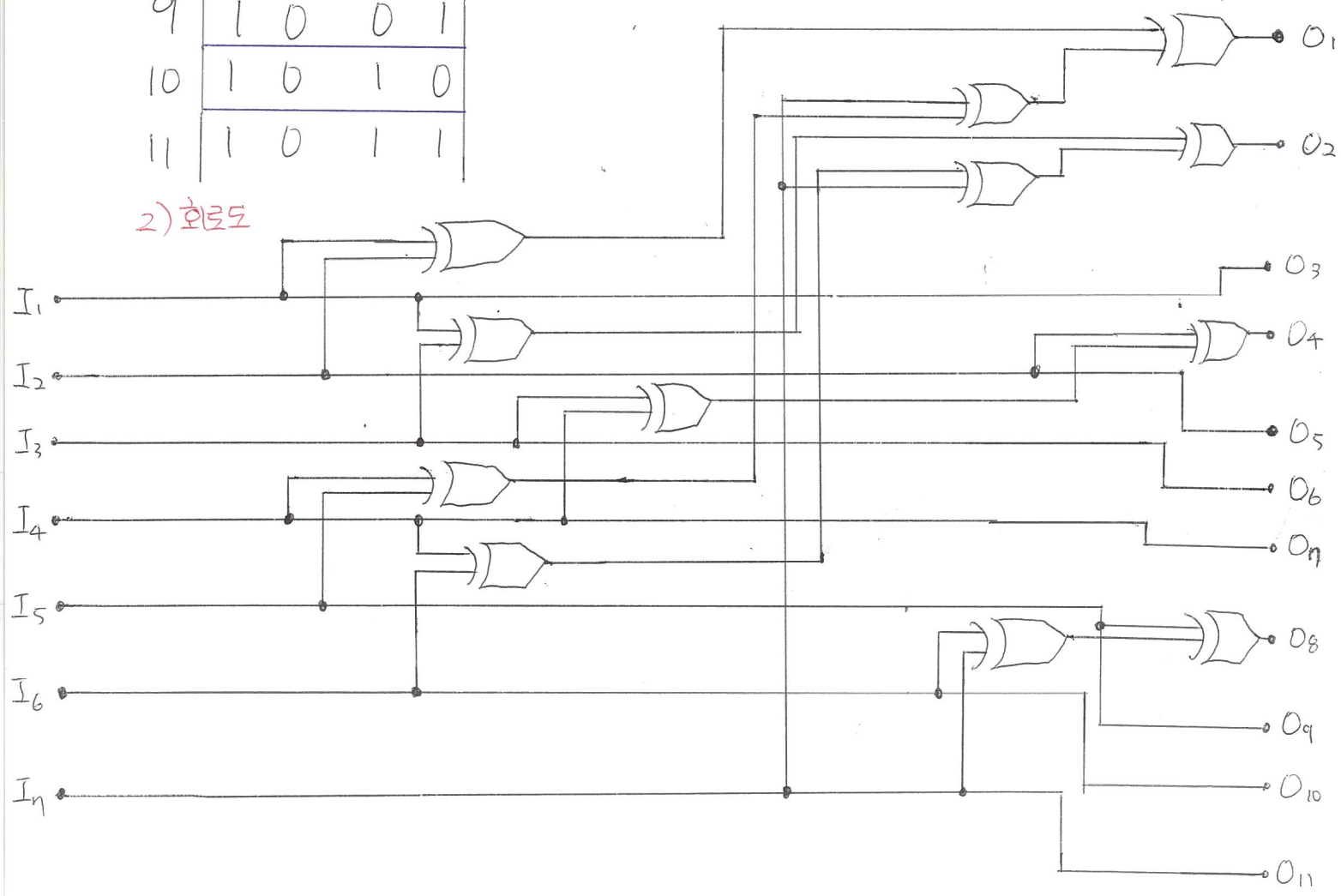
$O_8 = I_5 \oplus I_6 \oplus I_7$

$O_9 = I_5$

$O_{10} = I_6$

$O_{11} = I_7$

2) 회로도



② 11 bit → 7 bit 해밍코드 디코더

1) 대수식

$$D_0 = I_1 \oplus I_3 \oplus I_5 \oplus I_7 \oplus I_9 \oplus I_{11}$$
$$D_1 = I_2 \oplus I_3 \oplus I_6 \oplus I_7 \oplus I_{10} \oplus I_{11}$$
$$D_2 = I_4 \oplus I_5 \oplus I_6 \oplus I_7$$
$$D_3 = I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}$$
$$error = D_3 + D_2 + D_1 + D_0$$

$$O_1 = I_3 \oplus (\overline{D_3} \cdot \overline{D_2} \cdot \overline{D_1} \cdot \overline{D_0})$$
$$O_2 = I_5 \oplus (\overline{D_3} \cdot D_2 \cdot \overline{D_1} \cdot D_0)$$
$$O_3 = I_6 \oplus (\overline{D_3} \cdot D_2 \cdot D_1 \cdot \overline{D_0})$$
$$O_4 = I_7 \oplus (\overline{D_3} \cdot D_2 \cdot D_1 \cdot D_0)$$
$$O_5 = I_9 \oplus (D_3 \cdot \overline{D_2} \cdot \overline{D_1} \cdot D_0)$$
$$O_6 = I_{10} \oplus (D_3 \cdot \overline{D_2} \cdot D_1 \cdot \overline{D_0})$$
$$O_7 = I_{11} \oplus (D_3 \cdot \overline{D_2} \cdot D_1 \cdot D_0)$$

2) 회로도