Assignment 3 (Solutions)

- The report is to be submitted on Moodle using a pdf format.
- **You must write the following statement on the report: "I certify that this submission is my original work and meets the Faculty's Expectations of Originality", with your signature, I.D. #, and the date.**
- **In case your response is suspected to have been copied from other sources (such as Internet websites or classmates), you will be reported.**

Solve the following problems:

We study how bypassing affects program execution performance. We first consider the standard MIPS 5-stage pipeline, for which the load use latency is 1 cycle **(load use latency of 1 cycle means there is a BYPASS wire from the memory stage to the execute stage: the BYPASS allows to forward a data from MEM to EX but there is a 1 cycle delay - cf slides 53 and 56 from Lec08)**. The following code is used to evaluate the pipeline's performance:

```
1   add $t2, $s1, $sp
2   lw $t1, $t1, 0
3   addi $t2, $t1, 7
4   add $t1, $s2, $sp
5   lw $t1, $t1, 0
6   addi $t1, $t1, 9
7   sub $t1, $t1, $t2
```

a. Using the standard MIPS pipeline, identify whether the value for each register operand is coming from the bypass or from the register file. For clarity, please write REGISTER FILE or BYPASS in each box.

Instruction	Src Operand 1	Src Operand 2
1	Register File	Register File
2	Register File	N/A
3	Bypass	N/A
4	Register File	Register File
5	Bypass	N/A
6	Bypass	N/A
7	Bypass	Register File

b. How many cycles will the program take to execute on the standard MIPS pipeline?

It takes 13 cycles to execute on the standard MIPS pipeline.

c. Assume, due to circuit constraints, that the bypass wire from the memory stage back to the execute stage is omitted from the pipeline. What is the load-use latency for this modified pipeline?
The load use latency for this pipeline is 2 cycles.

d. Identify whether the value for each register operand is coming from the bypass or from the register file for the modified pipeline. For clarity, please write REGISTER FILE or BYPASS in each box.

Instruction	Src Operand 1	Src Operand 2
1	Register File	Register File
2	Register File	N/A
3	Register File	N/A
4	Register File	Register File
5	Bypass	N/A
6	Register File	N/A
7	Bypass	Register File

e. How **many cycles** does the program take to execute on the modified pipeline?
It takes 15 cycles to execute on the modified pipeline.

1. **Branch Prediction**. Consider the following sequence of actual outcomes for a single static branch. T means the branch is taken. N means the branch is not taken. For this question, assume that this is the only branch in the program.

   Outcomes: T T T N T N T T T N T N T T T N T N

   a. Assume that we try to predict this sequence with a BHT (Branch History Table) using one-bit counters. The counters in the BHT are initialized to the N state. Which of the branches in this sequence would be mis-predicted? You may use this table for your answer.

Predictor state before prediction	Branch outcome	Mis-prediction
N	T	Y
	T	N
	T	N
	N	Y
	T	Y

	N	Y
	T	Y
	T	N
	T	N
	N	Y
	T	Y
	N	Y
	T	Y
	T	N
	T	N
	N	Y
	T	Y
	N	Y

b. Now, assume a **2-bit predictor (cf slide 72 in the lecture 08)**. **Assume that all entries are initialized to the N state and that all previous branches were not taken.** Which of the branches in this sequence would be mis-predicted? Use the table below.

Predictor state before prediction	**Branch outcome**	**Mis-prediction**
N	T	Y
	T	Y
	T	N
	N	Y
	T	N
	N	N
	T	N
	T	Y
	T	N
	N	Y
	T	N
	N	N
	T	N
	T	Y
	T	N
	N	Y

	T	N
	N	N

c. What is a return-address-stack? When is a return address stack updated?
A return address stack is a hardware mechanism used to predict the target of return-from-function call instructions. The return address stack is updated after either a call instruction or a return instruction is predicted.