Report

on

COEN 316 Laboratory Experiment #1

**Arithmetic and Logic Unit**

Submitted to

*SEYED AMIRREZA MOUSAVI*

*Instructor’s name*

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By

Jasen Ratnam 40094237

Name student ID

Lab section: DI-X

“I certify that this submission is my original work and meets the Faculty's Expectations of Originality”

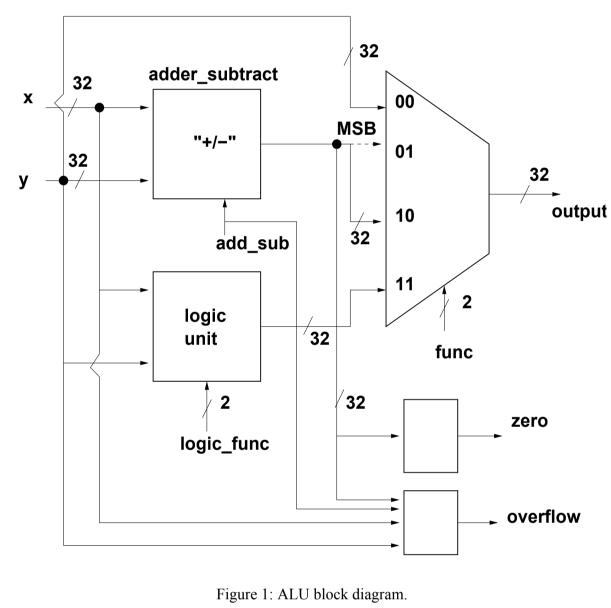


40094237 15/10/2020

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# **Objective:**

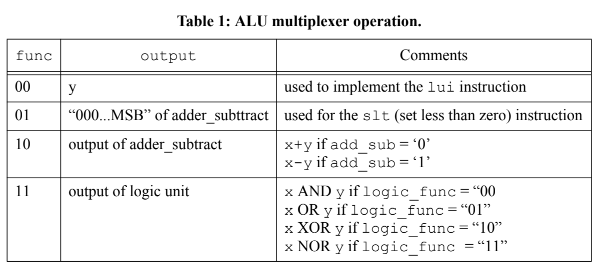
In this lab, we will use digital logic simulation and synthesis using Modelsim, and Xilinx ISE (Vivado) to become acquainted with the VHDL simulation software tool and FPGA implementation software tools. During this lab, we will simulate a 32-bit ALU design and implement it virtually. The ALU will be designed based on the figure below.



**Introduction:**

An arithmetic logic unit (ALU) is the digital circuit used to perform arithmetic and logic operations on a computer. This Lab consists of designing an ALU. The ALU will be used in the other labs to design components of a CPU.

The ALU design will have two 32-bit input operands, control inputs: func, logic\_func and add\_sub, and a 32-bit output port. These inputs control the operations that the ALU does on the operands x & y, the table below shows how different inputs affect the operations done. The ALU will also be designed to set the zero and overflow flags after every operation.



**Results:**

The complete VHDL code source for the ALU

| **library** IEEE; **use** IEEE.std\_logic\_1164.**all**; **use** IEEE.std\_logic\_unsigned.**all**;  **entity** alu **is** **port**(x, y : **in** std\_logic\_vector(31 **downto** 0); *-- two input operands* add\_sub : **in** std\_logic ; *-- 0 = add , 1 = sub* logic\_func : **in** std\_logic\_vector(1 **downto** 0 ) ; *-- 00 = AND, 01 = OR , 10 = XOR , 11 = NOR* func : **in** std\_logic\_vector(1 **downto** 0 ) ; *-- 00 = lui, 01 = setless , 10 = arith , 11 = logic* output : **out** std\_logic\_vector(31 **downto** 0) ; overflow : **out** std\_logic ; zero : **out** std\_logic); **end** alu ;  **architecture** alu\_arch **of** alu **is** **signal** add\_sub\_out,logic\_out : std\_logic\_vector(31 **downto** 0); **begin** *--add and subtractor unit* adder\_subtract: **process**(x,y,add\_sub) **begin** **case** add\_sub **is**  **when** '0' =>  add\_sub\_out <=x+y;  **when** '1' =>  add\_sub\_out <=x-y;  **when** **others** =>  **NULL**; **end** **case**; **end** **process**;  *--logic* logic\_unit: **process**(x,y,logic\_func) **begin**  **case** logic\_func **is**  **when** "00" =>  logic\_out <= x **and** y; *--AND gate*  **when** "01" =>  logic\_out <= x **or** y; *--or gate*  **when** "10" =>  logic\_out <= x **xor** y; *--xor gate*  **when** "11" =>  logic\_out<= x **nor** y; *-- NOR gate*  **when** **others** =>  **NULL**;  **end** **case**; **end** **process**;  *--multiplexer* multiplexer\_unit: **process**(add\_sub\_out,logic\_out,func) **begin**  **case** func **is**  **when** "00" =>  output <= y;  **when** "01" =>  **if** x < y **then**  output <= (0 => '1', **others** => '0');  **else**  output <= (0 => '0', **others** => '0');  **end** **if**;  **when** "10" =>  output<= **NOT** add\_sub\_out;  **when** "11" =>  output<= **NOT** logic\_out;  **when** **others** =>  **NULL**;  **end** **case**; **end** **process**;  *--zero* zero\_out\_unit: **process**(add\_sub\_out) **begin**  **if** add\_sub\_out = 0 **then**  zero <= '1';  **else**  zero <= '0';  **end** **if**; **end** **process**;   *--overflow* overflow\_unit: **process**(add\_sub\_out) **begin**  **case** add\_sub **is**   **when** '0' =>  **if** x(31) = '0' **and** y(31) = '0' **and** add\_sub\_out(31) = '1' **then**  overflow <= '1';  **elsif** x(31) = '1' **and** y(31) = '1' **and** add\_sub\_out(31) = '0' **then**  overflow <= '1';  **else**  overflow <= '0';  **end** **if**;  **when** '1' =>  **if** x(31) = '0' **and** y(31) = '1' **and** add\_sub\_out(31) = '1' **then**  overflow <= '1';  **elsif** x(31) = '1' **and** y(31) = '0' **and** add\_sub\_out(31) = '0' **then**  overflow <= '1';  **else**  overflow <= '0';  **end** **if**;  **when** **others** =>  **NULL**;  **end** **case**; **end** **process**;  **end** alu\_arch; |
| --- |

Xilinx XDC file:

| # Vivado does not support old UCF syntax  # must use XDC syntax  # input ports A,B,C,D,E are left unspecified  # of the Nexys board  # output port F,G,H is left unspecified  # we use the set\_property IOSTANDARD LVCMOS33 to eliminate  # the error during bitgen about unspecified IOSTANDARD  # without bothering to specify any mapping of ports to pins  # since we will not be downloading to the FPGA board  # XDC file for ALUcircuit.vhd  set\_property IOSTANDARD LVCMOS33 [ get\_ports { A } ] ;  set\_property IOSTANDARD LVCMOS33 [ get\_ports { B } ] ;  set\_property IOSTANDARD LVCMOS33 [ get\_ports { C } ] ;  set\_property IOSTANDARD LVCMOS33 [ get\_ports { D } ] ;  set\_property IOSTANDARD LVCMOS33 [ get\_ports { E } ] ;  set\_property IOSTANDARD LVCMOS33 [ get\_ports { F } ] ;  set\_property IOSTANDARD LVCMOS33 [ get\_ports { G } ] ;  set\_property IOSTANDARD LVCMOS33 [ get\_ports { H } ] ; |
| --- |

The TCL script file:

| # TCL script **for** running vivado **in** batch mode **to** synthesize # read **in** the VHDL source code files **and** the xdc constraints **file**  set\_property **SEVERITY** {Warning} [get\_drc\_checks UCIO-1]  read\_vhdl { ../Code/ALU.vhd ../Code/ALUcircuit.vhd } read\_xdc ALUcircuit.xdc  # the -top refers **to** the top level VHDL **entity** name # the -part specfies the target Xilinx FPGA  synth\_design -top ALUcircuit -part xc7a100tcsg324-1  opt\_design place\_design route\_design  # **generate** the bitsteam **file** write\_bitstream -**force** ALUcircuit.bit |
| --- |

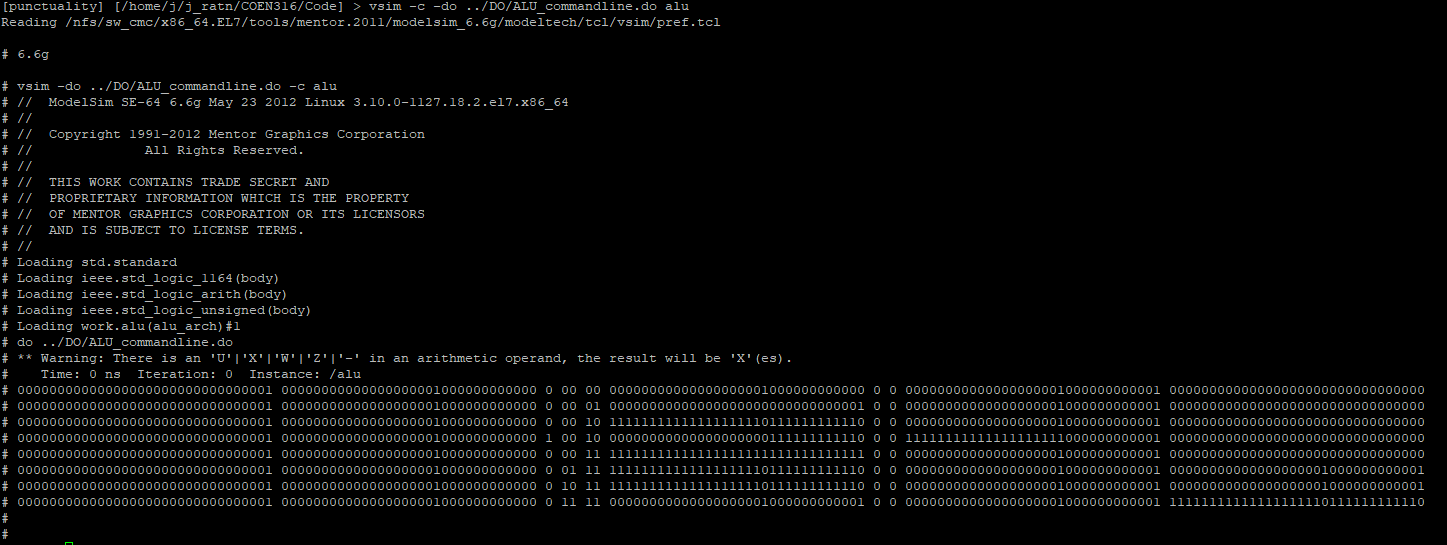
The DO file:

| **force** x X"00000001"  **force** y X"00001000"  **force** add\_sub 0 **force** logic\_func 00 **force** func 00  run 2  examine \*   **force** x X"00000001" **force** y X"00001000" **force** add\_sub 0 **force** logic\_func 00 **force** func 01  run 2 examine \*   **force** x X"00000001" **force** y X"00001000" **force** add\_sub 0 **force** logic\_func 00 **force** func 10  run 2 examine \*   **force** x X"00000001" **force** y X"00001000" **force** add\_sub 1 **force** logic\_func 00 **force** func 10  run 2 examine \*  **force** x X"00000001" **force** y X"00001000" **force** add\_sub 0 **force** logic\_func 00 **force** func 11  run 2 examine \*  **force** x X"00000001" **force** y X"00001000" **force** add\_sub 0 **force** logic\_func 01 **force** func 11  run 2 examine \*   **force** x X"00000001" **force** y X"00001000" **force** add\_sub 0 **force** logic\_func 10 **force** func 11  run 2 examine \*   **force** x X"00000001" **force** y X"00001000" **force** add\_sub 0 **force** logic\_func 11 **force** func 11  run 2 examine \* |
| --- |

The log file is available in the appendix.

**Simulation and implementation results using port maps:**

* The Modelsim simulation



**Conclusion:**

In conclusion, the experiment was done correctly since the results obtained are accurate compared to the theoretical results. We learned and understood all the steps to do a simulation of an ALU design.

**Appendix:**

The log file:

#-----------------------------------------------------------

# Vivado v2018.2 (64-bit)

# SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018

# IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018

# Start of session at: Thu Oct 15 20:32:33 2020

# Process ID: 26449

# Current directory: /nfs/home/j/j\_ratn/COEN316/ALUCIRCUIT\_SCRIPT

# Command line: vivado -log ALUcircuit.log -mode batch -source ALUcircuit\_script.tcl

# Log file: /nfs/home/j/j\_ratn/COEN316/ALUCIRCUIT\_SCRIPT/ALUcircuit.log

# Journal file: /nfs/home/j/j\_ratn/COEN316/ALUCIRCUIT\_SCRIPT/vivado.jou

#-----------------------------------------------------------

source ALUcircuit\_script.tcl

# set\_property SEVERITY {Warning} [get\_drc\_checks UCIO-1]

# read\_vhdl { ../Code/ALU.vhd ../Code/ALUcircuit.vhd }

# read\_xdc ALUcircuit.xdc

# synth\_design -top ALUcircuit -part xc7a100tcsg324-1

Command: synth\_design -top ALUcircuit -part xc7a100tcsg324-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 26587

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Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1468.184 ; gain = 86.727 ; free physical = 109995 ; free virtual = 158778

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INFO: [Synth 8-638] synthesizing module 'ALUcircuit' [/nfs/home/j/j\_ratn/COEN316/Code/ALUcircuit.vhd:13]

INFO: [Synth 8-3491] module 'alu' declared at '/nfs/home/j/j\_ratn/COEN316/Code/ALU.vhd:6' bound to instance 'U1' of component 'alu' [/nfs/home/j/j\_ratn/COEN316/Code/ALUcircuit.vhd:31]

INFO: [Synth 8-638] synthesizing module 'alu' [/nfs/home/j/j\_ratn/COEN316/Code/ALU.vhd:19]

INFO: [Synth 8-226] default block is never used [/nfs/home/j/j\_ratn/COEN316/Code/ALU.vhd:25]

INFO: [Synth 8-226] default block is never used [/nfs/home/j/j\_ratn/COEN316/Code/ALU.vhd:38]

INFO: [Synth 8-226] default block is never used [/nfs/home/j/j\_ratn/COEN316/Code/ALU.vhd:55]

WARNING: [Synth 8-614] signal 'y' is read in the process but is not in the sensitivity list [/nfs/home/j/j\_ratn/COEN316/Code/ALU.vhd:53]

WARNING: [Synth 8-614] signal 'x' is read in the process but is not in the sensitivity list [/nfs/home/j/j\_ratn/COEN316/Code/ALU.vhd:53]

INFO: [Synth 8-226] default block is never used [/nfs/home/j/j\_ratn/COEN316/Code/ALU.vhd:88]

WARNING: [Synth 8-614] signal 'add\_sub' is read in the process but is not in the sensitivity list [/nfs/home/j/j\_ratn/COEN316/Code/ALU.vhd:86]

WARNING: [Synth 8-614] signal 'x' is read in the process but is not in the sensitivity list [/nfs/home/j/j\_ratn/COEN316/Code/ALU.vhd:86]

WARNING: [Synth 8-614] signal 'y' is read in the process but is not in the sensitivity list [/nfs/home/j/j\_ratn/COEN316/Code/ALU.vhd:86]

INFO: [Synth 8-256] done synthesizing module 'alu' (1#1) [/nfs/home/j/j\_ratn/COEN316/Code/ALU.vhd:19]

INFO: [Synth 8-256] done synthesizing module 'ALUcircuit' (2#1) [/nfs/home/j/j\_ratn/COEN316/Code/ALUcircuit.vhd:13]

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Finished RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 1512.824 ; gain = 131.367 ; free physical = 110007 ; free virtual = 158790

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Handling Custom Attributes

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---------------------------------------------------------------------------------

Finished Handling Custom Attributes : Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 1512.824 ; gain = 131.367 ; free physical = 110006 ; free virtual = 158789

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 1512.824 ; gain = 131.367 ; free physical = 110006 ; free virtual = 158789

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INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/nfs/home/j/j\_ratn/COEN316/ALUCIRCUIT\_SCRIPT/ALUcircuit.xdc]

Finished Parsing XDC File [/nfs/home/j/j\_ratn/COEN316/ALUCIRCUIT\_SCRIPT/ALUcircuit.xdc]

Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1843.789 ; gain = 0.000 ; free physical = 109747 ; free virtual = 158531

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Finished Constraint Validation : Time (s): cpu = 00:00:13 ; elapsed = 00:00:46 . Memory (MB): peak = 1843.789 ; gain = 462.332 ; free physical = 109820 ; free virtual = 158603

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Start Loading Part and Timing Information

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Loading part: xc7a100tcsg324-1

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:13 ; elapsed = 00:00:46 . Memory (MB): peak = 1843.789 ; gain = 462.332 ; free physical = 109820 ; free virtual = 158603

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Start Applying 'set\_property' XDC Constraints

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:14 ; elapsed = 00:00:46 . Memory (MB): peak = 1843.789 ; gain = 462.332 ; free physical = 109821 ; free virtual = 158605

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INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [/nfs/home/j/j\_ratn/COEN316/Code/ALU.vhd:25]

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:14 ; elapsed = 00:00:46 . Memory (MB): peak = 1843.789 ; gain = 462.332 ; free physical = 109811 ; free virtual = 158596

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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+-+--------------+------------+----------+

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Start RTL Component Statistics

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Detailed RTL Component Info :

+---Adders :

3 Input 32 Bit Adders := 1

+---XORs :

2 Input 32 Bit XORs := 1

+---Muxes :

4 Input 32 Bit Muxes := 2

2 Input 32 Bit Muxes := 1

2 Input 1 Bit Muxes := 3

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Finished RTL Component Statistics

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---------------------------------------------------------------------------------

Start RTL Hierarchical Component Statistics

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Hierarchical RTL Component report

Module alu

Detailed RTL Component Info :

+---Adders :

3 Input 32 Bit Adders := 1

+---XORs :

2 Input 32 Bit XORs := 1

+---Muxes :

4 Input 32 Bit Muxes := 2

2 Input 32 Bit Muxes := 1

2 Input 1 Bit Muxes := 3

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Finished RTL Hierarchical Component Statistics

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---------------------------------------------------------------------------------

Start Part Resource Summary

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Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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Warning: Parallel synthesis criteria is not met

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Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:14 ; elapsed = 00:00:47 . Memory (MB): peak = 1867.070 ; gain = 485.613 ; free physical = 109790 ; free virtual = 158575

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:21 ; elapsed = 00:01:01 . Memory (MB): peak = 1867.070 ; gain = 485.613 ; free physical = 109668 ; free virtual = 158454

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Start Timing Optimization

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Finished Timing Optimization : Time (s): cpu = 00:00:21 ; elapsed = 00:01:01 . Memory (MB): peak = 1867.070 ; gain = 485.613 ; free physical = 109668 ; free virtual = 158454

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:21 ; elapsed = 00:01:01 . Memory (MB): peak = 1867.070 ; gain = 485.613 ; free physical = 109665 ; free virtual = 158451

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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Start IO Insertion

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Start Flattening Before IO Insertion

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Finished Flattening Before IO Insertion

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Start Final Netlist Cleanup

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Finished Final Netlist Cleanup

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Finished IO Insertion : Time (s): cpu = 00:00:22 ; elapsed = 00:01:01 . Memory (MB): peak = 1867.070 ; gain = 485.613 ; free physical = 109665 ; free virtual = 158451

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:22 ; elapsed = 00:01:01 . Memory (MB): peak = 1867.070 ; gain = 485.613 ; free physical = 109665 ; free virtual = 158451

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

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+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:22 ; elapsed = 00:01:01 . Memory (MB): peak = 1867.070 ; gain = 485.613 ; free physical = 109665 ; free virtual = 158451

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:22 ; elapsed = 00:01:01 . Memory (MB): peak = 1867.070 ; gain = 485.613 ; free physical = 109665 ; free virtual = 158451

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:22 ; elapsed = 00:01:01 . Memory (MB): peak = 1867.070 ; gain = 485.613 ; free physical = 109665 ; free virtual = 158451

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:22 ; elapsed = 00:01:01 . Memory (MB): peak = 1867.070 ; gain = 485.613 ; free physical = 109665 ; free virtual = 158451

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Start Writing Synthesis Report

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Report BlackBoxes:

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| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-------+------+

| |Cell |Count |

+------+-------+------+

|1 |CARRY4 | 12|

|2 |LUT1 | 1|

|3 |LUT2 | 3|

|4 |LUT3 | 33|

|5 |LUT4 | 37|

|6 |LUT6 | 71|

|7 |IBUF | 69|

|8 |OBUF | 34|

+------+-------+------+

Report Instance Areas:

+------+---------+-------+------+

| |Instance |Module |Cells |

+------+---------+-------+------+

|1 |top | | 260|

|2 | U1 |alu | 38|

+------+---------+-------+------+

---------------------------------------------------------------------------------

Finished Writing Synthesis Report : Time (s): cpu = 00:00:22 ; elapsed = 00:01:01 . Memory (MB): peak = 1867.070 ; gain = 485.613 ; free physical = 109665 ; free virtual = 158451

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Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:13 ; elapsed = 00:00:24 . Memory (MB): peak = 1867.070 ; gain = 154.648 ; free physical = 109721 ; free virtual = 158507

Synthesis Optimization Complete : Time (s): cpu = 00:00:22 ; elapsed = 00:01:01 . Memory (MB): peak = 1867.070 ; gain = 485.613 ; free physical = 109731 ; free virtual = 158516

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 81 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [/nfs/home/j/j\_ratn/COEN316/ALUCIRCUIT\_SCRIPT/ALUcircuit.xdc]

Finished Parsing XDC File [/nfs/home/j/j\_ratn/COEN316/ALUCIRCUIT\_SCRIPT/ALUcircuit.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

21 Infos, 5 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:23 ; elapsed = 00:01:03 . Memory (MB): peak = 1911.070 ; gain = 542.340 ; free physical = 109718 ; free virtual = 158503

# opt\_design

Command: opt\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command opt\_design

Starting DRC Task

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:03 . Memory (MB): peak = 1975.105 ; gain = 64.035 ; free physical = 109714 ; free virtual = 158499

Starting Cache Timing Information Task

INFO: [Timing 38-35] Done setting XDC timing constraints.

Ending Cache Timing Information Task | Checksum: 16f14376b

Time (s): cpu = 00:00:07 ; elapsed = 00:00:34 . Memory (MB): peak = 2301.277 ; gain = 326.172 ; free physical = 109380 ; free virtual = 158166

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: 150d87f19

Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2301.277 ; gain = 0.000 ; free physical = 109405 ; free virtual = 158191

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: 150d87f19

Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2301.277 ; gain = 0.000 ; free physical = 109405 ; free virtual = 158191

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: 13435f1ef

Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.05 . Memory (MB): peak = 2301.277 ; gain = 0.000 ; free physical = 109405 ; free virtual = 158191

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: 13435f1ef

Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.06 . Memory (MB): peak = 2301.277 ; gain = 0.000 ; free physical = 109405 ; free virtual = 158191

INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: b46e725b

Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.07 . Memory (MB): peak = 2301.277 ; gain = 0.000 ; free physical = 109405 ; free virtual = 158191

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist

Phase 6 Post Processing Netlist | Checksum: b46e725b

Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.07 . Memory (MB): peak = 2301.277 ; gain = 0.000 ; free physical = 109405 ; free virtual = 158191

INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2301.277 ; gain = 0.000 ; free physical = 109405 ; free virtual = 158191

Ending Logic Optimization Task | Checksum: b46e725b

Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.07 . Memory (MB): peak = 2301.277 ; gain = 0.000 ; free physical = 109405 ; free virtual = 158191

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

Ending Power Optimization Task | Checksum: b46e725b

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2301.277 ; gain = 0.000 ; free physical = 109405 ; free virtual = 158191

Starting Final Cleanup Task

Ending Final Cleanup Task | Checksum: b46e725b

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2301.277 ; gain = 0.000 ; free physical = 109405 ; free virtual = 158191

INFO: [Common 17-83] Releasing license: Implementation

16 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt\_design completed successfully

opt\_design: Time (s): cpu = 00:00:09 ; elapsed = 00:00:36 . Memory (MB): peak = 2301.277 ; gain = 390.207 ; free physical = 109405 ; free virtual = 158191

# place\_design

Command: place\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Running DRC as a precondition to command place\_design

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2365.309 ; gain = 0.000 ; free physical = 109401 ; free virtual = 158187

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 02160799

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2365.309 ; gain = 0.000 ; free physical = 109401 ; free virtual = 158187

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2365.309 ; gain = 0.000 ; free physical = 109401 ; free virtual = 158187

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 52073dd7

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.75 . Memory (MB): peak = 2365.309 ; gain = 0.000 ; free physical = 109395 ; free virtual = 158181

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: abacefc7

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.78 . Memory (MB): peak = 2365.309 ; gain = 0.000 ; free physical = 109396 ; free virtual = 158181

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: abacefc7

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.78 . Memory (MB): peak = 2365.309 ; gain = 0.000 ; free physical = 109396 ; free virtual = 158181

Phase 1 Placer Initialization | Checksum: abacefc7

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.79 . Memory (MB): peak = 2365.309 ; gain = 0.000 ; free physical = 109396 ; free virtual = 158181

Phase 2 Global Placement

Phase 2.1 Floorplanning

Phase 2.1 Floorplanning | Checksum: abacefc7

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.81 . Memory (MB): peak = 2365.309 ; gain = 0.000 ; free physical = 109394 ; free virtual = 158179

WARNING: [Place 46-29] place\_design is not in timing mode. Skip physical synthesis in placer

Phase 2 Global Placement | Checksum: 9e981eb2

Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2477.359 ; gain = 112.051 ; free physical = 109363 ; free virtual = 158148

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: 9e981eb2

Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2477.359 ; gain = 112.051 ; free physical = 109363 ; free virtual = 158148

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: f4c8013b

Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2477.359 ; gain = 112.051 ; free physical = 109362 ; free virtual = 158148

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: 6ba3f024

Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2477.359 ; gain = 112.051 ; free physical = 109362 ; free virtual = 158148

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: 6ba3f024

Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2477.359 ; gain = 112.051 ; free physical = 109362 ; free virtual = 158148

Phase 3.5 Small Shape Detail Placement

Phase 3.5 Small Shape Detail Placement | Checksum: 8f90d29f

Time (s): cpu = 00:00:04 ; elapsed = 00:00:01 . Memory (MB): peak = 2477.359 ; gain = 112.051 ; free physical = 109358 ; free virtual = 158144

Phase 3.6 Re-assign LUT pins

Phase 3.6 Re-assign LUT pins | Checksum: 8f90d29f

Time (s): cpu = 00:00:04 ; elapsed = 00:00:02 . Memory (MB): peak = 2477.359 ; gain = 112.051 ; free physical = 109358 ; free virtual = 158144

Phase 3.7 Pipeline Register Optimization

Phase 3.7 Pipeline Register Optimization | Checksum: 8f90d29f

Time (s): cpu = 00:00:04 ; elapsed = 00:00:02 . Memory (MB): peak = 2477.359 ; gain = 112.051 ; free physical = 109358 ; free virtual = 158144

Phase 3 Detail Placement | Checksum: 8f90d29f

Time (s): cpu = 00:00:04 ; elapsed = 00:00:02 . Memory (MB): peak = 2477.359 ; gain = 112.051 ; free physical = 109358 ; free virtual = 158144

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

Phase 4.1 Post Commit Optimization | Checksum: 8f90d29f

Time (s): cpu = 00:00:04 ; elapsed = 00:00:02 . Memory (MB): peak = 2477.359 ; gain = 112.051 ; free physical = 109358 ; free virtual = 158144

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: 8f90d29f

Time (s): cpu = 00:00:04 ; elapsed = 00:00:02 . Memory (MB): peak = 2477.359 ; gain = 112.051 ; free physical = 109358 ; free virtual = 158144

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: 8f90d29f

Time (s): cpu = 00:00:04 ; elapsed = 00:00:02 . Memory (MB): peak = 2477.359 ; gain = 112.051 ; free physical = 109358 ; free virtual = 158144

Phase 4.4 Final Placement Cleanup

Phase 4.4 Final Placement Cleanup | Checksum: 8f90d29f

Time (s): cpu = 00:00:04 ; elapsed = 00:00:02 . Memory (MB): peak = 2477.359 ; gain = 112.051 ; free physical = 109358 ; free virtual = 158144

Phase 4 Post Placement Optimization and Clean-Up | Checksum: 8f90d29f

Time (s): cpu = 00:00:04 ; elapsed = 00:00:02 . Memory (MB): peak = 2477.359 ; gain = 112.051 ; free physical = 109358 ; free virtual = 158144

Ending Placer Task | Checksum: 7c7eea47

Time (s): cpu = 00:00:04 ; elapsed = 00:00:02 . Memory (MB): peak = 2477.359 ; gain = 112.051 ; free physical = 109373 ; free virtual = 158159

INFO: [Common 17-83] Releasing license: Implementation

10 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

place\_design completed successfully

# route\_design

Command: route\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command route\_design

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 8 CPUs

Checksum: PlaceDB: 7a68e2ae ConstDB: 0 ShapeSum: 2160799 RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: 170896271

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2477.359 ; gain = 0.000 ; free physical = 109237 ; free virtual = 158023

Post Restoration Checksum: NetGraph: a4cad911 NumContArr: cbbe8960 Constraints: 0 Timing: 0

Phase 2 Router Initialization

INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints

Phase 2.1 Fix Topology Constraints | Checksum: 170896271

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2477.969 ; gain = 0.609 ; free physical = 109207 ; free virtual = 157993

Phase 2.2 Pre Route Cleanup

Phase 2.2 Pre Route Cleanup | Checksum: 170896271

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2477.969 ; gain = 0.609 ; free physical = 109207 ; free virtual = 157993

Number of Nodes with overlaps = 0

Phase 2 Router Initialization | Checksum: 1033fa9d5

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2485.234 ; gain = 7.875 ; free physical = 109204 ; free virtual = 157989

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: 121f5499f

Time (s): cpu = 00:00:24 ; elapsed = 00:00:19 . Memory (MB): peak = 2485.234 ; gain = 7.875 ; free physical = 109201 ; free virtual = 157986

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 27

Number of Nodes with overlaps = 0

Phase 4.1 Global Iteration 0 | Checksum: 13e572803

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2485.234 ; gain = 7.875 ; free physical = 109200 ; free virtual = 157985

Phase 4 Rip-up And Reroute | Checksum: 13e572803

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2485.234 ; gain = 7.875 ; free physical = 109200 ; free virtual = 157985

Phase 5 Delay and Skew Optimization

Phase 5 Delay and Skew Optimization | Checksum: 13e572803

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2485.234 ; gain = 7.875 ; free physical = 109200 ; free virtual = 157985

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1 Hold Fix Iter | Checksum: 13e572803

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2485.234 ; gain = 7.875 ; free physical = 109200 ; free virtual = 157985

Phase 6 Post Hold Fix | Checksum: 13e572803

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2485.234 ; gain = 7.875 ; free physical = 109200 ; free virtual = 157985

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 0.105497 %

Global Horizontal Routing Utilization = 0.16894 %

Routable Net Status\*

\*Does not include unroutable nets such as driverless and loadless.

Run report\_route\_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Congestion Report

North Dir 1x1 Area, Max Cong = 25.2252%, No Congested Regions.

South Dir 1x1 Area, Max Cong = 16.2162%, No Congested Regions.

East Dir 1x1 Area, Max Cong = 27.9412%, No Congested Regions.

West Dir 1x1 Area, Max Cong = 17.6471%, No Congested Regions.

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Reporting congestion hotspots

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Direction: North

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Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: South

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: East

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: West

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: 13e572803

Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2485.234 ; gain = 7.875 ; free physical = 109200 ; free virtual = 157985

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: 13e572803

Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2488.234 ; gain = 10.875 ; free physical = 109198 ; free virtual = 157984

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: 15c2c4f90

Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2488.234 ; gain = 10.875 ; free physical = 109198 ; free virtual = 157984

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:25 ; elapsed = 00:00:20 . Memory (MB): peak = 2488.234 ; gain = 10.875 ; free physical = 109231 ; free virtual = 158017

Routing Is Done.

INFO: [Common 17-83] Releasing license: Implementation

8 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

route\_design completed successfully

route\_design: Time (s): cpu = 00:00:27 ; elapsed = 00:00:23 . Memory (MB): peak = 2488.234 ; gain = 10.875 ; free physical = 109231 ; free virtual = 158017

# write\_bitstream -force ALUcircuit.bit

Command: write\_bitstream -force ALUcircuit.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command write\_bitstream

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado\_2018.2/Vivado/2018.2/data/ip'.

INFO: [DRC 23-27] Running DRC with 8 threads

WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG\_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG\_VOLTAGE voltage property is set in the current\_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG\_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

set\_property CFGBVS value1 [current\_design]

#where value1 is either VCCO or GND

set\_property CONFIG\_VOLTAGE value2 [current\_design]

#where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.

WARNING: [DRC UCIO-1] Unconstrained Logical Port: 103 out of 103 logical ports have no user assigned specific location constraint (LOC). This may cause I/O contention or incompatibility with the board power or connectivity affecting performance, signal integrity or in extreme cases cause damage to the device or the components to which it is connected. To correct this violation, specify all pin locations. This design will fail to generate a bitstream unless all logical ports have a user specified site LOC constraint defined. To allow bitstream creation with unspecified pin locations (not recommended), use this command: set\_property SEVERITY {Warning} [get\_drc\_checks UCIO-1]. NOTE: When using the Vivado Runs infrastructure (e.g. launch\_runs Tcl command), add this command to a .tcl file and add that file as a pre-hook for write\_bitstream step for the implementation run. Problem ports: A[31:0], B[31:0], D[1:0], E[1:0], F[31:0], C, G, and H.

INFO: [Vivado 12-3199] DRC finished with 0 Errors, 2 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.

INFO: [Designutils 20-2272] Running write\_bitstream with 8 threads.

Loading data files...

Loading site data...

Loading route data...

Processing options...

Creating bitmap...

Creating bitstream...

Writing bitstream ./ALUcircuit.bit...

INFO: [Vivado 12-1842] Bitgen Completed Successfully.

INFO: [Common 17-83] Releasing license: Implementation

10 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

write\_bitstream completed successfully

write\_bitstream: Time (s): cpu = 00:00:14 ; elapsed = 00:00:15 . Memory (MB): peak = 2837.055 ; gain = 348.820 ; free physical = 109192 ; free virtual = 157981

INFO: [Common 17-206] Exiting Vivado at Thu Oct 15 20:35:24 2020...