Report

on

COEN 316 Laboratory Experiment #2

**Register File**

Submitted to

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*Instructor’s name*

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By

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Name student ID

Lab section: DI-X

“I certify that this submission is my original work and meets the Faculty's Expectations of Originality”

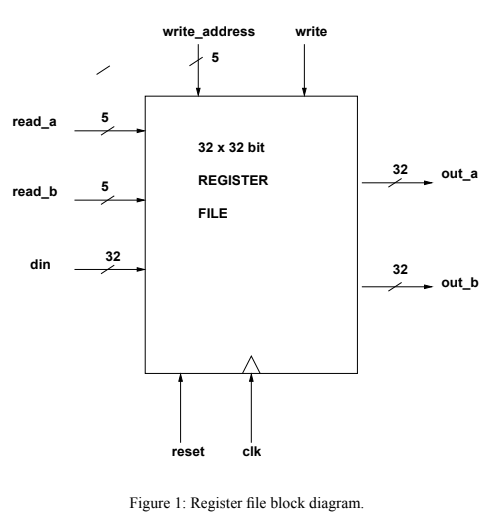


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# **Objective:**

In this lab, we will use digital logic simulation and synthesis using Modelsim, and Xilinx ISE (Vivado) to become acquainted with the VHDL simulation software tool and FPGA implementation software tools. During this lab, we will simulate a 32 x 32 register file with two read ports, one write port with write enable. The register file will be designed based on the figure below.



**Introduction:**

The lab consisted of designing a 32 bit register file for a CPU using VHDL. We simulate the register file array of a processor and test possible operations that may happen on it. The Register file contains 32 registers of 32 bits size each. The file is driven by a clock signal, and control signals to read/write data and select registers.

**Results:**

**The complete VHDL code source for the register file:**

| **library** IEEE; **use** IEEE.std\_logic\_1164.**all**; **use** IEEE.std\_logic\_unsigned.**all**; **use** IEEE.numeric\_std.**all**;  *--32 x 32 register file* *-- two read ports, one write port with write enable* **entity** regfile **is** **port**( din : **in** std\_logic\_vector(31 **downto** 0);  reset : **in** std\_logic;  clk : **in** std\_logic;  write : **in** std\_logic;  read\_a : **in** std\_logic\_vector(4 **downto** 0);  read\_b : **in** std\_logic\_vector(4 **downto** 0);  write\_address : **in** std\_logic\_vector(4 **downto** 0);  out\_a : **out** std\_logic\_vector(31 **downto** 0);  out\_b : **out** std\_logic\_vector(31 **downto** 0)); **end** regfile ;  **architecture** regfile\_arch **of** regfile **is**  *--create 32x32 regfile* **type** reg\_array **is** **array** (0 **to** 31) **of** std\_logic\_vector(31 **downto** 0); **signal** regarray : reg\_array; **begin**  *--map regsiter to output, for register reading command*  out\_a <= regarray(to\_integer(unsigned(read\_a)));  out\_b <= regarray(to\_integer(unsigned(read\_b)));  *--process for register file writing* write\_process : **process**(clk, reset) **begin**  *--reset array, make all registers 0 if reset is set*  **if** (reset = '1') **then**  regarray <= (**others** => (**others** => '0'));  **end** **if**;  *-- write to registers*  *-- only write at clock rises since synchronous*  *--if clock rise*  **if**(clk = '1' **and** clk'event) **then**  *--if write bit is set*  **if** (write = '1') **then**  regarray(to\_integer(unsigned(write\_address))) <= din;  **end** **if**;  **end** **if**; **end** **process**;  **end** regfile\_arch; |
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**Xilinx XDC file:**

| # Vivado does **not** support old UCF syntax # must **use** XDC syntax  # input ports A,B,C,D are connected **to** Switches 0,1,2,3 # **of** the Nexys board # output **port** E **is** connected **to** LED 0 **of** the Nexys board  set\_property IOSTANDARD LVCMOS33 [ get\_ports { A } ] ; set\_property IOSTANDARD LVCMOS33 [ get\_ports { B } ] ; set\_property IOSTANDARD LVCMOS33 [ get\_ports { C } ] ; set\_property IOSTANDARD LVCMOS33 [ get\_ports { D } ] ; set\_property IOSTANDARD LVCMOS33 [ get\_ports { E } ] ; set\_property IOSTANDARD LVCMOS33 [ get\_ports { F } ] ; set\_property IOSTANDARD LVCMOS33 [ get\_ports { G } ] ; set\_property IOSTANDARD LVCMOS33 [ get\_ports { H } ] ; set\_property IOSTANDARD LVCMOS33 [ get\_ports { I } ] ; |
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**The TCL script file:**

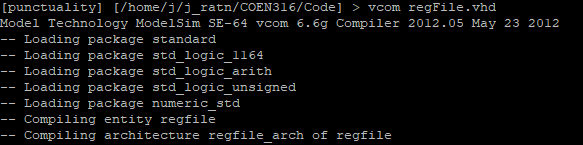
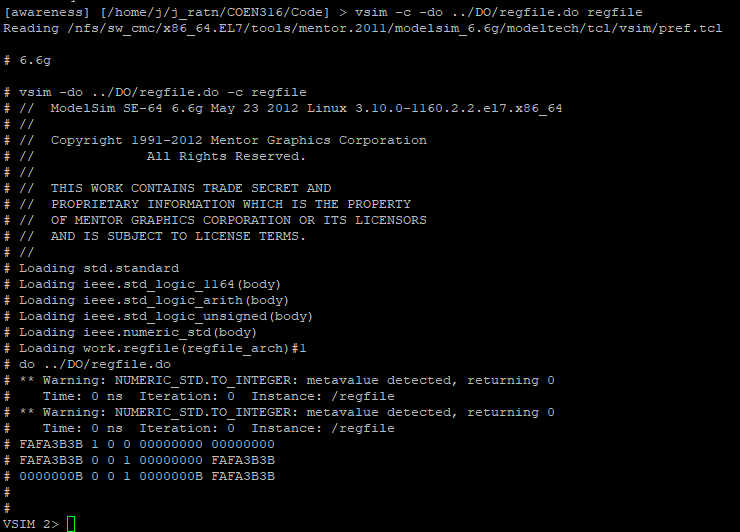
| # TCL script **for** running vivado **in** batch mode **to** synthesize  # **To** run the script first source the Vivado env **file**: # source /CMC/tools/xilinx/Vivado\_2018.2/Vivado/2018.2/settings64\_CMC\_central\_license.csh # #**Then** issue the following command from the Linux prompt: # vivado -log tedcircuit.log -mode batch -source tedcircuit\_script.tcl  # read **in** the VHDL source code files **and** the xdc constraints **file**  set\_property **SEVERITY** {Warning} [get\_drc\_checks UCIO-1]  read\_vhdl { ../Code/regFile.vhd ../Code/REGcircuit.vhd } read\_xdc REGcircuit.xdc  # the -top refers **to** the top level VHDL **entity** name # the -part specfies the target Xilinx FPGA  synth\_design -top REGcircuit -part xc7a100tcsg324-1  opt\_design place\_design route\_design  # **generate** the bitsteam **file** write\_bitstream -**force** REGcircuit.bit |
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**The DO file:**

| #reset registers #clk **is** zero so read **function** will **not** work  **force** reset 1 **force** clk 0 **force** din X"FAFA3B3B" **force** write 0 **force** write\_address "00001" #output ports mapped **to** read **register** 0 **and** 1 **force** read\_a "00000" **force** read\_b "00001"  run 2  #nothing should be writen **in** R0 **and** R1, since write **is** disabled examine -radix hex din reset clk write out\_a out\_b   #write din **in** **register** 1, remove reset, simulate clk #run **for** 2ms between commands **to** let ports be set, was causing problems without it **force** reset 0 run 2  #enable writing **force** write 1 run 2  #clk rising edge, **to** allow write **force** clk 1 run 2  #clk reset **to** 0, **to** **block** writing **force** clk 0 run 2  #din will be written **in** out\_b examine -radix hex din reset clk write out\_a out\_b  #now i want **to** put din into R32 **and** read it **in** **port** A  #write **in** R32 **force** write\_address "11111" run 2 **force** read\_a "11111" **force** din X"000000B" #do write **force** clk 1 run 2 #stop write **force** clk 0 run 2  #**force** din X"000000B" will be written **in** R32 **in** out\_a **and** **force** din X"FAFA3B3B" **in** R1 **in** out\_b examine -radix hex din reset clk write out\_a out\_b  #we know that write enable works, read registers work |
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**The log file is available in the appendix.**

**Simulation and implementation results using port maps:**

* The vcom of the vhdl code for the reg file
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* The Modelsim simulation
  + The modelsim results show that at the start of the simulation when the reset signal is asserted the registers are reset to zero.
  + Then the write signal is asserted the register that corresponds to the write\_address signal is written to and saves the data. When the write signal is deasserted the registers are not written to.
  + The read\_a and read\_b signals always display what values are written in the selected registers. It shows if any change happens to the register or not.
  + The VHDL code consists of a signal that is a user defined type of an array of std\_logic\_vectors.
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  + The result of the simulations with our do file shows that the results are accurate to what we expected to get from the do file.

**Conclusion:**

In conclusion, the experiment was done successfully since the results obtained are accurate compared to the theoretical results. We learned and understood all the steps to do a simulation of a register file.This is shown by the Modelsim simulations testing with the given DO file for all possible operations and it produced the correct outputs.

**Appendix:**

The log file:

| #*-----------------------------------------------------------* # Vivado v2018.2 (64-bit) # SW Build 2258646 **on** Thu Jun 14 20:02:38 MDT 2018 # IP Build 2256618 **on** Thu Jun 14 22:10:49 MDT 2018 # Start **of** session at: Tue Oct 27 10:33:42 2020 # **Process** ID: 27945 # Current directory: /nfs/home/j/j\_ratn/COEN316/REGCIRCUIT\_SCRIPT # Command line: vivado -log regcircuit.log -mode batch -source regcircuit\_script.tcl # Log **file**: /nfs/home/j/j\_ratn/COEN316/REGCIRCUIT\_SCRIPT/regcircuit.log # Journal **file**: /nfs/home/j/j\_ratn/COEN316/REGCIRCUIT\_SCRIPT/vivado.jou #*-----------------------------------------------------------* source regcircuit\_script.tcl # set\_property **SEVERITY** {Warning} [get\_drc\_checks UCIO-1] # read\_vhdl { ../Code/regFile.vhd ../Code/REGcircuit.vhd } read\_vhdl: Time (s): cpu = 00:00:02 ; elapsed = 00:00:05 . Memory (MB): peak = 1369.133 ; gain = 26.016 ; free physical = 58066 ; free virtual = 129252 # read\_xdc REGcircuit.xdc # synth\_design -top REGcircuit -part xc7a100tcsg324-1 Command: synth\_design -top REGcircuit -part xc7a100tcsg324-1 Starting synth\_design Attempting **to** get a license **for** feature 'Synthesis' **and**/**or** device 'xc7a100t' INFO: [Common 17-349] Got license **for** feature 'Synthesis' **and**/**or** device 'xc7a100t' INFO: Launching helper **process** **for** spawning children vivado processes INFO: Helper **process** launched **with** PID 28002  *---------------------------------------------------------------------------------* Starting RTL Elaboration : Time (s): cpu = 00:00:04 ; elapsed = 00:00:08 . Memory (MB): peak = 1468.586 ; gain = 86.727 ; free physical = 57959 ; free virtual = 129145 *---------------------------------------------------------------------------------* INFO: [Synth 8-638] synthesizing module 'REGcircuit' [/nfs/home/j/j\_ratn/COEN316/Code/REGcircuit.vhd:11] INFO: [Synth 8-3491] module 'regfile' declared at '/nfs/home/j/j\_ratn/COEN316/Code/regFile.vhd:9' bound **to** instance 'U1' **of** **component** 'reg' [/nfs/home/j/j\_ratn/COEN316/Code/REGcircuit.vhd:28] INFO: [Synth 8-638] synthesizing module 'regfile' [/nfs/home/j/j\_ratn/COEN316/Code/regFile.vhd:21] INFO: [Synth 8-256] done synthesizing module 'regfile' (1#1) [/nfs/home/j/j\_ratn/COEN316/Code/regFile.vhd:21] INFO: [Synth 8-256] done synthesizing module 'REGcircuit' (2#1) [/nfs/home/j/j\_ratn/COEN316/Code/REGcircuit.vhd:11] *---------------------------------------------------------------------------------* Finished RTL Elaboration : Time (s): cpu = 00:00:05 ; elapsed = 00:00:12 . Memory (MB): peak = 1513.227 ; gain = 131.367 ; free physical = 57968 ; free virtual = 129154 *---------------------------------------------------------------------------------*  **Report** Check Netlist:  +*------+------------------+-------+---------+-------+------------------+* | |Item |Errors |Warnings |Status |Description | +*------+------------------+-------+---------+-------+------------------+* |1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets | +*------+------------------+-------+---------+-------+------------------+* *---------------------------------------------------------------------------------* Start Handling Custom Attributes *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Handling Custom Attributes : Time (s): cpu = 00:00:06 ; elapsed = 00:00:13 . Memory (MB): peak = 1513.227 ; gain = 131.367 ; free physical = 57970 ; free virtual = 129156 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:06 ; elapsed = 00:00:13 . Memory (MB): peak = 1513.227 ; gain = 131.367 ; free physical = 57970 ; free virtual = 129156 *---------------------------------------------------------------------------------* INFO: [Device 21-403] Loading part xc7a100tcsg324-1 INFO: [Project 1-570] Preparing netlist **for** logic optimization  Processing XDC Constraints Initializing timing engine Parsing XDC **File** [/nfs/home/j/j\_ratn/COEN316/REGCIRCUIT\_SCRIPT/REGcircuit.xdc] Finished Parsing XDC **File** [/nfs/home/j/j\_ratn/COEN316/REGCIRCUIT\_SCRIPT/REGcircuit.xdc] Completed Processing XDC Constraints  INFO: [Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed.  Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1885.191 ; gain = 0.000 ; free physical = 57638 ; free virtual = 128824 *---------------------------------------------------------------------------------* Finished Constraint Validation : Time (s): cpu = 00:00:28 ; elapsed = 00:01:52 . Memory (MB): peak = 1885.191 ; gain = 503.332 ; free physical = 57771 ; free virtual = 128957 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Loading Part **and** Timing Information *---------------------------------------------------------------------------------* Loading part: xc7a100tcsg324-1 *---------------------------------------------------------------------------------* Finished Loading Part **and** Timing Information : Time (s): cpu = 00:00:28 ; elapsed = 00:01:52 . Memory (MB): peak = 1885.191 ; gain = 503.332 ; free physical = 57771 ; free virtual = 128957 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Applying 'set\_property' XDC Constraints *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:29 ; elapsed = 00:01:53 . Memory (MB): peak = 1885.191 ; gain = 503.332 ; free physical = 57772 ; free virtual = 128959 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:30 ; elapsed = 00:01:55 . Memory (MB): peak = 1885.191 ; gain = 503.332 ; free physical = 57765 ; free virtual = 128952 *---------------------------------------------------------------------------------*  **Report** RTL Partitions:  +-+*--------------+------------+----------+* | |RTL Partition |Replication |Instances | +-+*--------------+------------+----------+* +-+*--------------+------------+----------+* *---------------------------------------------------------------------------------* Start RTL **Component** Statistics  *---------------------------------------------------------------------------------* Detailed RTL **Component** Info :  +*---Registers :*   32 Bit Registers := 32  +*---Muxes :*   2 Input 32 Bit Muxes := 64   2 Input 1 Bit Muxes := 64  *---------------------------------------------------------------------------------* Finished RTL **Component** Statistics  *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start RTL Hierarchical **Component** Statistics  *---------------------------------------------------------------------------------* Hierarchical RTL **Component** **report**  Module regfile  Detailed RTL **Component** Info :  +*---Registers :*   32 Bit Registers := 32  +*---Muxes :*   2 Input 32 Bit Muxes := 64   2 Input 1 Bit Muxes := 64  *---------------------------------------------------------------------------------* Finished RTL Hierarchical **Component** Statistics *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Part Resource Summary *---------------------------------------------------------------------------------* Part Resources: DSPs: 240 (col length:80) BRAMs: 270 (col length: RAMB18 80 RAMB36 40) *---------------------------------------------------------------------------------* Finished Part Resource Summary *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Cross Boundary **and** Area Optimization *---------------------------------------------------------------------------------* Warning: Parallel synthesis criteria **is** **not** met  *---------------------------------------------------------------------------------* Finished Cross Boundary **and** Area Optimization : Time (s): cpu = 00:00:35 ; elapsed = 00:02:04 . Memory (MB): peak = 1885.191 ; gain = 503.332 ; free physical = 57733 ; free virtual = 128923 *---------------------------------------------------------------------------------*  **Report** RTL Partitions:  +-+*--------------+------------+----------+* | |RTL Partition |Replication |Instances | +-+*--------------+------------+----------+* +-+*--------------+------------+----------+* *---------------------------------------------------------------------------------* Start Applying XDC Timing Constraints *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:50 ; elapsed = 00:02:38 . Memory (MB): peak = 1885.191 ; gain = 503.332 ; free physical = 57607 ; free virtual = 128797 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Timing Optimization *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Timing Optimization : Time (s): cpu = 00:00:51 ; elapsed = 00:02:39 . Memory (MB): peak = 1885.191 ; gain = 503.332 ; free physical = 57606 ; free virtual = 128796 *---------------------------------------------------------------------------------*  **Report** RTL Partitions:  +-+*--------------+------------+----------+* | |RTL Partition |Replication |Instances | +-+*--------------+------------+----------+* +-+*--------------+------------+----------+* *---------------------------------------------------------------------------------* Start Technology Mapping *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Technology Mapping : Time (s): cpu = 00:00:52 ; elapsed = 00:02:40 . Memory (MB): peak = 1908.082 ; gain = 526.223 ; free physical = 57604 ; free virtual = 128794 *---------------------------------------------------------------------------------*  **Report** RTL Partitions:  +-+*--------------+------------+----------+* | |RTL Partition |Replication |Instances | +-+*--------------+------------+----------+* +-+*--------------+------------+----------+* *---------------------------------------------------------------------------------* Start IO Insertion *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Flattening Before IO Insertion *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Flattening Before IO Insertion *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Final Netlist Cleanup *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Final Netlist Cleanup *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished IO Insertion : Time (s): cpu = 00:00:53 ; elapsed = 00:02:42 . Memory (MB): peak = 1908.086 ; gain = 526.227 ; free physical = 57605 ; free virtual = 128795 *---------------------------------------------------------------------------------*  **Report** Check Netlist:  +*------+------------------+-------+---------+-------+------------------+* | |Item |Errors |Warnings |Status |Description | +*------+------------------+-------+---------+-------+------------------+* |1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets | +*------+------------------+-------+---------+-------+------------------+* *---------------------------------------------------------------------------------* Start Renaming Generated Instances *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Renaming Generated Instances : Time (s): cpu = 00:00:53 ; elapsed = 00:02:42 . Memory (MB): peak = 1908.086 ; gain = 526.227 ; free physical = 57605 ; free virtual = 128795 *---------------------------------------------------------------------------------*  **Report** RTL Partitions:  +-+*--------------+------------+----------+* | |RTL Partition |Replication |Instances | +-+*--------------+------------+----------+* +-+*--------------+------------+----------+* *---------------------------------------------------------------------------------* Start Rebuilding User Hierarchy *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:53 ; elapsed = 00:02:42 . Memory (MB): peak = 1908.086 ; gain = 526.227 ; free physical = 57605 ; free virtual = 128795 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Renaming Generated Ports *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Renaming Generated Ports : Time (s): cpu = 00:00:53 ; elapsed = 00:02:42 . Memory (MB): peak = 1908.086 ; gain = 526.227 ; free physical = 57605 ; free virtual = 128795 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Handling Custom Attributes *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Handling Custom Attributes : Time (s): cpu = 00:00:53 ; elapsed = 00:02:42 . Memory (MB): peak = 1908.086 ; gain = 526.227 ; free physical = 57605 ; free virtual = 128795 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Renaming Generated Nets *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Renaming Generated Nets : Time (s): cpu = 00:00:53 ; elapsed = 00:02:42 . Memory (MB): peak = 1908.086 ; gain = 526.227 ; free physical = 57605 ; free virtual = 128795 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Writing Synthesis **Report** *---------------------------------------------------------------------------------*  **Report** BlackBoxes:  +-+*--------------+----------+* | |BlackBox name |Instances | +-+*--------------+----------+* +-+*--------------+----------+*  **Report** Cell Usage:  +*------+------+------+* | |Cell |Count | +*------+------+------+* |1 |BUFG | 1| |2 |LUT2 | 14| |3 |LUT3 | 1| |4 |LUT4 | 1| |5 |LUT5 | 1| |6 |LUT6 | 645| |7 |MUXF7 | 256| |8 |FDRE | 1024| |9 |IBUF | 50| |10 |OBUF | 64| +*------+------+------+*  **Report** Instance Areas:  +*------+---------+--------+------+* | |Instance |Module |Cells | +*------+---------+--------+------+* |1 |top | | 2057| |2 | U1 |regfile | 1942| +*------+---------+--------+------+* *---------------------------------------------------------------------------------* Finished Writing Synthesis **Report** : Time (s): cpu = 00:00:53 ; elapsed = 00:02:42 . Memory (MB): peak = 1908.086 ; gain = 526.227 ; free physical = 57605 ; free virtual = 128795 *---------------------------------------------------------------------------------* Synthesis finished **with** 0 errors, 0 critical warnings **and** 0 warnings. Synthesis Optimization Runtime : Time (s): cpu = 00:00:35 ; elapsed = 00:01:12 . Memory (MB): peak = 1908.086 ; gain = 154.262 ; free physical = 57663 ; free virtual = 128853 Synthesis Optimization Complete : Time (s): cpu = 00:00:53 ; elapsed = 00:02:43 . Memory (MB): peak = 1908.090 ; gain = 526.227 ; free physical = 57674 ; free virtual = 128863 INFO: [Project 1-571] Translating synthesized netlist INFO: [Netlist 29-17] Analyzing 306 Unisim elements **for** replacement INFO: [Netlist 29-28] Unisim Transformation completed **in** 0 CPU seconds WARNING: [Netlist 29-101] Netlist 'REGcircuit' **is** **not** ideal **for** floorplanning, since the cellview 'regfile' contains a large number **of** primitives. Please consider enabling hierarchy **in** synthesis **if** you want **to** do floorplanning. INFO: [Project 1-570] Preparing netlist **for** logic optimization Parsing XDC **File** [/nfs/home/j/j\_ratn/COEN316/REGCIRCUIT\_SCRIPT/REGcircuit.xdc] Finished Parsing XDC **File** [/nfs/home/j/j\_ratn/COEN316/REGCIRCUIT\_SCRIPT/REGcircuit.xdc] INFO: [Opt 31-138] Pushed 0 inverter(s) **to** 0 load pin(s). INFO: [Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed.  INFO: [Common 17-83] Releasing license: Synthesis 16 Infos, 1 Warnings, 0 Critical Warnings **and** 0 Errors encountered. synth\_design completed successfully synth\_design: Time (s): cpu = 00:00:57 ; elapsed = 00:02:48 . Memory (MB): peak = 1940.102 ; gain = 570.969 ; free physical = 57696 ; free virtual = 128886 # opt\_design Command: opt\_design Attempting **to** get a license **for** feature 'Implementation' **and**/**or** device 'xc7a100t' INFO: [Common 17-349] Got license **for** feature 'Implementation' **and**/**or** device 'xc7a100t' Running DRC as a precondition **to** command opt\_design  Starting DRC Task INFO: [DRC 23-27] Running DRC **with** 8 threads INFO: [Project 1-461] DRC finished **with** 0 Errors INFO: [Project 1-462] Please refer **to** the DRC **report** (report\_drc) **for** more information.  Time (s): cpu = 00:00:03 ; elapsed = 00:00:08 . Memory (MB): peak = 2004.133 ; gain = 64.031 ; free physical = 57681 ; free virtual = 128871  Starting Cache Timing Information Task INFO: [Timing 38-35] Done setting XDC timing constraints. Ending Cache Timing Information Task | Checksum: dd1129e9  Time (s): cpu = 00:00:14 ; elapsed = 00:01:21 . Memory (MB): peak = 2317.297 ; gain = 313.164 ; free physical = 57371 ; free virtual = 128553  Starting Logic Optimization Task  Phase 1 Retarget INFO: [Opt 31-138] Pushed 0 inverter(s) **to** 0 load pin(s). INFO: [Opt 31-49] Retargeted 0 cell(s). Phase 1 Retarget | Checksum: dd1129e9  Time (s): cpu = 00:00:00.23 ; elapsed = 00:00:00.40 . Memory (MB): peak = 2317.297 ; gain = 0.000 ; free physical = 57387 ; free virtual = 128569 INFO: [Opt 31-389] Phase Retarget created 0 cells **and** removed 0 cells  Phase 2 **Constant** propagation INFO: [Opt 31-138] Pushed 0 inverter(s) **to** 0 load pin(s). Phase 2 **Constant** propagation | Checksum: dd1129e9  Time (s): cpu = 00:00:00.30 ; elapsed = 00:00:00.52 . Memory (MB): peak = 2317.297 ; gain = 0.000 ; free physical = 57387 ; free virtual = 128569 INFO: [Opt 31-389] Phase **Constant** propagation created 0 cells **and** removed 0 cells  Phase 3 Sweep Phase 3 Sweep | Checksum: dd1129e9  Time (s): cpu = 00:00:00.35 ; elapsed = 00:00:00.62 . Memory (MB): peak = 2317.297 ; gain = 0.000 ; free physical = 57387 ; free virtual = 128569 INFO: [Opt 31-389] Phase Sweep created 0 cells **and** removed 0 cells  Phase 4 BUFG optimization Phase 4 BUFG optimization | Checksum: dd1129e9  Time (s): cpu = 00:00:00.41 ; elapsed = 00:00:00.69 . Memory (MB): peak = 2317.297 ; gain = 0.000 ; free physical = 57387 ; free virtual = 128570 INFO: [Opt 31-662] Phase BUFG optimization created 0 cells **of** which 0 are BUFGs **and** removed 0 cells.  Phase 5 Shift **Register** Optimization Phase 5 Shift **Register** Optimization | Checksum: dd1129e9  Time (s): cpu = 00:00:00.45 ; elapsed = 00:00:00.77 . Memory (MB): peak = 2317.297 ; gain = 0.000 ; free physical = 57387 ; free virtual = 128570 INFO: [Opt 31-389] Phase Shift **Register** Optimization created 0 cells **and** removed 0 cells  Phase 6 Post Processing Netlist Phase 6 Post Processing Netlist | Checksum: dd1129e9  Time (s): cpu = 00:00:00.47 ; elapsed = 00:00:00.78 . Memory (MB): peak = 2317.297 ; gain = 0.000 ; free physical = 57387 ; free virtual = 128570 INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells **and** removed 0 cells  Starting Connectivity Check Task  Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2317.297 ; gain = 0.000 ; free physical = 57387 ; free virtual = 128570 Ending Logic Optimization Task | Checksum: dd1129e9  Time (s): cpu = 00:00:00.48 ; elapsed = 00:00:00.80 . Memory (MB): peak = 2317.297 ; gain = 0.000 ; free physical = 57387 ; free virtual = 128570  Starting Power Optimization Task INFO: [Pwropt 34-132] Skipping clock gating **for** clocks **with** a period < 2.00 ns. Ending Power Optimization Task | Checksum: dd1129e9  Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.09 . Memory (MB): peak = 2317.297 ; gain = 0.000 ; free physical = 57387 ; free virtual = 128570  Starting Final Cleanup Task Ending Final Cleanup Task | Checksum: dd1129e9  Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2317.297 ; gain = 0.000 ; free physical = 57387 ; free virtual = 128570 INFO: [Common 17-83] Releasing license: Implementation 16 Infos, 0 Warnings, 0 Critical Warnings **and** 0 Errors encountered. opt\_design completed successfully opt\_design: Time (s): cpu = 00:00:17 ; elapsed = 00:01:30 . Memory (MB): peak = 2317.297 ; gain = 377.195 ; free physical = 57387 ; free virtual = 128570 # place\_design Command: place\_design Attempting **to** get a license **for** feature 'Implementation' **and**/**or** device 'xc7a100t' INFO: [Common 17-349] Got license **for** feature 'Implementation' **and**/**or** device 'xc7a100t' INFO: [DRC 23-27] Running DRC **with** 8 threads INFO: [Vivado\_Tcl 4-198] DRC finished **with** 0 Errors INFO: [Vivado\_Tcl 4-199] Please refer **to** the DRC **report** (report\_drc) **for** more information. Running DRC as a precondition **to** command place\_design INFO: [DRC 23-27] Running DRC **with** 8 threads INFO: [Vivado\_Tcl 4-198] DRC finished **with** 0 Errors INFO: [Vivado\_Tcl 4-199] Please refer **to** the DRC **report** (report\_drc) **for** more information.  Starting Placer Task INFO: [Place 30-611] Multithreading enabled **for** place\_design using a maximum **of** 8 CPUs  Phase 1 Placer Initialization  Phase 1.1 Placer Initialization Netlist Sorting Netlist sorting complete. Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2381.328 ; gain = 0.000 ; free physical = 57371 ; free virtual = 128553 Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 65f3a7d6  Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2381.328 ; gain = 0.000 ; free physical = 57371 ; free virtual = 128553 Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2381.328 ; gain = 0.000 ; free physical = 57371 ; free virtual = 128553  Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device INFO: [Timing 38-35] Done setting XDC timing constraints. Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 834dcdad  Time (s): cpu = 00:00:04 ; elapsed = 00:00:03 . Memory (MB): peak = 2381.328 ; gain = 0.000 ; free physical = 57365 ; free virtual = 128547  Phase 1.3 Build Placer Netlist Model Phase 1.3 Build Placer Netlist Model | Checksum: f90655b4  Time (s): cpu = 00:00:04 ; elapsed = 00:00:03 . Memory (MB): peak = 2381.328 ; gain = 0.000 ; free physical = 57365 ; free virtual = 128548  Phase 1.4 Constrain Clocks/Macros Phase 1.4 Constrain Clocks/Macros | Checksum: f90655b4  Time (s): cpu = 00:00:04 ; elapsed = 00:00:03 . Memory (MB): peak = 2381.328 ; gain = 0.000 ; free physical = 57365 ; free virtual = 128548 Phase 1 Placer Initialization | Checksum: f90655b4  Time (s): cpu = 00:00:04 ; elapsed = 00:00:03 . Memory (MB): peak = 2381.328 ; gain = 0.000 ; free physical = 57365 ; free virtual = 128548  Phase 2 Global Placement  Phase 2.1 Floorplanning Phase 2.1 Floorplanning | Checksum: f90655b4  Time (s): cpu = 00:00:05 ; elapsed = 00:00:03 . Memory (MB): peak = 2381.328 ; gain = 0.000 ; free physical = 57364 ; free virtual = 128546 WARNING: [Place 46-29] place\_design **is** **not** **in** timing mode. Skip physical synthesis **in** placer Phase 2 Global Placement | Checksum: f5a32c3d  Time (s): cpu = 00:00:40 ; elapsed = 00:01:05 . Memory (MB): peak = 2477.371 ; gain = 96.043 ; free physical = 57345 ; free virtual = 128528  Phase 3 Detail Placement  Phase 3.1 Commit Multi Column Macros Phase 3.1 Commit Multi Column Macros | Checksum: f5a32c3d  Time (s): cpu = 00:00:40 ; elapsed = 00:01:05 . Memory (MB): peak = 2477.371 ; gain = 96.043 ; free physical = 57345 ; free virtual = 128528  Phase 3.2 Commit Most Macros & LUTRAMs Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: a00636fd  Time (s): cpu = 00:00:40 ; elapsed = 00:01:05 . Memory (MB): peak = 2477.371 ; gain = 96.043 ; free physical = 57345 ; free virtual = 128528  Phase 3.3 Area Swap Optimization Phase 3.3 Area Swap Optimization | Checksum: fd8e653d  Time (s): cpu = 00:00:41 ; elapsed = 00:01:05 . Memory (MB): peak = 2477.371 ; gain = 96.043 ; free physical = 57343 ; free virtual = 128526  Phase 3.4 Pipeline **Register** Optimization Phase 3.4 Pipeline **Register** Optimization | Checksum: fd8e653d  Time (s): cpu = 00:00:41 ; elapsed = 00:01:05 . Memory (MB): peak = 2477.371 ; gain = 96.043 ; free physical = 57345 ; free virtual = 128528  Phase 3.5 Small Shape Detail Placement Phase 3.5 Small Shape Detail Placement | Checksum: fb90c334  Time (s): cpu = 00:00:43 ; elapsed = 00:01:08 . Memory (MB): peak = 2477.371 ; gain = 96.043 ; free physical = 57340 ; free virtual = 128523  Phase 3.6 Re-assign LUT pins Phase 3.6 Re-assign LUT pins | Checksum: fb90c334  Time (s): cpu = 00:00:43 ; elapsed = 00:01:08 . Memory (MB): peak = 2477.371 ; gain = 96.043 ; free physical = 57341 ; free virtual = 128523  Phase 3.7 Pipeline **Register** Optimization Phase 3.7 Pipeline **Register** Optimization | Checksum: fb90c334  Time (s): cpu = 00:00:43 ; elapsed = 00:01:08 . Memory (MB): peak = 2477.371 ; gain = 96.043 ; free physical = 57339 ; free virtual = 128522 Phase 3 Detail Placement | Checksum: fb90c334  Time (s): cpu = 00:00:43 ; elapsed = 00:01:08 . Memory (MB): peak = 2477.371 ; gain = 96.043 ; free physical = 57341 ; free virtual = 128524  Phase 4 Post Placement Optimization **and** Clean-Up  Phase 4.1 Post Commit Optimization Phase 4.1 Post Commit Optimization | Checksum: fb90c334  Time (s): cpu = 00:00:43 ; elapsed = 00:01:08 . Memory (MB): peak = 2477.371 ; gain = 96.043 ; free physical = 57341 ; free virtual = 128524  Phase 4.2 Post Placement Cleanup Phase 4.2 Post Placement Cleanup | Checksum: fb90c334  Time (s): cpu = 00:00:43 ; elapsed = 00:01:08 . Memory (MB): peak = 2477.371 ; gain = 96.043 ; free physical = 57343 ; free virtual = 128525  Phase 4.3 Placer Reporting Phase 4.3 Placer Reporting | Checksum: fb90c334  Time (s): cpu = 00:00:43 ; elapsed = 00:01:08 . Memory (MB): peak = 2477.371 ; gain = 96.043 ; free physical = 57343 ; free virtual = 128525  Phase 4.4 Final Placement Cleanup Phase 4.4 Final Placement Cleanup | Checksum: fb90c334  Time (s): cpu = 00:00:43 ; elapsed = 00:01:08 . Memory (MB): peak = 2477.371 ; gain = 96.043 ; free physical = 57343 ; free virtual = 128525 Phase 4 Post Placement Optimization **and** Clean-Up | Checksum: fb90c334  Time (s): cpu = 00:00:43 ; elapsed = 00:01:08 . Memory (MB): peak = 2477.371 ; gain = 96.043 ; free physical = 57343 ; free virtual = 128525 Ending Placer Task | Checksum: a998ec71  Time (s): cpu = 00:00:43 ; elapsed = 00:01:08 . Memory (MB): peak = 2477.371 ; gain = 96.043 ; free physical = 57360 ; free virtual = 128542 INFO: [Common 17-83] Releasing license: Implementation 10 Infos, 1 Warnings, 0 Critical Warnings **and** 0 Errors encountered. place\_design completed successfully place\_design: Time (s): cpu = 00:00:47 ; elapsed = 00:01:16 . Memory (MB): peak = 2477.371 ; gain = 160.074 ; free physical = 57360 ; free virtual = 128542 # route\_design Command: route\_design Attempting **to** get a license **for** feature 'Implementation' **and**/**or** device 'xc7a100t' INFO: [Common 17-349] Got license **for** feature 'Implementation' **and**/**or** device 'xc7a100t' Running DRC as a precondition **to** command route\_design INFO: [DRC 23-27] Running DRC **with** 8 threads INFO: [Vivado\_Tcl 4-198] DRC finished **with** 0 Errors INFO: [Vivado\_Tcl 4-199] Please refer **to** the DRC **report** (report\_drc) **for** more information.   Starting Routing Task INFO: [Route 35-254] Multithreading enabled **for** route\_design using a maximum **of** 8 CPUs Checksum: PlaceDB: 43a5449b ConstDB: 0 ShapeSum: 65f3a7d6 RouteDB: 0  Phase 1 Build RT Design Phase 1 Build RT Design | Checksum: 1323dbbcb  Time (s): cpu = 00:00:56 ; elapsed = 00:01:01 . Memory (MB): peak = 2487.000 ; gain = 9.629 ; free physical = 57199 ; free virtual = 128381 Post Restoration Checksum: NetGraph: 71b46225 NumContArr: c08959a6 Constraints: 0 Timing: 0  Phase 2 Router Initialization INFO: [Route 35-64] No timing constraints were detected. The router will operate **in** resource-optimization mode.  Phase 2.1 Fix Topology Constraints Phase 2.1 Fix Topology Constraints | Checksum: 1323dbbcb  Time (s): cpu = 00:00:56 ; elapsed = 00:01:02 . Memory (MB): peak = 2493.988 ; gain = 16.617 ; free physical = 57167 ; free virtual = 128349  Phase 2.2 Pre Route Cleanup Phase 2.2 Pre Route Cleanup | Checksum: 1323dbbcb  Time (s): cpu = 00:00:56 ; elapsed = 00:01:02 . Memory (MB): peak = 2493.988 ; gain = 16.617 ; free physical = 57167 ; free virtual = 128349  Number **of** Nodes **with** overlaps = 0 Phase 2 Router Initialization | Checksum: 148a9e5c3  Time (s): cpu = 00:00:57 ; elapsed = 00:01:03 . Memory (MB): peak = 2502.254 ; gain = 24.883 ; free physical = 57160 ; free virtual = 128342  Phase 3 Initial Routing Phase 3 Initial Routing | Checksum: aa6cce0c  Time (s): cpu = 00:00:59 ; elapsed = 00:01:03 . Memory (MB): peak = 2502.254 ; gain = 24.883 ; free physical = 57161 ; free virtual = 128344  Phase 4 Rip-up **And** Reroute  Phase 4.1 Global Iteration 0  Number **of** Nodes **with** overlaps = 279  Number **of** Nodes **with** overlaps = 1  Number **of** Nodes **with** overlaps = 0 Phase 4.1 Global Iteration 0 | Checksum: 899e7dc4  Time (s): cpu = 00:01:12 ; elapsed = 00:01:08 . Memory (MB): peak = 2502.254 ; gain = 24.883 ; free physical = 57162 ; free virtual = 128344 Phase 4 Rip-up **And** Reroute | Checksum: 899e7dc4  Time (s): cpu = 00:01:12 ; elapsed = 00:01:08 . Memory (MB): peak = 2502.254 ; gain = 24.883 ; free physical = 57162 ; free virtual = 128344  Phase 5 Delay **and** Skew Optimization Phase 5 Delay **and** Skew Optimization | Checksum: 899e7dc4  Time (s): cpu = 00:01:12 ; elapsed = 00:01:08 . Memory (MB): peak = 2502.254 ; gain = 24.883 ; free physical = 57162 ; free virtual = 128344  Phase 6 Post Hold Fix  Phase 6.1 Hold Fix Iter Phase 6.1 Hold Fix Iter | Checksum: 899e7dc4  Time (s): cpu = 00:01:12 ; elapsed = 00:01:08 . Memory (MB): peak = 2502.254 ; gain = 24.883 ; free physical = 57162 ; free virtual = 128344 Phase 6 Post Hold Fix | Checksum: 899e7dc4  Time (s): cpu = 00:01:12 ; elapsed = 00:01:08 . Memory (MB): peak = 2502.254 ; gain = 24.883 ; free physical = 57162 ; free virtual = 128344  Phase 7 Route finalize  Router Utilization Summary  Global Vertical Routing Utilization = 0.400531 %  Global Horizontal Routing Utilization = 0.496164 %  Routable Net Status\*  \*Does **not** include unroutable nets such as driverless **and** loadless.  Run report\_route\_status **for** detailed **report**.  Number **of** Failed Nets = 0  Number **of** Unrouted Nets = 0  Number **of** Partially Routed Nets = 0  Number **of** Node Overlaps = 0  Congestion **Report** North Dir 1x1 Area, Max Cong = 27.027%, No Congested Regions. South Dir 1x1 Area, Max Cong = 45.9459%, No Congested Regions. East Dir 1x1 Area, Max Cong = 42.6471%, No Congested Regions. West Dir 1x1 Area, Max Cong = 36.7647%, No Congested Regions.  *------------------------------* Reporting congestion hotspots *------------------------------* Direction: North *----------------* Congested clusters found at Level 0 Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0 Direction: South *----------------* Congested clusters found at Level 0 Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0 Direction: East *----------------* Congested clusters found at Level 0 Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0 Direction: West *----------------* Congested clusters found at Level 0 Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0  Phase 7 Route finalize | Checksum: 899e7dc4  Time (s): cpu = 00:01:12 ; elapsed = 00:01:08 . Memory (MB): peak = 2502.254 ; gain = 24.883 ; free physical = 57161 ; free virtual = 128344  Phase 8 Verifying routed nets   Verification completed successfully Phase 8 Verifying routed nets | Checksum: 899e7dc4  Time (s): cpu = 00:01:12 ; elapsed = 00:01:08 . Memory (MB): peak = 2505.254 ; gain = 27.883 ; free physical = 57160 ; free virtual = 128342  Phase 9 Depositing Routes Phase 9 Depositing Routes | Checksum: d2f29b40  Time (s): cpu = 00:01:12 ; elapsed = 00:01:09 . Memory (MB): peak = 2505.254 ; gain = 27.883 ; free physical = 57161 ; free virtual = 128343 INFO: [Route 35-16] Router Completed Successfully  Time (s): cpu = 00:01:12 ; elapsed = 00:01:09 . Memory (MB): peak = 2505.254 ; gain = 27.883 ; free physical = 57196 ; free virtual = 128379  Routing **Is** Done. INFO: [Common 17-83] Releasing license: Implementation 8 Infos, 0 Warnings, 0 Critical Warnings **and** 0 Errors encountered. route\_design completed successfully route\_design: Time (s): cpu = 00:01:17 ; elapsed = 00:01:17 . Memory (MB): peak = 2505.254 ; gain = 27.883 ; free physical = 57196 ; free virtual = 128379 # write\_bitstream -**force** REGcircuit.bit Command: write\_bitstream -**force** REGcircuit.bit Attempting **to** get a license **for** feature 'Implementation' **and**/**or** device 'xc7a100t' INFO: [Common 17-349] Got license **for** feature 'Implementation' **and**/**or** device 'xc7a100t' Running DRC as a precondition **to** command write\_bitstream INFO: [IP\_Flow 19-234] Refreshing IP repositories INFO: [IP\_Flow 19-1704] No user IP repositories specified INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado\_2018.2/Vivado/2018.2/data/ip'. INFO: [DRC 23-27] Running DRC **with** 8 threads WARNING: [DRC CFGBVS-1] Missing CFGBVS **and** CONFIG\_VOLTAGE Design Properties: Neither the CFGBVS **nor** CONFIG\_VOLTAGE voltage **property** **is** set **in** the current\_design. **Configuration** bank voltage **select** (CFGBVS) must be set **to** VCCO **or** GND, **and** CONFIG\_VOLTAGE must be set **to** the correct **configuration** voltage, **in** order **to** determine the I/O voltage support **for** the pins **in** bank 0. It **is** suggested **to** specify these either using the 'Edit Device Properties' **function** **in** the GUI **or** directly **in** the XDC **file** using the following syntax:   set\_property CFGBVS value1 [current\_design]  #where value1 **is** either VCCO **or** GND   set\_property CONFIG\_VOLTAGE value2 [current\_design]  #where value2 **is** the voltage provided **to** **configuration** bank 0  Refer **to** the device **configuration** user guide **for** more information. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[0] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[10] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[11] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[12] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[13] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[14] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[15] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[16] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[17] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[18] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[19] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[1] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[20] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[21] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[22] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[23] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[24] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[25] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[26] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[27] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[28] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[29] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[2] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[30] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[31] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[3] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[4] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[5] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[6] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[7] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[8] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC IOSR-1] IOB set reset sharing: IO A[9] connects **to** flops which have these U1/regarray[28][31]\_i\_1\_n\_0, U1/regarray[9][31]\_i\_1\_n\_0, U1/regarray[7][31]\_i\_1\_n\_0, U1/regarray[8][31]\_i\_1\_n\_0, U1/regarray[18][31]\_i\_1\_n\_0, U1/regarray[2][31]\_i\_1\_n\_0, U1/regarray[15][31]\_i\_1\_n\_0, U1/regarray[24][31]\_i\_1\_n\_0, U1/regarray[20][31]\_i\_1\_n\_0, U1/regarray[27][31]\_i\_1\_n\_0, U1/regarray[5][31]\_i\_1\_n\_0, U1/regarray[10][31]\_i\_1\_n\_0, U1/regarray[1][31]\_i\_1\_n\_0, U1/regarray[0][31]\_i\_1\_n\_0, U1/regarray[29][31]\_i\_1\_n\_0... **and** (the first 15 **of** 32 listed) set/reset signals. **For** optimal IOB flop packing there should be only one set/reset **signal** coming into the IOB. WARNING: [DRC UCIO-1] Unconstrained Logical **Port**: 114 **out** **of** 114 logical ports have no user assigned specific location constraint (LOC). This may cause I/O contention **or** incompatibility **with** the board power **or** connectivity affecting performance, **signal** integrity **or** **in** extreme cases cause damage **to** the device **or** the components **to** which it **is** connected. **To** correct this violation, specify **all** pin locations. This design will fail **to** **generate** a bitstream unless **all** logical ports have a user specified site LOC constraint defined. **To** allow bitstream creation **with** unspecified pin locations (**not** recommended), **use** this command: set\_property **SEVERITY** {Warning} [get\_drc\_checks UCIO-1]. NOTE: **When** using the Vivado Runs infrastructure (e.g. launch\_runs Tcl command), add this command **to** a .tcl **file** **and** add that **file** as a pre-hook **for** write\_bitstream step **for** the implementation run. Problem ports: A[31:0], E[4:0], F[4:0], G[4:0], H[31:0], I[31:0], B, C, **and** D. INFO: [Vivado 12-3199] DRC finished **with** 0 Errors, 34 Warnings INFO: [Vivado 12-3200] Please refer **to** the DRC **report** (report\_drc) **for** more information. INFO: [Designutils 20-2272] Running write\_bitstream **with** 8 threads. Loading data files... Loading site data... Loading route data... Processing options... Creating bitmap... Creating bitstream... Writing bitstream ./REGcircuit.bit... INFO: [Vivado 12-1842] Bitgen Completed Successfully. INFO: [Common 17-83] Releasing license: Implementation 10 Infos, 34 Warnings, 0 Critical Warnings **and** 0 Errors encountered. write\_bitstream completed successfully write\_bitstream: Time (s): cpu = 00:00:32 ; elapsed = 00:01:00 . Memory (MB): peak = 2850.074 ; gain = 344.820 ; free physical = 57160 ; free virtual = 128346 INFO: [Common 17-206] Exiting Vivado at Tue Oct 27 10:42:05 2020... |
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