Report

on

COEN 316 Laboratory Experiment #3

**Next-address Unit**

Submitted to

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*Instructor’s name*

Date Performed: October 10th, 2020

Date Submitted: November 24th, 2020

By

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Lab section: DI-X

“I certify that this submission is my original work and meets the Faculty's Expectations of Originality”



40094237 19/11/2020

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# **Objective:**

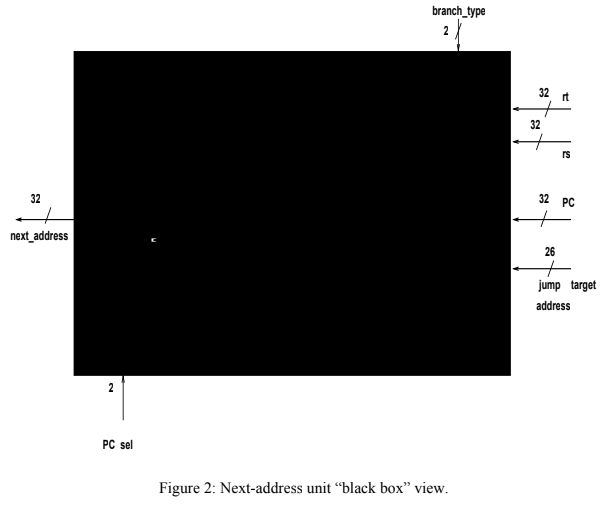
In this lab, we will use digital logic simulation and synthesis using Modelsim, and Xilinx ISE (Vivado) to become acquainted with the VHDL simulation software tool and FPGA implementation software tools. During this lab, we will simulate a Next-Address unit that will generate the next address and store it in the program counter register of the system.

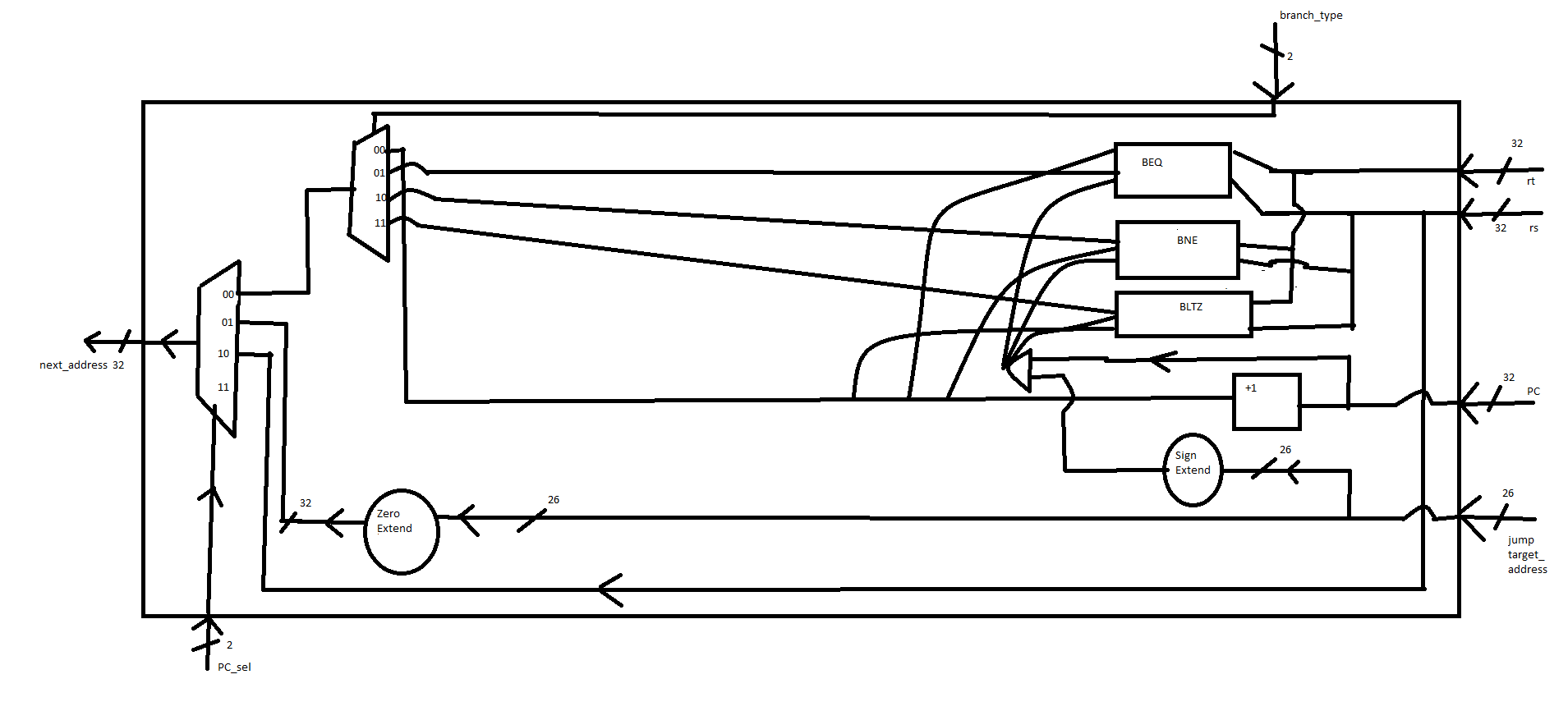
**Introduction:**

The lab consisted of designing a Next-Address unit using VHDL. We simulate the Next-Address unit of a processor and test possible operations that may happen on it. The unit uses 32 bit instructions and saves into 32 bits registers.

In normal operation, the program counter of the CPU is updated to point to the next instruction after every clock cycle. To point at the next instruction, it’s address is needed that can be the following address of the current one or it can be pointed to a completely different part of the memory by using a jump or branch instruction. Our design needs to be able to calculate the address of the next instruction for every case.

We are given the black box diagram below with the inputs and outputs of the unit. We then created an RTL diagram based on it with the necessary multiplexers and adders to complete the design. From the RTL schematic the VHDL code was derived and simulated using ModelSim. The ModelSim tested all the possible combinations of inputs to verify that the unit was functioning properly and producing the correct output.



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**RTL DESIGN**

**Results:**

**The complete VHDL code source for the register file:**

| **library** IEEE; **use** IEEE.std\_logic\_1164.**all**; **use** IEEE.std\_logic\_unsigned.**all**; **use** ieee.numeric\_std.**ALL**;  **entity** next\_address **is**  **port**(  *-- inputs*  rt, rs : **in** std\_logic\_vector(31 **downto** 0);   pc : **in** std\_logic\_vector(31 **downto** 0);  target\_address : **in** std\_logic\_vector(25 **downto** 0);  branch\_type : **in** std\_logic\_vector(1 **downto** 0);  pc\_sel : **in** std\_logic\_vector(1 **downto** 0);    *-- outputs*  next\_pc : **out** std\_logic\_vector(31 **downto** 0));   **end** next\_address ;   **architecture** arch\_next **of** next\_address **is**  **begin**    next\_addr: **process** (pc, pc\_sel, branch\_type, rt, rs, target\_address)  *--intialize variables*  **variable** pc\_unsigned: unsigned(31 **downto** 0);  **variable** sign\_extended\_offset: unsigned(31 **downto** 0); *-- assuming 2's complement offset*    **begin**    pc\_unsigned := unsigned(pc);    **if** (target\_address(15) = '0') **then**  *--positive offset*  sign\_extended\_offset := unsigned("0000000000000000" & target\_address(15 **downto** 0));  **else**   *--negative offset*  sign\_extended\_offset := unsigned("1111111111111111" & target\_address(15 **downto** 0));  **end** **if**;    **case** pc\_sel **is**    **when** "00" => *--no jump, check for type of branch*    **case** branch\_type **is**     **when** "00" => *--no jump, PC = PC + 1*  next\_pc <= std\_logic\_vector(pc\_unsigned + 1);    **when** "01" => *--beq: PC = PC + 1 + sign\_extend(target\_address) iff rs=rt*    *--check equality*  **if** (rs = rt) **then**   next\_pc <= std\_logic\_vector(pc\_unsigned + 1 + sign\_extended\_offset);  **else** *-- condition fails, just PC = PC + 1;*   next\_pc <= std\_logic\_vector(pc\_unsigned + 1);   **end** **if**;    **when** "10" => *--bne: PC = PC + 1 + sign\_extend(target\_address[15:0]) iff rs/=rt*    *--check inequality*  **if** (rs /= rt) **then**   next\_pc <= std\_logic\_vector(pc\_unsigned + 1 + sign\_extended\_offset);  **else** *-- condition fails, just PC = PC + 1;*   next\_pc <= std\_logic\_vector(pc\_unsigned + 1);   **end** **if**;    **when** "11" => *--bltz: PC = PC + 1 + sign\_extend(target\_address[15:0]) if rs < 0*    *--if negative*  **if** (signed(rs) < 0) **then**   next\_pc <= std\_logic\_vector(pc\_unsigned + 1 + sign\_extended\_offset);  **else** *-- condition fails, just PC = PC + 1;*   next\_pc <= std\_logic\_vector(pc\_unsigned + 1);   **end** **if**;      **when** **others** =>  next\_pc <= std\_logic\_vector(pc\_unsigned + 1);   **end** **case**;     **when** "01" => *-- pseudo-direct jump: PC = '000000' & target\_address*  next\_pc <= "000000" & target\_address;    **when** "10" => *-- jump register: PC = contents of register rs*  next\_pc <= rs;    *--Error code, shouldnt happen*  **when** **others** =>   next\_pc <= std\_logic\_vector(pc\_unsigned + 1);     **end** **case**;     **end** **process**;    **end** arch\_next; |
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**Xilinx XDC file:**

| # Vivado does **not** support old UCF syntax # must **use** XDC syntax  # input ports A,B,C,D are connected **to** Switches 0,1,2,3 # **of** the Nexys board # output **port** E **is** connected **to** LED 0 **of** the Nexys board  set\_property IOSTANDARD LVCMOS33 [ get\_ports { A } ] ; set\_property IOSTANDARD LVCMOS33 [ get\_ports { B } ] ; set\_property IOSTANDARD LVCMOS33 [ get\_ports { C } ] ; set\_property IOSTANDARD LVCMOS33 [ get\_ports { D } ] ; set\_property IOSTANDARD LVCMOS33 [ get\_ports { E } ] ; set\_property IOSTANDARD LVCMOS33 [ get\_ports { F } ] ; set\_property IOSTANDARD LVCMOS33 [ get\_ports { G } ] ; |
| --- |

**The TCL script file:**

| # TCL script **for** running vivado **in** batch mode **to** synthesize # **To** run the script first source the Vivado env **file**: # source /CMC/tools/xilinx/Vivado\_2018.2/Vivado/2018.2/settings64\_CMC\_central\_license.csh #**Then** issue the following command from the Linux prompt: # vivado -log tedcircuit.log -mode batch -source tedcircuit\_script.tcl # read **in** the VHDL source code files **and** the xdc constraints **file**  set\_property **SEVERITY** {Warning} [get\_drc\_checks UCIO-1]  read\_vhdl { ../Code/next\_address.vhd ../Code/nextAddressCircuit.vhd } read\_xdc NEXTADRcircuit.xdc  # the -top refers **to** the top level VHDL **entity** name # the -part specfies the target Xilinx FPGA  synth\_design -top NextCircuit -part xc7a100tcsg324-1  opt\_design place\_design route\_design # **generate** the bitsteam **file** write\_bitstream -**force** Nextcircuit.bit |
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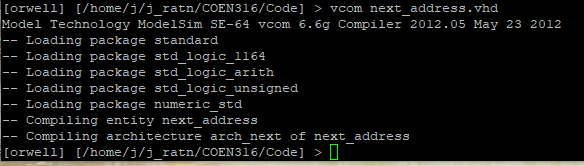
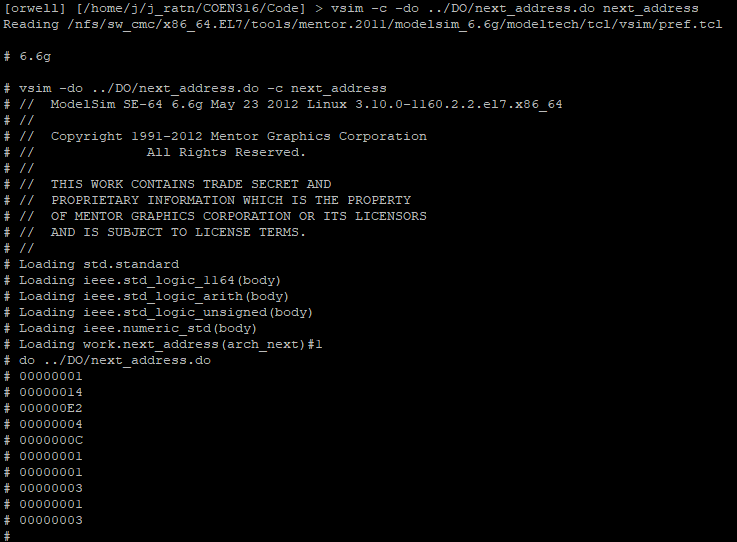
**The DO file:**

| # do **file** **to** test the next\_address  add wave rs add wave rt add wave pc add wave target\_address add wave branch\_type add wave pc\_sel add wave next\_pc  #jump there ; jump **to** memory location "there" #jr rs ; jump **to** memory location whose address **is** **in** rs #beq rs,rt, **loop** ; jump **to** memory location "loop" **if** rs=rt #bne rs,rt, **loop** ; jump **to** memory location "loop" **if** rs /= rt #bltz rs, **loop** ; jump **to** memory location "loop" **if** rs < 0  #JUMPS  #test no jump, no branch #expect pc\_next = x"00000001" **force** pc x"00000000"  **force** pc\_sel "00" **force** branch\_type "00" run 2 examine -radix hex next\_pc  #test jump there #expect pc\_next= x"000000014" #offet **is** 1 **force** pc x"00000000"  **force** target\_address "00000000000000000000010100"  **force** pc\_sel "01" run 2 examine -radix hex next\_pc  #test jr rs #expect pc\_next=x"000000E2" #rs holds E2 **force** pc x"00000000"  **force** rs x"000000E2"  **force** pc\_sel "10" run 2 examine -radix hex next\_pc  #BRANCHING #*-----------------------------------------------------*  #test beq rs,rt, **loop** **with** rs = rt #expect pc\_next= x"00000004" #rs holds 1 #rt holds 1 **force** pc x"00000000"  **force** rs x"00000001"  **force** rt x"00000001"  **force** target\_address "00000000000000000000000011" **force** pc\_sel "00" **force** branch\_type "01" run 2 examine -radix hex next\_pc  #test beq rs,rt, **loop** **with** rs = rt #pc\_next should be x"0000000C" #rs holds 1 #rt holds 1 **force** pc x"00000015"  **force** rs x"00000001"  **force** rt x"00000001"  **force** target\_address "00000000001111111111110110" **force** pc\_sel "00" **force** branch\_type "01" run 2 examine -radix hex next\_pc  #test beq rs,rt, **loop** **with** rs /= rt #pc\_next should be x"00000001" #rs holds 1 #rt holds 3 **force** pc x"00000000"  **force** rs x"00000001"  **force** rt x"00000003"  **force** target\_address "00000000000000000000000001" **force** pc\_sel "00" **force** branch\_type "01" run 2 examine -radix hex next\_pc  #test bne rs,rt, **loop** **with** rs = rt #pc should **not** change **use** offset, increment by 1 #next\_pc pc x"00000001"  #rs holds 1 #rt holds 1 **force** pc x"00000000"  **force** rs x"00000001"  **force** rt x"00000001"  **force** target\_address "00000000000000000000000111" **force** pc\_sel "00" **force** branch\_type "10" run 2 examine -radix hex next\_pc  #test bne rs,rt, **loop** **with** rs /= rt #expect pc\_next=x"00000003" #start from 00000000 #rs holds 1 #rt holds 3 #target **is** 2 **force** pc x"00000000"  **force** rs x"00000001" **force** rt x"00000003"  **force** target\_address "00000000000000000000000010" **force** pc\_sel "00" **force** branch\_type "10" run 2 examine -radix hex next\_pc   #test bltz rs, **loop** **with** rs > 0 #expect pc\_next= x"00000001" #rs holds 1 #target **is** 6 **force** pc x"00000000"  **force** rs x"00000001"  **force** target\_address "00000000000000000000000110" **force** pc\_sel "00" **force** branch\_type "11" run 2 examine -radix hex next\_pc  #test bltz rs, **loop** **with** rs < 0 #expect pc\_next= x"00000003" #rs holds F0000000 #target **is** 2 **force** pc x"00000000"  **force** rs x"F0000000"  **force** target\_address "00000000000000000000000010" **force** pc\_sel "00" **force** branch\_type "11" run 2 examine -radix hex next\_pc |
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**The log file is available in the appendix.**

The log file does not have any warnings of importance to us that will affect the execution of the program.

**Simulation and implementation results using port maps:**

* The vcom of the vhdl code for the reg file
  + 
* The Modelsim simulation
  + 
  + The outputted numbers are the next PC that the system gives, they are accurate and consistent to the expected PC value given in the DO file comments. Hence, we can conclude that the system works perfectly.
  + The result of the simulations with our do file shows that the results are accurate to what we expected to get from the do file.

**Conclusion:**

In conclusion, the experiment was done successfully since the results obtained are accurate compared to the theoretical results. We learned and understood all the steps to do a simulation of a register file.This is shown by the Modelsim simulations testing with the given DO file for all possible operations and it produced the correct outputs. The lab was successful in designing a next-address unit. All of the combinations of inputs were tested and the correct outputs were obtained. The jump instructions would target the location of the jump and the branch instructions would check the condition and branch relative to the PC.

**Appendix:**

The log file:

| #*-----------------------------------------------------------* # Vivado v2018.2 (64-bit) # SW Build 2258646 **on** Thu Jun 14 20:02:38 MDT 2018 # IP Build 2256618 **on** Thu Jun 14 22:10:49 MDT 2018 # Start **of** session at: Tue Nov 10 09:56:21 2020 # **Process** ID: 40020 # Current directory: /nfs/home/j/j\_ratn/COEN316/NEXTADRCIRCUIT\_SCRIPT # Command line: vivado -log nextAddrCircuit.log -mode batch -source nextaddress\_script.tcl # Log **file**: /nfs/home/j/j\_ratn/COEN316/NEXTADRCIRCUIT\_SCRIPT/nextAddrCircuit.log # Journal **file**: /nfs/home/j/j\_ratn/COEN316/NEXTADRCIRCUIT\_SCRIPT/vivado.jou #*-----------------------------------------------------------* source nextaddress\_script.tcl # set\_property **SEVERITY** {Warning} [get\_drc\_checks UCIO-1] # read\_vhdl { ../Code/next\_address.vhd ../Code/nextAddressCircuit.vhd } # read\_xdc NEXTADRcircuit.xdc # synth\_design -top NextCircuit -part xc7a100tcsg324-1 Command: synth\_design -top NextCircuit -part xc7a100tcsg324-1 Starting synth\_design Attempting **to** get a license **for** feature 'Synthesis' **and**/**or** device 'xc7a100t' INFO: [Common 17-349] Got license **for** feature 'Synthesis' **and**/**or** device 'xc7a100t' INFO: Launching helper **process** **for** spawning children vivado processes INFO: Helper **process** launched **with** PID 40087  *---------------------------------------------------------------------------------* Starting RTL Elaboration : Time (s): cpu = 00:00:04 ; elapsed = 00:00:10 . Memory (MB): peak = 1468.594 ; gain = 86.727 ; free physical = 1827 ; free virtual = 129967 *---------------------------------------------------------------------------------* INFO: [Synth 8-638] synthesizing module 'NextCircuit' [/nfs/home/j/j\_ratn/COEN316/Code/nextAddressCircuit.vhd:11] INFO: [Synth 8-3491] module 'next\_address' declared at '/nfs/home/j/j\_ratn/COEN316/Code/next\_address.vhd:6' bound **to** instance 'U1' **of** **component** 'nextadr' [/nfs/home/j/j\_ratn/COEN316/Code/nextAddressCircuit.vhd:29] INFO: [Synth 8-638] synthesizing module 'next\_address' [/nfs/home/j/j\_ratn/COEN316/Code/next\_address.vhd:22] INFO: [Synth 8-226] **default** **block** **is** never used [/nfs/home/j/j\_ratn/COEN316/Code/next\_address.vhd:47] INFO: [Synth 8-256] done synthesizing module 'next\_address' (1#1) [/nfs/home/j/j\_ratn/COEN316/Code/next\_address.vhd:22] INFO: [Synth 8-256] done synthesizing module 'NextCircuit' (2#1) [/nfs/home/j/j\_ratn/COEN316/Code/nextAddressCircuit.vhd:11] *---------------------------------------------------------------------------------* Finished RTL Elaboration : Time (s): cpu = 00:00:05 ; elapsed = 00:00:15 . Memory (MB): peak = 1513.234 ; gain = 131.367 ; free physical = 1832 ; free virtual = 129973 *---------------------------------------------------------------------------------*  **Report** Check Netlist:  +*------+------------------+-------+---------+-------+------------------+* | |Item |Errors |Warnings |Status |Description | +*------+------------------+-------+---------+-------+------------------+* |1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets | +*------+------------------+-------+---------+-------+------------------+* *---------------------------------------------------------------------------------* Start Handling Custom Attributes *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Handling Custom Attributes : Time (s): cpu = 00:00:06 ; elapsed = 00:00:16 . Memory (MB): peak = 1513.234 ; gain = 131.367 ; free physical = 1824 ; free virtual = 129965 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:06 ; elapsed = 00:00:16 . Memory (MB): peak = 1513.234 ; gain = 131.367 ; free physical = 1824 ; free virtual = 129965 *---------------------------------------------------------------------------------* INFO: [Device 21-403] Loading part xc7a100tcsg324-1 INFO: [Project 1-570] Preparing netlist **for** logic optimization  Processing XDC Constraints Initializing timing engine Parsing XDC **File** [/nfs/home/j/j\_ratn/COEN316/NEXTADRCIRCUIT\_SCRIPT/NEXTADRcircuit.xdc] Finished Parsing XDC **File** [/nfs/home/j/j\_ratn/COEN316/NEXTADRCIRCUIT\_SCRIPT/NEXTADRcircuit.xdc] Completed Processing XDC Constraints  INFO: [Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed.  Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 1837.199 ; gain = 0.000 ; free physical = 1520 ; free virtual = 129770 *---------------------------------------------------------------------------------* Finished Constraint Validation : Time (s): cpu = 00:00:22 ; elapsed = 00:02:03 . Memory (MB): peak = 1837.199 ; gain = 455.332 ; free physical = 1508 ; free virtual = 129809 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Loading Part **and** Timing Information *---------------------------------------------------------------------------------* Loading part: xc7a100tcsg324-1 *---------------------------------------------------------------------------------* Finished Loading Part **and** Timing Information : Time (s): cpu = 00:00:22 ; elapsed = 00:02:03 . Memory (MB): peak = 1837.199 ; gain = 455.332 ; free physical = 1508 ; free virtual = 129809 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Applying 'set\_property' XDC Constraints *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:23 ; elapsed = 00:02:05 . Memory (MB): peak = 1837.199 ; gain = 455.332 ; free physical = 1493 ; free virtual = 129807 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:23 ; elapsed = 00:02:06 . Memory (MB): peak = 1837.199 ; gain = 455.332 ; free physical = 1514 ; free virtual = 129828 *---------------------------------------------------------------------------------*  **Report** RTL Partitions:  +-+*--------------+------------+----------+* | |RTL Partition |Replication |Instances | +-+*--------------+------------+----------+* +-+*--------------+------------+----------+* *---------------------------------------------------------------------------------* Start RTL **Component** Statistics  *---------------------------------------------------------------------------------* Detailed RTL **Component** Info :  +*---Adders :*   2 Input 32 Bit Adders := 2  +*---Muxes :*   2 Input 32 Bit Muxes := 4   4 Input 32 Bit Muxes := 2  *---------------------------------------------------------------------------------* Finished RTL **Component** Statistics  *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start RTL Hierarchical **Component** Statistics  *---------------------------------------------------------------------------------* Hierarchical RTL **Component** **report**  Module next\_address  Detailed RTL **Component** Info :  +*---Adders :*   2 Input 32 Bit Adders := 2  +*---Muxes :*   2 Input 32 Bit Muxes := 4   4 Input 32 Bit Muxes := 2  *---------------------------------------------------------------------------------* Finished RTL Hierarchical **Component** Statistics *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Part Resource Summary *---------------------------------------------------------------------------------* Part Resources: DSPs: 240 (col length:80) BRAMs: 270 (col length: RAMB18 80 RAMB36 40) *---------------------------------------------------------------------------------* Finished Part Resource Summary *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Cross Boundary **and** Area Optimization *---------------------------------------------------------------------------------* Warning: Parallel synthesis criteria **is** **not** met  *---------------------------------------------------------------------------------* Finished Cross Boundary **and** Area Optimization : Time (s): cpu = 00:00:25 ; elapsed = 00:02:08 . Memory (MB): peak = 1860.480 ; gain = 478.613 ; free physical = 1493 ; free virtual = 129809 *---------------------------------------------------------------------------------*  **Report** RTL Partitions:  +-+*--------------+------------+----------+* | |RTL Partition |Replication |Instances | +-+*--------------+------------+----------+* +-+*--------------+------------+----------+* *---------------------------------------------------------------------------------* Start Applying XDC Timing Constraints *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:38 ; elapsed = 00:02:41 . Memory (MB): peak = 1862.465 ; gain = 480.598 ; free physical = 1323 ; free virtual = 129666 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Timing Optimization *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Timing Optimization : Time (s): cpu = 00:00:38 ; elapsed = 00:02:41 . Memory (MB): peak = 1862.465 ; gain = 480.598 ; free physical = 1322 ; free virtual = 129665 *---------------------------------------------------------------------------------*  **Report** RTL Partitions:  +-+*--------------+------------+----------+* | |RTL Partition |Replication |Instances | +-+*--------------+------------+----------+* +-+*--------------+------------+----------+* *---------------------------------------------------------------------------------* Start Technology Mapping *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Technology Mapping : Time (s): cpu = 00:00:38 ; elapsed = 00:02:41 . Memory (MB): peak = 1863.465 ; gain = 481.598 ; free physical = 1322 ; free virtual = 129665 *---------------------------------------------------------------------------------*  **Report** RTL Partitions:  +-+*--------------+------------+----------+* | |RTL Partition |Replication |Instances | +-+*--------------+------------+----------+* +-+*--------------+------------+----------+* *---------------------------------------------------------------------------------* Start IO Insertion *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Flattening Before IO Insertion *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Flattening Before IO Insertion *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Final Netlist Cleanup *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Final Netlist Cleanup *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished IO Insertion : Time (s): cpu = 00:00:40 ; elapsed = 00:02:44 . Memory (MB): peak = 1863.469 ; gain = 481.602 ; free physical = 1324 ; free virtual = 129667 *---------------------------------------------------------------------------------*  **Report** Check Netlist:  +*------+------------------+-------+---------+-------+------------------+* | |Item |Errors |Warnings |Status |Description | +*------+------------------+-------+---------+-------+------------------+* |1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets | +*------+------------------+-------+---------+-------+------------------+* *---------------------------------------------------------------------------------* Start Renaming Generated Instances *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Renaming Generated Instances : Time (s): cpu = 00:00:40 ; elapsed = 00:02:44 . Memory (MB): peak = 1863.469 ; gain = 481.602 ; free physical = 1322 ; free virtual = 129665 *---------------------------------------------------------------------------------*  **Report** RTL Partitions:  +-+*--------------+------------+----------+* | |RTL Partition |Replication |Instances | +-+*--------------+------------+----------+* +-+*--------------+------------+----------+* *---------------------------------------------------------------------------------* Start Rebuilding User Hierarchy *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:40 ; elapsed = 00:02:44 . Memory (MB): peak = 1863.469 ; gain = 481.602 ; free physical = 1322 ; free virtual = 129665 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Renaming Generated Ports *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Renaming Generated Ports : Time (s): cpu = 00:00:40 ; elapsed = 00:02:44 . Memory (MB): peak = 1863.469 ; gain = 481.602 ; free physical = 1322 ; free virtual = 129665 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Handling Custom Attributes *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Handling Custom Attributes : Time (s): cpu = 00:00:40 ; elapsed = 00:02:44 . Memory (MB): peak = 1863.469 ; gain = 481.602 ; free physical = 1322 ; free virtual = 129665 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Renaming Generated Nets *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Finished Renaming Generated Nets : Time (s): cpu = 00:00:40 ; elapsed = 00:02:44 . Memory (MB): peak = 1863.469 ; gain = 481.602 ; free physical = 1321 ; free virtual = 129664 *---------------------------------------------------------------------------------* *---------------------------------------------------------------------------------* Start Writing Synthesis **Report** *---------------------------------------------------------------------------------*  **Report** BlackBoxes:  +-+*--------------+----------+* | |BlackBox name |Instances | +-+*--------------+----------+* +-+*--------------+----------+*  **Report** Cell Usage:  +*------+-------+------+* | |Cell |Count | +*------+-------+------+* |1 |CARRY4 | 22| |2 |LUT1 | 2| |3 |LUT2 | 33| |4 |LUT3 | 6| |5 |LUT4 | 29| |6 |LUT5 | 1| |7 |LUT6 | 53| |8 |IBUF | 126| |9 |OBUF | 32| +*------+-------+------+*  **Report** Instance Areas:  +*------+---------+-------------+------+* | |Instance |Module |Cells | +*------+---------+-------------+------+* |1 |top | | 304| |2 | U1 |next\_address | 82| +*------+---------+-------------+------+* *---------------------------------------------------------------------------------* Finished Writing Synthesis **Report** : Time (s): cpu = 00:00:40 ; elapsed = 00:02:44 . Memory (MB): peak = 1863.469 ; gain = 481.602 ; free physical = 1321 ; free virtual = 129664 *---------------------------------------------------------------------------------* Synthesis finished **with** 0 errors, 0 critical warnings **and** 0 warnings. Synthesis Optimization Runtime : Time (s): cpu = 00:00:27 ; elapsed = 00:01:07 . Memory (MB): peak = 1863.469 ; gain = 157.637 ; free physical = 1375 ; free virtual = 129718 Synthesis Optimization Complete : Time (s): cpu = 00:00:40 ; elapsed = 00:02:44 . Memory (MB): peak = 1863.473 ; gain = 481.602 ; free physical = 1384 ; free virtual = 129727 INFO: [Project 1-571] Translating synthesized netlist INFO: [Netlist 29-17] Analyzing 148 Unisim elements **for** replacement INFO: [Netlist 29-28] Unisim Transformation completed **in** 0 CPU seconds INFO: [Project 1-570] Preparing netlist **for** logic optimization Parsing XDC **File** [/nfs/home/j/j\_ratn/COEN316/NEXTADRCIRCUIT\_SCRIPT/NEXTADRcircuit.xdc] Finished Parsing XDC **File** [/nfs/home/j/j\_ratn/COEN316/NEXTADRCIRCUIT\_SCRIPT/NEXTADRcircuit.xdc] INFO: [Opt 31-138] Pushed 0 inverter(s) **to** 0 load pin(s). INFO: [Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed.  INFO: [Common 17-83] Releasing license: Synthesis 17 Infos, 0 Warnings, 0 Critical Warnings **and** 0 Errors encountered. synth\_design completed successfully synth\_design: Time (s): cpu = 00:00:43 ; elapsed = 00:02:49 . Memory (MB): peak = 1911.484 ; gain = 542.344 ; free physical = 1372 ; free virtual = 129715 # opt\_design Command: opt\_design Attempting **to** get a license **for** feature 'Implementation' **and**/**or** device 'xc7a100t' INFO: [Common 17-349] Got license **for** feature 'Implementation' **and**/**or** device 'xc7a100t' Running DRC as a precondition **to** command opt\_design  Starting DRC Task INFO: [DRC 23-27] Running DRC **with** 8 threads INFO: [Project 1-461] DRC finished **with** 0 Errors INFO: [Project 1-462] Please refer **to** the DRC **report** (report\_drc) **for** more information.  Time (s): cpu = 00:00:02 ; elapsed = 00:00:05 . Memory (MB): peak = 1975.516 ; gain = 64.031 ; free physical = 1373 ; free virtual = 129716  Starting Cache Timing Information Task INFO: [Timing 38-35] Done setting XDC timing constraints. Ending Cache Timing Information Task | Checksum: 1d3e210cc  Time (s): cpu = 00:00:10 ; elapsed = 00:01:27 . Memory (MB): peak = 2304.688 ; gain = 329.172 ; free physical = 1124 ; free virtual = 129467  Starting Logic Optimization Task  Phase 1 Retarget INFO: [Opt 31-138] Pushed 0 inverter(s) **to** 0 load pin(s). INFO: [Opt 31-49] Retargeted 0 cell(s). Phase 1 Retarget | Checksum: 1d3e210cc  Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2304.688 ; gain = 0.000 ; free physical = 1120 ; free virtual = 129464 INFO: [Opt 31-389] Phase Retarget created 0 cells **and** removed 0 cells  Phase 2 **Constant** propagation INFO: [Opt 31-138] Pushed 0 inverter(s) **to** 0 load pin(s). Phase 2 **Constant** propagation | Checksum: 1d3e210cc  Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.12 . Memory (MB): peak = 2304.688 ; gain = 0.000 ; free physical = 1120 ; free virtual = 129463 INFO: [Opt 31-389] Phase **Constant** propagation created 0 cells **and** removed 0 cells  Phase 3 Sweep Phase 3 Sweep | Checksum: 1f89fb344  Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.15 . Memory (MB): peak = 2304.688 ; gain = 0.000 ; free physical = 1120 ; free virtual = 129464 INFO: [Opt 31-389] Phase Sweep created 0 cells **and** removed 0 cells  Phase 4 BUFG optimization Phase 4 BUFG optimization | Checksum: 1f89fb344  Time (s): cpu = 00:00:00.09 ; elapsed = 00:00:00.18 . Memory (MB): peak = 2304.688 ; gain = 0.000 ; free physical = 1120 ; free virtual = 129463 INFO: [Opt 31-662] Phase BUFG optimization created 0 cells **of** which 0 are BUFGs **and** removed 0 cells.  Phase 5 Shift **Register** Optimization Phase 5 Shift **Register** Optimization | Checksum: a65be4bb  Time (s): cpu = 00:00:00.11 ; elapsed = 00:00:00.23 . Memory (MB): peak = 2304.688 ; gain = 0.000 ; free physical = 1119 ; free virtual = 129462 INFO: [Opt 31-389] Phase Shift **Register** Optimization created 0 cells **and** removed 0 cells  Phase 6 Post Processing Netlist Phase 6 Post Processing Netlist | Checksum: a65be4bb  Time (s): cpu = 00:00:00.12 ; elapsed = 00:00:00.24 . Memory (MB): peak = 2304.688 ; gain = 0.000 ; free physical = 1119 ; free virtual = 129462 INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells **and** removed 0 cells  Starting Connectivity Check Task  Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2304.688 ; gain = 0.000 ; free physical = 1119 ; free virtual = 129462 Ending Logic Optimization Task | Checksum: a65be4bb  Time (s): cpu = 00:00:00.12 ; elapsed = 00:00:00.25 . Memory (MB): peak = 2304.688 ; gain = 0.000 ; free physical = 1119 ; free virtual = 129462  Starting Power Optimization Task INFO: [Pwropt 34-132] Skipping clock gating **for** clocks **with** a period < 2.00 ns. Ending Power Optimization Task | Checksum: a65be4bb  Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2304.688 ; gain = 0.000 ; free physical = 1115 ; free virtual = 129458  Starting Final Cleanup Task Ending Final Cleanup Task | Checksum: a65be4bb  Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2304.688 ; gain = 0.000 ; free physical = 1115 ; free virtual = 129458 INFO: [Common 17-83] Releasing license: Implementation 16 Infos, 0 Warnings, 0 Critical Warnings **and** 0 Errors encountered. opt\_design completed successfully opt\_design: Time (s): cpu = 00:00:13 ; elapsed = 00:01:33 . Memory (MB): peak = 2304.688 ; gain = 393.203 ; free physical = 1115 ; free virtual = 129458 # place\_design Command: place\_design Attempting **to** get a license **for** feature 'Implementation' **and**/**or** device 'xc7a100t' INFO: [Common 17-349] Got license **for** feature 'Implementation' **and**/**or** device 'xc7a100t' INFO: [DRC 23-27] Running DRC **with** 8 threads INFO: [Vivado\_Tcl 4-198] DRC finished **with** 0 Errors INFO: [Vivado\_Tcl 4-199] Please refer **to** the DRC **report** (report\_drc) **for** more information. Running DRC as a precondition **to** command place\_design INFO: [DRC 23-27] Running DRC **with** 8 threads INFO: [Vivado\_Tcl 4-198] DRC finished **with** 0 Errors INFO: [Vivado\_Tcl 4-199] Please refer **to** the DRC **report** (report\_drc) **for** more information.  Starting Placer Task INFO: [Place 30-611] Multithreading enabled **for** place\_design using a maximum **of** 8 CPUs  Phase 1 Placer Initialization  Phase 1.1 Placer Initialization Netlist Sorting Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2368.719 ; gain = 0.000 ; free physical = 1092 ; free virtual = 129435 Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 602112b3  Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2368.719 ; gain = 0.000 ; free physical = 1092 ; free virtual = 129435 Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2368.719 ; gain = 0.000 ; free physical = 1092 ; free virtual = 129435  Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device INFO: [Timing 38-35] Done setting XDC timing constraints. Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 14044d28a  Time (s): cpu = 00:00:03 ; elapsed = 00:00:04 . Memory (MB): peak = 2368.719 ; gain = 0.000 ; free physical = 1082 ; free virtual = 129425  Phase 1.3 Build Placer Netlist Model Phase 1.3 Build Placer Netlist Model | Checksum: 180816566  Time (s): cpu = 00:00:03 ; elapsed = 00:00:04 . Memory (MB): peak = 2368.719 ; gain = 0.000 ; free physical = 1085 ; free virtual = 129428  Phase 1.4 Constrain Clocks/Macros Phase 1.4 Constrain Clocks/Macros | Checksum: 180816566  Time (s): cpu = 00:00:03 ; elapsed = 00:00:04 . Memory (MB): peak = 2368.719 ; gain = 0.000 ; free physical = 1084 ; free virtual = 129427 Phase 1 Placer Initialization | Checksum: 180816566  Time (s): cpu = 00:00:03 ; elapsed = 00:00:04 . Memory (MB): peak = 2368.719 ; gain = 0.000 ; free physical = 1084 ; free virtual = 129427  Phase 2 Global Placement  Phase 2.1 Floorplanning Phase 2.1 Floorplanning | Checksum: 180816566  Time (s): cpu = 00:00:03 ; elapsed = 00:00:04 . Memory (MB): peak = 2368.719 ; gain = 0.000 ; free physical = 1082 ; free virtual = 129425 WARNING: [Place 46-29] place\_design **is** **not** **in** timing mode. Skip physical synthesis **in** placer Phase 2 Global Placement | Checksum: 1560dbaf6  Time (s): cpu = 00:00:10 ; elapsed = 00:00:16 . Memory (MB): peak = 2456.758 ; gain = 88.039 ; free physical = 1065 ; free virtual = 129409  Phase 3 Detail Placement  Phase 3.1 Commit Multi Column Macros Phase 3.1 Commit Multi Column Macros | Checksum: 1560dbaf6  Time (s): cpu = 00:00:10 ; elapsed = 00:00:16 . Memory (MB): peak = 2456.758 ; gain = 88.039 ; free physical = 1065 ; free virtual = 129409  Phase 3.2 Commit Most Macros & LUTRAMs Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 98285ca0  Time (s): cpu = 00:00:10 ; elapsed = 00:00:16 . Memory (MB): peak = 2456.758 ; gain = 88.039 ; free physical = 1063 ; free virtual = 129407  Phase 3.3 Area Swap Optimization Phase 3.3 Area Swap Optimization | Checksum: a90435fe  Time (s): cpu = 00:00:10 ; elapsed = 00:00:16 . Memory (MB): peak = 2456.758 ; gain = 88.039 ; free physical = 1063 ; free virtual = 129407  Phase 3.4 Pipeline **Register** Optimization Phase 3.4 Pipeline **Register** Optimization | Checksum: a90435fe  Time (s): cpu = 00:00:10 ; elapsed = 00:00:16 . Memory (MB): peak = 2456.758 ; gain = 88.039 ; free physical = 1063 ; free virtual = 129407  Phase 3.5 Small Shape Detail Placement Phase 3.5 Small Shape Detail Placement | Checksum: 171bd39a0  Time (s): cpu = 00:00:11 ; elapsed = 00:00:16 . Memory (MB): peak = 2456.758 ; gain = 88.039 ; free physical = 1056 ; free virtual = 129400  Phase 3.6 Re-assign LUT pins Phase 3.6 Re-assign LUT pins | Checksum: 171bd39a0  Time (s): cpu = 00:00:11 ; elapsed = 00:00:17 . Memory (MB): peak = 2456.758 ; gain = 88.039 ; free physical = 1057 ; free virtual = 129401  Phase 3.7 Pipeline **Register** Optimization Phase 3.7 Pipeline **Register** Optimization | Checksum: 171bd39a0  Time (s): cpu = 00:00:11 ; elapsed = 00:00:17 . Memory (MB): peak = 2456.758 ; gain = 88.039 ; free physical = 1057 ; free virtual = 129401 Phase 3 Detail Placement | Checksum: 171bd39a0  Time (s): cpu = 00:00:11 ; elapsed = 00:00:17 . Memory (MB): peak = 2456.758 ; gain = 88.039 ; free physical = 1057 ; free virtual = 129401  Phase 4 Post Placement Optimization **and** Clean-Up  Phase 4.1 Post Commit Optimization Phase 4.1 Post Commit Optimization | Checksum: 171bd39a0  Time (s): cpu = 00:00:11 ; elapsed = 00:00:17 . Memory (MB): peak = 2456.758 ; gain = 88.039 ; free physical = 1058 ; free virtual = 129401  Phase 4.2 Post Placement Cleanup Phase 4.2 Post Placement Cleanup | Checksum: 171bd39a0  Time (s): cpu = 00:00:11 ; elapsed = 00:00:17 . Memory (MB): peak = 2456.758 ; gain = 88.039 ; free physical = 1059 ; free virtual = 129403  Phase 4.3 Placer Reporting Phase 4.3 Placer Reporting | Checksum: 171bd39a0  Time (s): cpu = 00:00:11 ; elapsed = 00:00:17 . Memory (MB): peak = 2456.758 ; gain = 88.039 ; free physical = 1059 ; free virtual = 129403  Phase 4.4 Final Placement Cleanup Phase 4.4 Final Placement Cleanup | Checksum: 171bd39a0  Time (s): cpu = 00:00:11 ; elapsed = 00:00:17 . Memory (MB): peak = 2456.758 ; gain = 88.039 ; free physical = 1059 ; free virtual = 129403 Phase 4 Post Placement Optimization **and** Clean-Up | Checksum: 171bd39a0  Time (s): cpu = 00:00:11 ; elapsed = 00:00:17 . Memory (MB): peak = 2456.758 ; gain = 88.039 ; free physical = 1059 ; free virtual = 129403 Ending Placer Task | Checksum: ebe45421  Time (s): cpu = 00:00:11 ; elapsed = 00:00:17 . Memory (MB): peak = 2456.758 ; gain = 88.039 ; free physical = 1074 ; free virtual = 129418 INFO: [Common 17-83] Releasing license: Implementation 10 Infos, 1 Warnings, 0 Critical Warnings **and** 0 Errors encountered. place\_design completed successfully place\_design: Time (s): cpu = 00:00:14 ; elapsed = 00:00:22 . Memory (MB): peak = 2456.758 ; gain = 152.070 ; free physical = 1074 ; free virtual = 129418 # route\_design Command: route\_design Attempting **to** get a license **for** feature 'Implementation' **and**/**or** device 'xc7a100t' INFO: [Common 17-349] Got license **for** feature 'Implementation' **and**/**or** device 'xc7a100t' Running DRC as a precondition **to** command route\_design INFO: [DRC 23-27] Running DRC **with** 8 threads INFO: [Vivado\_Tcl 4-198] DRC finished **with** 0 Errors INFO: [Vivado\_Tcl 4-199] Please refer **to** the DRC **report** (report\_drc) **for** more information.   Starting Routing Task INFO: [Route 35-254] Multithreading enabled **for** route\_design using a maximum **of** 8 CPUs Checksum: PlaceDB: 8bc3416e ConstDB: 0 ShapeSum: 602112b3 RouteDB: 0  Phase 1 Build RT Design Phase 1 Build RT Design | Checksum: 5fd33d21  Time (s): cpu = 00:00:51 ; elapsed = 00:01:22 . Memory (MB): peak = 2473.391 ; gain = 16.633 ; free physical = 607 ; free virtual = 128951 Post Restoration Checksum: NetGraph: 58d3c2e5 NumContArr: 6ff7a3c Constraints: 0 Timing: 0  Phase 2 Router Initialization INFO: [Route 35-64] No timing constraints were detected. The router will operate **in** resource-optimization mode.  Phase 2.1 Fix Topology Constraints Phase 2.1 Fix Topology Constraints | Checksum: 5fd33d21  Time (s): cpu = 00:00:51 ; elapsed = 00:01:22 . Memory (MB): peak = 2480.379 ; gain = 23.621 ; free physical = 575 ; free virtual = 128920  Phase 2.2 Pre Route Cleanup Phase 2.2 Pre Route Cleanup | Checksum: 5fd33d21  Time (s): cpu = 00:00:51 ; elapsed = 00:01:22 . Memory (MB): peak = 2480.379 ; gain = 23.621 ; free physical = 575 ; free virtual = 128920  Number **of** Nodes **with** overlaps = 0 Phase 2 Router Initialization | Checksum: 8fc0b246  Time (s): cpu = 00:00:52 ; elapsed = 00:01:23 . Memory (MB): peak = 2486.645 ; gain = 29.887 ; free physical = 570 ; free virtual = 128916  Phase 3 Initial Routing Phase 3 Initial Routing | Checksum: eda897cc  Time (s): cpu = 00:00:53 ; elapsed = 00:01:23 . Memory (MB): peak = 2486.645 ; gain = 29.887 ; free physical = 562 ; free virtual = 128909  Phase 4 Rip-up **And** Reroute  Phase 4.1 Global Iteration 0  Number **of** Nodes **with** overlaps = 8  Number **of** Nodes **with** overlaps = 0 Phase 4.1 Global Iteration 0 | Checksum: f3484f52  Time (s): cpu = 00:00:54 ; elapsed = 00:01:24 . Memory (MB): peak = 2486.645 ; gain = 29.887 ; free physical = 557 ; free virtual = 128903 Phase 4 Rip-up **And** Reroute | Checksum: f3484f52  Time (s): cpu = 00:00:54 ; elapsed = 00:01:24 . Memory (MB): peak = 2486.645 ; gain = 29.887 ; free physical = 557 ; free virtual = 128903  Phase 5 Delay **and** Skew Optimization Phase 5 Delay **and** Skew Optimization | Checksum: f3484f52  Time (s): cpu = 00:00:54 ; elapsed = 00:01:24 . Memory (MB): peak = 2486.645 ; gain = 29.887 ; free physical = 557 ; free virtual = 128903  Phase 6 Post Hold Fix  Phase 6.1 Hold Fix Iter Phase 6.1 Hold Fix Iter | Checksum: f3484f52  Time (s): cpu = 00:00:54 ; elapsed = 00:01:24 . Memory (MB): peak = 2486.645 ; gain = 29.887 ; free physical = 557 ; free virtual = 128903 Phase 6 Post Hold Fix | Checksum: f3484f52  Time (s): cpu = 00:00:54 ; elapsed = 00:01:24 . Memory (MB): peak = 2486.645 ; gain = 29.887 ; free physical = 557 ; free virtual = 128903  Phase 7 Route finalize  Router Utilization Summary  Global Vertical Routing Utilization = 0.209166 %  Global Horizontal Routing Utilization = 0.224851 %  Routable Net Status\*  \*Does **not** include unroutable nets such as driverless **and** loadless.  Run report\_route\_status **for** detailed **report**.  Number **of** Failed Nets = 0  Number **of** Unrouted Nets = 0  Number **of** Partially Routed Nets = 0  Number **of** Node Overlaps = 0  Congestion **Report** North Dir 1x1 Area, Max Cong = 17.1171%, No Congested Regions. South Dir 1x1 Area, Max Cong = 32.4324%, No Congested Regions. East Dir 1x1 Area, Max Cong = 41.1765%, No Congested Regions. West Dir 1x1 Area, Max Cong = 17.6471%, No Congested Regions.  *------------------------------* Reporting congestion hotspots *------------------------------* Direction: North *----------------* Congested clusters found at Level 0 Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0 Direction: South *----------------* Congested clusters found at Level 0 Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0 Direction: East *----------------* Congested clusters found at Level 0 Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0 Direction: West *----------------* Congested clusters found at Level 0 Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0  Phase 7 Route finalize | Checksum: f3484f52  Time (s): cpu = 00:00:55 ; elapsed = 00:01:24 . Memory (MB): peak = 2486.645 ; gain = 29.887 ; free physical = 554 ; free virtual = 128901  Phase 8 Verifying routed nets   Verification completed successfully Phase 8 Verifying routed nets | Checksum: f3484f52  Time (s): cpu = 00:00:55 ; elapsed = 00:01:25 . Memory (MB): peak = 2489.645 ; gain = 32.887 ; free physical = 550 ; free virtual = 128896  Phase 9 Depositing Routes Phase 9 Depositing Routes | Checksum: ce9f6391  Time (s): cpu = 00:00:55 ; elapsed = 00:01:25 . Memory (MB): peak = 2489.645 ; gain = 32.887 ; free physical = 550 ; free virtual = 128896 INFO: [Route 35-16] Router Completed Successfully  Time (s): cpu = 00:00:55 ; elapsed = 00:01:25 . Memory (MB): peak = 2489.645 ; gain = 32.887 ; free physical = 582 ; free virtual = 128929  Routing **Is** Done. INFO: [Common 17-83] Releasing license: Implementation 8 Infos, 0 Warnings, 0 Critical Warnings **and** 0 Errors encountered. route\_design completed successfully route\_design: Time (s): cpu = 00:00:58 ; elapsed = 00:01:31 . Memory (MB): peak = 2489.645 ; gain = 32.887 ; free physical = 581 ; free virtual = 128927 # write\_bitstream -**force** Nextcircuit.bit Command: write\_bitstream -**force** Nextcircuit.bit Attempting **to** get a license **for** feature 'Implementation' **and**/**or** device 'xc7a100t' INFO: [Common 17-349] Got license **for** feature 'Implementation' **and**/**or** device 'xc7a100t' Running DRC as a precondition **to** command write\_bitstream INFO: [IP\_Flow 19-234] Refreshing IP repositories INFO: [IP\_Flow 19-1704] No user IP repositories specified INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado\_2018.2/Vivado/2018.2/data/ip'. INFO: [DRC 23-27] Running DRC **with** 8 threads WARNING: [DRC CFGBVS-1] Missing CFGBVS **and** CONFIG\_VOLTAGE Design Properties: Neither the CFGBVS **nor** CONFIG\_VOLTAGE voltage **property** **is** set **in** the current\_design. **Configuration** bank voltage **select** (CFGBVS) must be set **to** VCCO **or** GND, **and** CONFIG\_VOLTAGE must be set **to** the correct **configuration** voltage, **in** order **to** determine the I/O voltage support **for** the pins **in** bank 0. It **is** suggested **to** specify these either using the 'Edit Device Properties' **function** **in** the GUI **or** directly **in** the XDC **file** using the following syntax:   set\_property CFGBVS value1 [current\_design]  #where value1 **is** either VCCO **or** GND   set\_property CONFIG\_VOLTAGE value2 [current\_design]  #where value2 **is** the voltage provided **to** **configuration** bank 0  Refer **to** the device **configuration** user guide **for** more information. WARNING: [DRC UCIO-1] Unconstrained Logical **Port**: 158 **out** **of** 158 logical ports have no user assigned specific location constraint (LOC). This may cause I/O contention **or** incompatibility **with** the board power **or** connectivity affecting performance, **signal** integrity **or** **in** extreme cases cause damage **to** the device **or** the components **to** which it **is** connected. **To** correct this violation, specify **all** pin locations. This design will fail **to** **generate** a bitstream unless **all** logical ports have a user specified site LOC constraint defined. **To** allow bitstream creation **with** unspecified pin locations (**not** recommended), **use** this command: set\_property **SEVERITY** {Warning} [get\_drc\_checks UCIO-1]. NOTE: **When** using the Vivado Runs infrastructure (e.g. launch\_runs Tcl command), add this command **to** a .tcl **file** **and** add that **file** as a pre-hook **for** write\_bitstream step **for** the implementation run. Problem ports: A[31:0], B[31:0], C[31:0], D[25:0], E[1:0], F[1:0], **and** G[31:0]. INFO: [Vivado 12-3199] DRC finished **with** 0 Errors, 2 Warnings INFO: [Vivado 12-3200] Please refer **to** the DRC **report** (report\_drc) **for** more information. INFO: [Designutils 20-2272] Running write\_bitstream **with** 8 threads. Loading data files... Loading site data... Loading route data... Processing options... Creating bitmap... Creating bitstream... Writing bitstream ./Nextcircuit.bit... INFO: [Vivado 12-1842] Bitgen Completed Successfully. INFO: [Common 17-83] Releasing license: Implementation 10 Infos, 2 Warnings, 0 Critical Warnings **and** 0 Errors encountered. write\_bitstream completed successfully write\_bitstream: Time (s): cpu = 00:00:29 ; elapsed = 00:00:57 . Memory (MB): peak = 2838.465 ; gain = 348.820 ; free physical = 759 ; free virtual = 128811 INFO: [Common 17-206] Exiting Vivado at Tue Nov 10 10:04:13 2020... |
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