jashshah0801@gmail.com
linkedin.com/jash-shah-98ab171a0

# Jash Shah

Contact: +1 (805) 695-6949
https://github.com/Jash-2000

## Education

**University of California, Santa Barbara** — **Santa Barbara, CA**
*M.S. in Electrical and Computer Engineering* — Sept 2024 – June 2026(Expected)

**Birla Institute of Technology and Science(BITS), Pilani** — **Pilani, India**
*B.E(Hons) in Electronics and Instrumentation Engineering* — Aug 2018 – Jul 2022

## Work Experience

**NVIDIA Corporation(Nvidia Graphics)** — **Bangalore, India**
*ASIC Design Verification Engineer* — Jan 2022 – Aug 2024

- Verified PCIe PHY IP using SystemVerilog UVM, covering unit, integration, and gate-level simulations; validated reset robustness, glitch behavior, and X-propagation, supporting high functional coverage.
- Developed and maintained testbench IP for logic analyzer, resets and error-logging features; and designed functional coverage framework for PCIe 6.0 error injection and multi-link PHY/DL.
- Handled PCIe PHY/DL, unified regression and testbench integration, enabling concurrent sub-block execution, resolving cross-team issues, and improving regression pass rate from 63% to 94%.

**Silvertouch Technologies** — **Gujarat, India**
*Edge ML, Summer Program* — May 2021 – Jul 2021

- Automated driving license test system using RFID and multi-camera vehicle identification and real-time tracking.
- Implemented real-time object tracking with SSD (Single Shot Multibox Detector) and Kalman filter, integrating pole-mounted cameras to detect and classify driving faults.

## Relevant Projects

- **Real-Time Embedded System with Audio Processing and Interactive Graphics**: Designed and implemented a hardware-accelerated wake-word detection pipeline on an AMD SoC FPGA using a 128-point radix-2 FFT, including fixed-point DSP blocks, ROM-based bit-reversal, FSM-driven control, and PCM-to-PDM microphone interfacing; integrated AXI-Stream and AXI-Lite with interrupt generation for low-latency hardware/software co-design.
- **Development of Probabilistic Compute Processor**: Designed sparsified Boltzmann-machine-based hardware for reversible logic, max-cut optimizers and full adders, achieving speed improvement (27% reduced critical path delay).
- **Fully Pipelined RISC-V Encryption Unit with MAC(Github)**: Developed a custom pipelined encryption processor in Verilog with integrated branch prediction, cache architecture, and hardware matrix multiplication unit; completed full custom schematic and layout implementation using Cadence Virtuoso.
- **Neural Particle Filter for Stochastic Noise(Paper Link)**: Demonstrated a spiking-event based algorithm to implement particle filtering and developed its equivalent digital design block.
- **Brain Control Interface Design(Paper Link)**: Developed an attention-based embedded microsleep alert system using wearable EEG, wavelet–STFT features, and signal-processing-aware models, achieving 90% test accuracy and significant kappa improvement over existing sleep staging methods.
- **Automated Generation of SystemVerilog Assertions from Golden Waveforms**: Built an AI-driven tool that converts golden waveforms (VCD, tabular, or image-based) into SystemVerilog assertions and testbench skeletons, automating timing verification and reducing manual SVA development.

## Leadership & Technical Experience

- **Inspired Karters - Formula Student (IKR-FS)**: Lead Embedded Systems Engineer for low-voltage vehicle electronics and safety-critical control systems, including multi-board PCB integration and CAN-based architectures. Implemented STM32-based control with advanced CAN communication and OTA support
- **Neuromorphic Smart Glasses (WIP)**: Leading development of smart glasses integrating neuromorphic algorithms with custom event-camera hardware for real-time eye tracking and gaze estimation, followed by a lightweight vision-language model for contextual understanding and intuitive HMI.

## Technical Skills

**Languages**: SystemVerilog (UVM), Verilog, C/C++, Python, MATLAB
**EDA Tools**: Synopsys VCS, Cadence Virtuoso, Vivado, ModelSim, HSPICE, LTSpice
**Methodologies**: UVM, SVA, functional coverage, STA, GLS, AXI, PCIe, FPGA, interconnect & buffer optimization