

To study timer and PLL

Analog Electronics Lab Experiment -9

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Lab Section: P5

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1. Objective

To study Timer and PLL

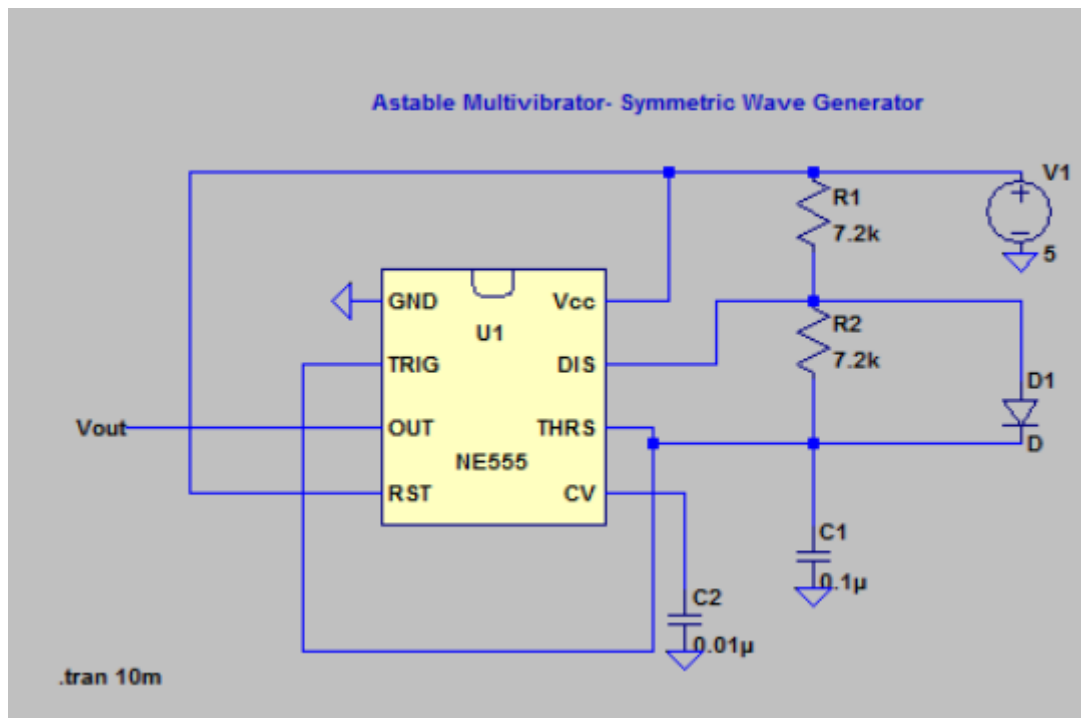
- 1) Astable Multivibrator (Symmetrical Square Wave Generator)
- 2) Astable Multivibrator (Asymmetrical Square Wave Generator)

Upload a single PDF file on Nalanda which includes

- 1) Circuit diagrams for all configurations.
- 2) Waveforms for two configurations.
- 3) Measure duty cycle, frequency, amplitude and compare your theoretical and simulated values.

2. Astable Multivibrator -Symmetrical Square Wave Generator

2.1 Circuit Diagram:



2.2 Resultant Curve :



We take $R1=R2 = 7.2k$ ohm to make freq near to 1kHz

2.3 Simulation result :

TH=0.5006mS & TL=0.50057mS

=> T=1.00117mS

Duty Cycle=50.001%

freq=998.88 Hz

Amplitude 4.999V ~ 5V

2.4 Theoretical formulation :

TH=0.69*R1*C1 = TL = 4.986mS

freq=1.443/(2*R1*C1)= 1.002 kHz

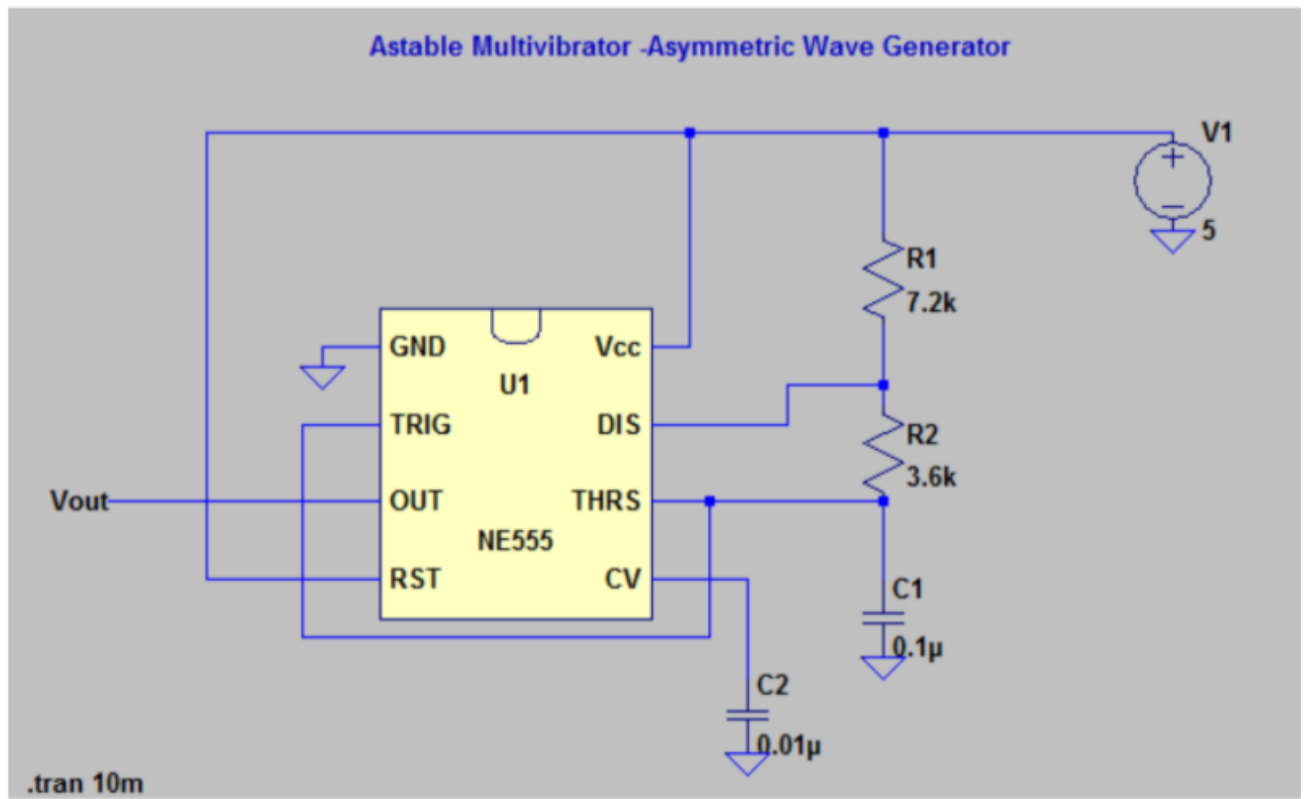
Duty Cycle=50%

2.5 Conclusions

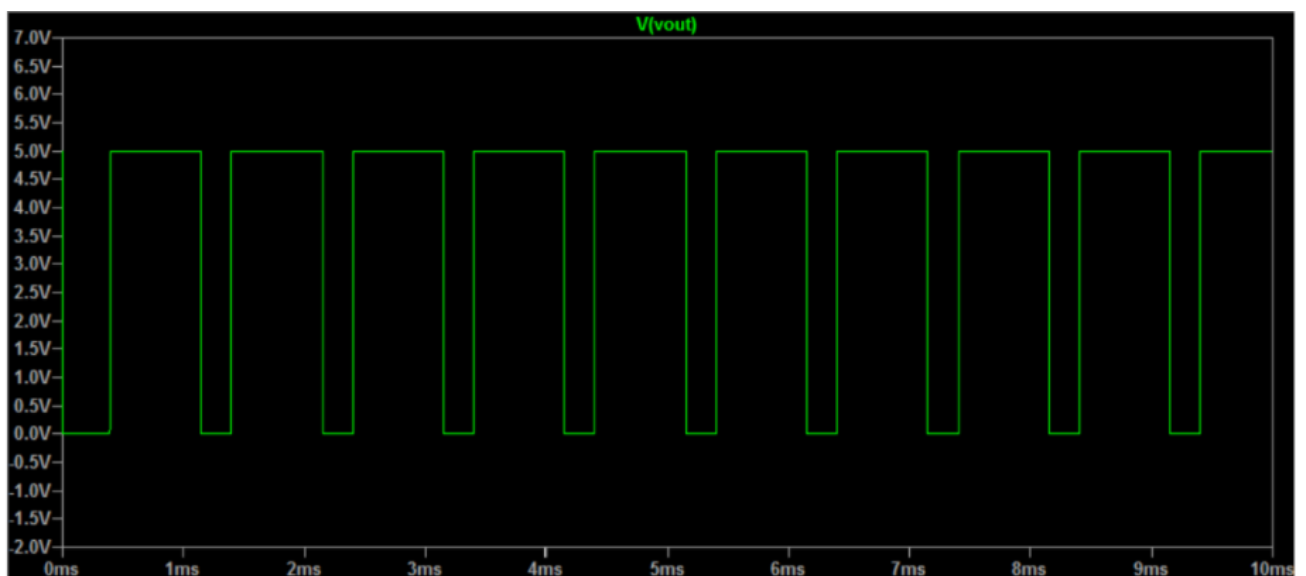
- The theoretical frequency is 3.2 Hz more than the simulated
- The theoretical Duty Cycle is 0.001% less than the Simulated (after making diode drop is negligible in LTSpice and changing R1=R2=7.2 Kohm)

3. Astable Multivibrator -Asymmetrical Square Wave Generator

3.1 Circuit Diagram:



3.2 Resultant Curve :



3.3 Simulation result :

TH=0.7492mS & TL=0.25063mS

=>T=0.99983

freq=1.00017 kHz

Duty Cycle=74.93%

Amplitude 4.999v~5V

3.4 Theoretical formulation :

TH = $0.69 \cdot (R1 + R2) \cdot C1 = 0.7452\text{mS}$

TL = $0.69 \cdot R2 \cdot C1 = 0.2484\text{mS}$

=> T = TH + TL = 0.9936

freq= $1.443 / [(R1 + 2 \cdot R2) \cdot C] = 1.002 \text{ kHz}$

Duty Cycle=75%

3.5 Conclusions

- The theoretical frequency is 1.83 Hz more than the Simulated.
- The theoretical Duty Cycle is 0.07% more than the Simulated.