Study the basic configuration of OPAMP (IC-741)

Analog Electronics Lab Experiment -3

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1. Objective

To study the following basic configuration of an Operational Amplifier and verify the same using LTSpice simulation of IC 741:

1) Inverting Mode
2) Non-inverting mode
3) Adder
4) Subtractor

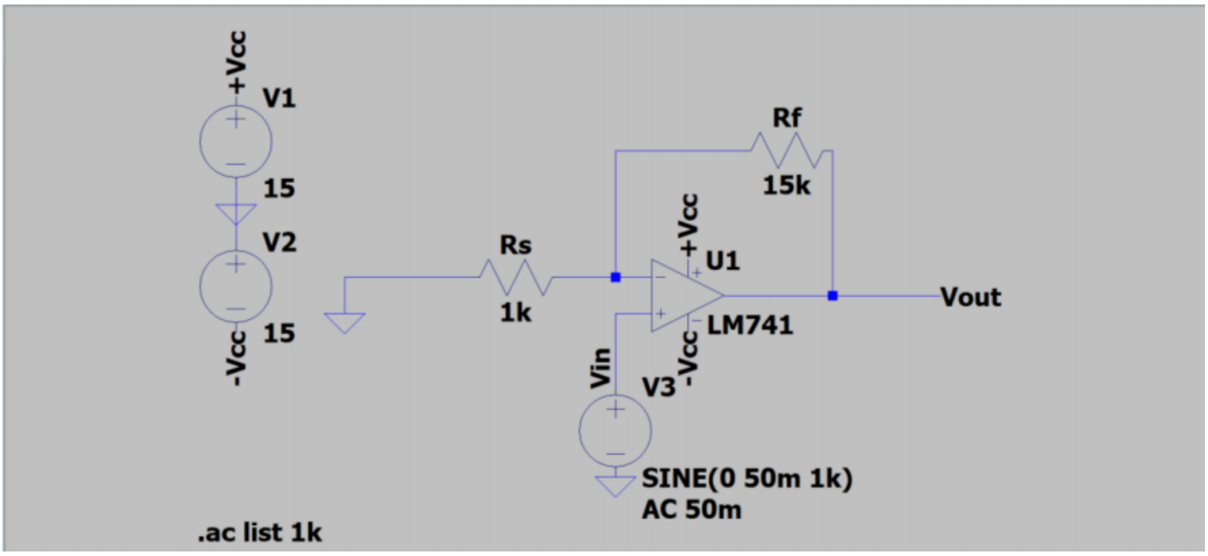
Report the following:

1)Circuit diagrams for all four configurations.
2)Simulated and theoretical values of voltage gain (A_V) and input-output voltage waveforms with magnitude for inverting and non-inverting mode.
3)Simulated and theoretical values of output voltage (V_O) for adder
4)Simulated and theoretical values of output voltage (V_O) for subtractor

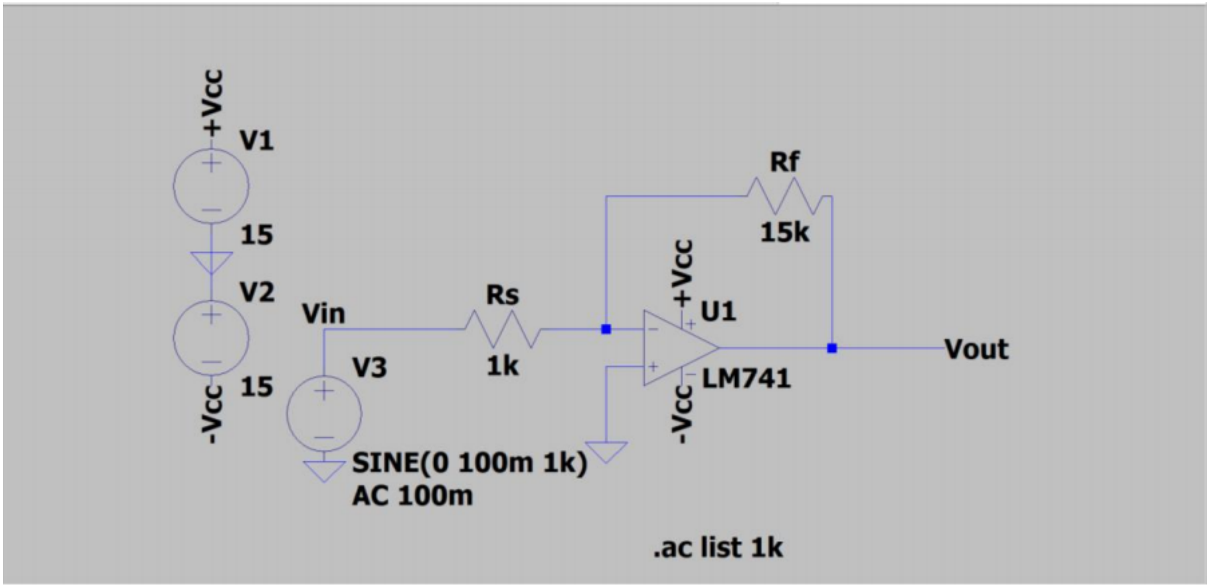
Assumptions: Ideal behaviour of the OPAMP.

2. Schematic

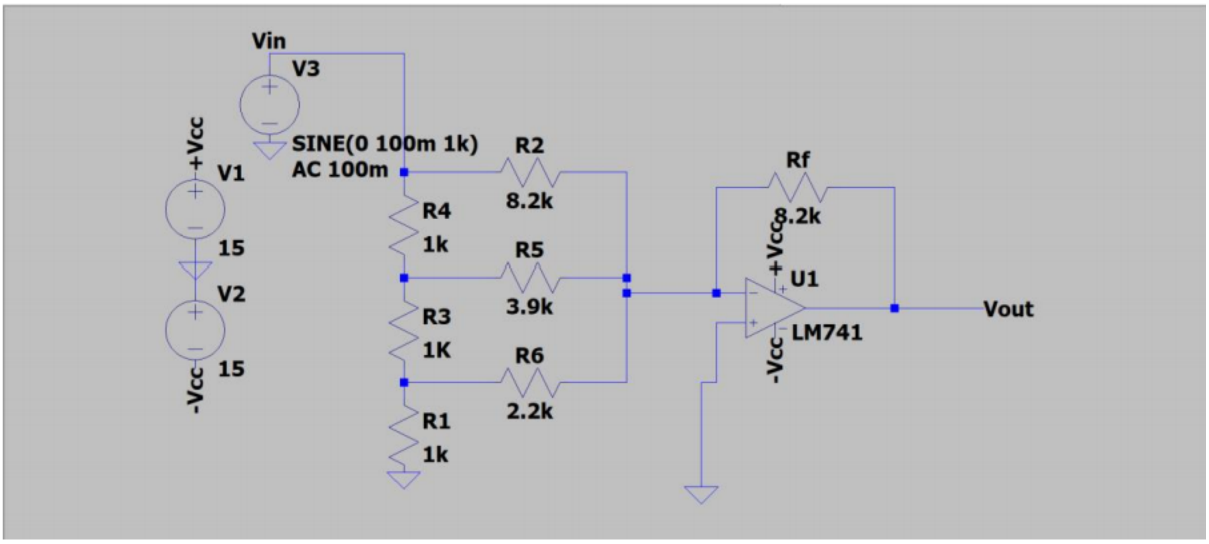
A. Inverting Amplifier :



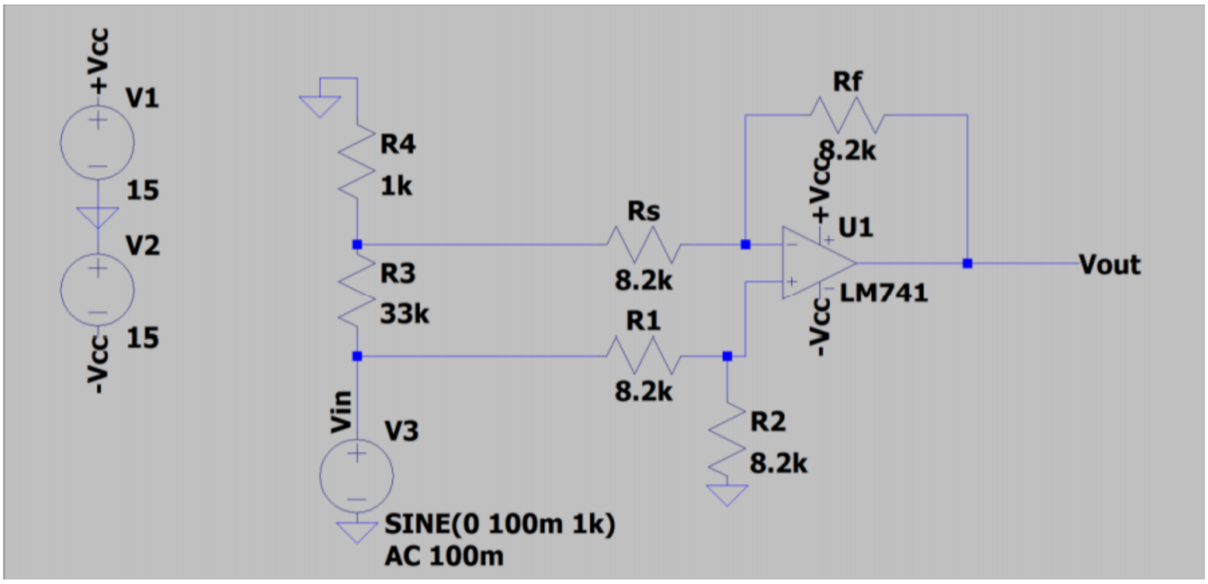
B. Non-inverting Amplifier :



C. Adder circuit :



D. Subtractor circuit :



3. Volage Gain

A. Inverting Amplifier :

```
        --- AC Analysis ---

frequency:     1000          Hz
V(n001):       mag: 0.000758591 phase:    88.8112°        voltage
V(vs):         mag:        0.05 phase:         0°        voltage
V(vout):       mag:    0.749846 phase:    179.07°        voltage
V(-vcc):       mag:           0 phase:         0°        voltage
V(+vcc):       mag:           0 phase:         0°        voltage
I(Rf):         mag: 4.999e-005 phase:    179.128°        device_current
I(Rs):         mag: 4.999e-005 phase:    179.131°        device_current
I(V2):         mag: 2.48267e-005 phase:    179.128°      device_current
I(V1):         mag: 2.51633e-005 phase:  -0.872383°      device_current
I(Vs):         mag: 4.999e-005 phase:    179.131°        device_current
Ix(u1:1):      mag: 2.68845e-009 phase:   -91.1901°      subckt_current
Ix(u1:2):      mag: 2.68845e-009 phase:    88.8099°      subckt_current
Ix(u1:99):     mag: 2.51633e-005 phase:    179.128°      subckt_current
Ix(u1:50):     mag: 2.48267e-005 phase:    179.128°      subckt_current
Ix(u1:28):     mag: 4.999e-005 phase:  -0.872383°        subckt_current
```

Practical Gain = V(vout)/V(vs) = 0.749846/0.05 = -14.98692
Theoretical Gain = Rf/Rs = 15k/1k = -15

B. Non-Inverting Amplifier :

AC analysis at 1kHz (to calculate gain A_v):

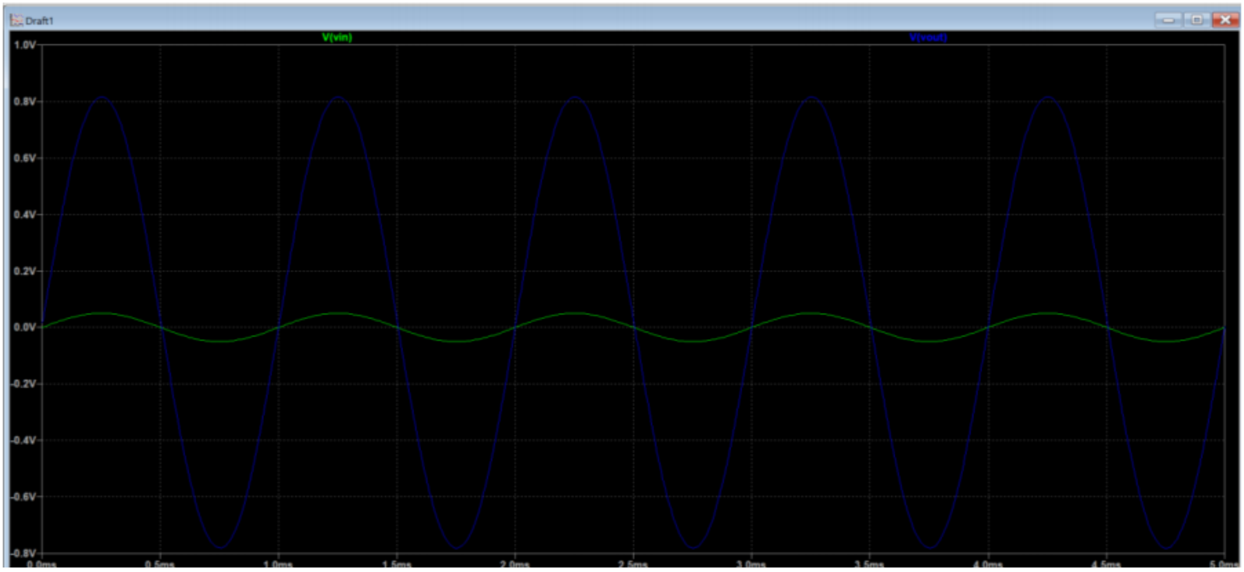
```
        --- AC Analysis ---

frequency:     1000          Hz
V(n001):       mag:  0.0499913 phase:  -0.920529°        voltage
V(vout):       mag:   0.799861 phase:  -0.923597°        voltage
V(vs):         mag:       0.05 phase:         0°         voltage
V(-vcc):       mag:          0 phase:         0°         voltage
V(+vcc):       mag:          0 phase:         0°         voltage
I(Rf):         mag: 4.99913e-005 phase:  -0.923802°      device_current
I(Rs):         mag: 4.99913e-005 phase:  -0.920529°      device_current
I(Vs):         mag: 2.85502e-009 phase:    -91.126°      device_current
I(V2):         mag: 2.48274e-005 phase:  -0.923802°      device_current
I(V1):         mag: 2.51639e-005 phase:    179.076°      device_current
Ix(u1:1):      mag: 2.85502e-009 phase:     88.874°      subckt_current
Ix(u1:2):      mag: 2.85501e-009 phase:    -91.124°      subckt_current
Ix(u1:99):     mag: 2.51639e-005 phase:  -0.923802°      subckt_current
Ix(u1:50):     mag: 2.48274e-005 phase:  -0.923802°      subckt_current
Ix(u1:28):     mag: 4.99913e-005 phase:    179.076°      subckt_current
```

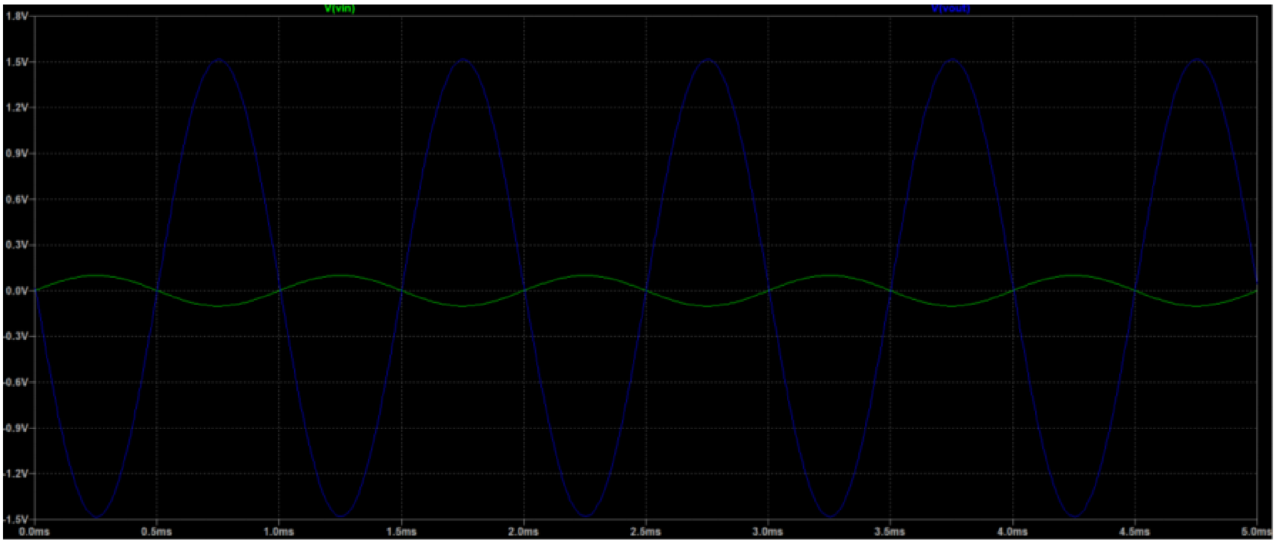
Practical Gain = V(vout)/V(vs) = 0.79986/0.05 = 15.9892
Theoretical Gain = 1+(Rf/Rs) = 1+15k/1k = 1+15 = 16

4. Input and Output Waveforms

A. Inverting Amplifier :



B. Non-Inverting Amplifier :



5. Output Voltages

A. Adder Circuit :

```
       --- AC Analysis ---

frequency:     1000          Hz
V(n001):       mag: 0.000302253 phase:    89.3731°        voltage
V(-vcc):       mag:           0 phase:          0°        voltage
V(+vcc):       mag:           0 phase:          0°        voltage
V(vout):       mag:    0.295825 phase:    179.631°        voltage
V(v1):         mag:         0.1 phase:          0°        voltage
V(v2):         mag:    0.054084 phase:   0.076469°        voltage
V(v3):         mag:    0.022035 phase:      0.222°        voltage
I(R6):         mag: 2.2035e-005 phase:      0.222°        device_current
I(R5):         mag: 3.20492e-005 phase: -0.0235887°       device_current
I(R4):         mag: 4.59161e-005 phase:  -0.090072°       device_current
I(R3):         mag: 1.00148e-005 phase:    179.436°       device_current
I(R2):         mag: 1.3867e-005 phase:    179.756°        device_current
I(R1):         mag: 1.21948e-005 phase:    179.827°       device_current
I(Rf):         mag: 3.60764e-005 phase:     179.69°       device_current
I(Vs):         mag: 5.81108e-005 phase:    179.892°       device_current
I(V2):         mag: 1.79561e-005 phase:     179.69°       device_current
I(V1):         mag: 1.81203e-005 phase:  -0.310472°       device_current
Ix(u1:1):      mag: 1.07119e-009 phase:   -90.6282°       subckt_current
Ix(u1:2):      mag: 1.07119e-009 phase:    89.3718°       subckt_current
Ix(u1:99):     mag: 1.81203e-005 phase:     179.69°       subckt_current
Ix(u1:50):     mag: 1.79561e-005 phase:     179.69°       subckt_current
Ix(u1:28):     mag: 3.60764e-005 phase:  -0.310472°       subckt_current
```

Practical Vout(V(vout)) = 0.295825V
TheoreticalVout={(Rf/R1)*V1+(Rf/R2)*V2+(Rf/R3)*V3}={1*0.1+2.102*0.054+3.72*0.02}=0.295584V

B. Subtractor circuit :

```
       --- AC Analysis ---

frequency:     1000          Hz
V(n001):       mag:  0.0500011 phase:  -0.101991°         voltage
V(n002):       mag:       0.05 phase: -0.00149847°        voltage
V(-vcc):       mag:          0 phase:          0°         voltage
V(+vcc):       mag:          0 phase:          0°         voltage
V(vout):       mag:  0.0920803 phase:  -0.106532°         voltage
V(v2):         mag: 0.00792186 phase: -0.0681324°         voltage
V(v1):         mag:        0.1 phase:          0°         voltage
I(R6):         mag: 7.92186e-006 phase:    179.932°       device_current
I(R5):         mag: 2.79025e-006 phase:   -179.994°       device_current
I(R4):         mag: 6.09756e-006 phase: -0.00149847°      device_current
I(R3):         mag: 6.09756e-006 phase:   -179.999°       device_current
I(R2):         mag: 5.13161e-006 phase:  -0.108366°       device_current
I(Rf):         mag: 5.13161e-006 phase:  -0.111927°       device_current
I(V2):         mag: 2.56291e-006 phase:  -0.111927°       device_current
I(V1):         mag: 2.56871e-006 phase:    179.888°       device_current
I(Vs):         mag: 8.88781e-006 phase:   -179.997°       device_current
Ix(u1:1):      mag: 3.18942e-010 phase:    90.1799°       subckt_current
Ix(u1:2):      mag: 3.18943e-010 phase:   -89.8021°       subckt_current
Ix(u1:99):     mag: 2.56871e-006 phase:  -0.111927°       subckt_current
Ix(u1:50):     mag: 2.56291e-006 phase:  -0.111927°       subckt_current
Ix(u1:28):     mag: 5.13161e-006 phase:    179.888°       subckt_current
```

Practical Vout(V(vout)) = 0.0920803V
Theoretical Vout = (Rf/R1)*(V1-V2) = 1*(0.1-0.00792186) = 0.09207814