DIGITAL ASSIGNMENT

BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

FINAL REPORT

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EEE F313- ANALOG & DIGITAL VLSI DESIGN

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ABSTRACT

The primary project aims at designing a **Four-input pseudo-NMOS NOR** using Microwind. This design includes the MOS schematic with single-fingered layout for both PMOS and NMOS. The design has been completed with design rule check which resulted in zero errors.

The secondary project involves developing an **odd parity checker**, by developing its **Finite State Diagram**. The serial input odd parity checker has been implemented using MUX and D flip flop. The final structural level verilog code has been simulated and the results have been attached.

The following report consists of all the details and the proofs with the step by step implementation for the same.

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Primary Assignment - Microwind

1. Problem Statement and Specifications

Design a 4-input Four-input pseudo-NMOS NOR circuit at 500MHz frequency with 500fF load capacitance using the digital MOSFETs in SCL 180 nm technology. Core voltage (VDD) for this technology is 1.8 V.

2. Schematic Diagram

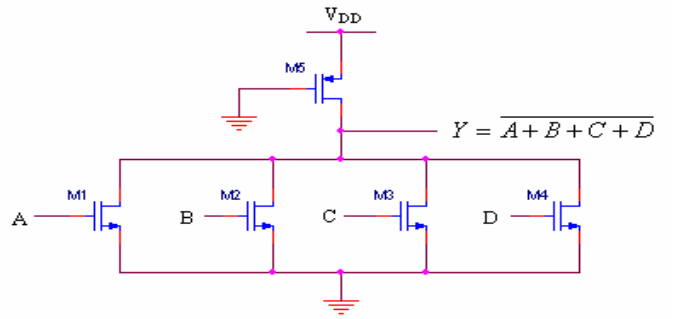


Fig 1: Schematic for 4 input Pseudo NMOS NOR gate Here, the A, B, C, D are the inputs and Y is the output.

The same schematic, as seen in DSCH is attached below.

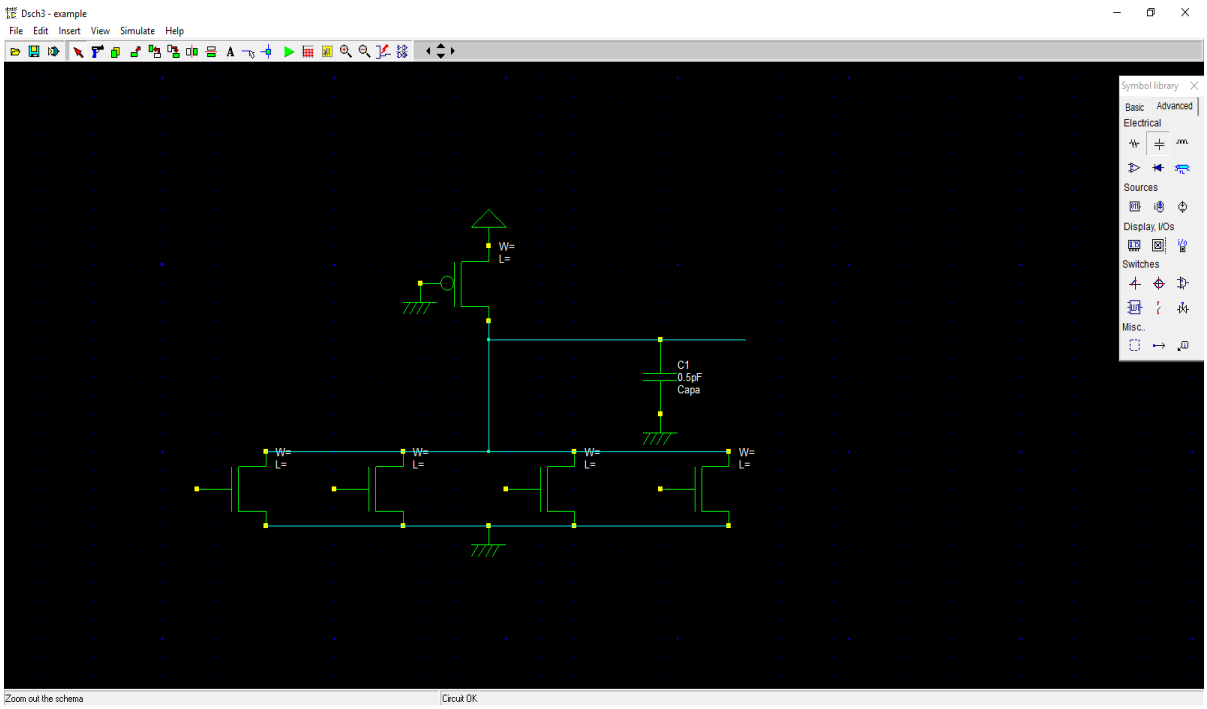


Fig 2: Schematic diagram in DSCH tool (helper tool for Microwind)

As it can be seen, the **W/L ratios and the Capacitances** are yet to be inserted. We do that simulation in the next sections.

3. Design Parameters analysis

According to the problem statement, we have determined the design parameters of the device using the **Logical Effort approach**. Challenges were faced in the hand calculations owing to the fact minimal literature available for Pseudo-NMOS type design.

According to the given CMOS_018.rul parameters, we extracted the following for hand calculations:

	NMOS	**PMOS**
U (charge carrier mobility)	0.038 cm2/V-s	0.020 cm2/V-s
Tox (oxide thickness)	4 nm	4 nm
Vt (Threshold Voltage)	0.5 V	0.6 V (negative)

So, $\frac{\mu_p}{\mu_n} = 1.9$

Further, following steps were followed;

1. W/L of PMOS was assumed to be 1 and that of NMOS was assumed to be β . Henceforth, the ratio of current produced by PMOS and NMOS with respect to reference inverter is β and 1.9 β respectively.
2. The logical effort is the ratio of input capacitance of the gate to the input capacitance of the inverter following the same current patterns.
3. In case of rising time, the device follows CMOS like pattern and is thus easy to analyse but in case of falling time, the device has complex pattern, thus, we need to define the g(logical effort) separately for rising and falling time.
4. The following is an detailed description of the calculations done:

Let W/L of PMOS be 1

And W/L of NMOS be β

$$\text{As } \frac{\mu_n}{\mu_p} = 1.9$$

The inverter is assumed to be symmetric, so correspondingly the current produced by PMOS and NMOS wrt to reference inverter is 1 and 1.9β respectively

For rising transition output current is 1 and corresponding output current while falling is $1.9\beta - 1$

$$\text{Capacitance} = \frac{(1.9\beta - 1) + 1}{\beta + 1}$$

$$\text{Finally, } G_{rising} = \frac{(1.9\beta - 1) + 1}{3(\beta + 1)}$$

$$G_{falling} = \frac{(1.9\beta - 1)((1.9\beta - 1) + 1)}{3(\beta + 1)}$$

5) As the logical effort is inversely proportional to frequency of operation, we try to minimize g. Thus, by some approximations and calculations, we find that **W_n/W_p must be close to 2.1.**

6) Further, we try to calculate the exact W/L and henceforth, we need h and p for the pseudo-NMOS device. From the CMOS ring Oscillator circuit, we find out that τ **is 12 ps.**

Also, the value for Cox ($\frac{\varepsilon}{t_{ox}}$) is calculated as follows:

Coxn = Coxp = (3.45. E-17 / 4) F/m2

= 8.625 nF/nm2

7) Our ultimate aim is to solve the following equation:

1/(τ *(gh + p)) > 500MHz

Where, g,h,p are functions of W/L ratio of the 2 transistors.

8) The following are the calculations (instead of 1 and β, now we take α and 2.1α):

Calculating P

Rising = α/3

Falling = (α+8.4β)/3 = 9.4$*$ $\alpha/3$

Calculating h

Rising = $C_L/W_pL_pC_{oxp}$ = $C_L/\alpha(C_{oxp})$

Falling = $C_L/(W_pL_pC_{oxp} + W_nL_nC_{oxn}) = C_L/(\alpha(C_{oxp} + 2.1C_{oxn})$

9) Finally, using a recursive trial and error method, we find out that it α is close to 0.667.

4. Final Layout

Complete layout has been designed in Mircowind and various parameters were kept in consideration while designing layout –

1.) Area – To reduce area we preferred avoiding multi-fingured layout for NMOS transistors. Following parameters were obtained –
    a. Area with multi-fingered layout – 398.5um^2
    b. Area with single fingered layout for PMOS only – 245.3 um^2

Therefore, b was preferred.

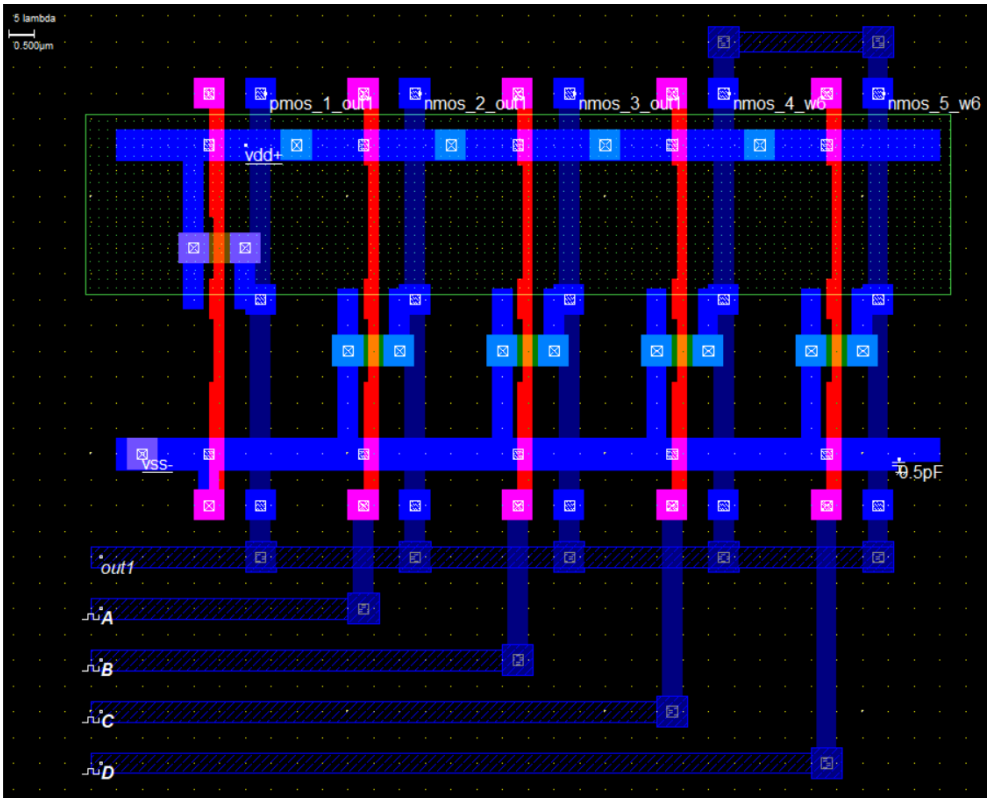
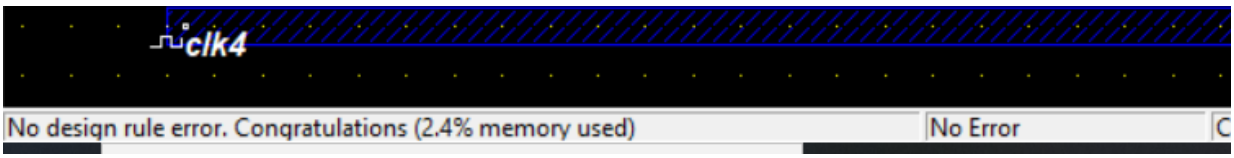


Fig 3: Final layout of Pseudo NMOS NOR circuit in Microwind

5. Output and Simulations

This section demonstrates the use of Microwind for creating the layout and various other checks that have been performed.

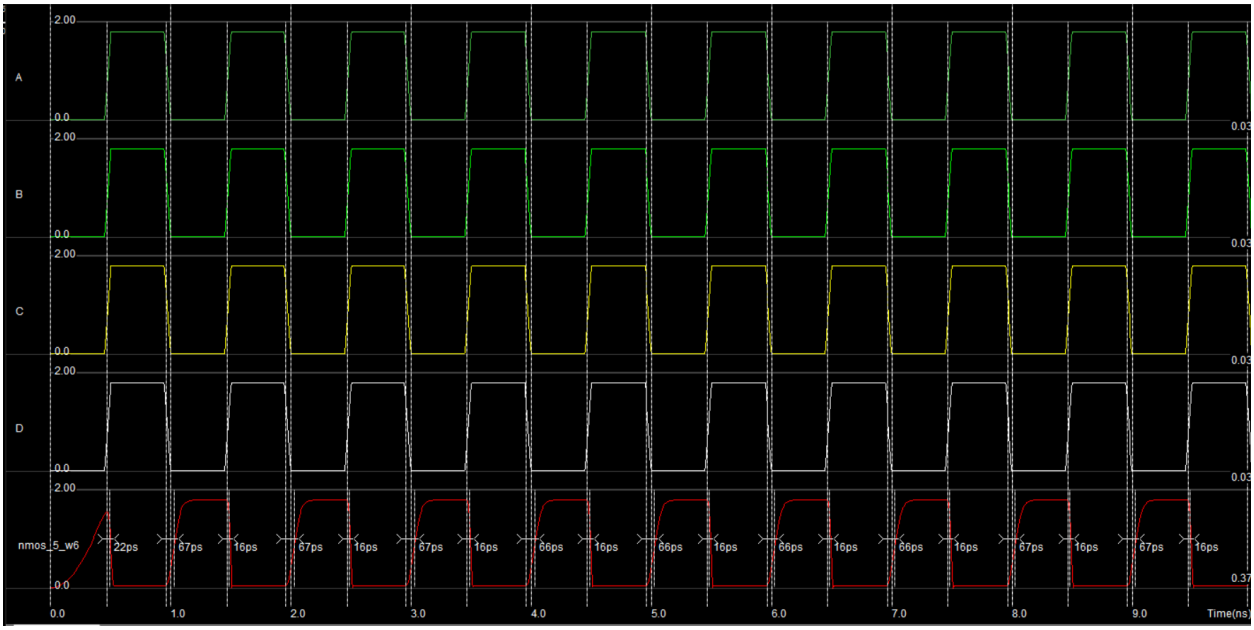
Design rule check – Design rule check was done with respect to the foundry rule file corresponding to 180 nm. Following image shows proof of the same



Rise time and fall time of input for all observations is kept 0.05ns

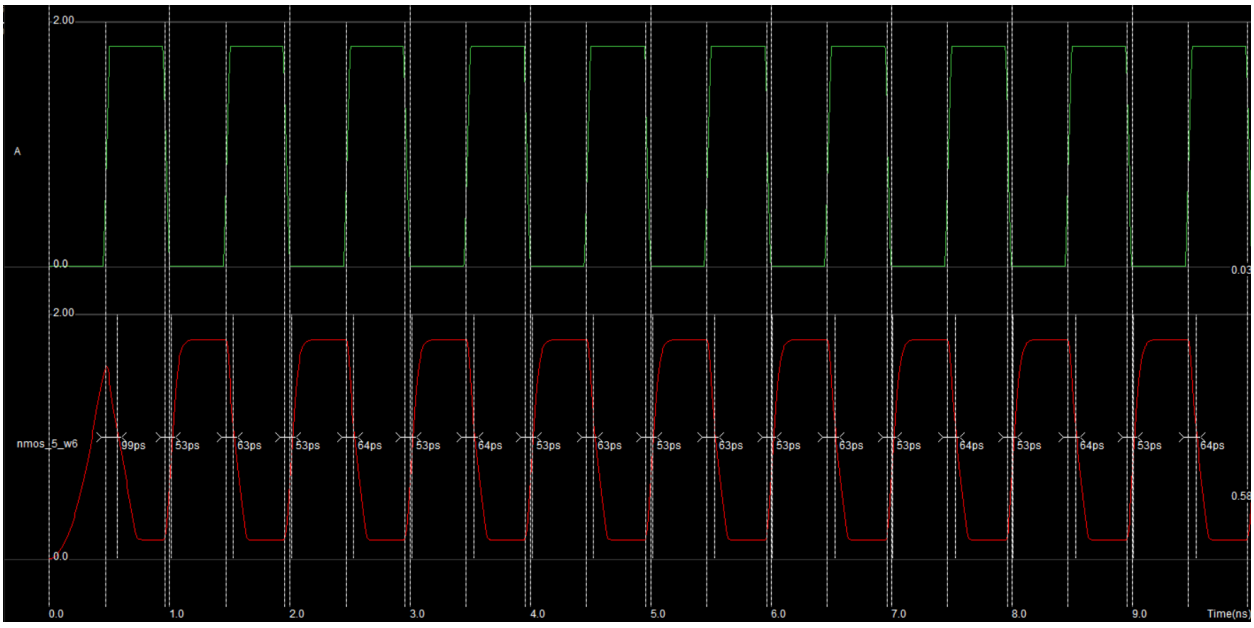
Max voltage for all inputs is 1.8V

Observation1 – Best case with all clocks same and frequency 500Mhz



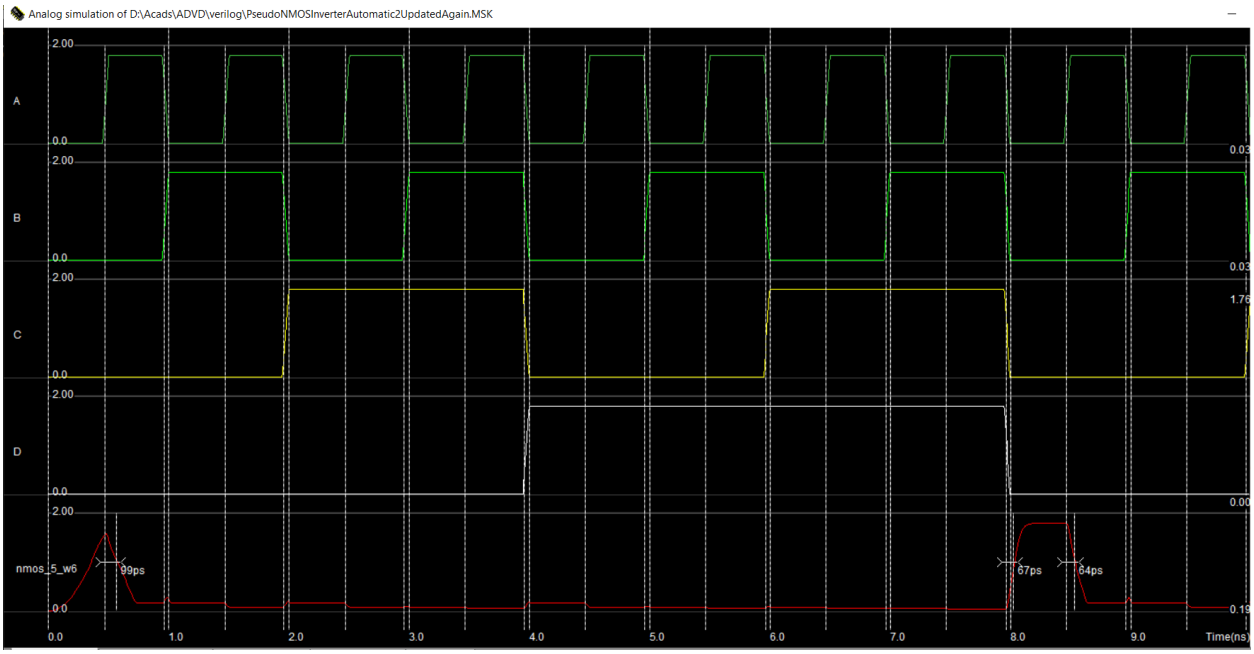
a.) Rise time – 67ps
b.) Fall time – 16ps
c.) Max Voltage – 1.8V
d.) Power Consumption – 0.206mW

Observation2 – Worst case with only one input and frequency 500Mhz



a.) Rise time – 53ps
b.) Fall time – 63ps
c.) Max Voltage – 1.8V
d.) Power Consumption – 0.196mW

Observation3 – All inputs with frequency f, f/2,f/4,f/8 where f = 500Mhz



a.) Rise time – 67ps
b.) Fall time – 64ps
c.) Power Consumption – 0.315mw
d.) Max Voltage – 1.8V

6. Result and Conclusion

Parameter	Value
Vdd	1.8V
Area	245.3 sq um
Output Rise time (best case)	37ps
Output Fall time (best case)	20ps
Power Consumption	0.184mW
Frequency	500Mhz
W nmos	240nm
W pmos	120nm
L	180nm
W/L for pmos	0.667
W/L for nmos	1.334

Secondary Assignment - Verilog

1. Problem Statement

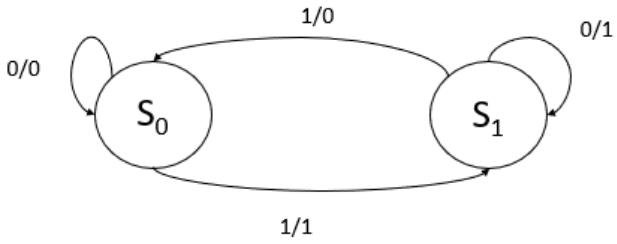
A sequence of bits has odd parity if numbers of ‘1’ are odd. Design a circuit which accepts a string of bits and outputs a '1', if parity thus far is odd; or else outputs a '0'. Develop the FSM. Use structural level style to implement (MUX and FF). Develop a stimulus model for functional verification.

2. State Diagram and Truth Table

To get the circuit of odd parity checkers using FF and mux we need to design FSM to get the circuit.

S_0 = Reset State

S_1= Odd parity State



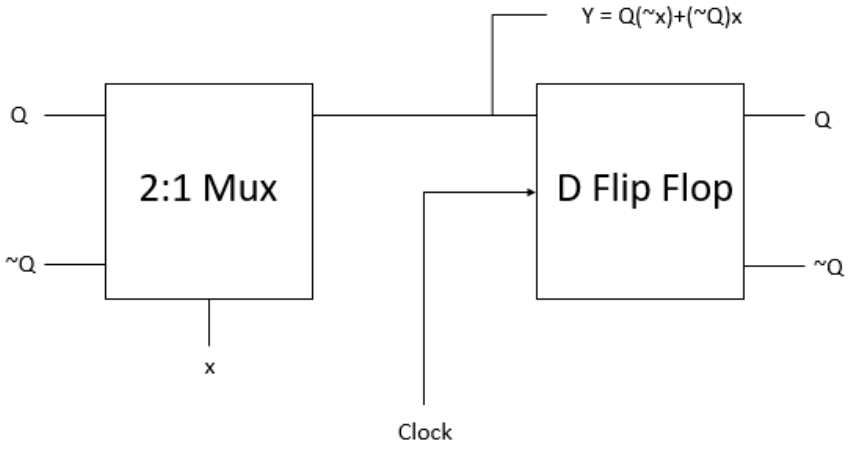
Q (Present State)	X(Input)	Q_0’ (Next State)	Y(input)
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

Q\x	0	1
0	0	1
1	1	0

$$Q' = Q(\sim x) + (\sim Q)x$$

Q'\x	0	1
0	0	1
1	1	0

$$Q' = Q(\sim x) + (\sim Q)x$$



3. Code for MUX

In the circuit there is 2:1 mux whose select line is the serial input(x) and two other inputs are Q(at position 0) and complement of Q (at position 1). Code for designing above mux is given below:

```
module mux2to1(out, in_0, in_1, x);
    output out;
    //reg out;
    input in_0;
    input in_1;
    input reset;
    input x;
    wire xb;
    wire tmp1, tmp2;
    wire out_tmp;

    not n1(xb,x);
    and and1(tmp1,in_0,xb);
    and and2(tmp2,in_1,x);
    or or1(out_tmp, tmp1, tmp2);

    assign out = out_tmp;
endmodule
```

4. Code for D Flip Flop

The output of the MUX is passed through a positive edge triggered D-Flip Flop. The verilog code for the same is:

```
module dff(q,clk,d,reset);
    output q;
    input clk, d, reset;
    reg q;
    always@ (posedge clk or reset)
        begin
            if (reset)
                q<=0;
            else
                q<=d;
        end
endmodule
```

5. Code for final Module

```
module answer(y,x,clk,flag,reset);
    output y;
    input x,clk,flag,reset;
    wire q1,q2,q3;
    dff m2(q1,clk,q3,reset);
    mux2to1 m1(q3,q1,~q1,x);
    assign y = q3;
endmodule
```

6. Code for Testbench

```
module test;
    reg x,clk,flag,reset;
    wire y;
    answer f(y,x,clk,flag,reset);
    initial $monitor(,$time,"x=%b,clk=%b,y=%b",x,clk,y);
always
    #10 clk=~clk;
initial clk=0;
initial flag=0;
initial reset=1;
initial x=0;
initial #5 flag=1;
initial #4 reset=0;
initial
    begin
        #10 x=0;
        #10 x=1;
        #10 x=0;
        #10 x=1;
        #10 x=0;
        #100;
        end
initial
    begin
        $dumpfile("testbench.vcd");
        $dumpvars;
    end
endmodule
```

7. IVerilog Simulation Results

The output y is changing only on positive edge of clock.

```
VCD info: dumpfile testbench.vcd opened for output.
                   0x=0,clk=0,y=0
                  10x=0,clk=1,y=0
                  20x=1,clk=0,y=1
                  30x=0,clk=1,y=1
                  40x=1,clk=0,y=0
                  50x=0,clk=1,y=0
                  60x=0,clk=0,y=0
                  70x=0,clk=1,y=0
                  80x=0,clk=0,y=0
                  90x=0,clk=1,y=0
                 100x=0,clk=0,y=0
                 110x=0,clk=1,y=0
                 120x=0,clk=0,y=0
                 130x=0,clk=1,y=0
                 140x=0,clk=0,y=0
                 150x=0,clk=1,y=0
                 160x=0,clk=0,y=0
                 170x=0,clk=1,y=0
                 180x=0,clk=0,y=0
                 190x=0,clk=1,y=0
                 200x=0,clk=0,y=0
                 210x=0,clk=1,y=0
                 220x=0,clk=0,y=0
                 230x=0,clk=1,y=0
                 240x=0,clk=0,y=0
                 250x=0,clk=1,y=0
```

Fig16: Output after simulating in Iverilog

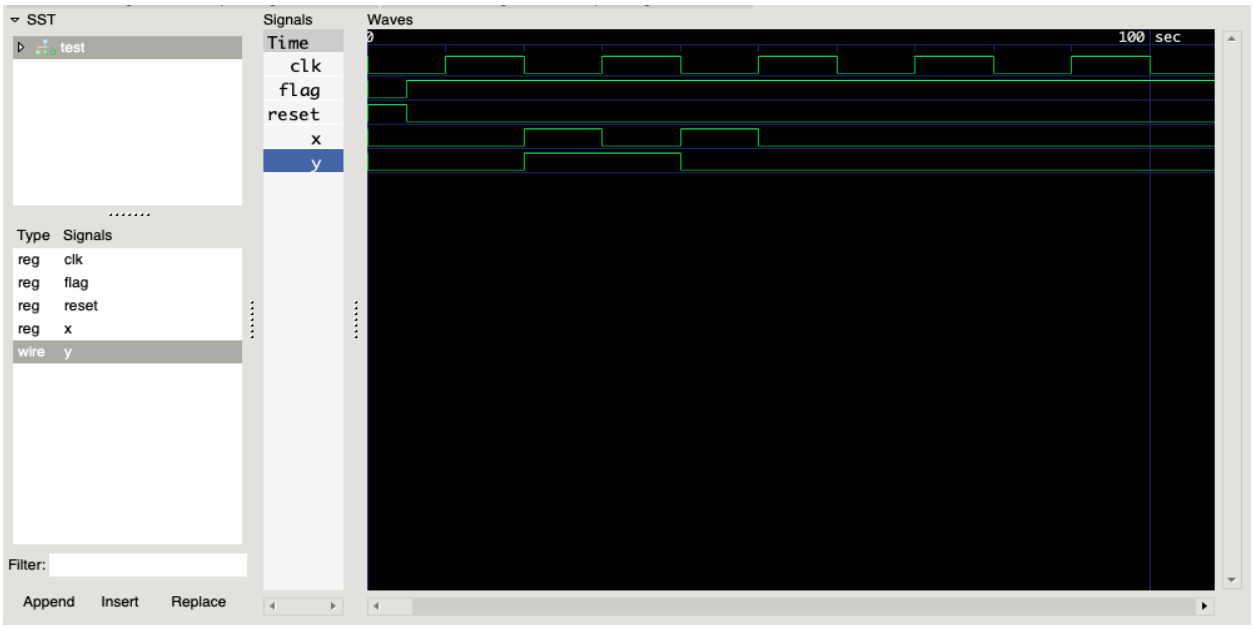


Fig16: GTKWave Simulation

References

For theory

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https://nptel.ac.in/content/storage2/courses/117101058/downloads/Lec-17.pdf
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[2] Behzad Razavi. 2000. Design of Analog CMOS Integrated Circuits (1st. ed.). McGraw-Hill, Inc., USA.

[3] Raghav, Himadri & Maheshwari, Sachin & Gupta, Anu. (2014). A comparative analysis of power and delay optimise digital logic families for high performance system design. Int. J. of Signal and Imaging Systems Engineering. 7. 12 - 20. 10.1504/IJSISE.2014.057934.

[4] “INVERTER-switching characteristics”,
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For Microwind

[5] “CMOS inverter layout using Microwind by jayendra kumar ” https://youtu.be/xolYEjgWhU8. Accessed: October 3, 2020

For Verilog

[6] “Verilog HDL Basics” https://www.youtube.com/watch?v=PJGvZSlsLKs. Accessed: October 3, 2020
[7] “EDA Playground” https://www.edaplayground.com/. Accessed: October 3, 2020

Appendices

This section reports the additional analysis and simulations that we worked out so as to understand the concepts better.
Appendix A corresponds to Primary Assignment and Appendix B corresponds to Secondary Assignment.

I. Appendix A:

According to the given CMOS_018.rul parameters, we extracted the following for hand calculations:

	NMOS	**PMOS**
U (charge carrier mobility)	0.038 cm2/V-s	0.020 cm2/V-s
Tox (oxide thickness)	4 nm	4 nm
Vt (Threshold Voltage)	0.5 V	0.6 V (negative)

Using these parameters, we hand calculated the device switching delay using the exact (differential method). The procedure we followed was as follows:

1. Assuming that we want the worst case delay, we have only considered 1 NMOS in series with the PMOS.
2. In the case when NMOS is in "*off*" state, we have taken Voh as full Vdd = 1.8V. Hence, V50% is **1.8/2 = 0.9V.**
3. The delay is calculated by equating the PMOS current with current in the load capacitive node. Equivalently, the output node charges from LOW to HIGH, similar to charge up condition in CMOS logic.
4. In the condition when NMOS turns on, the analysis is complicated, resulting in the following states :

	PMOS	**NMOS**
Stage 0 - Vin just above 0 V		Off condition
Stage 1 - Vin > Vthn	Linear	Saturated
Stage 2	Linear	Linear
Stage 3	Saturated	Linear

5. According to the above table, when Vout = V50% (0.9V), we are in Stage 2

{

NMOS -> Vd = 0.9V Vth = 0.5 Vs = 0 Vg = 1.8V

PMOS -> Vd = 0.9V Vth = -0.6V Vs = 1.8V Vg = 0V

}

6. For ease in estimating Thl, we **assumed** that for the entire discharging period, our PMOS is in the Saturation region, thus giving constant current. Only the NMOS changes its regions of operation.
7. Throught, we have used long differentiation methods and calculated the switching delays, in terms of Kp and Kn.
8. Once we have the final equations, we have applied trial and error methods to find (W/L)p and (W/L)n such that the **frequency is no less than 500 MHz and also Power consumption is minimized**.
9. Finally, these values were also verified using Microwind's tools.The proof for the same has been attached in the following section. Following are the hand calculation performed –

Delay Calculations –

a.) T_{LH} = This is going to be CMOS charging so directly,

$$t_{LH} = \frac{C_L}{K_p(V_{oh} - V_{Top})}\left(\frac{2V_{Top}}{V_{oh} - V_{Top}} + \ln\left(\frac{V_{dd} + V_{oh} - V_{Top}}{V_{oh} - V_{Top}}\right)\right)$$

$$= \frac{0.6295}{K_p} . PS$$

b.) Fall Time, we assume PMOS to be in saturation region throughout,

$I_n + \frac{C\, dV_{out}}{dt} = I_p$

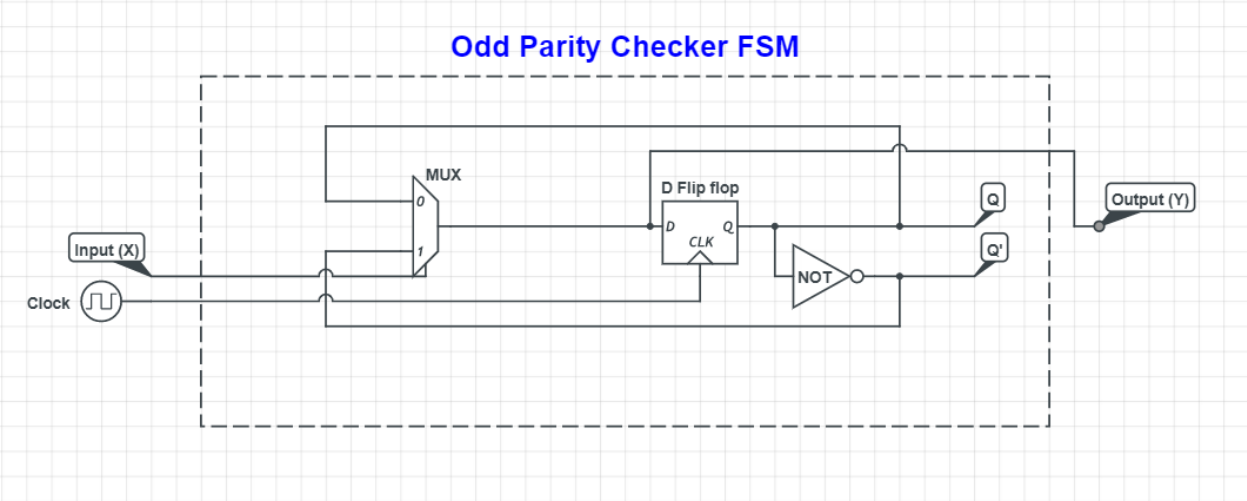
Now we have two step integration,

$$t_{HL} = \frac{C_L}{K_n(V_i - V_{Top})}\left(\frac{V_{dd} + V_i + V_T}{V_{oh} - V_{Top}} + \ln\left(\frac{V_{dd} + V_{oh} - V_{Top}}{V_{oh} - V_{Top}}\right)\right)$$

After this, we have used a logical method using Cin and Cout to estimate for the W/L. This way, we could verify the solution.

II. Appendix B:

In this section, we have added the schematic of the FSM generated using Fritzing.



<Thank You>