2 The MOS devices and technology

This chapter presents the MOS transistors, their layout, static characteristics and dynamic characteristics. Details on the materials used to build the devices are provided. The vertical aspect of the devices and the three dimensional sketch of the fabrication are also described.

1. Properties of Silicon

IA																		0
H 1 Hydrogen	IIA												III	IVA	VA	VIA	VIIA	He 2 Helium
Li 3 Lithium	Be 4 Berylliu m												B 5 Boron	C 6 Carbon	N 7 Nitrogen	O 8 Oxygen	F 9 Fluorine	Ne 10 Neon
Na 11 Sodium	Mg 12 Magnesium	IIIB	IVB	VB	VIB	VIIB	VII	VII	VII	IB	IIB		Al 13 Aluminum	Si 14 Silicon	P 15 Phosphorus	S 16 Sulfur	Cl 17 Chlorine	Ar 18 Argon
K 19 Potassium	Ca 20 Calcium	Sc 21 Scandium	Ti 22 Titanium	V 23 Vanadium	Cr 24 Chromium	Mn 25 Manganese	Fe 26 Iron	Co 27 Cobalt	Ni 28 Nickel	Cu29 Copper	Zn 30 Zinc		Ga 31 Gallium	Ge 32 Germanium	As 33 Arsenic	Se 24 Selenium	Br 35 Bromine	Kr 36 Krypton
Rb 37	Sr 38	Y 39	Ze 40	Nb 41	Mo 42	Tc 43	Ru 44	Rh 45	Pd 46	Ag 47 Silver	Cd 48 Cadmium		In 49 Indium	Sn 50 Tin	Sb 51	Te 52	I 53	Xe 54
Cs 55	Ba 56	La 57	Hf 72	Ta 73 Tantalum	W 74 Tungsten	Re 75	Os 76	Ir 77	Pt 78	Au 79 Gold	Hg 80		Tl 81	Pb 82 Lead	Bi 83	Po 84	At 85	Rn 86

Figure 2-1: periodic table of elements and position of silicon

The table of figure 2-1 illustrates the table of elements. In CMOS integrated circuits, we mainly focus on Silicon, situated in the column IVA, as the basic material (Also called substrate <glossary>) for all our designs.

The silicon atom has 14 electrons, 2 electrons situated in the first energy level, 8 in the second and 4 in the third. The four electrons in the third energy level are called valence electrons, which are shared with other atoms.

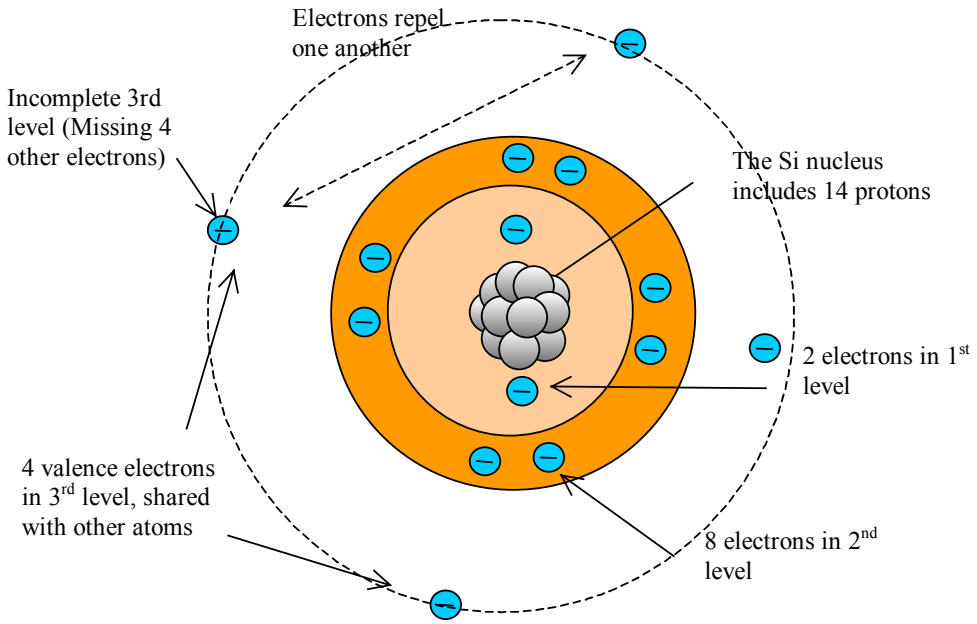

Figure 2-2: The structure of the silicon atom

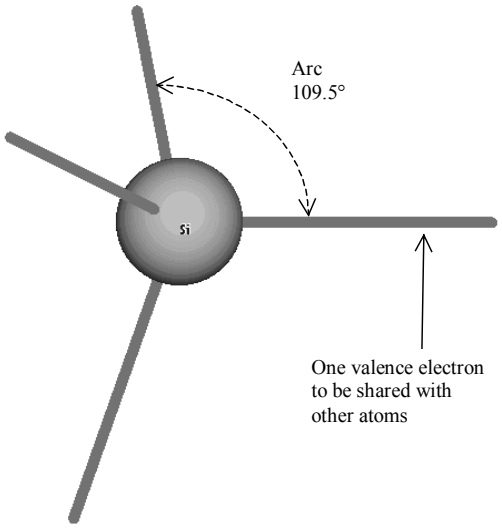

Figure 2-3: The 3D symbol of the silicon atom

The silicon atom has 4 valence electrons, which tend to repel each another. The 3rd level would be completed with 8 electrons. The four missing electrons will be shared with other atoms. The position of electrons which minimizes the mutual repulsion is shown in figure 2-3: each valence electron is represented by a line with an angle of 109.5°. In order to complete its valence shell, the silicon atom tends to share its valence electrons with 4 other electrons, by pairs. Each line between Si atoms in figure 2-3

represents a pair of shared valence electrons. The distance between two Si nucleus is 0.235 nm (10^{-9} m), equivalent to 2.35 Angstrom (10^{-10} m, also represented by the letter Å).

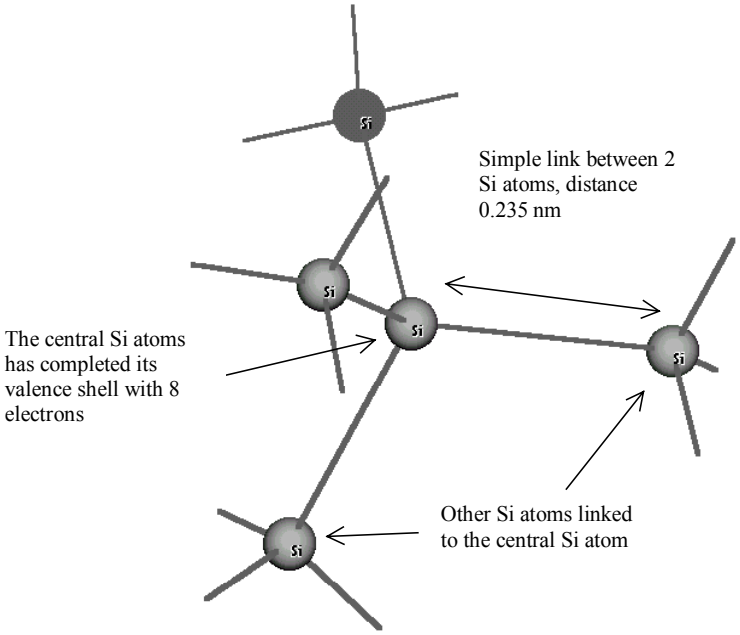

Figure 2- 4: The Si atom has four links, usually to other Si atoms

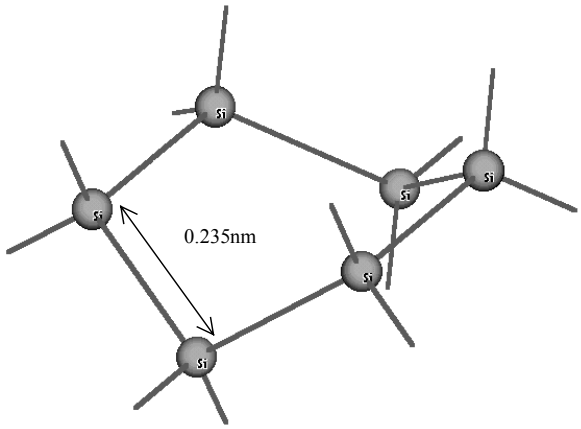

Figure 2-5: The atom arrangement is based on a 6 atom pattern

The Silicon lattice exhibits particular properties in terms of atom arrangements. The crystalline silicon is based on a 6-atom pattern shown in figure 2-5. The structure is repeated infinitely in all directions to form the silicon substrate as used for integrated circuit design. The pure silicon crystal is mechanically very strong and hard, and electrically a very poor conductor, as all valence electrons are shared within the structure (Figure 2-6). The atomic density of a silicon crystal is about $5x10^{22}$ atoms per cubic centimeter (cm^{-3}).

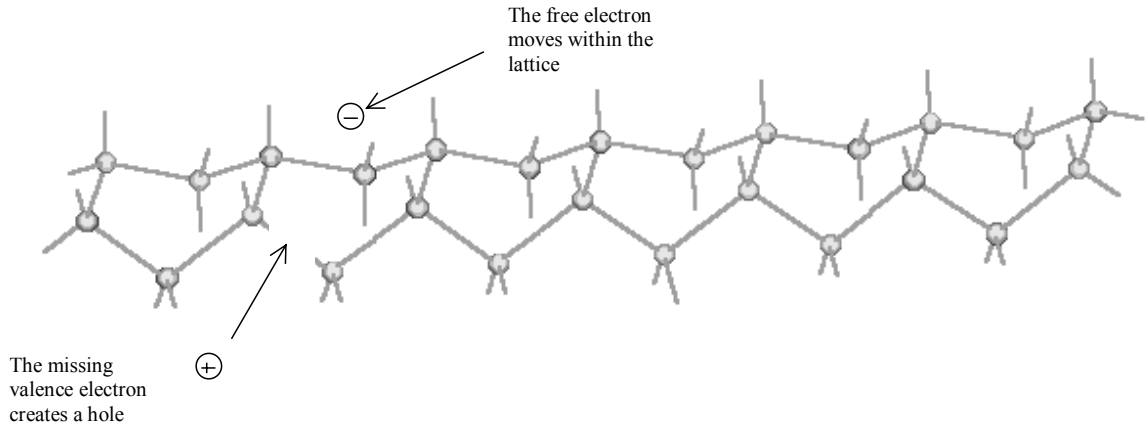

Figure 2-6: The chain of 6 atom pattern creates the silicon lattice

However, the random vibration of the silicon lattice due to thermal agitation may transmit enough energy to some electrons valence for them to leave their position. The electron moves freely within the lattice, and thus participate to the conduction of electricity. The lack of electron is called a hole (Figure 2-6). This is why silicon is not an insulator, nor a good conductor. It is called a semi-conductor <glossary> due to its intermediate electrical properties. The number of electrons which participate to the conduction are called intrinsic carriers <gloss>. The concentration of intrinsic carriers per cubic centimeter, namely *ni*, is around 1.45×10^{10} cm^{-3}. When the temperature increases, the intrinsic carrier density also increases. The concentration of free electrons is equal to the concentration of free holes.

2. N-type and P-type Silicon

To increase the conductivity of silicon, materials called dopant are introduced into the silicon lattice. To add more electrons in the lattice artificially, phosphorus or arsenic atoms (Group VA) are inserted in small proportions in the silicon crystal (Figure 2-7). As only four valence electrons find room in the lattice, one electron is released and participates to electrical conduction. Consequently, Phosphorus and arsenic are named "electron donors", with an N-type symbol. A very high concentration of donors is coded N++ (Around 1 N-type atom per 10,000 silicon atoms, corresponding to 10^{18} atoms per cm^{-3}). A high concentration of donor is coded N+ (1 N-type atom per 1,000,000 silicon atom, that is 10^{16} atoms per cm^{-3}), while a low concentration of donors is called N- (1 N-type atom per 100,000,000 silicon atom, or 10^{14} atoms per cm^{-3}).

III	IVA	VA
Acceptor		Donor
Add holes		Add electrons
P-type		N-Type

B 5 Boron	C 6 Carbon	N 7 Nitrogen
Al 13 Aluminium	Si 14 Silicum	P 15 Phosphorus
Ga 31 Gallium	Ge 32 Germanium	As 33 Arsenic

Figure 2-7: Boron, Phosphorus and Arsenic are used as acceptors and donors of electrons to change the electrical properties of silicon

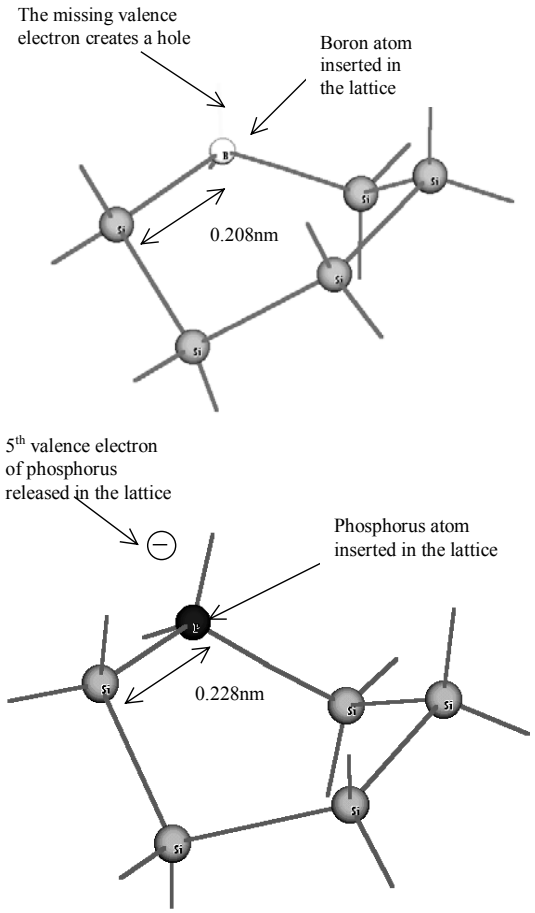

Figure 2-8: Boron added to the lattice creates a hole (P-type property), phosphorus creates a free electron (N-type property)

To increase artificially the number of holes in silicon, boron is injected into the lattice, as shown in figure 2-8. The missing valence link is due to the fact that boron only shares three valence electrons. The electron vacancy creates a hole, which gives the lattice a P-type property. A very high concentration of acceptors is coded P++ (10^{18} atoms per cm^{-3}) , a high concentration of acceptors is coded P+(10^{16} atoms per cm^{-3}), a low concentration of acceptors is called P-(10^{14} atoms per cm^{-3}). The silicon substrate used to manufacture CMOS integrated circuits is lightly doped with boron, characterized by the P- symbol. The

aspect of a small portion of silicon substrate is shown in 3d in figure 2-9. It usually consists of very thick substrate (350µm) lightly doped P-. Close from the upper surface, a buried layer saturated with P-type acceptors is usually created, to form a good conductor beneath the active region, connected to the ground voltage.

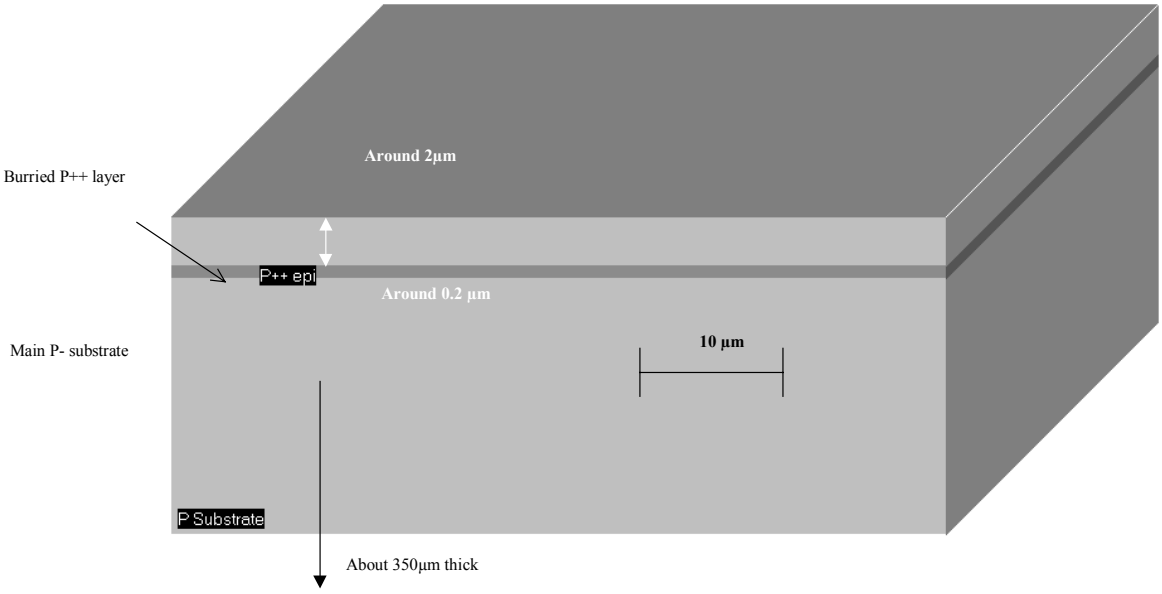

Figure 2-9: 3D aspect of a portion of silicon substrate used to manufacture CMOS integrated circuits. The substrate is based on a P- substrate with a buried P++ layer

3. Silicon Dioxide

The natural and most convenient insulator is silicon dioxide, noted SiO_2. Its molecular aspect is shown in figure 2-10. Notice that the distance between Si and O atoms is smaller than for Si-Si, which leads to some interface regularity problems. Silicon dioxide is grown on the silicon lattice by high temperature contact with oxygen gas. Oxygen molecules not only combine with surface atoms, but also with underlying atoms. Silicon dioxide has an ε_r permittivity equal to 3.9. This number quantifies the capacitance effect of the insulator. The permittivity of air is equal to 1, which is the minimum value. The SiO2 material is a very high quality insulator that is used extensively in CMOS circuits, both for devices and interconnections between devices. The "O" of CMOS corresponds to "oxide", and refers to SiO2.

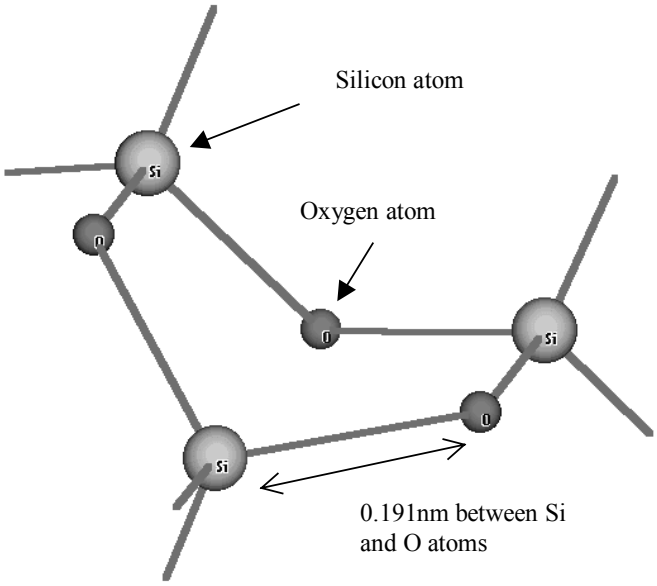

Figure 2- 10: Slicon is linked to Oxygen to form the SiO2 molecular structure

4. Metal materials

Integrated circuits also use several metal materials to build interconnects. Aluminum (III), Tungsten (IVB), Gold (IB), and Copper (IB) are commonly used in the manufacturing of microelectronic circuits.

VIB	VIIB	VII	VII	VII	IB	IIB	Al 13 Aluminum
Cr 24 Chromium	Mn 25 Manganese	Fe 26 Iron	Co 27 Cobalt	Ni 28 Nickel	Cu29 Copper	Zn 30 Zinc	Ga 31 Gallium
Mo 42	Tc 43	Ru 44	Rh 45	Pd 46	Ag 47 Silver	Cd 48 Cadmium	In 49 Indium
W 74 Tungsten	Re 75	Os 76	Ir 77	Pt 78	Au 79 Gold	Hg 80	Tl 81

Table 2-1: Metal materials used in CMOS integrated circuit manufacturing

Metal layers are characterized by their resistivity (**σ**). We notice that copper is the best conductor as its resistivity is very low, followed by gold and aluminium (Table 2-2). A highly doped silicon crystal does not exhibit a low resistivity, while the intrinsic silicon crystal is half way between a conductor and an insulator [Hastings].

Material	**Symbol**	**Resistivity σ** (Ω.cm)
Copper	Cu	1.72×10^{-6}

Gold	Au	$2.4x10^{-6}$
Aluminium	Al	$2.7x10^{-6}$
Tungsten	W	$5.3x10^{-6}$
Silicon, N+ doped	N+	0.25
Silicon, intrinsic	Si	$2.\ 5x10^{5}$

Table 2-2: Conductivity of the most common materials used in CMOS integrated

Conductivity is sometimes used instead of resistivity. In that case, the formulation is as follows:

$$\rho = \frac{1}{\sigma} \qquad \text{(Equ. 2-1)}$$

with

ρ= conductivity $(\Omega.cm)^{-1}$

σ = Resistivity (Ω.cm)

5. The MOS switch

The MOS transistor (MOS for metal-oxide-semiconductor)<gloss> is by far the most important basic element of the integrated circuit. The MOS transistor is the integrated version of the electrical switch. When it is on, it allows current to flow, and when it is off, it stops current from flowing. The MOS switch is turned on and off by electricity. Two types of MOS device exist in CMOS technology (Complementary Metal Oxide Semiconductor)<gloss>: the n-channel MOS device (also called nMOS <gloss>)and the p-channel MOS device (also called pMOS <gloss>).

Logic Levels

Three logic levels 0,1 and X are defined as follows:

Logical value	**Voltage**	**Name**	**Symbol in DSCH**	**Symbol in Microwind**
0	0.0V	VSS	 (Green in logic simulation)	 (Green in analog simulation)
1	1.2V in cmos 0.12µm	VDD	 (Red in logic simulation)	 (Red in analog simulation)
X	Undefined	X	(Gray in simulation)	(Gray in simulation)

Table 2-3: the logic levels and their corresponding symbols in Dsch and Microwind tools

The n-channel MOS switch

Despite its extremely small size (less than 1µm square), the current that the MOS transistor may switch is sufficient to turn on and off a led, for example. The MOS device consists of two electrical regions called drain and source, separated by a channel. A channel of electrons may exist or not in this channel, depending on a voltage applied to the gate. The gate is a conductor placed on the top of the channel, and electrically isolated by an ultra thin oxide. The MOS is basically a switch between drain and source. A schematic cross-section of the MOS device is given in figure 2-11. Theoretically, the source is the origin of channel impurities. In the case of this nMOS device, the channel impurities are the electrons. Therefore, the source is the diffusion area with the lowest voltage.

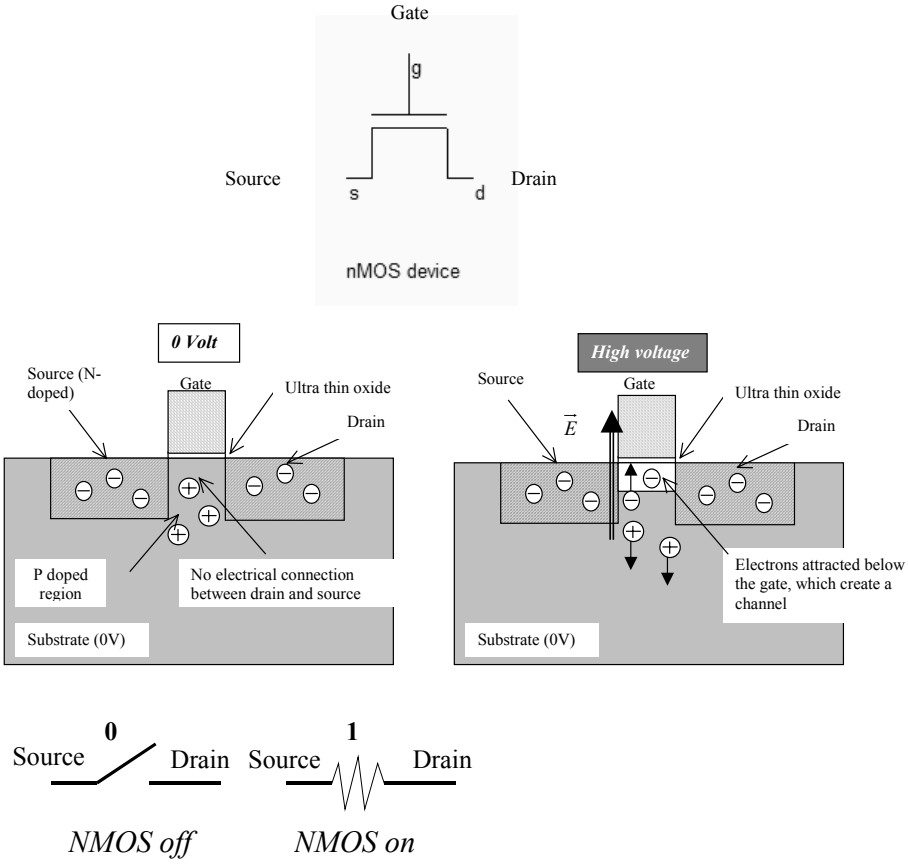

Figure 2-11: Basic principles of a MOS device

When used in logic cell design, it can be *on* or *off*. As illustrated in figure 2-xxx, the n-channel MOS device requires a high supply voltage to be on. When *on*, a current can flow between drain and source. When the MOS device is on, the link between the source and drain is equivalent to a resistor. The resistance may vary from less than 0.1Ω to several hundred KΩ. Low resistance MOS devices are used

for power application, while high resistance MOS devices are widely used in analog low power designs. In logic gate, the Ron resistance is around 1 KΩ.

The 'off' resistance is considered infinite at first order, but its value is several MΩ. When off, almost no current flow between drain and source. The device is equivalent to an open switch, and the voltage of the floating node (The drain in the case of table 2-xxx) is undetermined. The n-channel MOS logic table can be described as follows.

Gate	Source	Drain
0	0	X
0	1	X
1	0	0
1	1	1

Table 2-5: the n-channel MOS switch truth-table

The p-channel MOS switch

In contrast, the p-channel MOS device requires a zero voltage supply to be on. The p-channel MOS symbol differs from the n-channel device with a small circle near the gate. The channel carriers for pMOS are holes.

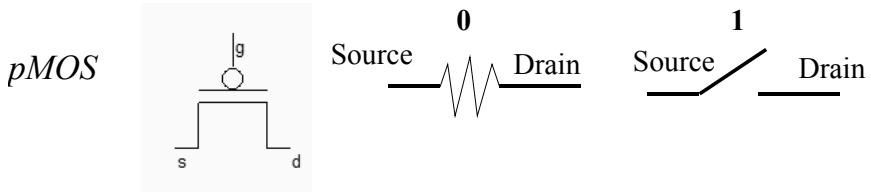

Figure 2-12: the MOS symbol and switch

The p-channel MOS logic table can be described as follows.

Gate	Source	Drain
0	0	0
0	1	1
1	0	X
1	1	X

Table 2-6: the p-channel MOS switch truth-table

For the p-channel MOS, a high voltage disables the channel. Almost no current flows between the source and drain. A zero voltage VDD on the gate, attracts holes below the gate, creates a hole channel and enables current to flow, as shown below.

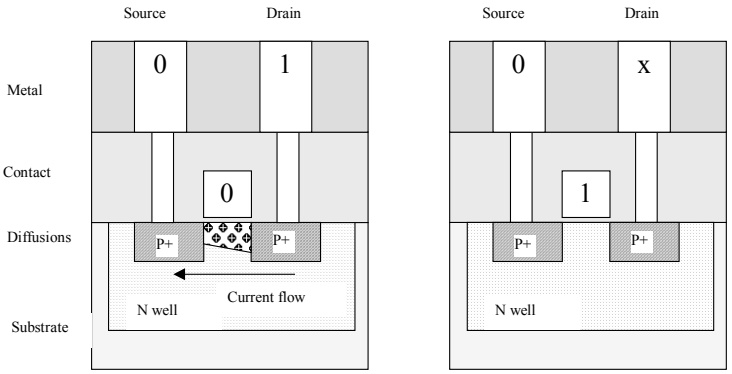

Figure 2-13. The channel generation below the gate in a pMOS device.

6. The MOS aspect

The bird's view of the layout including one n-channel MOS device and one p-channel MOS devices placed at the minimum distance is given in figure 2-xxx A two-dimensional zoom at micron scale in the active region of an integrated circuit designed in 0.12µm technology is reported in figure 2-15. This view corresponds to a vertical cross-section of the silicon wafer, in location X-X' in figure 2-14. The Microwind tool has been used to build the layout of the MOS devices (The corresponding file is **allMosDevices.MSK**), and to visualize its cross-section, using the command **Simulate →2D vertical cross-section**.

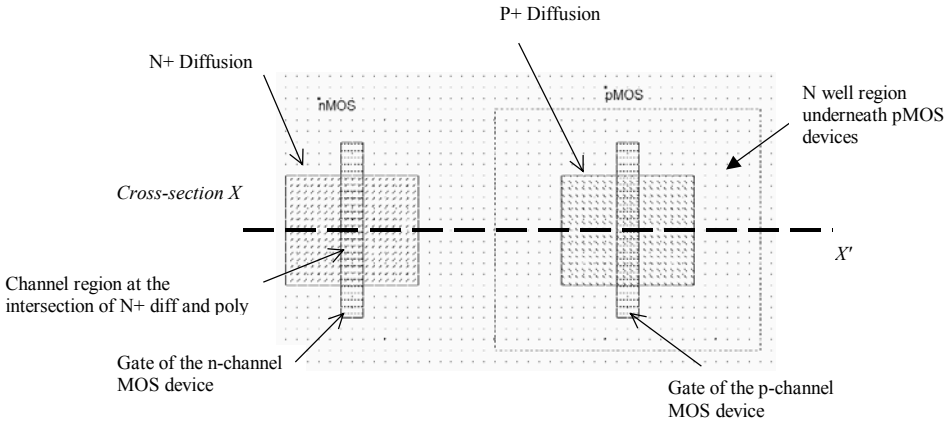

Figure 2-14: Bird's view of the n-channel and p-channel MOS device layout (allMosDevices.MSK)

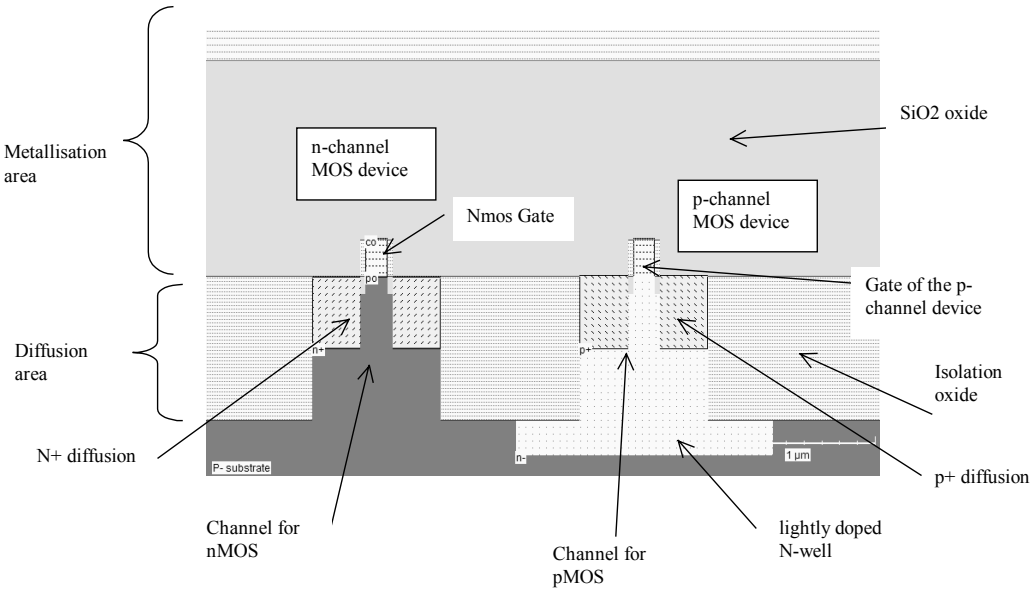

Figure 2-15: Vertical cross-section of an n-channel and p-channel MOS devices in 0.12µm technology (allMosDevices.MSK)

The layout of the nMOS and pMOS devices, seen from the top of the circuit, is shown in figure 2-xxx. The MOS is built using a set of layers that are summarized below. CMOS circuits are fabricated on a piece of silicon called wafer, <gloss> usually lightly doped with boron, that gives a p-type property to the material.

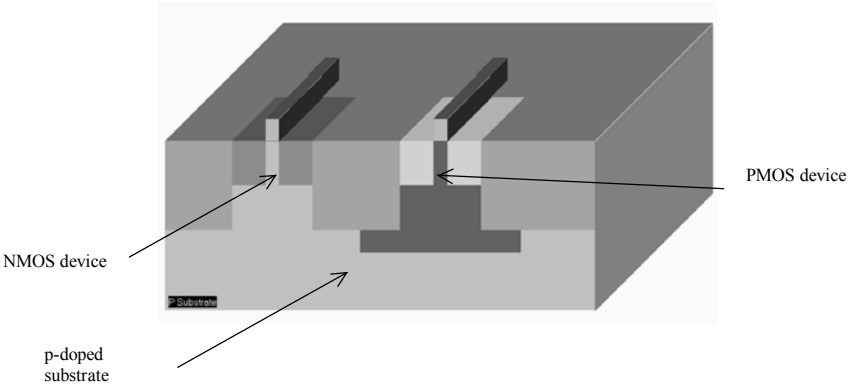

Figure 2-16: 3D view of the n-channel and p-channel MOS devices (AllMosDevices.MSK)

Zoom at Atomic Scale

When zooming on the gate structure, we distinguish the thin oxide beneath the gate, the low doped diffusion regions on both sides of the channel, the metal deposit on the diffusion surface, and the spacers on each side of the gate, as shown in figure 2-17.

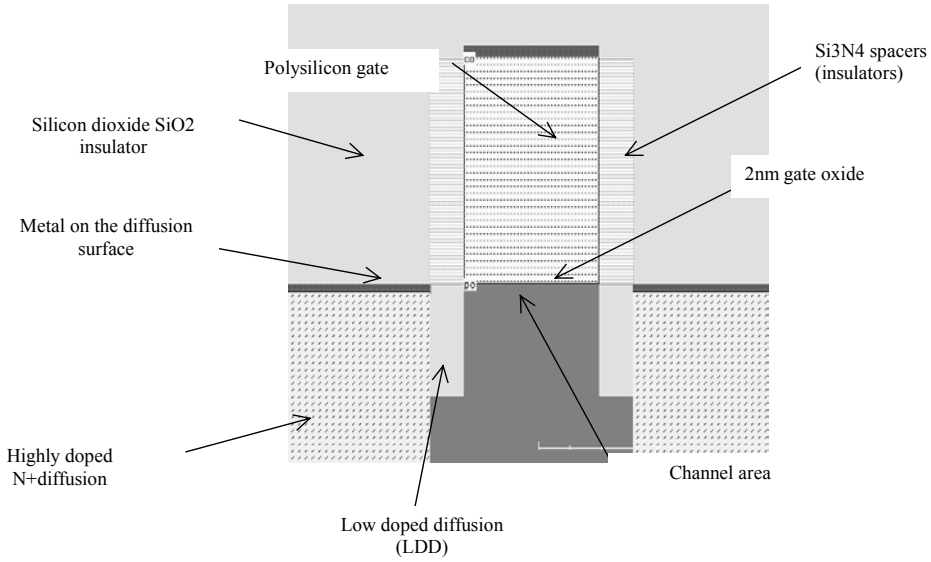

Fig. 2-17: Zoom at the gate oxide for a 0.12µm n-channel MOS device (AllMosDevices.MSK)

When zooming at maximum scale, we see the atomic structure of the transistor. The gate oxide accumulates between 5 and 20 atoms of silicon dioxide. In 0.12µm , the oxide thickness is around 2nm for the core logic, which is equivalent to 8 atoms of SiO2.

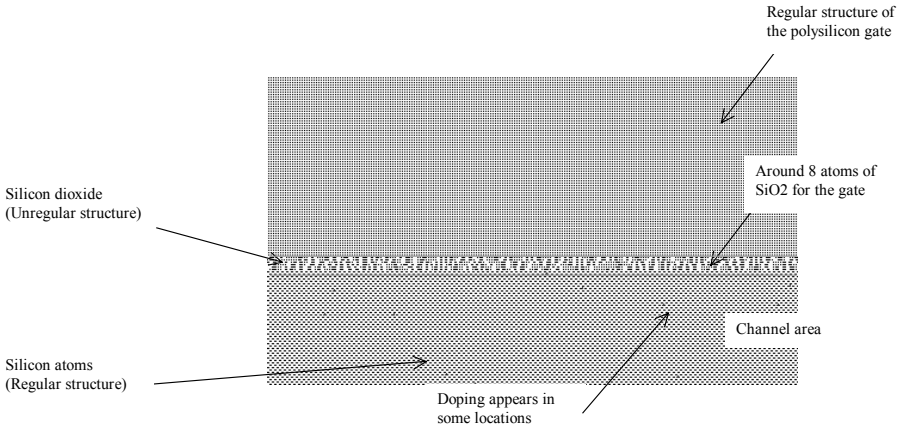

Fig. 2-18: Zoom at atomic scale near the gate oxide for a 0.12µm n-channel MOS device (AllMosDevices.MSK)

7. MOS layout

The objective of this paragraph is to draw the n-channel and p-channel MOS devices according to the design rules and usual design practices. The Microwind tool provided in the companion CD-Rom is used to draw the MOS layout and simulate its behavior.

The Microwind main screen shown in figure 2-19 includes two windows: one for the main menu and the layout display, the other for the icon menu and the layer palette. The main layout window features a grid, scaled in lambda (λ) units. The size of the grid constantly adapts to the layout. In figure 2-19, the grid is 5 lambda. The lambda unit is fixed to half of the minimum available lithography of the technology L_{min}. For example, the default technology is a CMOS 6-metal layers 0.12µm technology, consequently lambda is 0.06µm.

$$\lambda = \frac{L_{min}}{2} \qquad \text{(Equ. 2-2)}$$

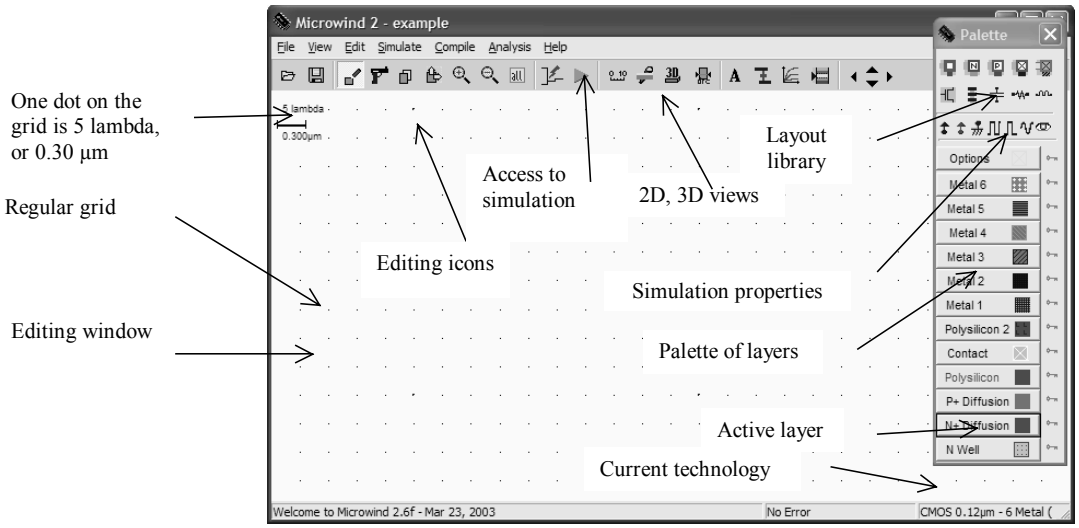

Figure 2-19 The MICROWIND2 window as it appears at the initialization stage

The palette is located in the right corner of the screen. A red color indicates the current layer. Initially the selected layer in the palette is polysilicon.

n-channel MOS layout

By using the following procedure, you can create a manual design of the n-channel MOS device. The n-channel MOS device consists of a polysilicon gate and a heavily doped diffusion area. Select the "polysilicon" layer in the palette window.

1) Fix the first corner of the box with the mouse. While keeping the mouse button pressed, move the mouse to the opposite corner of the box. Release the button. This creates a narrow box in polysilicon layer as shown in Figure 2-20. The box width should not be inferior to 2 λ, which is the minimum and optimal thickness of the polysilicon gate.

2) Change the current layer into N+ diffusion by a click on the palette of the N+ Diffusion button. Make sure that the red layer is now the N+ Diffusion. Draw a n-diffusion box at the bottom of the drawing as in Figure 2-20. The N+ diffusion should have a minimum of 4 lambda on both sides of the polysilicon gate. The intersection between diffusion and polysilicon creates the channel of the nMOS device.

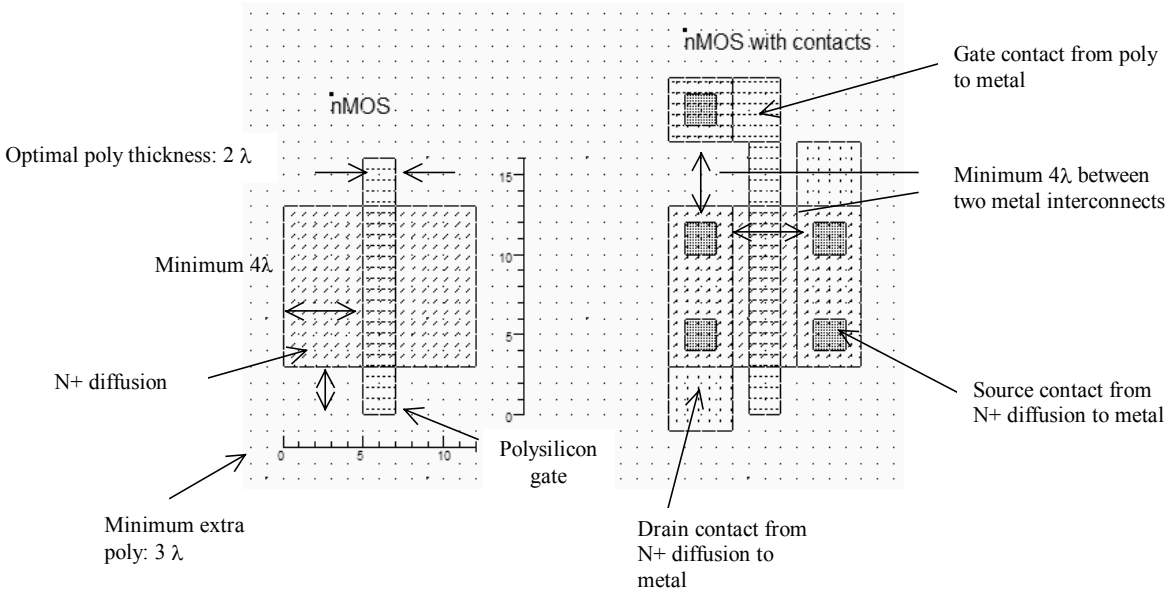

Figure 2-20. Creating the N-channel MOS transistor and adding contacts (AllMosDevices.MSK)

Now, we add the metal contacts to enable an electrical access to the source and drain regions. In the palette, such contacts are ready to instantiate on the layout (Figure 2-21). Click on the appropriate icon, and then the appropriate location in the left N+ diffusion. Repeat the process and add an other contact on the right part of the N+ diffusion. The layout aspect should correspond to the layout shown in figure 2-21.

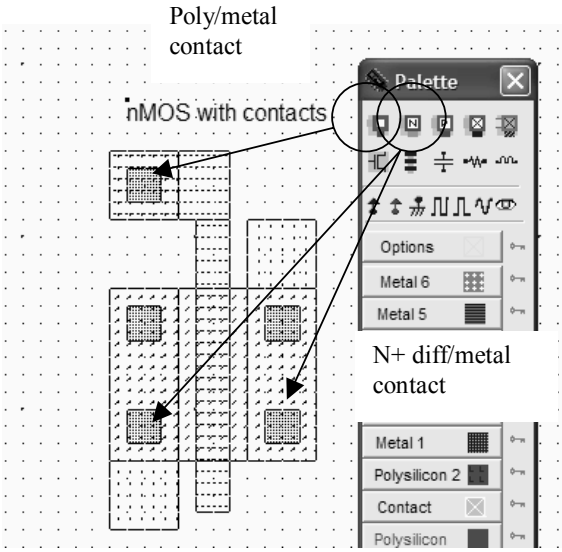

Figure 2-21. Access to the n-diffusion/metal and poly/metal contacts

Basic layers

The wafer serves as the substrate (or bulk) to N-channel MOS, which can be implemented directly on the p-type substrate. The n-channel MOS device is based on a polysilicon gate, deposited on the surface of the substrate, isolated by an ultra thin oxide (called gate oxide), and an N+ implantation that forms two electrically separated diffusions, on both side of the gate. The list of layers commonly used for the design of MOS devices is given in table 2-6.

Layer name	**Code**	**Description**	**Color in Microwind**
Polysilicon	Poly	Gate of the n-channel and p-channel MOS devices	Red
N+ diffusion	Diffn	Delimits the active part of the n-channel device. Also used to polarize the N-well	Dark green
P+ diffusion	Diffn	Delimits the active part of the p-channel device. Also used to polarize the bulk	Maroon
Contact	Contact	Makes the connection between diffusions and metal for routing. The contact plug is fabricated by drilling a hole in the oxide and filling the hole with metal.	White cross
First level of metal	Metal1	Used to rout devices together, in order to create the logic or analog function	Blue
N well	Nwell	Low doped diffusion used to invert the doping of the substrate. All p-channel MOS are located within N well areas.	Dotted green

Table 2-6: Materials used to build n-channel and p-channel MOS devices

p-channel MOS layout

The p-channel MOS is built using polysilicon as the gate material and P+ diffusion to build the source and drain. The pMOS device requires the addition of the n-well layer, into which the P+ implant is completely included, in order to work properly (Figure 2-22). By using the following procedure, you can create manually the layout of the p-channel MOS device.

- Select the "polysilicon" layer in the palette window.
- Create a narrow polysilicon box to create the p-channel MOS gate (The minimum value 2 lambda is often used). The material is the samel as for the n-channel MOS.
- Change the layer into P+ diffusion. Draw a p-diffusion box at the bottom of the drawing as in Figure 2-22. The P+ diffusion should have a minimum of 4 λ on both sides of the polysilicon gate.
- Select the *n-well* layer. Add an n-well region that completely includes the P+ diffusion, with a border of 6 λ, as illustrated in figure 2-22.

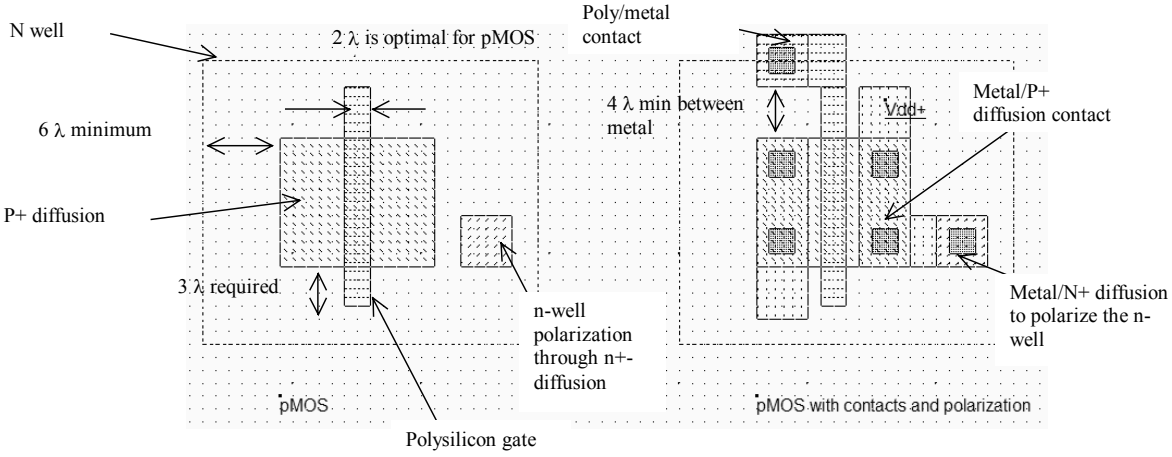

Figure 2-22. Creating the P-channel MOS transistor (AllMosDevices.MSK)

Moreover, the n-well region cannot be kept floating. A specific contact, that can be seen on the right side of the n-well, serves as a permanent connection to high voltage. Why high voltage? Let us consider the two cross sections in figure 2-23. On the left side, the n-well is floating. The risk is that the n-well potential decreases enough to turn on the P+/Nwell diode. This case corresponds to a parasitic PNP device. The consequence may be the generation of a direct path from the VDD supply of the drain to the ground supply of the substrate. In many cases the circuit can be damaged.

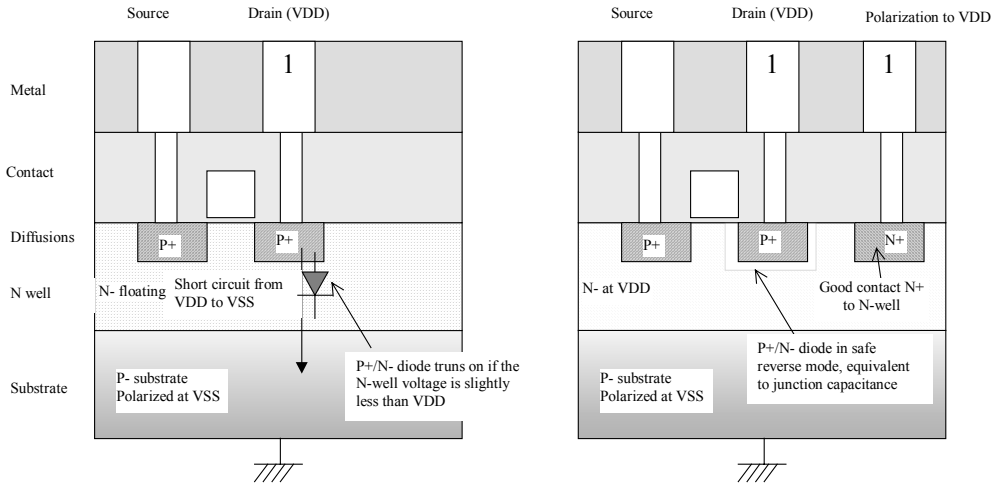

Fig. 2-23: Incorrect and correct polarization of the N-well

The correct approach is indicated in the right part of figure 2-24. A polarization contact carries the VDD supply down to the n-well region, thanks to an N+ diffusion. A direct contact to n-well would generate parasitic electrical effects, consequently, the N+ region embedded in the n-well area is mandatory. There is no more fear of parasitic PNP device effect as the P+/Nwell junctions are in inverted mode, and thus may be considered as junction capacitance.

Useful Editing Tools

Editing layout is rarely a simple task at the beginning, when cumulating the discovery of the editor user's interface and the application of new microelectronics concepts. The following commands may help you in the layout design and verification processes.

Command	Icon/Short cut	Menu	Description
UNDO	CTRL+U	Edit menu	Cancel the last editing operation
DELETE	 CTRL+X	Edit menu	Erase some layout included in the given area or pointed by the mouse.
STRETCH		Edit menu	Changes the size of one box, or moves the layout included in the given area.
COPY	 CTRL+C	Edit Menu	Copy of the layout included in the given area.

Table 2-7: A set of useful editing tools

Vertical aspect of the MOS

Click on this icon to access *process simulation* (Command ***Simulate → Process section in 2D***). The cross-section is given by a click of the mouse at the first point and the release of the mouse at the second point.

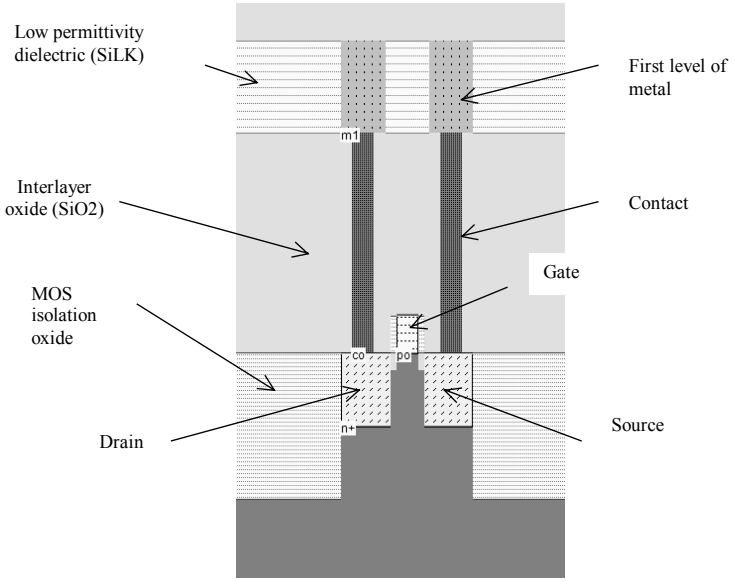

Figure 2-23. The cross-section of the nMOS devices (AllMosDevices.MSK)

In the example of Figure 2-23, three nodes appear in the cross-section of the n-channel MOS device: the gate (red), the left diffusion called *source* (green) and the right diffusion called *drain* (green), over a substrate (gray). A thin oxide called the gate oxide isolates the gate. Various steps of oxidation have led to stacked oxides on the top of the gate.

The lateral drain diffusion (LDD) is a small region of lightly doped diffusion, at the interface between the drain/source and the channel. A light doping reduces the local electrical field at the corner of the drain/source and gate. Electrons accelerated below the gate at maximum electrical field, such as in figure2-24 acquire sufficient energy to create a pair of electrons and holes in the drain region. Such electrons are called "hot electrons" <gloss>.

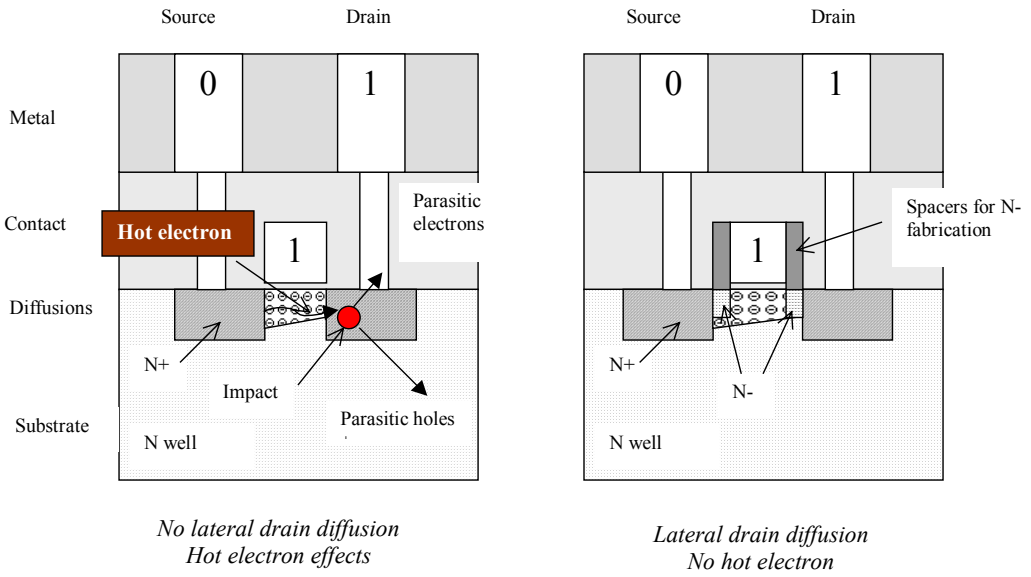

Figure 2-24. Lateral drain diffusion reduces the hot electron effect.

Consequently, parasitic currents are generated in the drain region. One part of the current flows down to the substrate, an other part is collected at the drain contact. The lateral drain diffusion <gloss> efficiently reduces this parasitic effect. This technique has been introduced since the 0.5µm process generation.

8. Dynamic MOS behavior

In this paragraph, we stimulate the MOS device with variable voltages in order to verify by analog simulation their correct behavior as switches. The proposed simulation setup (Figure 2-25) consists in applying 0 and 1 to the gate and the source, and see the effect on the drain, as outlined in the schematic diagram below.

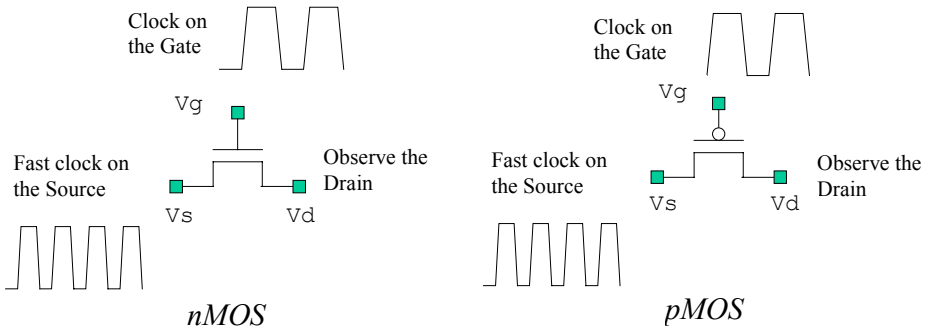

Fig. 2-25. Verification of the MOS switching properties using clocks

n-channel MOS behavior

The expected behavior of the n-channel MOS device is summarized in figure 2-26. The 0 on the gate should leave the drain floating. The 1 on the gate should link the drain to the source, via a resistive path.

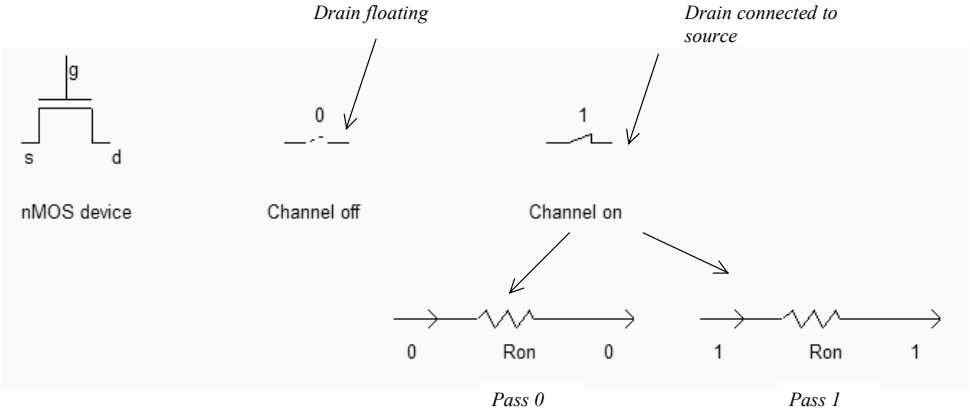

Fig. 2-26. Expected n-channel MOS switching characteristics(MosExplain.SCH)

The most convenient way to operate the MOS is to apply a clock property to the gate, another to the source and to observe the drain. The summary of available properties that can be applied to the layout is reported below.

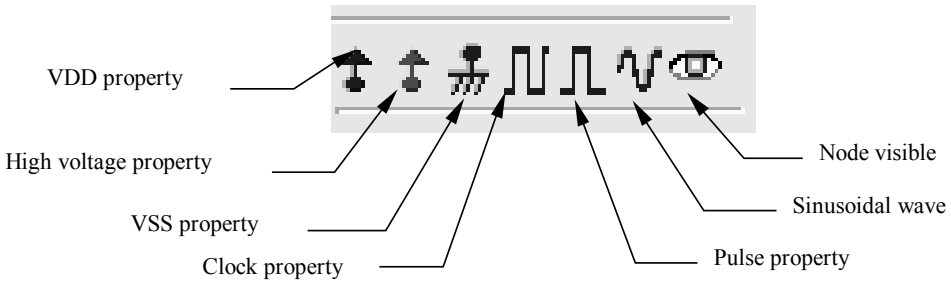

Fig. 2-27. Simulation properties used to conduct the simulation from layout

A clock should be applied to the source, which is situated on the green diffusion area at the left side of the gate. Click on the Clock icon and then, click on the polysilicon gate. The clock menu appears again. Change the name into « Vdrain» and click on OK to apply a clock with 1ns period (0.225ns at 0, 25ps rise, 0.225ns at 1, 25ps fall). The label « Vdrain» appears at the desired location in italic, meaning that the waveform of this node will appear at the next simulation.

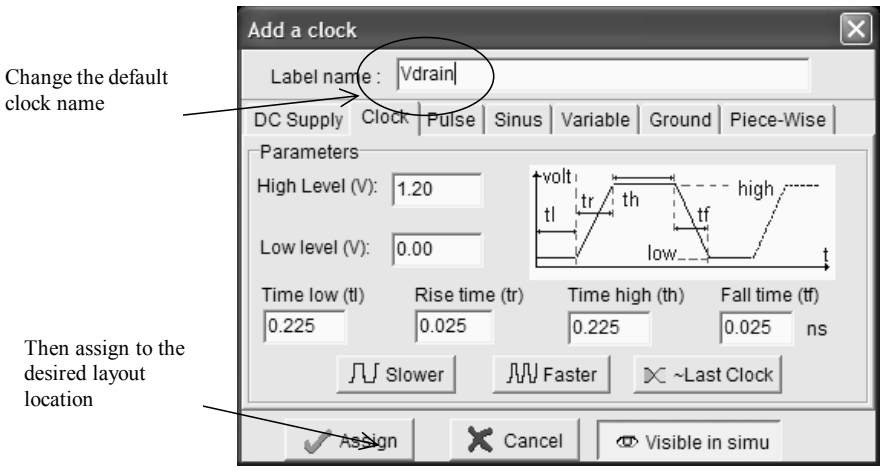

Fig. 2-28. Details on the clock parameters and clock menu.

Now, to apply a clock to the gate, click again on the Clock icon, and click on the polysilicon gate. The Clock menu appears. Notice that the clock parameters "Time low" and "Time high" has been automatically increased by 2, to create a clock with a period twice slower than previously. Change the name into « Vclock» and click on OK. The Clock property is sent to the gate and appears at the right hand side of the label « Vgate ».

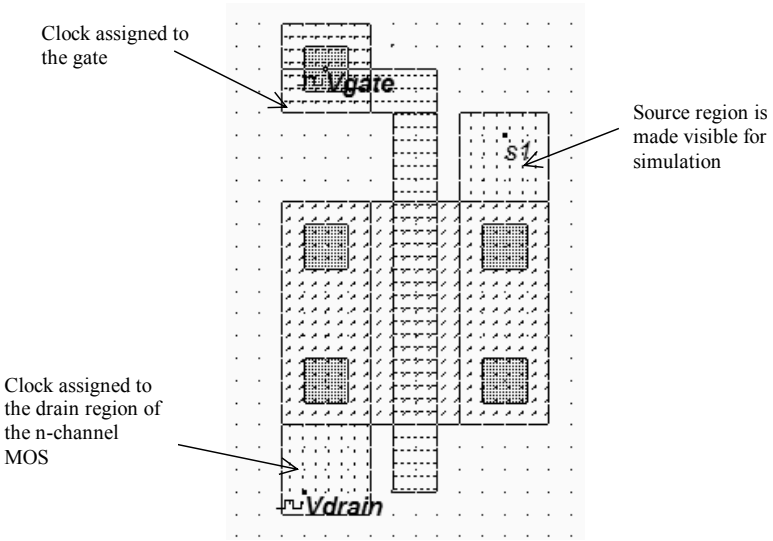

Fig.2- 29. Properties added to the layout for controlling the analog simulation (mosN.MSK)

In order to see the source, click on the eye ("Node Visible") property situated in the palette menu (See fig. 2-30) and click on the right diffusion. Change the label name into "Vout". Click OK. The visible property is then sent to the node. The associated text « Vout » is in italic, meaning that the waveform of this node will appear at the next simulation.

The layout should then appear as illustrated in figure 2-31. The clock properties are situated on the gate and the left N+ diffusion, the "node visible" property is located on the right part of the N+ diffusion. The layout is now ready for analog simulation.

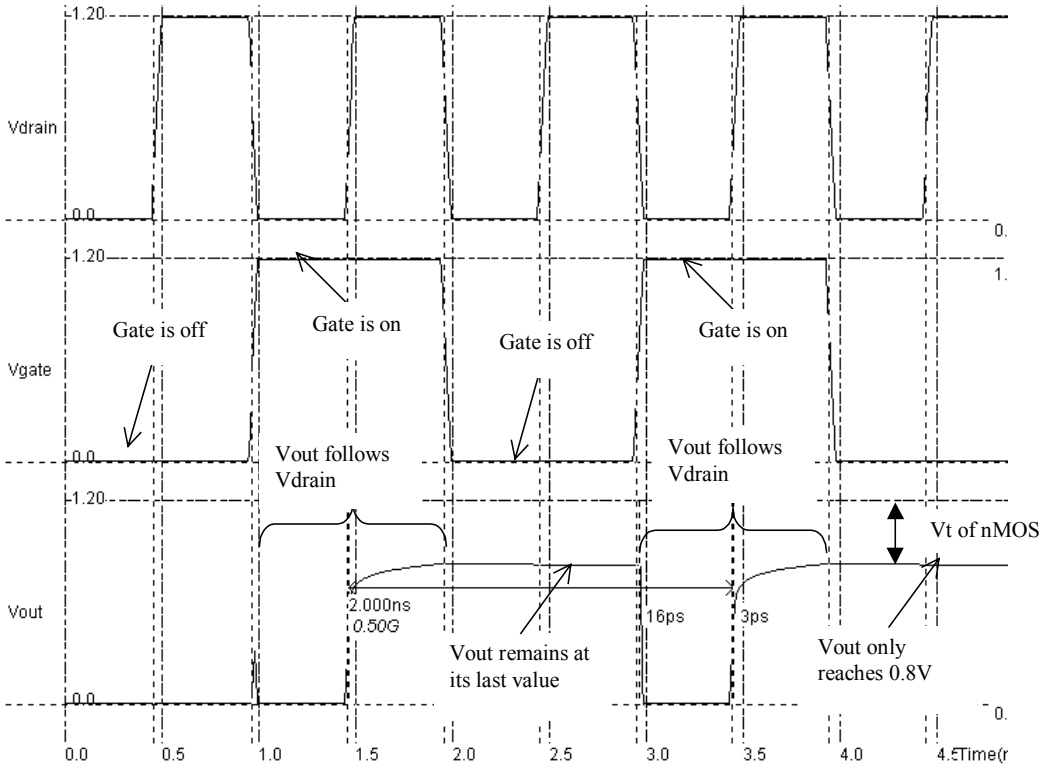

Fig.2- 31. Analog simulation of the n-channel MOS device (MosN.MSK)

Click on **Simulate → Run Simulation → Voltage vs. Time** (Or CTRL+S, or the icon "Run Simulation" in the main iucon menu). The timing diagrams of the nMOS device appear, as shown in Figure 2-31. Most of the logic and analog behavior of the MOS device are summarized in this single figure.

The upper waveform correspond to Vdrain, with a clock from 0 to 1.2V (VDD is 1.2V in 0.12µm), exhibiting a 1ns period. Below is the gate voltage. The n-channel MOS is off when Vgate is zero, and on if Vgate is 1.2V. The third waveform concerns Vout. Its aspect is very interesting: from 0 to 1ns, its value is zero, which is the default voltage value of all nodes in the layout. The channel is off, consequently nothing happens to the drain. When the gate is on, the channel enables Vout to copy the value of Vdrain (Time 1.0 to 2.0ns).

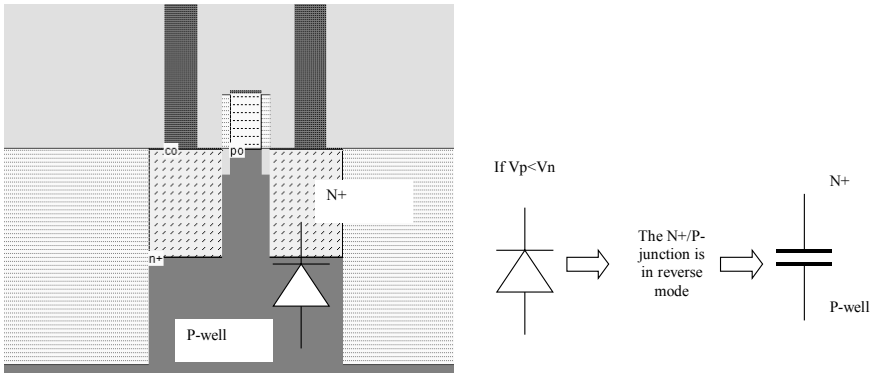

Fig.2- 32. The P/N junction in reverse mode is equivalent to a capacitor that memorizes s the voltage when the channel is off (MosN.MSK)

Then, when the gate is off again (Time 2.0 to 3.0), the voltage remains almost at its last value. The reason is illustrated in figure 2-xxx: the junction P-well/N+ diffusion is in reverse mode and can be considered as a capacitor. The charges are stored in this junction capactor while the channel is off, xwhich keep its voltage stable, indepedantly of the source fluctuations.

Notice a very small decrease of the voltage, due to parasitic leakage effect <gloss> between source and drain. Click **More** in order to perform more simulations. Click on **Close** to return to the editor.

Threshold Voltage

You probably noticed that the voltage Vout never reaches 1.2V. It "saturates" to around 0.8V. The reason is the parasitic effect called threshold voltage, which is around 0.4V in the default technology 0.12µm. In summary, the n-channel MOS device behaves as a switch, but when on, it do not passes correctly the high voltages. A zero on one side leads to a good zero, a logic 1 on one side leads to a poor 1. The main reason is the threshold voltage of the MOS.

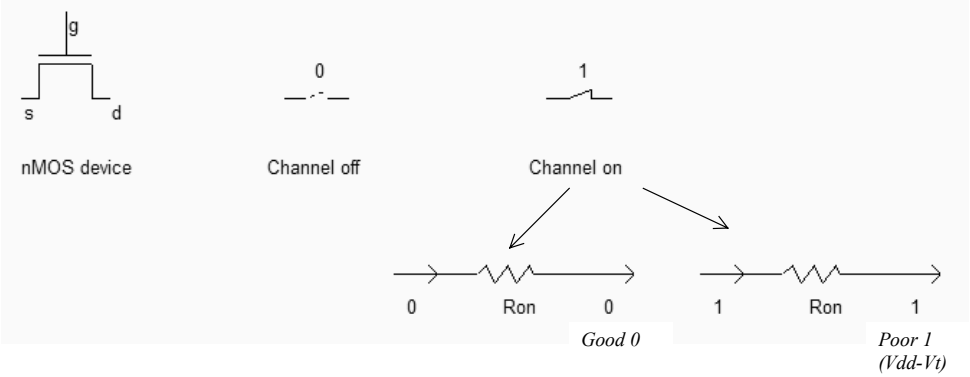

Fig.2- 33. The nMOS device behavior summar (MosExplain.SCH)

p-channel MOS behavior

The expected behavior of the n-channel MOS device is summarized in figure 2-34. The 0 on the gate should link the drain to the source, via a resistive path. The 1 on the gate should leave the drain floating. In other words, the p-channel transistor simulation features the same functions as the n-channel device, but with opposite voltage control of the gate.

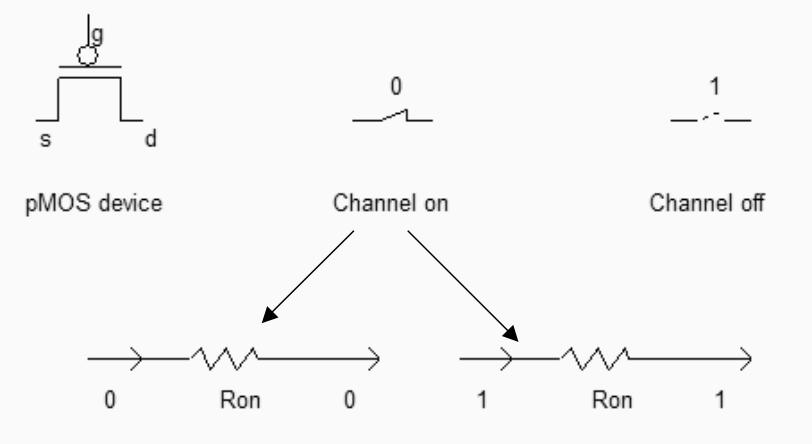

Fig. 2-34. Expected p-channel MOS switching characteristics(MosExplain.SCH)

Again, we operate the p-channel MOS device by using two clocks, one to the gate, another to the source and to observe the drain. Be sure to add the polarization contact inside the n-well region, and add a supplementary VDD property on top of the contact.

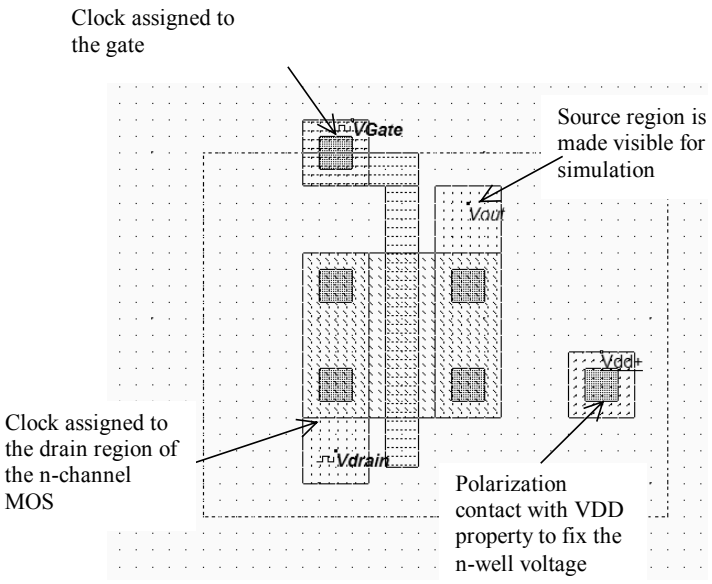

Fig.2- 35. Properties added to the layout for controlling the analog simulation of the p-channel device (Mosp.MSK)

Click on **Simulate → Run Simulation → Voltage vs. Time**. The timing diagrams of the pMOS device appear, as shown in Figure 2-36. The upper waveform correspond to Vdrain, with a clock from 0 to 1.2V (VDD is 1.2V in 0.12µm), exhibiting a 1ns period. Below is the gate voltage. The p-channel MOS is on when Vgate is zero, and off when Vgate is 1.2V. When the gate is on, the channel enables Vout to copy the value of Vdrain (Time 0 to 1.0ns). Then, when the gate is off again, the voltage remains almost at its last value. The reason why Vout kept around 1.0V from 1.0 to 2.0ns is that the channel turned off synchronously with a change in the value of Vdrain.

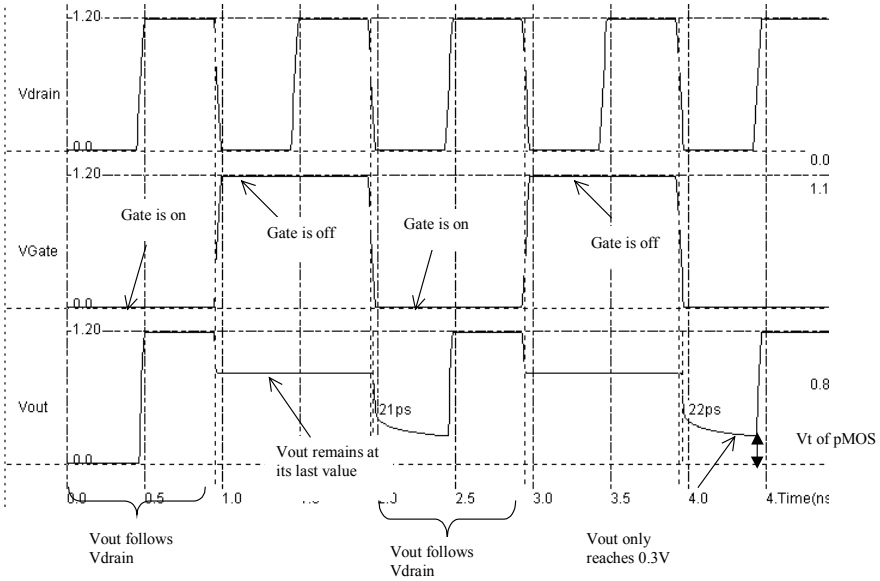

Fig. 2-36. Time domain simulation of the p-channel MOS (Mosp.MSK)

Notice that for the p-channel MOS, the voltage Vout never reaches 0.0V. It "saturates" to around 0.3V, due to the threshold voltage of the device. In summary (Figure 2-37), the p-channel MOS device behaves as a switch, but when on, it do not passes correctly the low voltages. A zero on one side leads to a poor zero, a logic 1 on one side leads to a good 1.

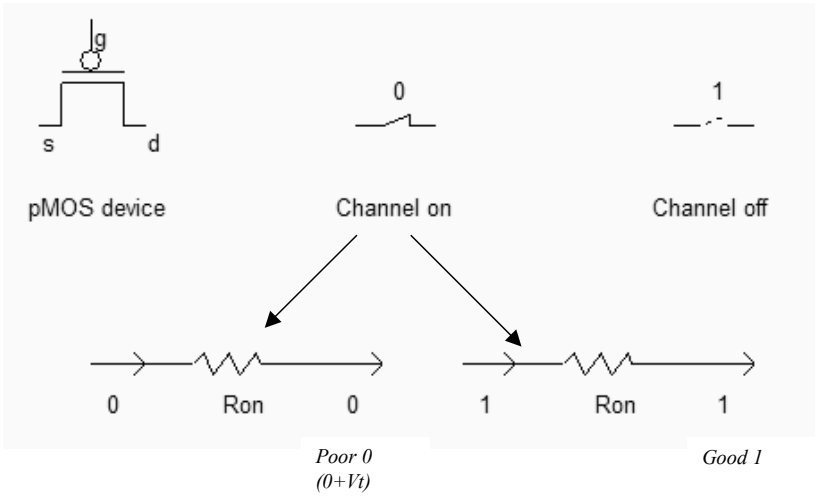

Fig. 2-37. Summary of the performances of a pMOS device

9. The Perfect switch

Both NMOS devices and PMOS devices exhibit poor performances when transmitting one particular logic information. The nMOS degrades the logic level 1, the pMOS degrades the logic level 0. Thus, a perfect pass gate can be constructed from the combination of nMOS and pMOS devices working in a complementary way, leading to improved switching performances. Such a circuit, presented in figure 2-38, is called the transmission gate <gloss>. In DSCH2, the symbol may be found in the "advance" menu in the palette. The main drawback of the transmission gate is the need for two control signals Enable and /Enable, thus an inverter is required.

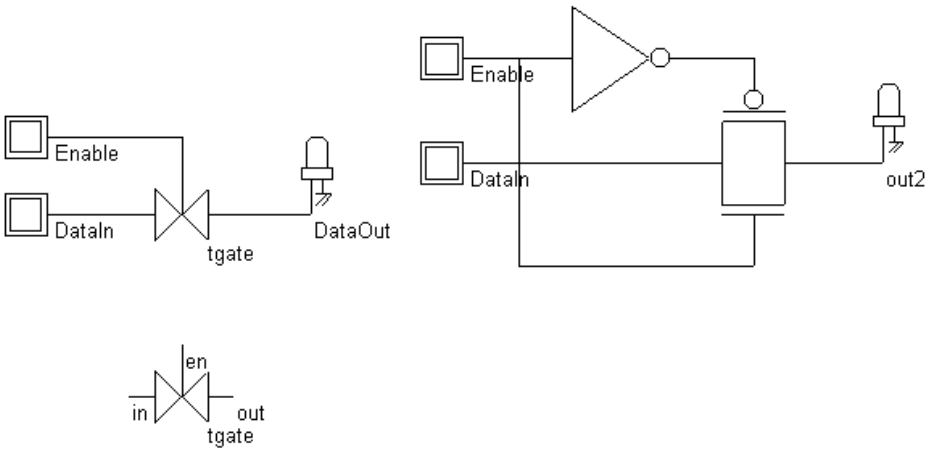

Fig. 2-38. Schematic diagram of the transmission gate (Tgate.SCH)

The transmission gate let a signal flow if *en*=1 and *~en*=0. In that case both the n-channel and p-channel devices are on. The n-channel MOS transmits low voltage signals, while the p-channel device preferably transmits high voltage signals (Figure 2-39).

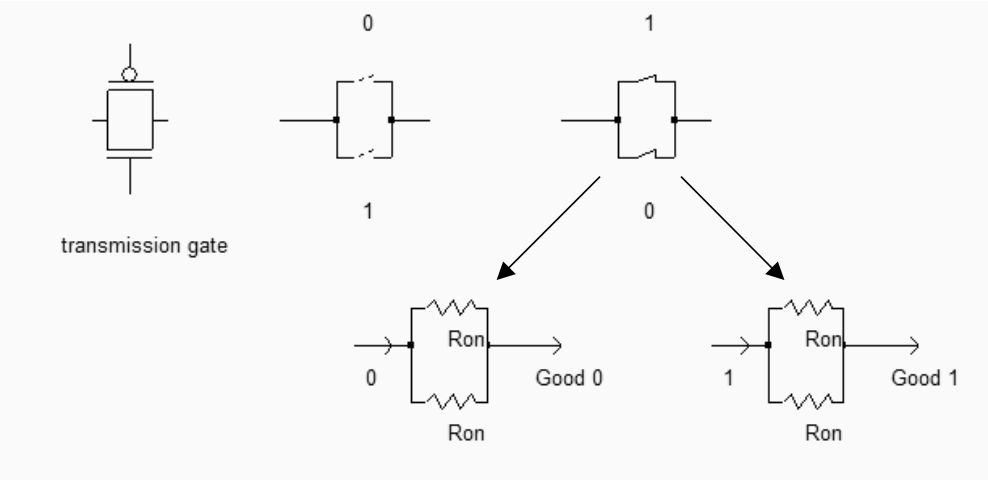

Fig. 2-39. The transmission gate used to pass logic signals(Tgate.SCH)

Implementation

We need to create an electrical connection between the N+ and P+ regions, in order to comply with the schematic diagram shown in figure 2-39. The most efficient solution consists in using metal and contacts to create a bridge from the N+ region to the P+ region. Figure 2-40 shows the cross-section of the bridge.

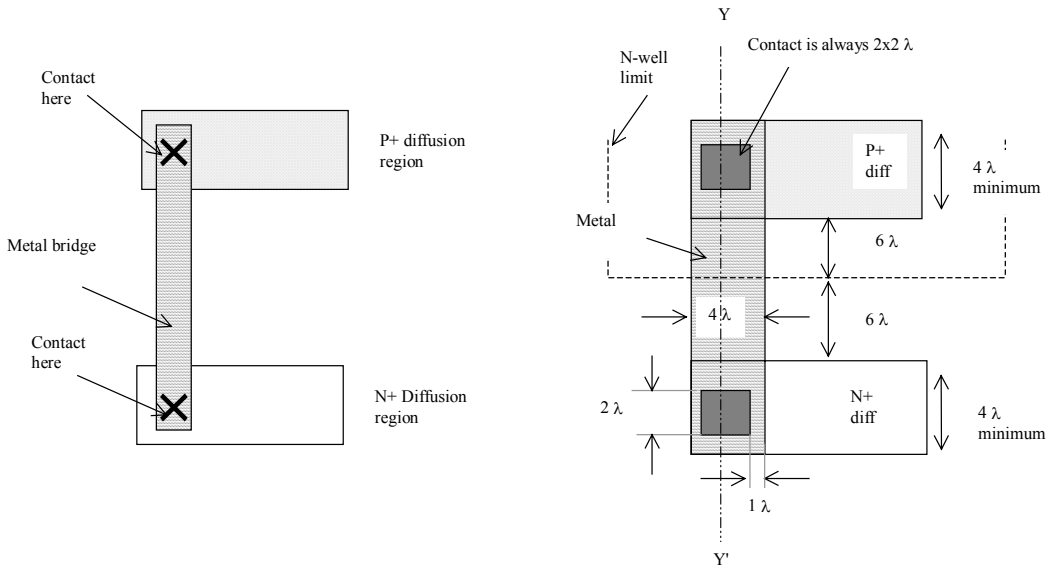

Fig. 2-40. Principles for metal bridge between N+ diffusion and P+ diffusion regions, and associated design rules.

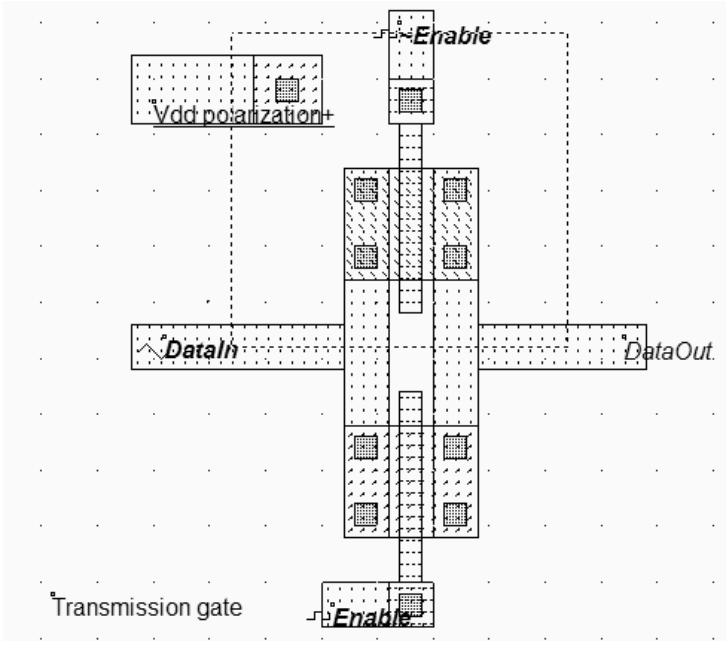

Fig. 2-41: Layout of the transmission gate (TGATE.MSK)

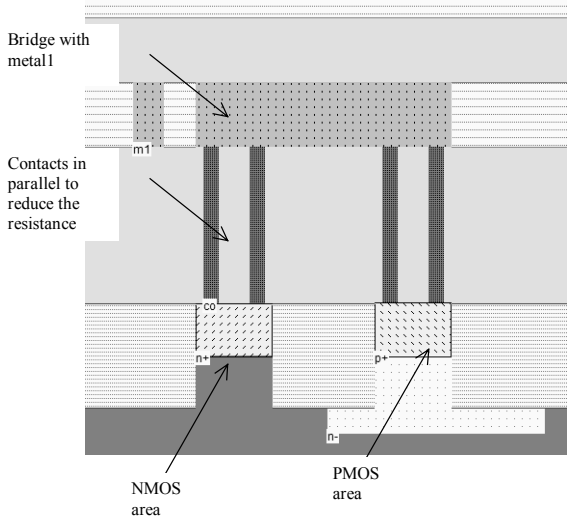

Fig. 2-42. Cross-section at location Y-Y' showing the metal bridge and contacts to N+ diffusion and P+ diffusion regions

The layout of the transmission gate is reported in figure 2-41. The n-channel MOS is situated arbitrarily on the bottom, and the p-channel MOS on the top. Notice that the gate controls are not connected, as *~Enable* is the opposite of *Enable*. The operation of the transmission gate is illustrated in figure 2-43. A sinusoidal wave with a frequency of 2GHz is assigned to *DataIn*. The sinusoidal property may be found in the palette of Microwind2, near the clock and pulse properties. With a zero on Enable (And a 1 on *~Enable*), the switch is off, and no signal is transferred. When *Enable* is asserted, the sinusoidal wave appears nearly identical to the output.

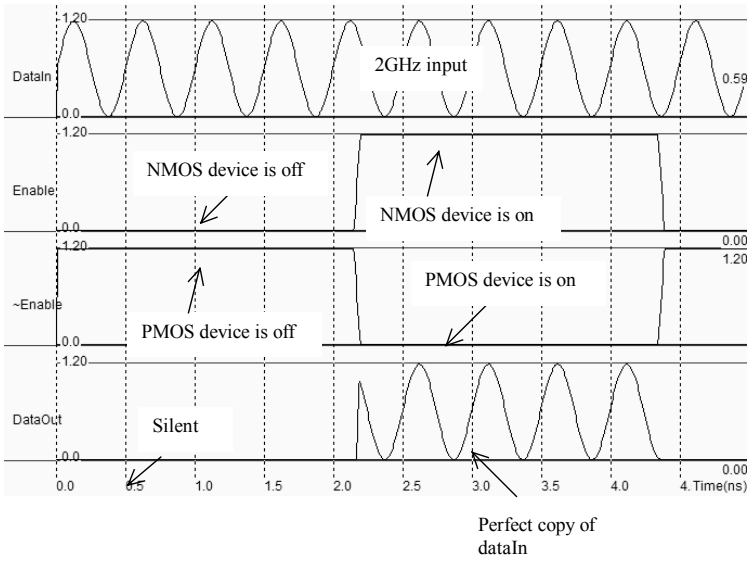

Fig. 2-43. Simulation of the transmission gate (TGATE.MSK)

10. Layout considerations

MOS generation

The safest way to create a MOS device is to use the MOS generator. In the palette, click the MOS generator icon. A window appears as reported below. The mains parameters are the MOS type (either n-channel or p-channel), the width and the length. By default, the proposed MOS is a n-channel device, with a width 0.6µm and minimum length 0.12µm. The maximum current that can flow in the MOS channel is given for information (0.262mA in that case). The units for width and length are in µm by default. You may change the units and use lambda values instead.

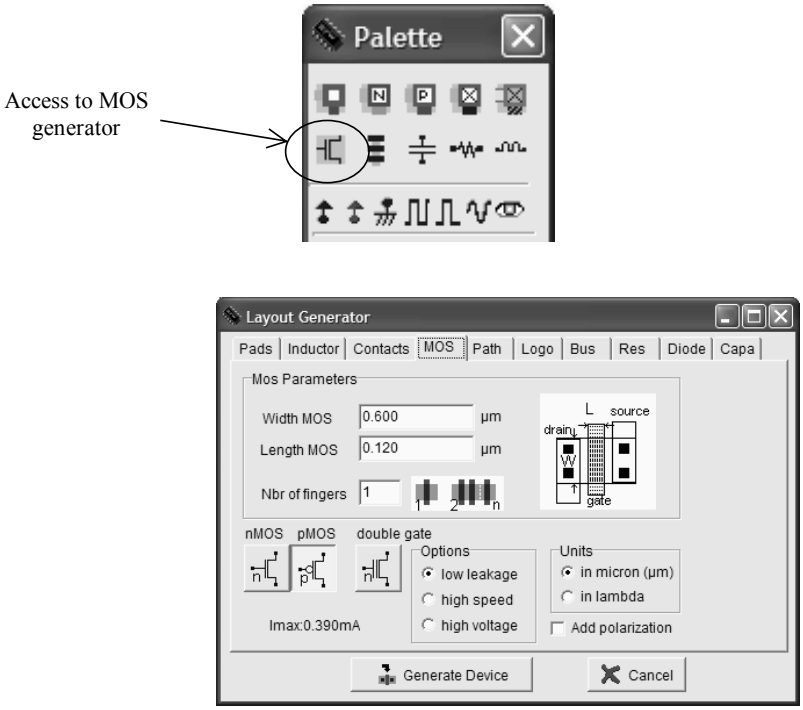

Fig.2-44. Access to the MOS generator menu

Starting 0.18µm technology, three types of MOS devices have been made available: low leakage, high speed and high voltage devices. Those concepts will be developed in the next chapter.

If we increase the width of the MOS device to 2µm, the layout generated by Microwind2 takes the aspect of figure 2-45. Notice the length equal to 2 λ, that is 0.12µm in the default technology, the width equal to 2µm.

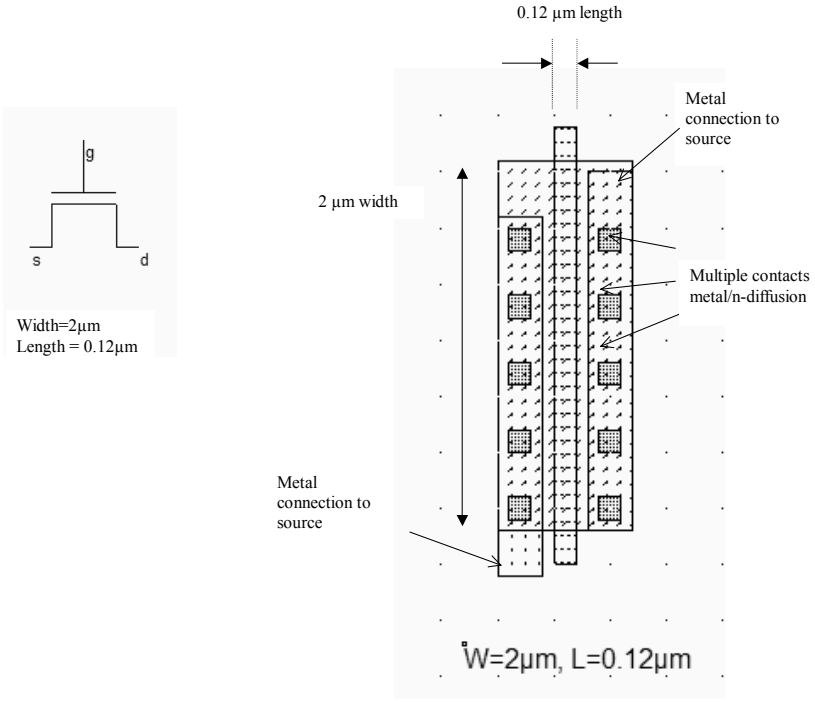

Fig.2-45. A n-channel MOS with 2µm width generated by Microwind2(MosLayout.MSK)

Multiple contacts

In the layout of figure 2-45, the surprise comes from the multiple contacts on the drain and source regions. The reason for this addition of contacts is due to the intrinsic current limitation of each elementary contact plug, as well as the high resistance of one single contact. One single contact can suffer less than 1mA current without any reliability problem. When the current is stronger 1mA, the contact can be damaged (Figure 2-46). The effect is called electromigration: if too much current flows within the contact, the metal structure starts to change as atoms move inside the conductor. A very strong current such as 10mA would even destroy one lonely contact.

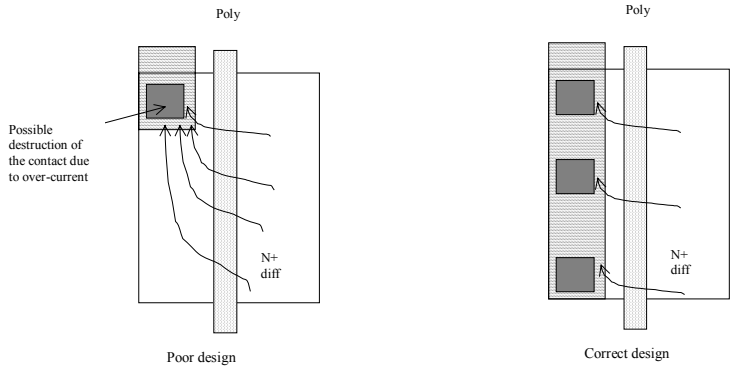

Fig.2-46. A strong current through a single contact could damage the metal structure.

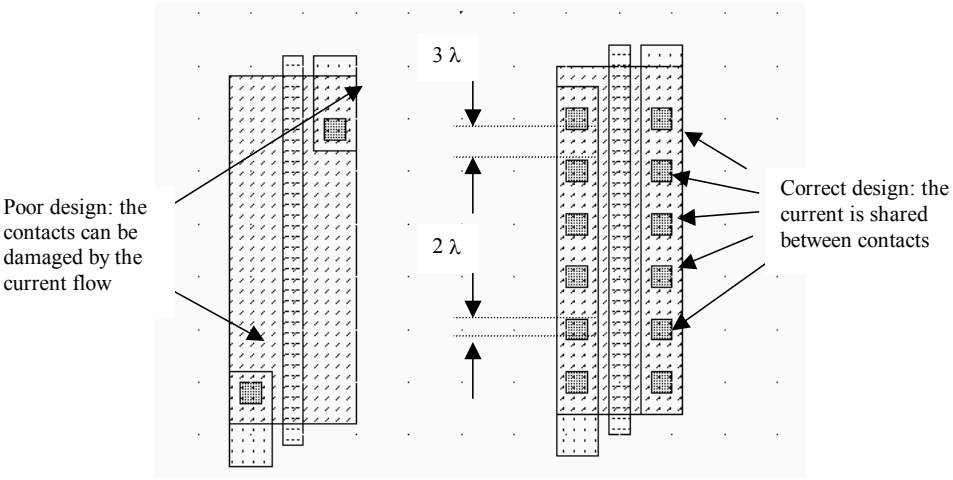

Fig.2-47. A single contact cannot handle more that 1mA. A series of contacts is preferred (MosLayout.MSK)

The illustration of this important limitation is given in figure 2-48. Basic rules for contact design are also reported in the figure. The contact is 2x2 λ, and the separation is 4 λ.

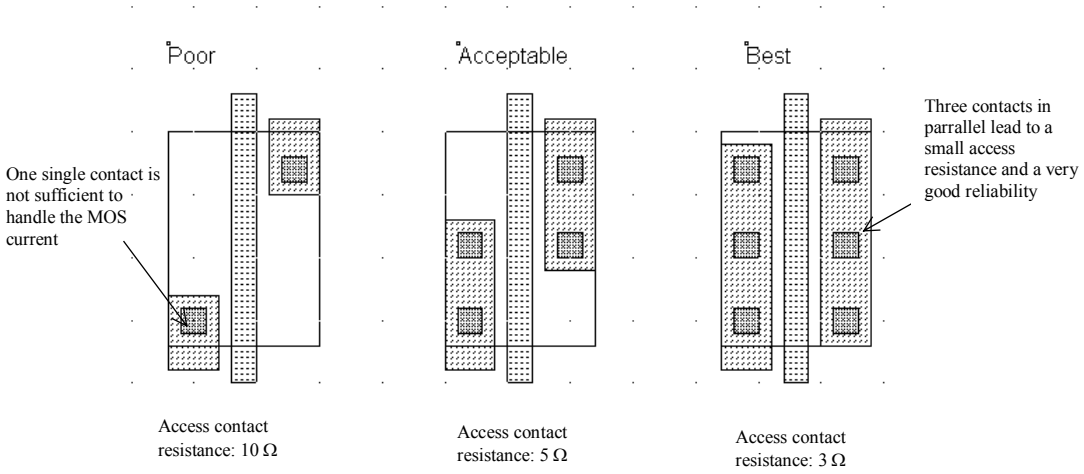

Fig.2-48. A series of contacts also reduced the serial access resistance(MosContacts.MSK)

Adding as many contacts as the design rules permit also limits the contact resistance. The equivalent resistance of the access to drain and source regions is reduced proportionally to the number of contacts.

Multiple gates

The use of MOS devices with long width is very common, for example in analog design and buffer design such as clocks and interface structures. Let us try to design a 5mA MOS switch., which can be found in a

standard output buffer structure. A rapid investigation using the maximum current evaluation in the MOS generator menu leads to the need of a MOS device with W=12µm, L=0.12µm. The corresponding layout is reported in figure 2-49. The two main drawbacks of this layout are the very unpractical shape of the structure, and the important parasitic resistance along the polysilicon gate, that delays the propagation of the control voltage, thus slows down the switching of the device.

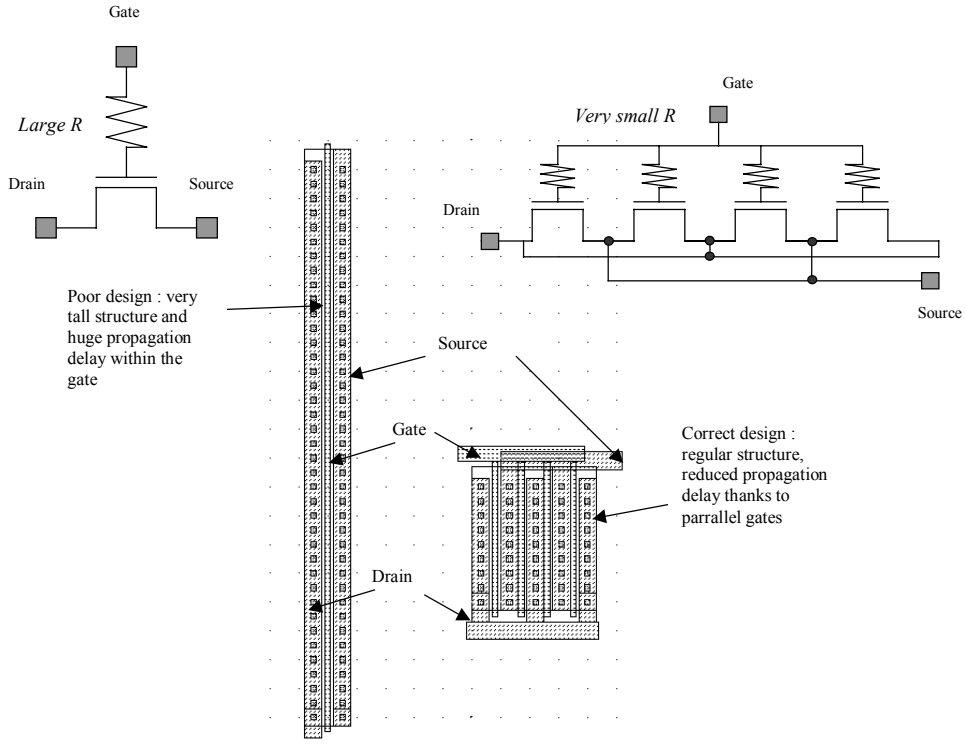

Fig.2-49. MOS devices with large with must be designed with parallel gates to reduce the delay (MosLayout.MSK)

The most efficient solution is to connect MOS devices in parallel. Firstly, the polysilicon gate length is divided by four in the case of figure 2-49, secondly, the structures becomes regular, easing the future interconnections. Notice how drains and sources are interleaved to create an equivalent device with the same channel with and length, and consequently the same current ability.

11. CMOS process

The process <gloss> steps to fabricate the integrated circuit are illustrated in this paragraph. The starting material is an extremely pure silicon substrate, entering in the foundry as a thin circular wafer. The wafer diameter for 0.12µm technology is 8 inches. Most CMOS processes use lightly doped p-type wafers.

Masks

The complete fabrication includes a series of chemical steps in order to diffuse doping materials (n-well, N+ and P+ diffusions), or to deposit materials (polysilicon, contacts and metals). The chemical attack is driven by optical masks <gloss> on which the patterns are drawn. The masks are listen in figure 2-50.

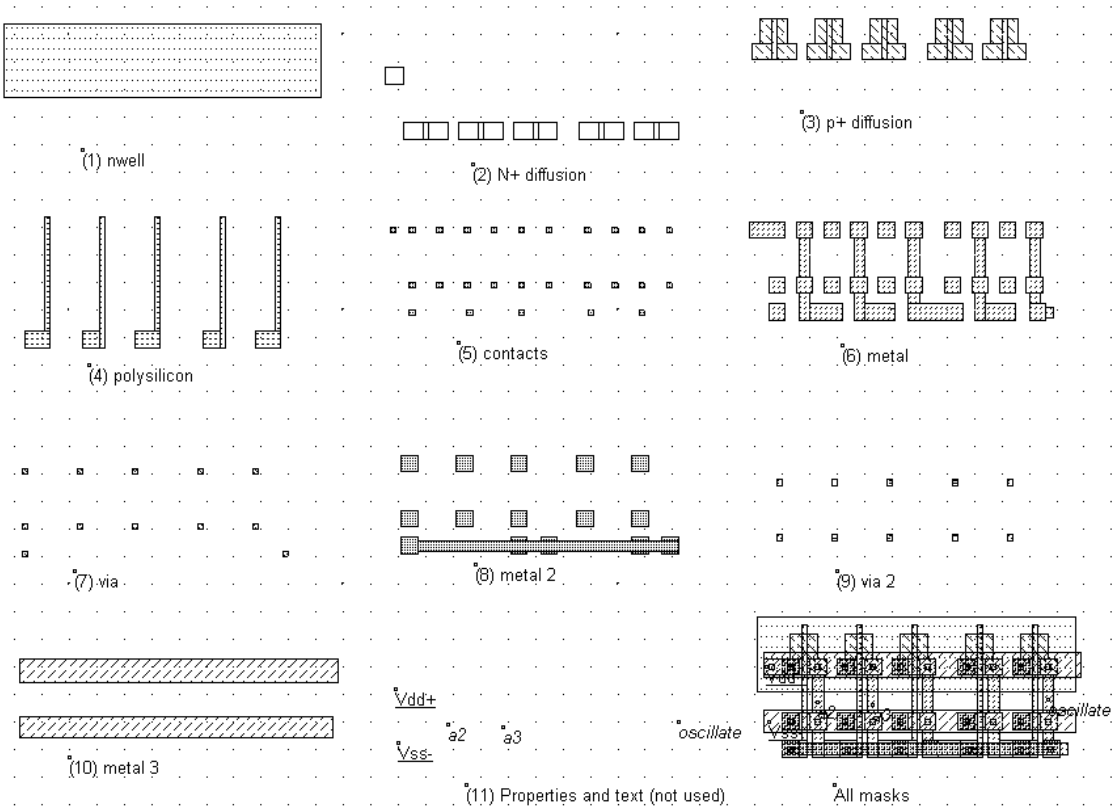

Fig. 2-50: Splitting the layers of the INV5 circuit into separate masks (Inv5Steps.MSK)

In deep submicron technologies, the price of these mask accouts for a significant percentage of the total cost of the chip fabrication. The reason is the extreme precision of each mask, which must have no defect at all, in order to succeed in fabrication the chip correctly. The complete set of masks in 0.12µm is around 100,000 euro. This price should rise significantly in nano-scale technologies (90nm and below), and become the primary limiting factor.

CMOS process steps

Let us load first the ring oscillator used in Chapter 1 to illustrate the operating frequency increase with the scale down (INV5.MSK). The masks can be split into 11 layers as described in figure 2-50. The

illustration of the process steps piloted by these masks is included in Microwind2. The access command is **Simulate →Process steps in 3D**.

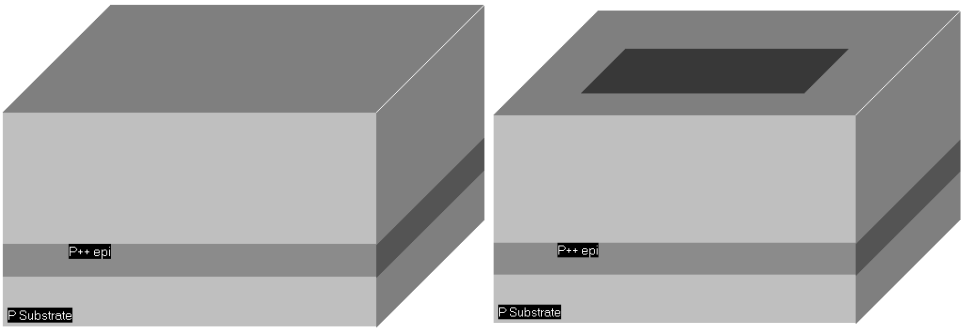

Fig. 2-51: The fabrication of the nwell (Inv5.MSK)

A portion of the substrate is shown in figure 2-51. The substrate is a p-type wafer, with a resistivity around 10 Ωcm. A P++ layer is situated some microns below the surface of the wafer. Due to its very low resistivity, it serves as a ground plane. Not all CMOS processes use this P++ layer, mainly for cost reasons. In the 3D process window, click "Next step" to skip to the next technological step.

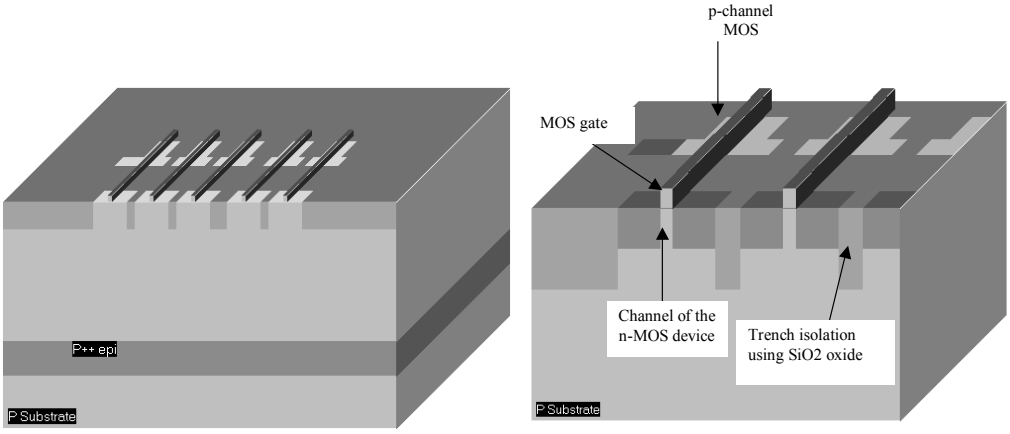

Fig. 2-52: N+ diffusion, P+ diffusion (left) and polysilicon deposit (right) (Inv5.MSK)

The n-well mask is used here to build the n-well area, into which p-channel devices will operate. N-channel devices use the native p-type substrate, without the need of a P-well. Next, a thick oxide is created to isolate MOS devices. In 0.12µm this step is called shallow trench isolation <gloss>. Then, a crucial step consists in growing a very high quality, extremely thin oxide that isolates the gate from the channel. Extraordinary precautions are taken to create millions of atomic-scale gate oxides, around 18 Å thick in 0.12µm, that is 8 atoms of SiO_2. On the top of that ultra-thin oxide, the polysilicon gate is deposited (Figure 2-52).

Then, n-type dopant ions, usually using arsenic of phosphor, are implanted to form the drain and source regions of the n-channel MOS devices. The polysilicon gates block the ions and prevent the underlying

channel from any n+ dopant. The gate serve as a mask to separate the implanted area into two electrically different regions, the source and the drain. Consecutively, p-type boron ions are implanted to form the p-channel drain and sources.

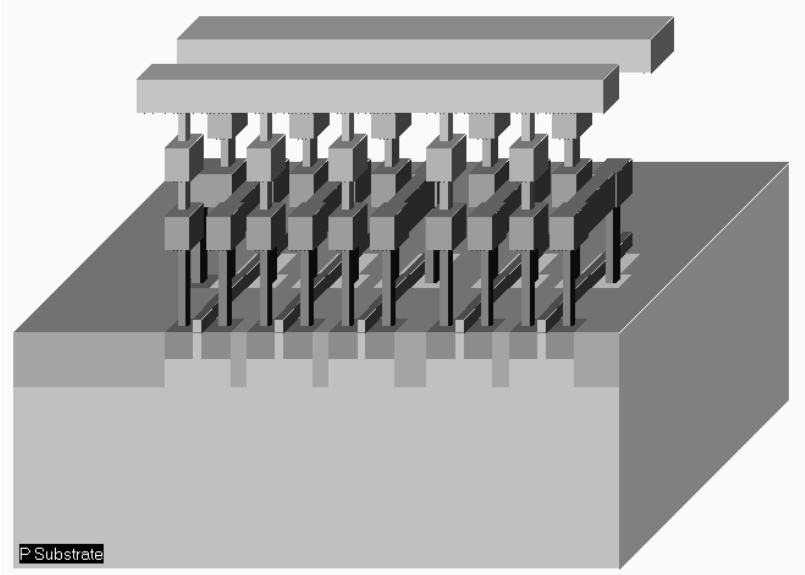

Fig. 2-53: Fabrication of the metal interconnects (oxide not shown for clarity) (Inv5.MSK)

The next steps are related to metallization. Up to 6 metal layers can be fabricated, on the top of each other, in 0.12µm. When the contact and metal steps are completed, the chip takes the aspect shown above. Notice that oxides have been removed for clarity (Figure 2-53). You may see the oxide in the window showing the process aspect in 2D, accessible from the Simulation menu of Microwind2.

At the end of the process comes the passivation <gloss>, consisting the growth an oxide, usually Si3N4. The structure of the oxides that separate the metal layers is not homogeneous. Recent advances in lithography have generalized the use of low dielectric oxides together with the traditional native oxide SiO2. The combinational use of $Si0_2$ and low dielectric oxide will be justified in chapter 5, dedicated to interconnects.

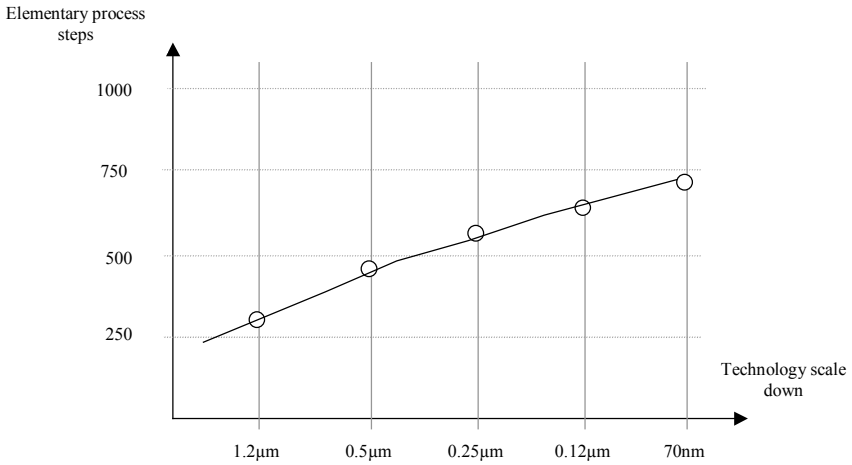

Fig. 2-54: Increase of elementary process steps with the technology scale down.

Each process step appearing in the process simulation window of Microwind2 is the sum of elementary chemical, mechanical and optical steps. Consequently, a complete technological process such as 0.12µm is made up with more than 600 elementary steps. The global trend is the increase of technological steps with the technology scale down, as shown in figure 2-54. Therefore, the cost of fabrication is also increased accordingly.

12. Conclusion

In this chapter, we described the atomic structure of silicon, and gave some information about P-type and N-type materials. The silicon dioxide has also been investigated. Then, we presented the MOS device from a simple functional point of view, and focused on its switching properties. We presented the two types of MOS devices: n-channel and p-channel MOS. Though analog simulation, we exhibited the good and poor performances of these switches, depending on the logical information. We also proposed a good switch that takes advantage of nMOS and pMOS properties. Finally, we described the MOS layout editing using Microwind, shown how to conduct analog simulation by adding simulation properties such as clocks, supplies, and sinusoidal voltages directly on the layout. The final part of this chapter was dedicated to the CMOS process steps.

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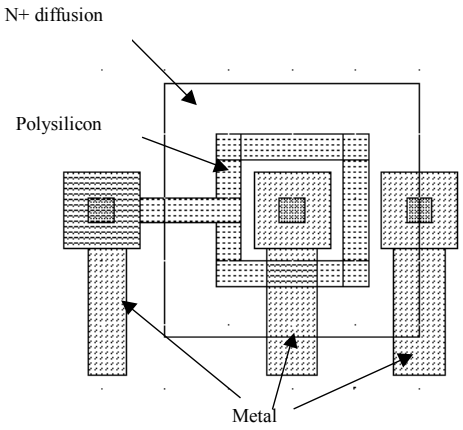
EXERCISES

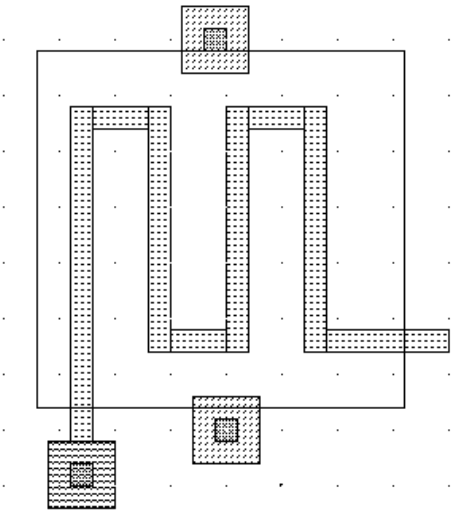
2.1 Layout a single gate n-channel MOS with W=1.0µm, L=0.12µm. What is the maximum current? Build the equivalent MOS device with parallel gates.

2.2 Using the current evaluator in the MOS generator menu in Microwind2, find a simple relationship between the maximum current Imax and the width and length of the device.

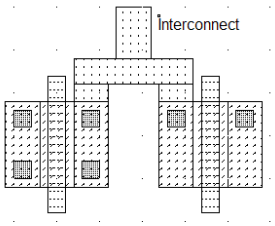
2.3 What is the equivalent width and length of the device drawn in the figure below? What is the possible application of such a design style ?



2.4 What is the width and length of this device? What is the main drawback of this design style?



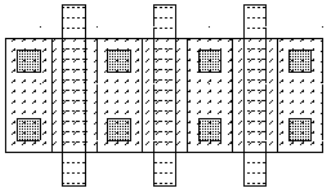
2.5 What is the maximum current which can flow within the interconnect without any damage ?



2.6 Add the appropriate layers to create the biggest MOS you can create with the following structure.

What is the MOS size ?

Find the maximum current which can flow within this MOS without any damage.

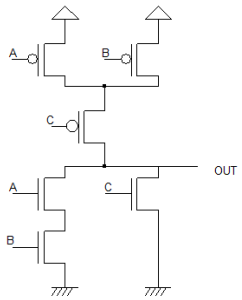


2.7 Consider a sample of silicon (at room temperature) doped pType with a boron density around 10^{16} cm^{-3}.

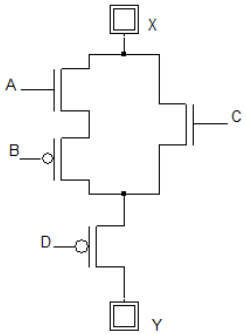
Find The number of minority carrier in this ptype sample.

Anw: Np=2.2 10^{4} cm^{-3}

2.8 For each transistor NMOS and PMOS show the drain and the source.



2.9 Considering each transistor as a perfect switch, find all the combination allowing the connection between X and Y.



Anw: [ABCD]=[1000], [1010], [1110], [0110], [0010]