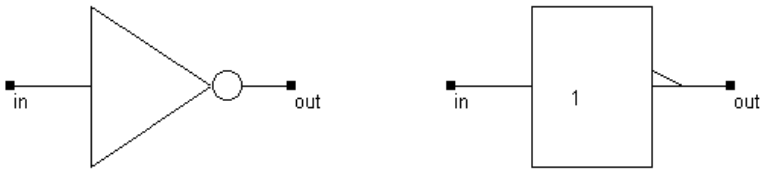
4 The Inverter

The inverter is probably the most important basic logic cell in circuit design. This chapter introduces the logical concepts of the inverter, its layout implementation, the link between the transistor size and the static and analog characteristics. The manual design of the inverter is detailed. The performances of the inverter are analyzed in terms of static transfer function, switching speed, MOS options influence, and power consumption.

1. Logic symbol

Two logic symbols are often used to represent the inverter: the "old style" inverter (Left of figure 4-1), and the IEEE symbol (right of figure 4-1). In DSCH, we preferably use traditional symbol layout. As the logic truth table of figure 4-1 shows, the cell inverts the logic value of the input *In* into an output *Out*.



In	Out
0	1
1	0
X	X

Fig. 4-1: Symbols used to represent the logic inverter

In the truth table, the symbol 0 represents 0.0V while 1 represents the logic supply, which is 1.2V in 0.12µm. The symbol *X* means "undefined". This state is equivalent to an undefined voltage, just like with a floating input node without any input connection. The undefined state appears in gray in the simulations and chronograms.

2. CMOS Inverter

The CMOS inverter design is detailed in the figure 4-2. Here one p-channel MOS and one n-channel MOS transistors are used as switches. Notice that the size of each device is plotted (W accounts for the width, L for the length). The channel width for pMOS devices is set to twice the channel width for nMOS devices. The reason is described in details in the next chapters.

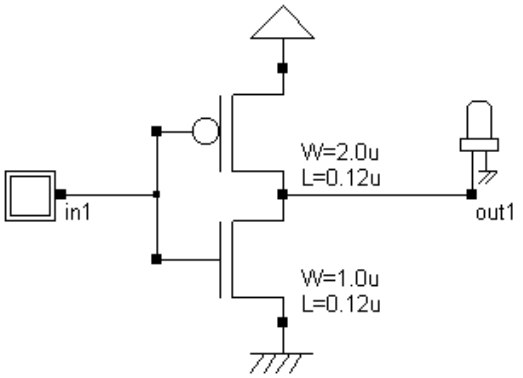


Fig. 4-2: The CMOS inverter is based on one n-channel and one p-channel MOS device

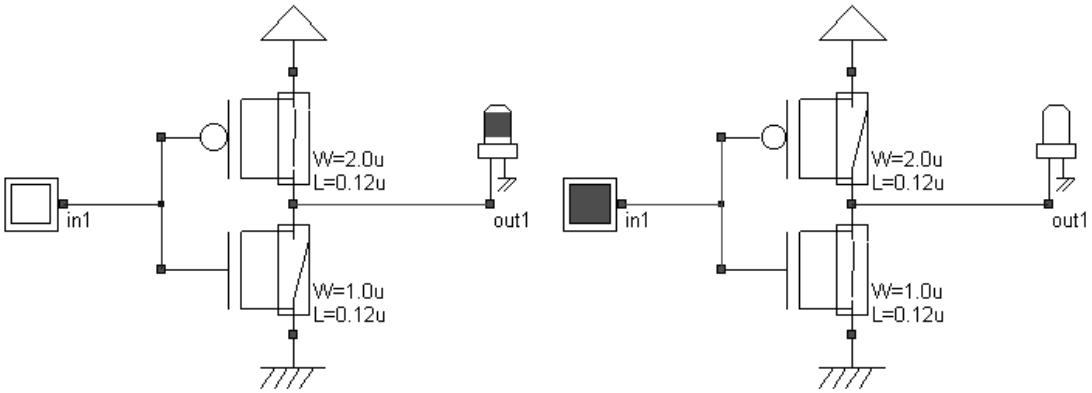


Fig. 4-3: Logic simulation of the CMOS inverter (CmosInv.sch)

When the input signal is logic 0 (Fig. 4-3 left), the nMOS is switched off while the PMOS passes VDD through the output, which turns to 1. When the input signal is logic 1 (Fig. 4-3 b), the pMOS is switched off while the nMOS passes VSS to the output which goes back to 0. In that simulation, the MOS is considered as a simple switch. The n-channel MOS symbol is a device that allows the current to flow between the source and the drain when the gate voltage is "1".

To simulate the inverter at logic level, start the software DSCH2, load the file “CmosInv.SCH”, and launch the simulation by the command **Simulate →Start Simulate**. Click inside the button *in1*. The result is displayed on the output *out1*. The red value indicates logic 1, the black value means a logic 0.

Click the button **Stop simulation** of the simulation menu to return to the schematic editor. Click the **chronogram** icon to get access to the chronograms of the previous simulation (Figure 4-4). As seen in the waveform, the value of the output is the logic opposite of that of the input.

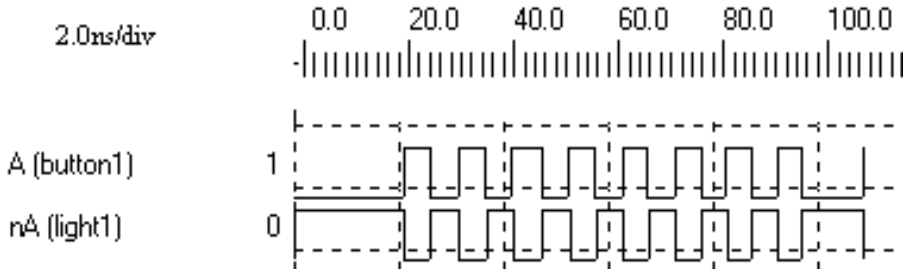


Fig. 4-4 Chronograms of the inverter simulation (CmosInv.SCH)

3. Inverter Layout

In this paragraph, details on the layout of a CMOS inverter are provided. The simplest way to create a CMOS inverter is to generate both n-channel MOS an p-channel MOS devices using the cell generator provided by Microwind. The advantage of this approach is to avoid any design rule error. The corresponding menu is reported below. You can generate an n-channel or p-channel device. A double gate device may also be created for EEPROM memory devices (See chapter 10). By default the proposed length is the minimum length available in the technology (2 lambda), and the width is 10 lambda. In 0.12µm technology, where lambda is 0.06µm, the corresponding size is 0.12µm for the length and 0.6µm for the width.

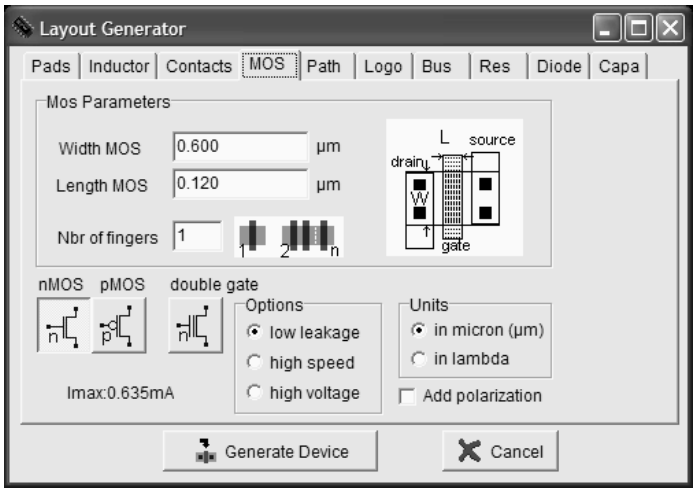


Fig. 4-5 Using the MOS generator to add n-channel and p-channel MOS devices on the layout

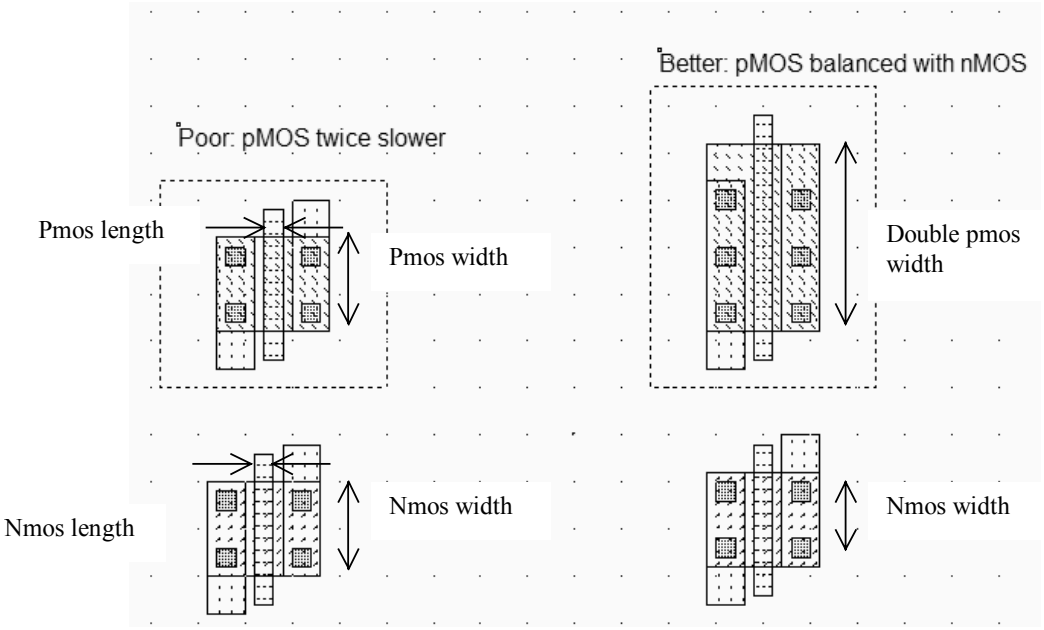


Fig. 4-6 The layout of one nMOS and one pMOS to build the CMOS inverter (invSizing.MSK)

The design starts with the implementation of one nMOS and one pMOS, as shown in figure 4-6. Using the same default channel width (0.6µm in CMOS 0.12µm) for nMOS and pMOS is not the best idea, as the p-channel MOS switches half the current of the n-channel MOS. The origin of this mismatch can be seen in the general expression of the current delivered by n-channel MOS devices (equation 4-1) and p-channel MOS devices (equation 4-2).

$$Ids(Nmos) \approx \varepsilon_0 \varepsilon_r \frac{\mu_n}{TOX} \frac{W_{Nmos}}{L_{Nmos}} f(Vd,Vg,Vs,Vb) \qquad \text{(Equ. 4-1)}$$

$$Ids(Pmos) \approx \varepsilon_0 \varepsilon_r \frac{\mu_p}{TOX} \frac{W_{Pmos}}{L_{Pmos}} f(Vd,Vg,Vs,Vb) \qquad \text{(Equ. 4-2)}$$

If Wnmos=Wpmos and Lnmos=Lpmos, Ids(Nmos) is proportional to µn while Ids(Pmos) is proportional to µp. Typical mobility values are:

$\mu_n = 0.068 m^2 / v.s$ for electrons

$\mu_p = 0.025 m^2 / v.s$ for holes

Consequently, the current delivered by the n-channel MOS device is more than twice that of the p-channel MOS. Usually, the inverter is designed with balanced currents to avoid significant switching discrepancies. In other words, switching from 0 to 1 should take approximately the same time as switching from 1 to 0. Therefore, balanced current performances are required.

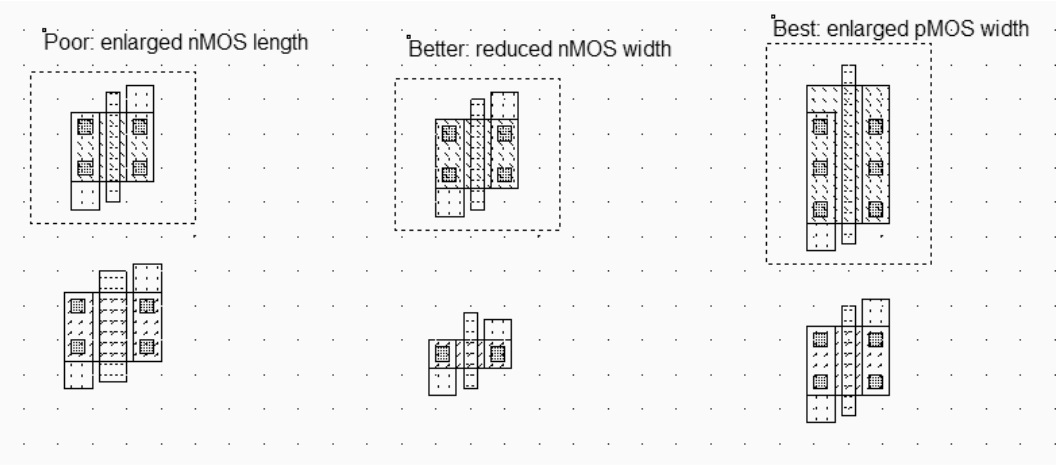


Fig. 4-7 Three techniques to compensate the poor hole mobility (invSizing.MSK)

There are several techniques to counterbalance the intrinsic mobility difference: increase the nMOS channel length (left of figure 4-7), decrease the nMOS channel width (middle), or increase the pMOS channel width. The main drawback of the design of figure 4-7(left) is the spared silicon area. The design in the middle is equivalent, but consumes less silicon space. However, reducing the nMOS width slows down the switching. The best approach (right) consists in enlarging the pMOS width. Its *Ion* current is doubled, and becomes comparable to the nMOS current. The behavior will be balanced in terms of switching speed.

Connection between Devices

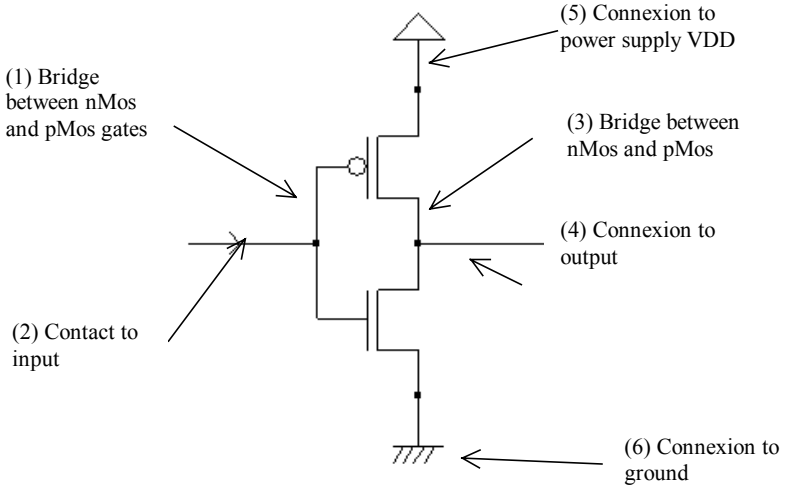


Fig. 4-8 Connections required to build the inverter (CmosInv.SCH)

Within CMOS cells, metal and polysilicon are used as interconnects for signals. Metal is a much better conductor than polysilicon. Consequently, polysilicon is only used to interconnect gates, such as the bridge (1) between pMOS and nMOS gates, as described in the schematic diagram of figure 4-8. Polysilicon is rarely used for long interconnects, except if a huge resistance value is expected.

In the layout shown in figure 4-9, the polysilicon bridge links the gate of the n-channel MOS with the gate of the p-channel MOS device. The polysilicon serves as the gate control and the bridge between MOS gates.

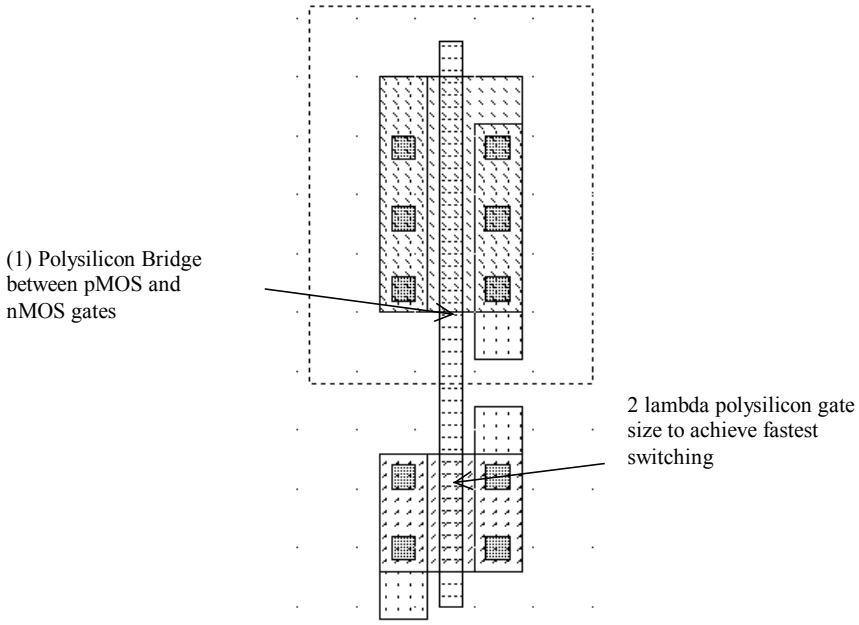


Fig. 4-9 Polysilicon bridge between nMOS and pMOS devices (InvSteps.MSK)

Useful Editing Tools

The following commands may help you in the layout design and verification processes.

Command	Icon/Short cut	Menu	Description
UNDO	CTRL+U	Edit menu	Cancels the last editing operation
DELETE	 CTRL+X	Edit menu	Erases some layout included in the given area or pointed by the mouse.
STRETCH		Edit menu	Changes the size of one box, or moves the layout included in the given area.
COPY	 CTRL+C	Edit Menu	Copies the layout included in the given area.
VIEW ELECTRICAL NODE	 CTRL+N	View Menu	Verifies the electrical net connections.
2D CROSS-SECTION		Simulate Menu	Shows the aspect of the circuit in vertical cross-section.

Table 4-1: A set of useful editing tools

Metal-to-poly

As polysilicon is a poor conductor, metal is preferred to interconnect signals and supplies. Consequently, the input connection of the inverter is made with metal. Metal and polysilicon are separated by an oxide which prevents electrical connections. Therefore, a box of metal drawn across a box of polysilicon does not allow an electrical connection (Figure 4-10). To build an electrical connection, a physical contact is needed. The corresponding layer is called "contact". You may insert a metal-to-polysilicon contact in the layout using a direct macro situated in the palette.

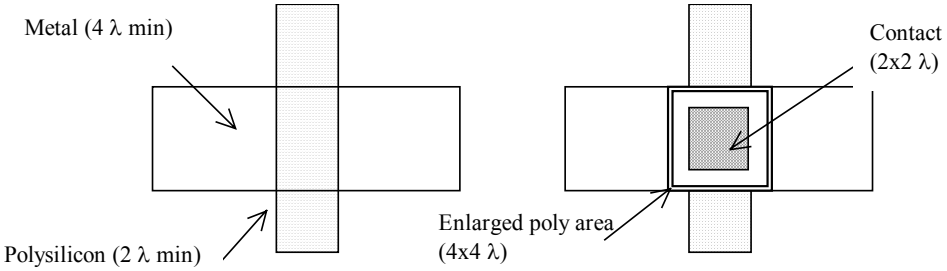


Fig. 4-10 Physical contact between metal and polysilicon

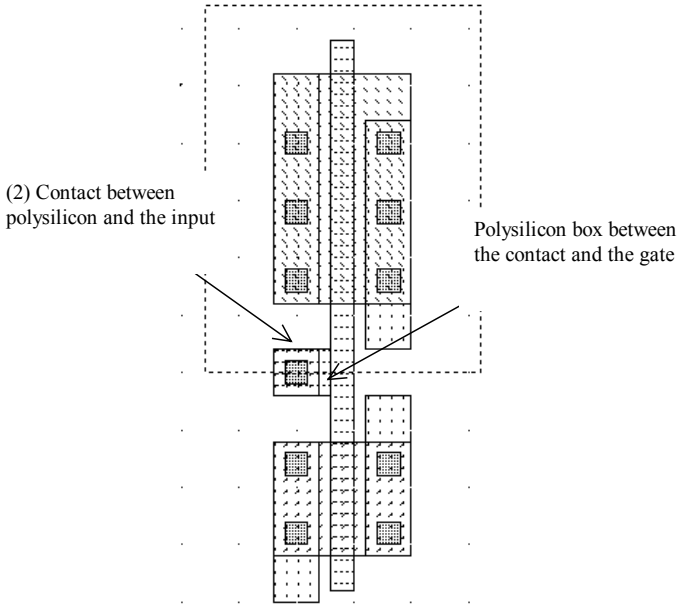


Fig. 4-11 Physical contact between metal and polysilicon (InvSteps.MSK)

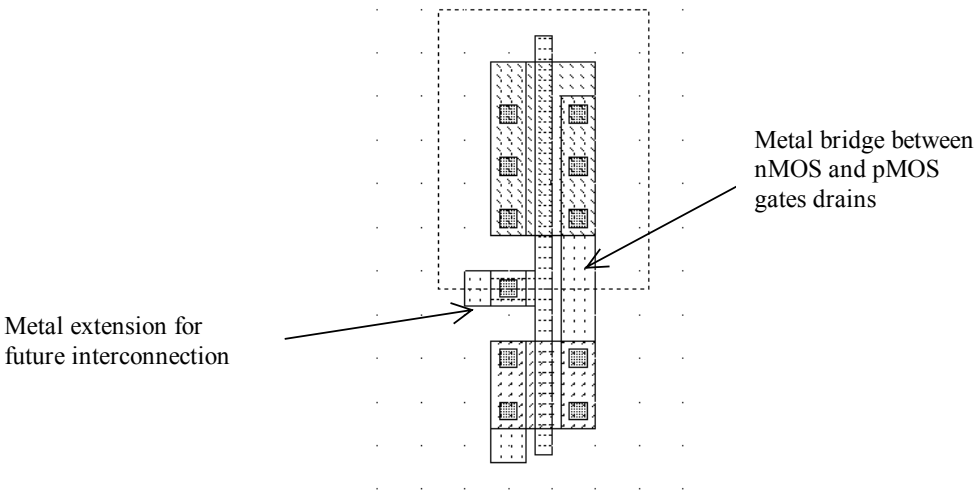


Fig. 4-12 Adding a poly contact, poly and metal bridges to construct the CMOS inverter (InvSteps.MSK)

The *Process Simulator* shows the vertical aspect of the layout, as when fabrication has been completed. This feature is a significant aid to understand the circuit structure and the way layers are stacked on top of each other. A click of the mouse on the left side of the n-channel device layout and the release of the mouse at the right side give the cross-section reported in figure 4-13.

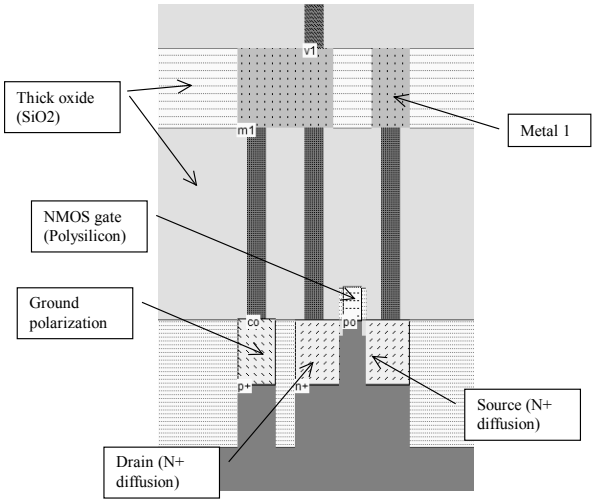


Fig.4-13 The 2D process section of the inverter circuit near the nMOS device (InvSteps.MSK)

Supply Connections

The next design step consists in adding supply connections, that is the positive supply VDD and the ground supply VSS. In figure 4-14, we use the metal2 layer (Second level of metallization) to create horizontal supply connections. Notice that the metal connections have a large width. This is because a strong current may flow within these supply

interconnects. Enlarging the supply metal lines reduces the resistance and avoids electrical overstress called electromigration (More details are given in chapter 5 dedicated to interconnects).

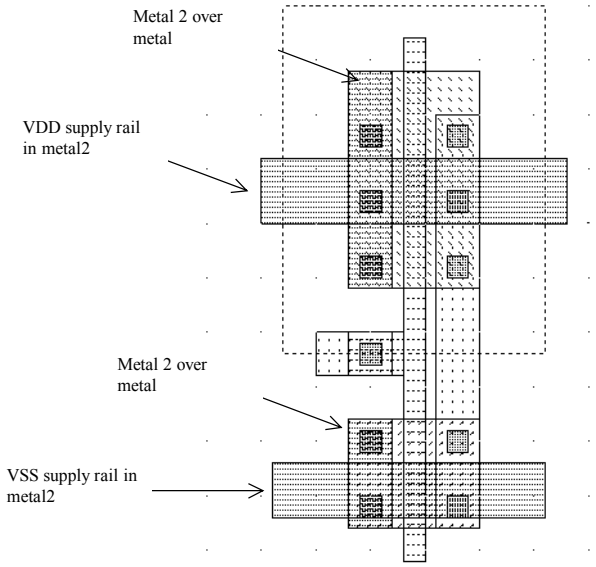


Fig.4-14 Adding metal2 supply lines and the appropriate vias (InvSteps.MSK)

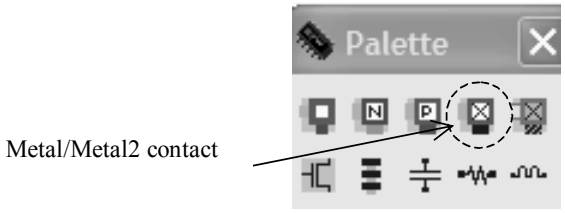


Fig.4-15 The metal/Metal2 contact in the palette

The metal layers are electrically isolated by a SiO2 dielectric. Consequently, the metal2 supply line floats over the inverter cell and no physical connection exists down to the MOS source region. The simplest way to build the physical connection is to add a metal/Metal2 contact that may be found in the palette (Figure 4-15).

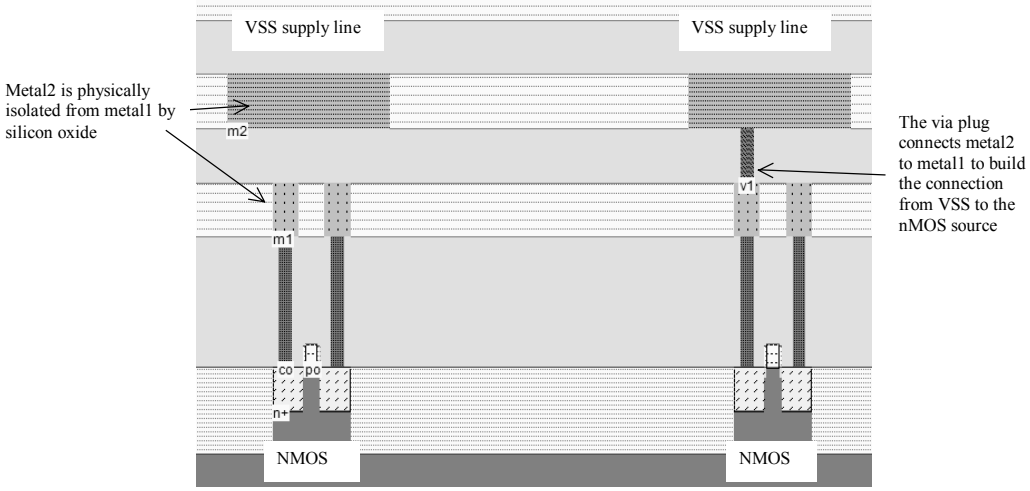


Fig.4-16 2-D view of the connection built near the nMOS region to connect the source to the VSS supply line

As seen in figure 4-16, the connection is created by a plug called "via" between metal2 and metal layers.
The final layout design step consists in adding polarization contacts. These contacts convey the VSS and VDD voltage supply close to the bulk regions of the device. We have seen that the MOS behavior is influenced by the bulk polarization. For example, *Ion* is directly dependent on V_{BS}, which represents the voltage difference between the bulk and the source (See for example equation 3-31). See also the characteristics *Ids* versus *Vgs* for varying bulk voltage like in figure 3-26. If we ensure a clean supply polarization near each device (VSS for nMOS, VDD for pMOS), we avoid such variations. Remember that the n-well region should always be polarized to a high voltage to avoid short-circuit between VDD and VSS.

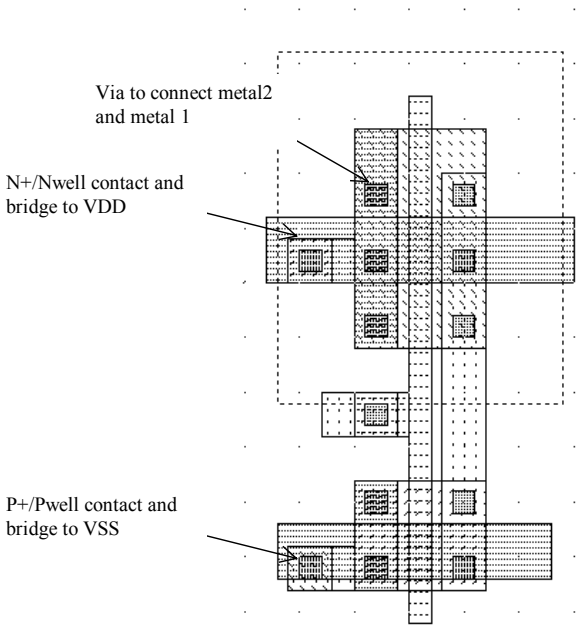


Fig.4-17 Adding polarization contacts

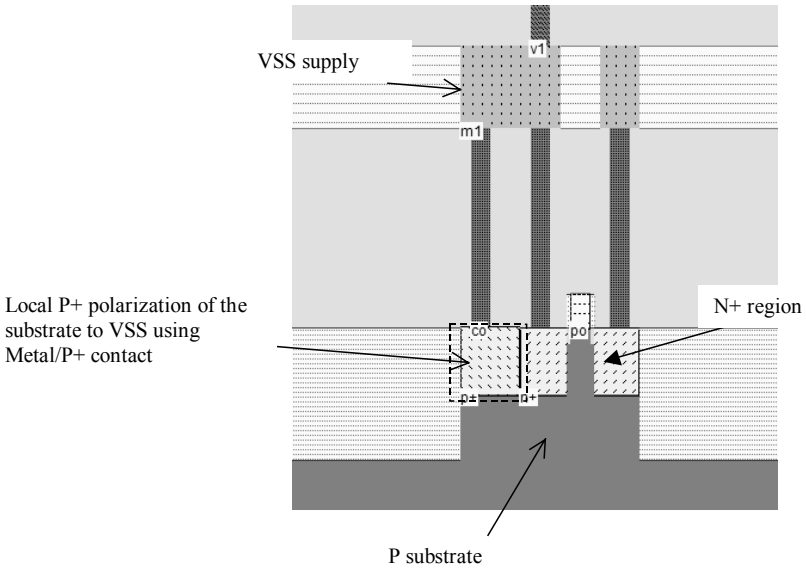


Fig.4-18 2-D view of the VSS polarization built near the nMOS source

More details about the vertical aspect of the VSS polarization is given in figure 4-18. When adding the metal/P+ contact, we create a VSS supply path to the P substrate. Consequently, the surrounding of the n-MOS device is firmly tied to VSS supply voltage. We also illustrate the VDD polarization near the pMOS channel in figure 4-19. The n-well region cannot be left without polarization.

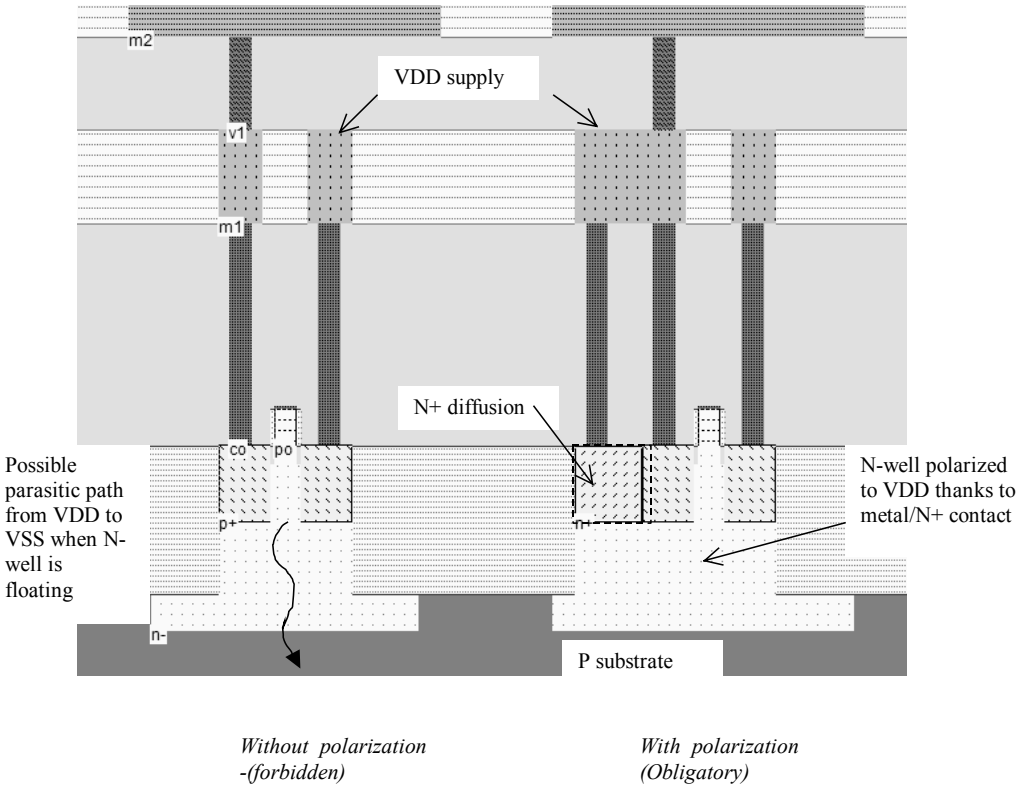


Fig.4-19 2-D view of the VDD polarization built near the pMOS source

Adding the VDD polarization in the n-well region is a very strict rule. The local polarization built with a metal/N+ diffusion contact, as shown in figure 4-19, is efficient to avoid a floating n-well region, which may result in parasitic current path from the PMOS source down to the P substrate usually tied to VSS. The current path may be strong enough to damage the chip. This effect is called latchup <Gloss>.

Process steps to build the Inverter

At that point, it might be interesting to illustrate the steps of fabrication as they would sequence in a foundry. Microwind includes a 3D process viewer for that purpose. Click **Simulate→ Process steps in 3D**. The simulation of the CMOS fabrication process is performed, step by step by a click on **Next Step**. On figure 4-20, the picture on the left represents the nMOS device, pMOS device, common polysilicon gate and contacts. The picture on the right represents the same portion of layout with the metal layers stacked on top of the active devices.

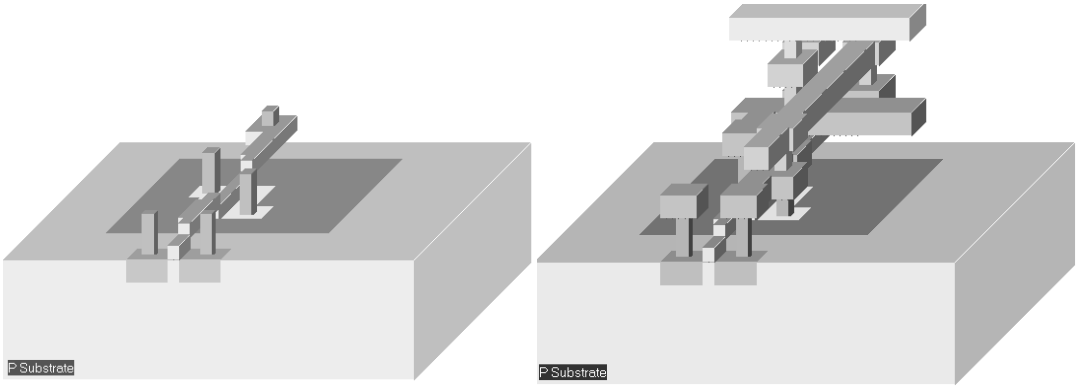


Fig.4-20 The step-by-step fabrication of the Inverter circuit (InvSteps.MSK)

4. Inverter Simulation

The inverter simulation is conducted as follows. Firstly, a VDD supply source (1.2V) is fixed to the upper metal2 supply line, and a VSS supply source (0.0V) is fixed to the lower metal2 supply line. The properties are located in the palette menu. Simply click the desired property , and click on the desired location in the layout. Add a clock on the inverter input node (The default node name *clock1* has been changed into *Vin*)and a visible property on the output node (The default name *out1* has been changed into *Vout*).

The expected behavior is shown in figure 4-22. The basic phenomenon is the charge and discharge of the output parasitic capacitor *Cout*, which is the sum of junction and wire capacitance. When *In1* is equal to 0, the pMOS device is on, and the capacitor *Cout* is charged until its voltage rises to VDD. When *In1* is equal to 1, the nMOS device is on, and the capacitor *Cout* is discharged until its voltage reaches VSS.

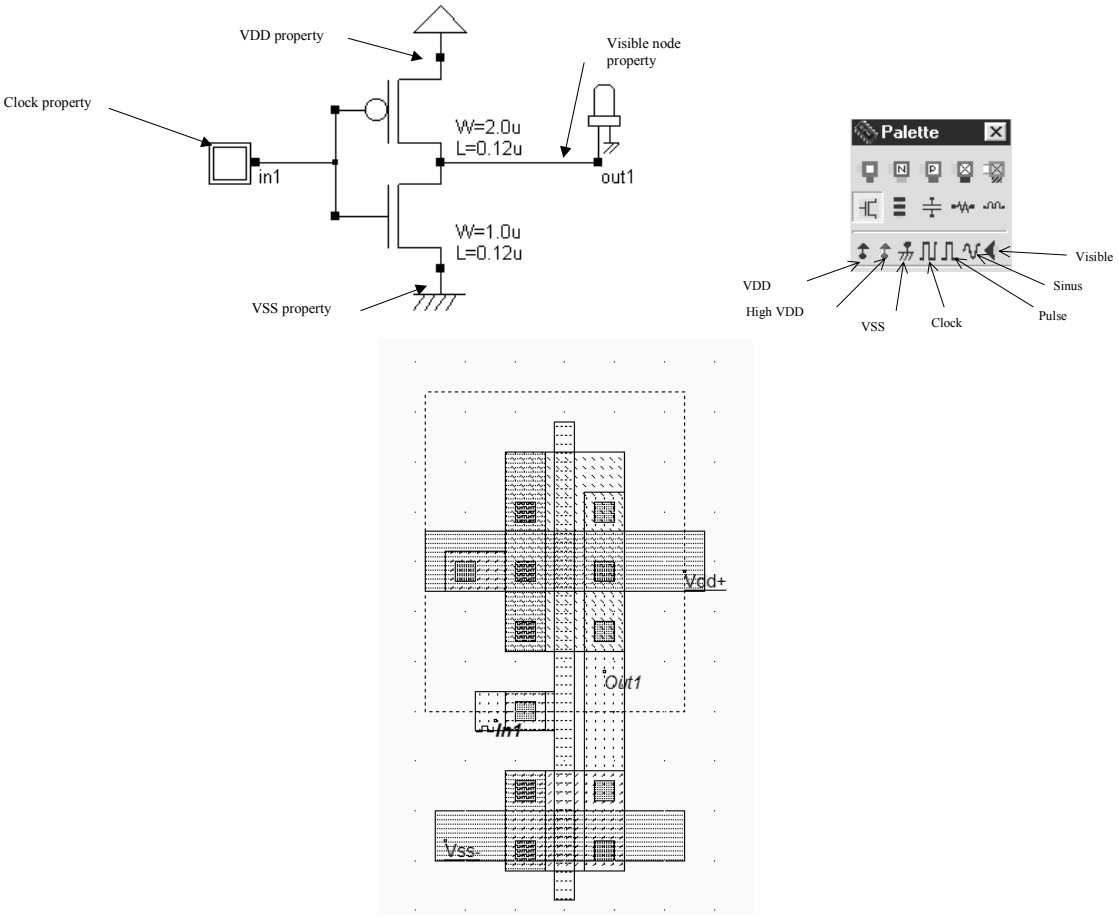


Fig.4-21 Adding simulation properties (InvSteps.MSK)

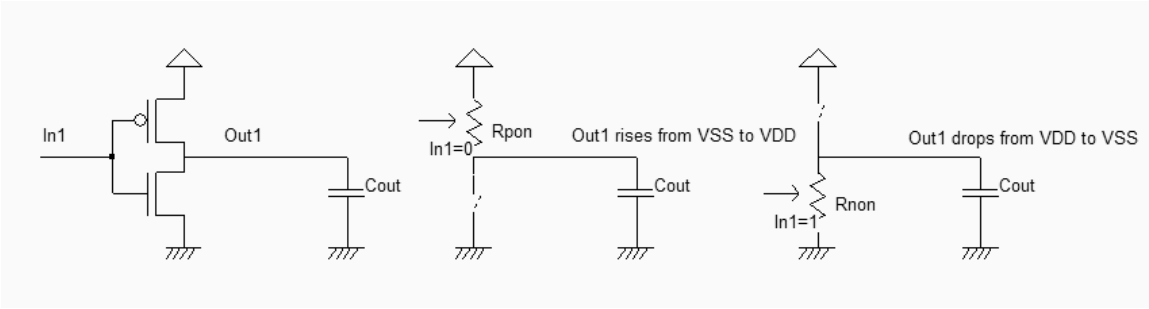


Fig.4-22 Expected behavior of the CMOS inverte (InverterLoad.SCH)

Starting Simulation

The command **Simulate → Run Simulation** gives access to four simulation modes: **Voltage vs. time**, **Voltage and current vs. Time**, **Voltage vs. voltage** and **Frequency vs. time**. All these simulation modes are applicable to the inverter simulation.

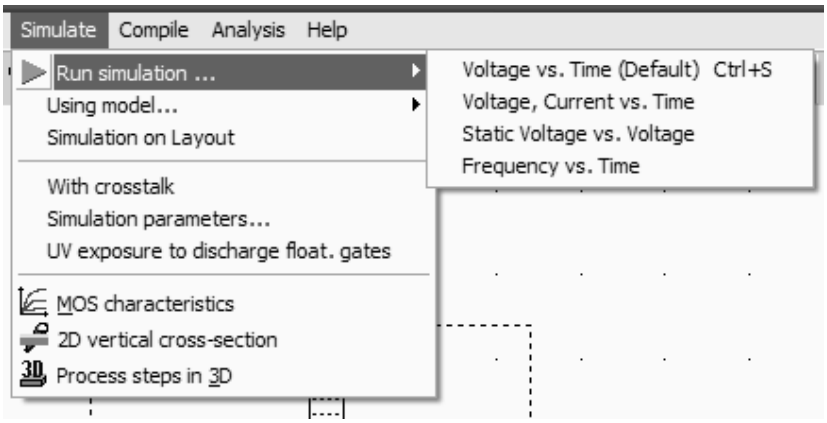


Fig.4-23 The four simulation modes in Microwind

Due to the fact that the layout **InvSteps.MSK** not only includes the inverter correctly polarized, but also several other mos devices without any simulation properties, a warning window appears prior to the analog simulation, as shown in figure 4-24. In this case, you may click **Simulate as it**. In normal cases, all n-well regions should be stuck at VDD.

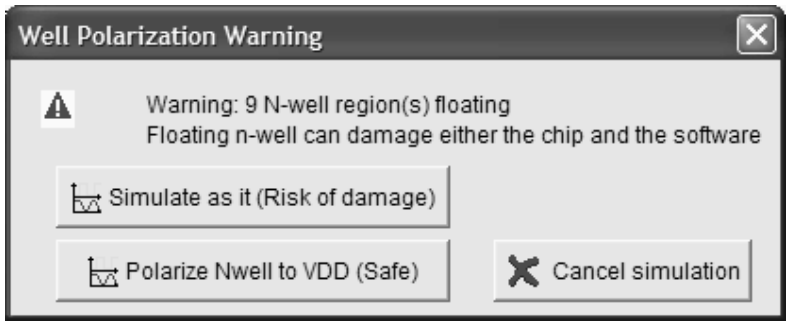


Fig.4-24 Missing polarization in n-well regions provoke a warning prior to simulation (InvSteps.MSK)

Voltage vs. Time

Select the simulation mode **Voltage vs. Time**. The analog simulation of the circuit is performed. The time domain waveform, proposed by default, details the evolution of the voltages *in1* and *out1* versus time. This mode is also called transient simulation, as shown in figure 4-25.

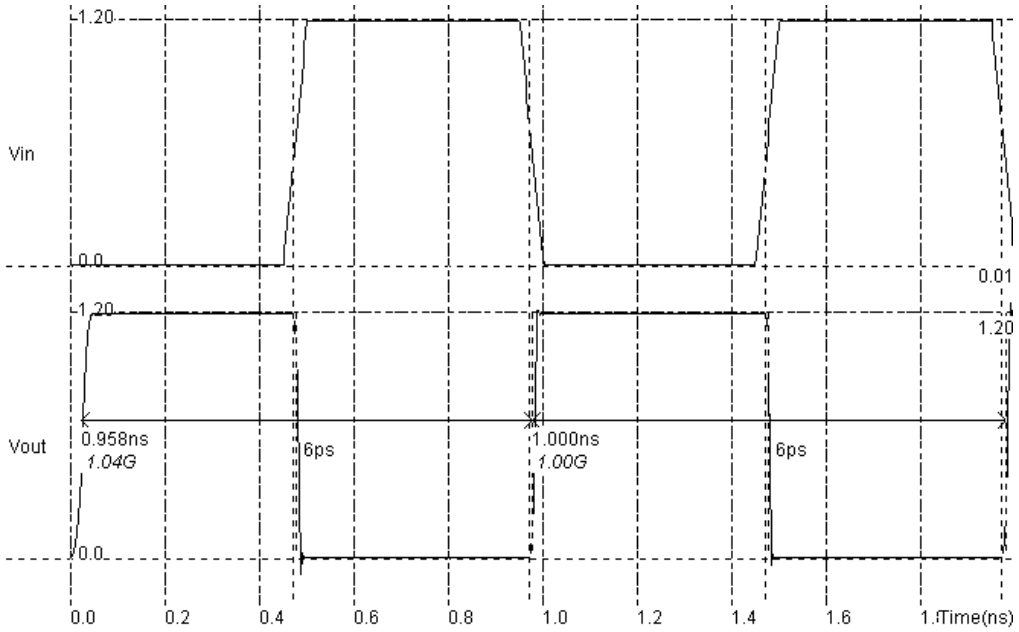


Fig.4-25 Transient simulation of the CMOS inverter (InvSteps.MSK)

The truth-table is verified as follows. A logic zero corresponds to a zero voltage and a logic 1 to a 1.20V. When the input rises to 1, the output falls to 0, with a 6 Pico-second delay (6.10^{-12} second).

In	Out
0	1
1	0

Logic table

In (V)	Out (V)
0.0	1.2
1.2	0.0

Analog voltage table

Current vs. Time

The inverter consumes power during transitions, due to two separate effects. The first is short circuit power arising from momentary short-circuit current that flows from *VDD* to *VSS* when the transistor functions in the incomplete-on/off state (Figure 4-26). The second is the charging/discharging power, which depends on the output wire capacitance. With small loading, the short circuit power loss is dominant. With a huge loading, that is a large output node capacitance, the loading power is dominant.

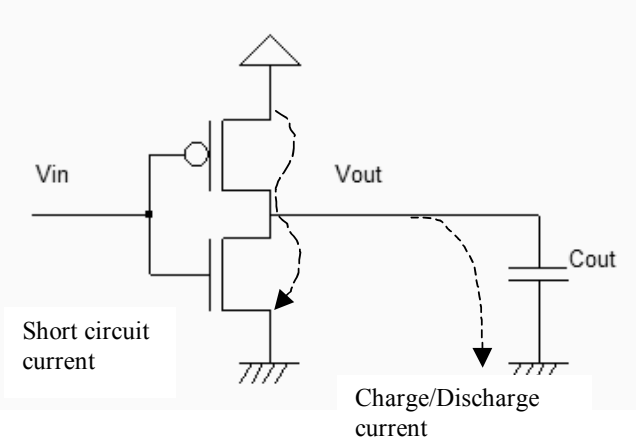


Fig. 4-26: Short circuit current in CMOS inverters (InverterLoad.SCH)

The power consumption occurs briefly during transitions of the output, either from 0 to 1 or from 1 to 0 (Fig. 4-27). The simulation contains the supply currents in the upper window, and all voltage waveforms in the lower window. The current consumption is important only during a very short period corresponding to the charge or discharge of the output node. Without any switching activity, the current is almost equal to zero.

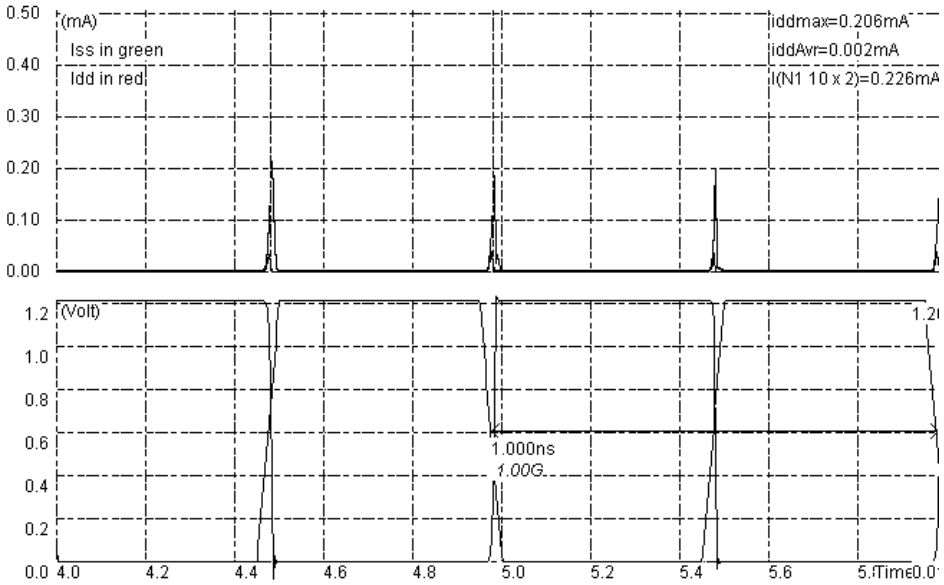


Fig. 4-27: Simulation of the current peaks appearing between VDD and VSS in the CMOS inverter at each output transition (InvSteps.MSK)

Inverter Delay

As the number of gates connected to the inverter output node increase, the load capacitance increases. The fanout <glossary> corresponds to the number of gates connected to the cell output. Physically, a large fanout means a large number of connections (Figure 4-28), that is a large load capacitance.

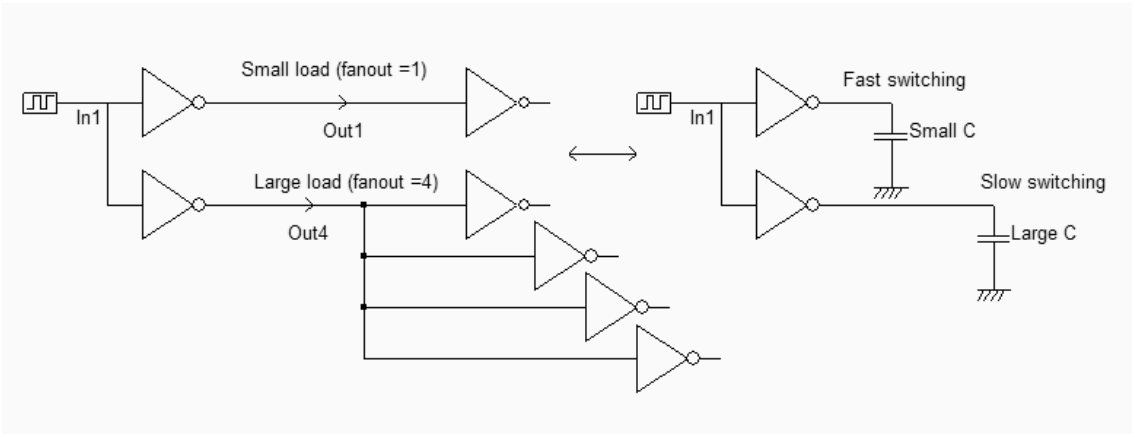


Fig. 4-28 One inverter connected either to a single inverter or to 4 inverters in parallel (InverterLoad.SCH)

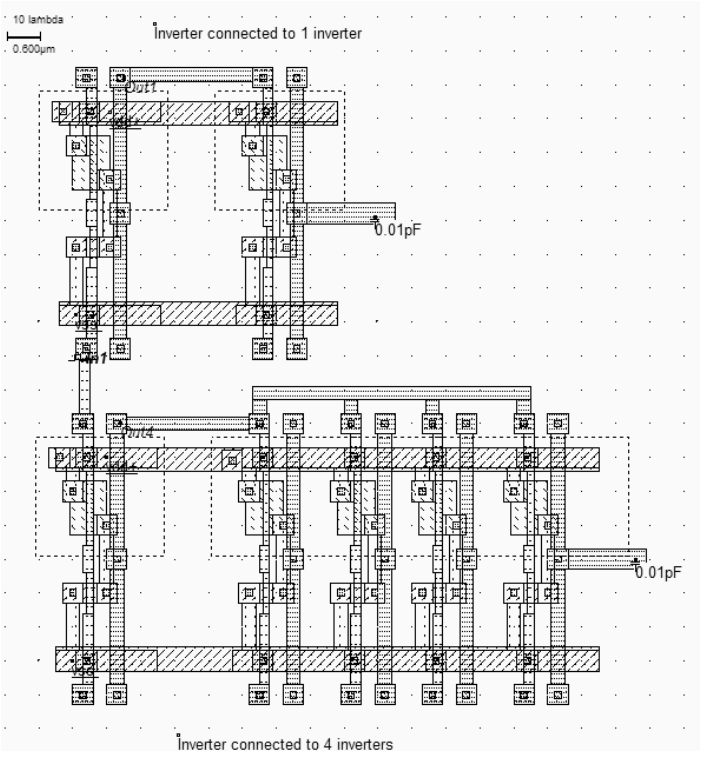


Fig. 4-29 One inverter connected either to a single inverter or to 4 inverters in parallel (InvFanout.MSK)

An inverter circuit is simulated using different clock, fanout and supply conditions. The initial configuration is based on one inverter controlled by a 2GHz clock, with its output connected either to a single inverter or to four inverters (Fig. 4-30). The supply voltage is 1.2V, with a 0.12µm CMOS technology.

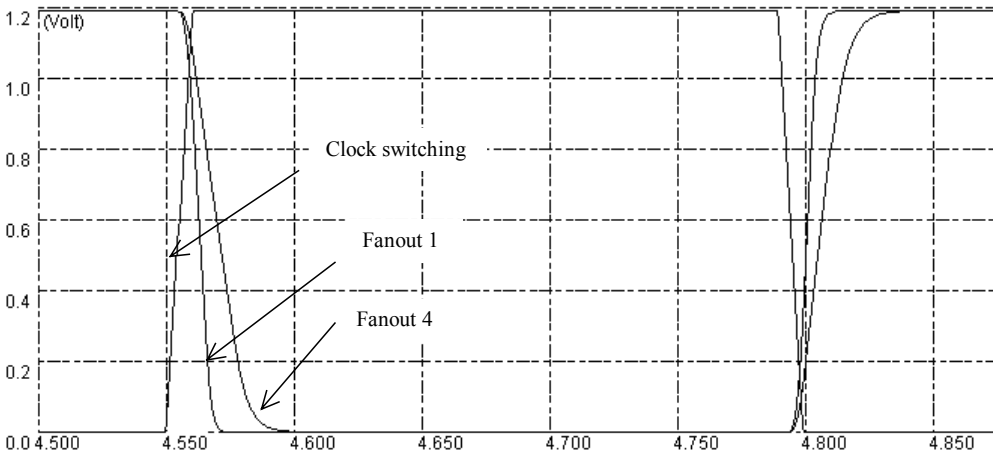


Fig. 4-30: Influence of the output capacitance on the current and switching response (InvFanout.MSK)

Now, we connect 4 inverter circuits to the output node, thus increasing the charge capacitance. In the simulation chronograms reported in figure 4-30, the inverter delay is significantly increased. When we investigate the delay variation with the output capacitance load, we observe the curve reported in figure 4-31. It can be seen that the gate delay variation with the loading capacitance is quite linear. A 100fF load leads to around 300ps delay in CMOS 0.12µm technology.

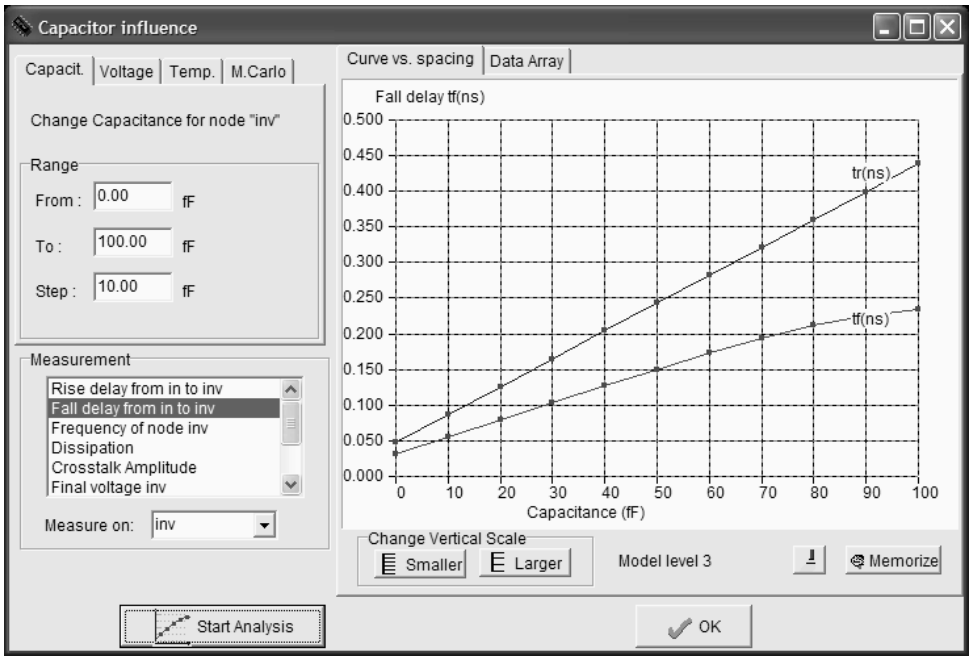


Fig. 4-31: Inverter delay increases with the output capacitance (InvCapa.MSK)

In Microwind2, we may obtain directly this type of screen thanks to the command **Parametric Analysis**. Load the file InvCapa.MSK, invoke the command **Parametric Analysis,** click in the output node, and click **Start Analysis**. By default, the capacitance of the output node is increased step by step from its default value C_{def} to C_{def}+100fF. For each value of the output capacitance, the analog simulation is performed, and the last computed rise time is plotted, appearing as one single red dot in the graphs. The complete graph is built once all analog simulations have been

completed. The memory button enables to store one curve (evaluation of the rise time for example) prior to a new parametric simulation, for comparison purposes. Three main parameters may vary in the parametric analysis: the capacitance as in figure 4-31, voltage, or temperature. Several analog parameters may be monitored: rise and fall delay, oscillating frequency, power consumption, final voltage of a node, crosstalk, etc..

5. Power Consumption

The power consumption P is computed by Microwind as the average product of the supply voltage VDD and the supply current IDD, computed at each iteration step. In other words:

$$P = \frac{\sum I_{DD}.V_{DD}}{steps} \qquad \text{(Equ. 4-3)}$$

Three main factors contribute to the power consumption P: the load capacitance *C*, the supply voltage *VDD* and the clock frequency *f*. For a CMOS inverter, this relation is usually represented by the first-order approximation below. The equation 4-4 shows a linear dependence of the power consumption P with the total capacitance C and the operating frequency *f*. The power consumption is also proportional to the square of the supply voltage *VDD*.

$$P = \frac{1}{2}\ \eta.C\ V_{DD}{}^{2} f \qquad \text{(Equ. 4-4)}$$

Where:

k: technological factor (close to 1)

C: Output load capacitance (Farad)

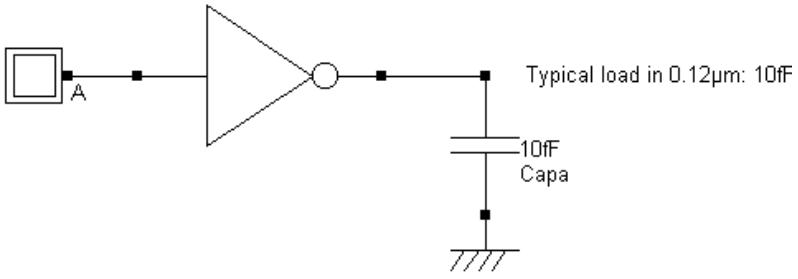
VDD: supply voltage (V)

f: Clock frequency (Hz)

η: switching activity factor (Between 0 and 1)

Frequency dependence

We can verify the linear dependence of the power consumption with the operating frequency by simulating a CMOS inverter circuit. At each time-domain analog simulation, we get a value of the power consumption, which is computed by Microwind as the average product of the supply voltage VDD and the supply current IDD (Equation 4-3).



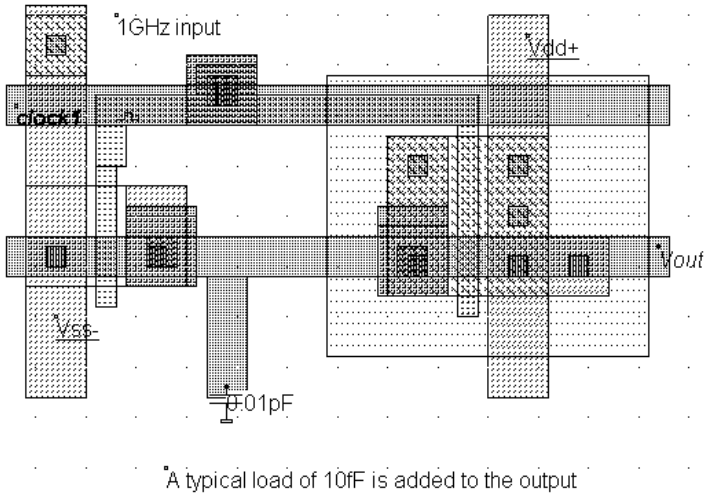


Fig. 4-32: CMOS inverter setup used to simulate the effect of the clock frequency on the power consumption. A 10fF load is added to the output to represent a typical loading condition in 0.12µm (CmosLoad.MSK)

In the case of figure 4-32, a 1GHz switching of the inverter induces a circuit power dissipation of 15.7µW. When we change the frequency, we observe a linear increase of P with the clock frequency, as forecast in equation 4-4 (Figure 4-33).

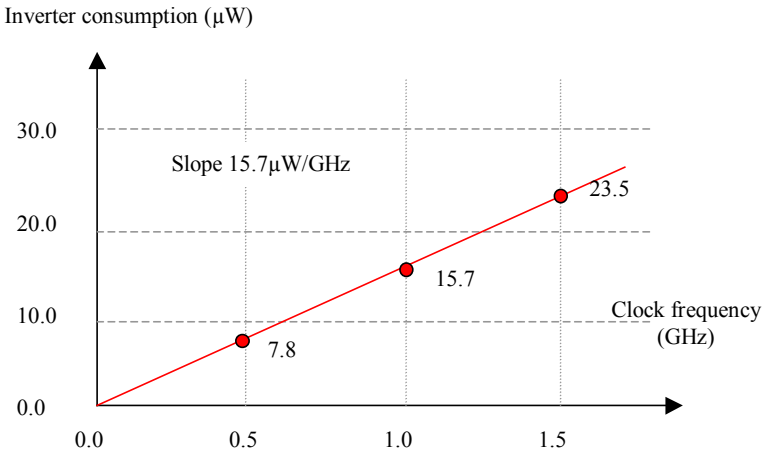


Fig. 4-33: Power consumption increase with the clock frequency, for an inverter with a 10fF load, in 0.12µm CMOS technology (CmosLoad.MSK)

As the power consumption is linearly proportional to the clock frequency, a usual metric found in most cell libraries is the µW/GHz. In the case of the simple inverter and its 10fF load, we get 15.7µW/GHz.

Supply Voltage dependence

It can be considered, as a first-order approximation that the average power consumption is proportional to VDD^2 (Equation 4-4). We use the parametric analysis tool in Microwind to control the incremental change of the supply voltage, from 0.5 to 2.0V. The supply voltage step is 0.1V. In the measurement window, the item "Dissipation " is selected. The result plotted in the figure 4-44 shows a non-linear dependence of the power dissipation with VDD. The square law fits with the experimental data from 0.8 to 1.5V. We notice a very important rise of the power consumption over 1.5V, due to the avalanche effects in n-channel MOS devices. This simulation demonstrates the interest for a minimum supply operation to achieve optimum low-power operation.

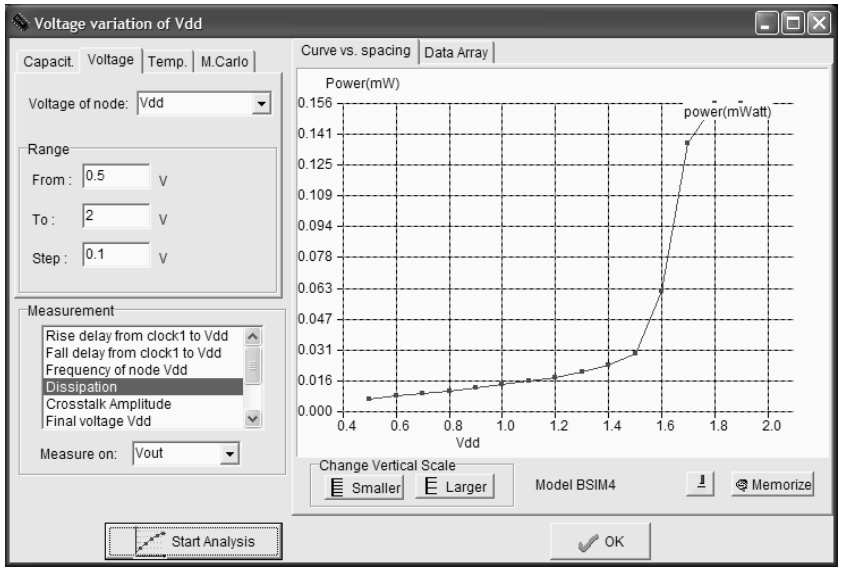


Fig. 4-44: Analysis of the power consumption increase with the supply voltage VDD (CmosLoad.MSK)

Minimum Supply Voltage

The question is: what is the supply voltage below which the inverter does not work anymore? The answer can be given by the parametric analysis, focusing this time on the inverter delay dependence versus the supply voltage. Load the file **CmosLoad.MSK** for this study. Invoke the command **Parametric Analysis** of the Analysis menu. Click the layout region corresponding to the node VDD. Verify that the Voltage menu is selected in the parametric analysis window. Verify that the node "VDD" is selected. Modify the VDD voltage range from 0.5 to 1.5V, step 0.1V. Finally, in the measurement menu, select the item **Rise delay** and click **Start Analysis**.

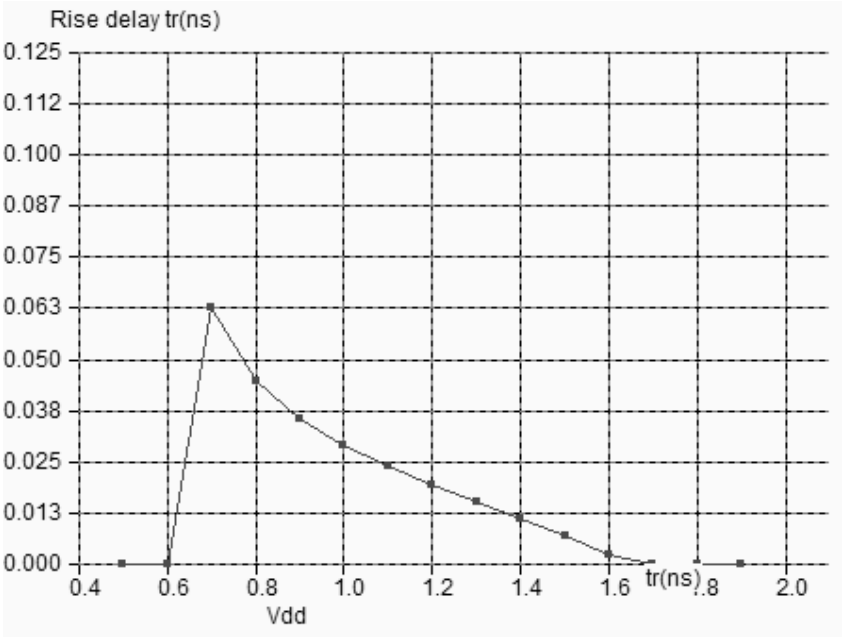


Fig. 4-45: Switching delay dependence with the supply voltage VDD (CmosLoad.MSK)

We observe that the delay is significantly increased as we decrease VDD from its nominal value 1.2V down to 0.6V. Below 0.7V, the inverter delay is higher than the default transient simulation time (10ns) so that the delay evaluator does not work anymore.

6. Static Characteristics

The static characteristics of the inverter correspond to the variation plot of the output voltage versus the input voltage. The simulation involves a step by step increase of *Vin*, and the monitoring of *Vout*. In the simulation window, the static characteristics are obtained by a click on the item **Voltage vs. Voltage** situated in the selection menu, at the bottom of the chronograms. The curve shown in figure 4-46 appears.

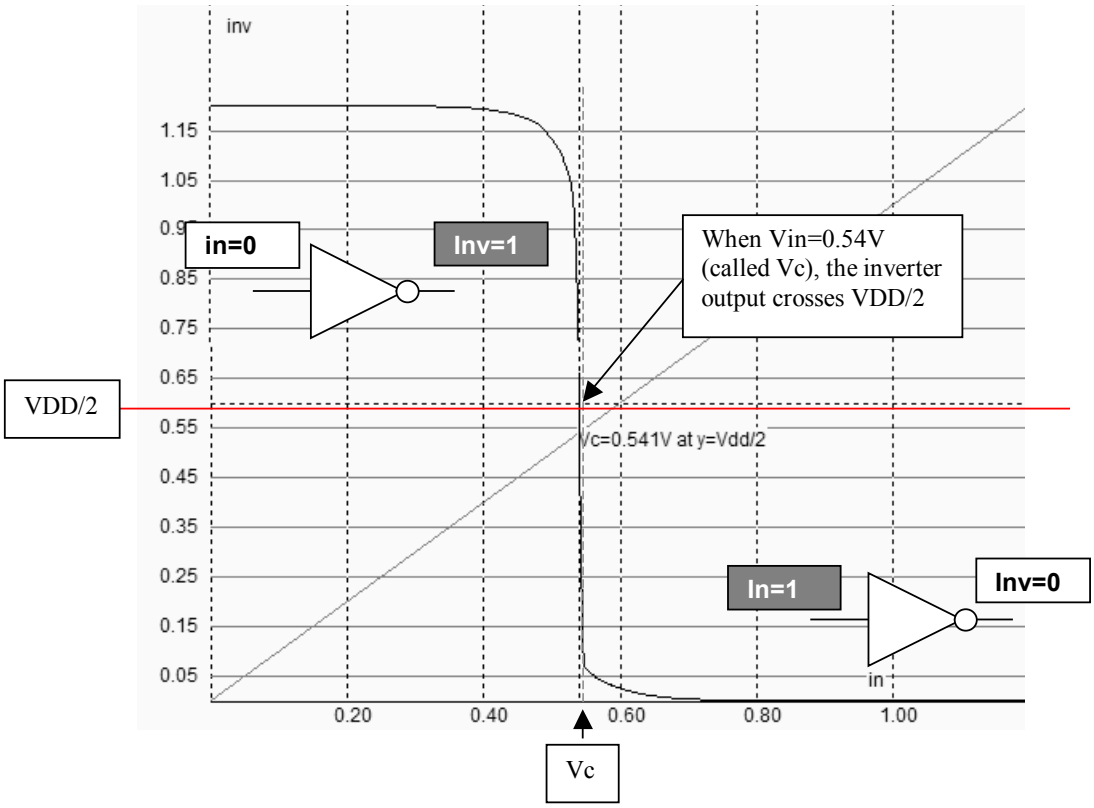


Fig. 4-46: The static characteristics of the inverter (Inv.MSK)

When *Vin* is low, *Vout* is high, which corresponds to one logic state of the inverter. When *Vin* increases, *Vout* starts to decrease slowly, and suddenly crosses the VDD/2 boundary. At that point, the value of *Vin* is the commutation point <Glossary> of the inverter, called *Vc*. Then, when *Vin* rises to VDD, *Vout* reaches 0, which corresponds to the other logic state of the inverter.

Modify the commutation point

Several theoretical formulations of the commutation voltage versus layout parameters exist. A simple formula derived from MOS model 1 is reported in equation 4-5 [Baker]. Although based on an obsolete model, this formulation may be applied for first order hand calculations. The verification must be performed by simulation.

$$Vc = \frac{K.V_{TN} + V_{DD} - V_{TP}}{1+K} \qquad \text{(Equ. 4-5)}$$

with

$$K = \sqrt{\frac{\mu_n \frac{Wn}{Ln}}{\mu_p \frac{Wp}{Lp}}}$$

µn= mobility of electrons (600 $V.cm^{-2}$)

µp= mobility of holes (270 $V.cm^{-2}$)

Wn = n-channel MOS width (in µm)

Ln = n-channel MOS length (in µm)

Wp = p-channel MOS width (in µm)

Lp = p-channel MOS length (in µm)

V_{DD} = supply voltage (1.2V)

V_{TN} = threshold voltage of n-channel device (0.30V)

V_{TP} = threshold voltage of p-channel device (0.30V)

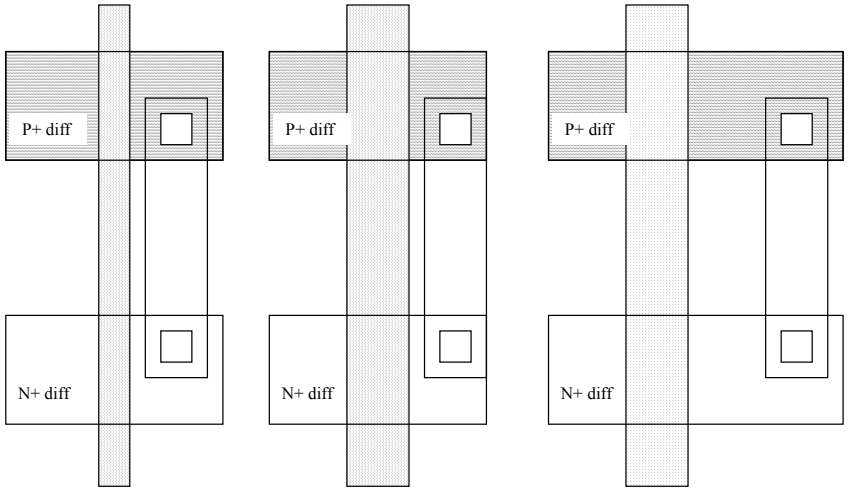


Figure 4-47: Layout modifications that do not change the commutation point

As predicted by the formulation, the sizing of the n-channel and p-channel MOS devices has a strong influence on the commutation point *Vc*. Enlarging both the nMOS and pMOS channels does not change the commutation, nor a supplementary diffusion area (Figure 4-47). As the ratio between the nMOS and pMOS sizes has an effect on *Vc*, only one device should be modified.

In figure 4-48, we have designed three inverters with almost identical characteristics. The only change is the n-channel or p-channel sizing. The inverter on the left uses the default MOS size, that is *Wp*=16, *Lp*=2 lambda, *Wn*=6, *Ln*=2 lambda. The large width for the pMOS device compensates the low mobility of holes compared to electrons, in order to achieve a balanced inverter in terms of switching performances. As a result, the static characteristics are almost symmetrical. In other words, when *Vin* is VDD/2, *Vout* is nearly VDD/2 (Curve inv_1 in figure 4-49).

For the inverter situated in the middle of the layout, the width and length of the n-channel MOS are identical to those of the p-channel MOS. The result is a lower commutation point, as shown in curve *inv_2* of figure 4-49. Thanks to this modification, the nMOS device can drive stronger currents and moves the whole curve towards lower voltages. Now, if we enlarge the n-channel MOS channel to reduce its current, the opposite result is achieved, with a commutation point shifted to higher voltages (Curve *inv_3*).

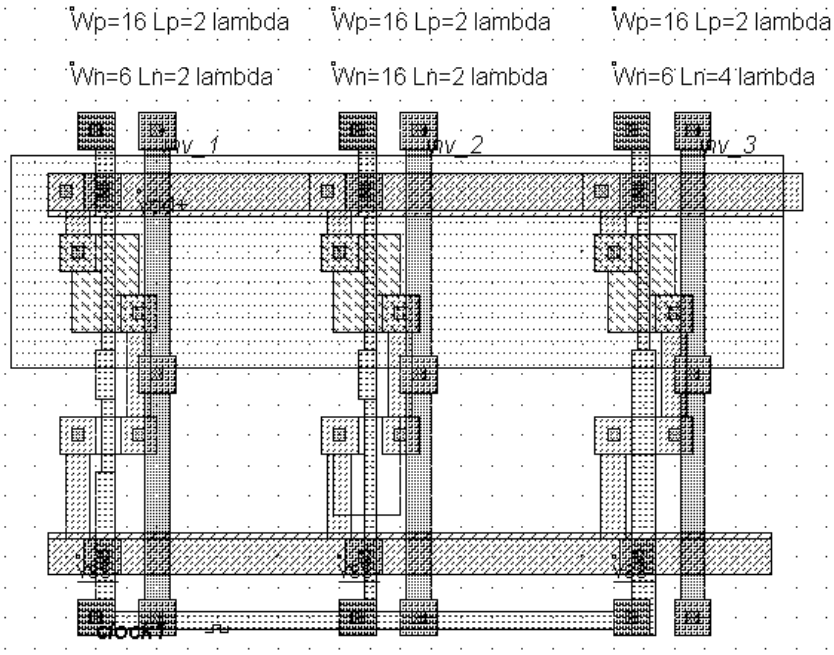


Fig. 4-48: Three different inverter sizing used to investigate its influence on the commutation point Vc (InvSizing.MSK)

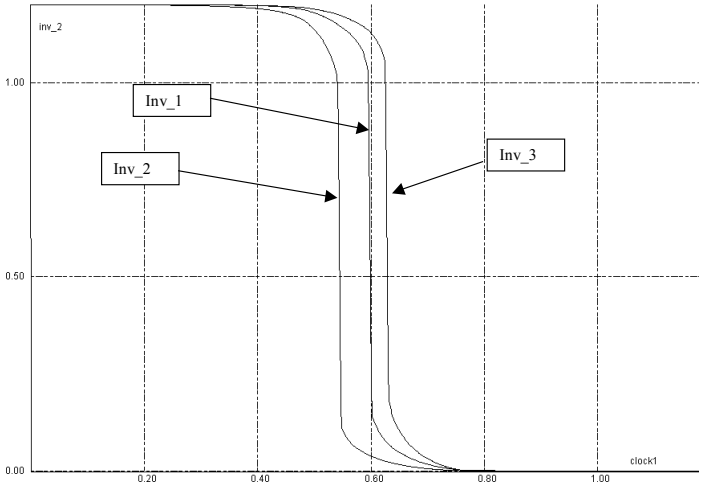


Fig. 4-49: Influence of the inverter sizing on the commutation point (InvSizing.MSK)

Influence of the model

Using the analog simulation with various models, we may obtain significantly different estimations of the switching characteristics. In figure 4-50, we superimpose the static characteristics of the same inverter using model 3 and BSIM4. While the simulation with model 3 gives *Vc*=0.6V, the simulation with BSIM4 gives *Vc*=0.63V. This difference is not significant as far as logic behavior is concerned, but may lead to wrong performance estimation in the case of analog design.

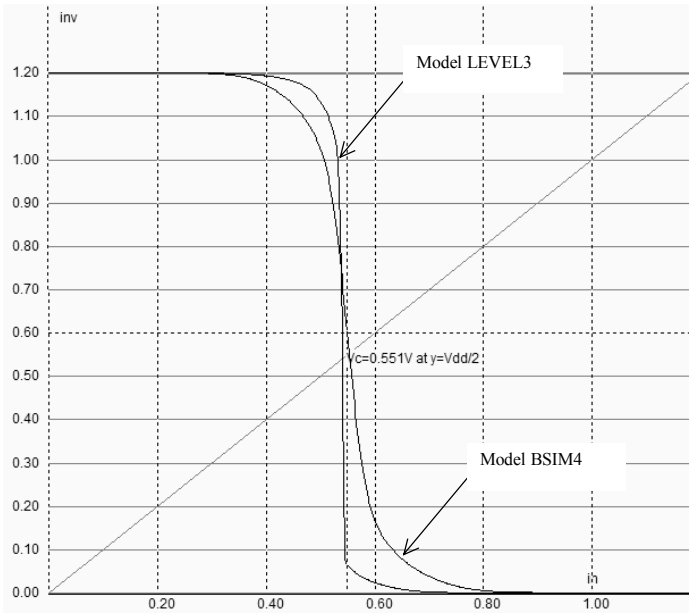


Fig. 4-50: Influence of the model on the simulation (Inv.MSK)

7. Random simulation

As explained in chapter 3, unavoidable process variations may occur during the integrated circuit fabrication, which may impact the static and dynamic characteristics of the inverter. In the menu **Simulate → Simulation parameters** the default set of parameters corresponds to the "typical" case. We may simulate the inverter in "minimum" or "maximum" case, as we did for the MOS device. An interesting alternative consists in using the "random" mode, also called "Monte-Carlo" analysis, where the threshold voltage and the mobility are chosen in a random way, as illustrated in figure 4-51. There is a high probability that `VTO` is close to the typical value, and almost no chance that `VTO` is higher than 0.44V or lower than 0.36V.

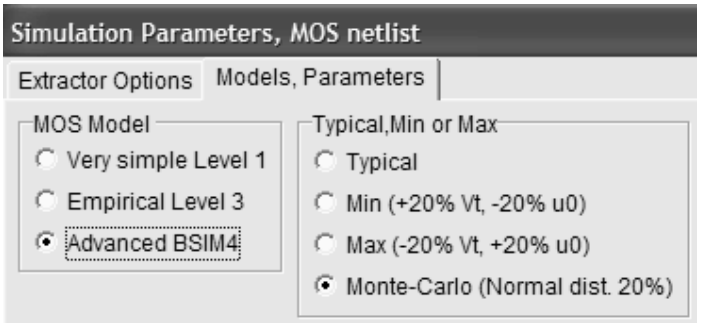


Fig. 4-51: Access to random simulation using an arbitrary set of MOS model parameters (Inv.MSK)

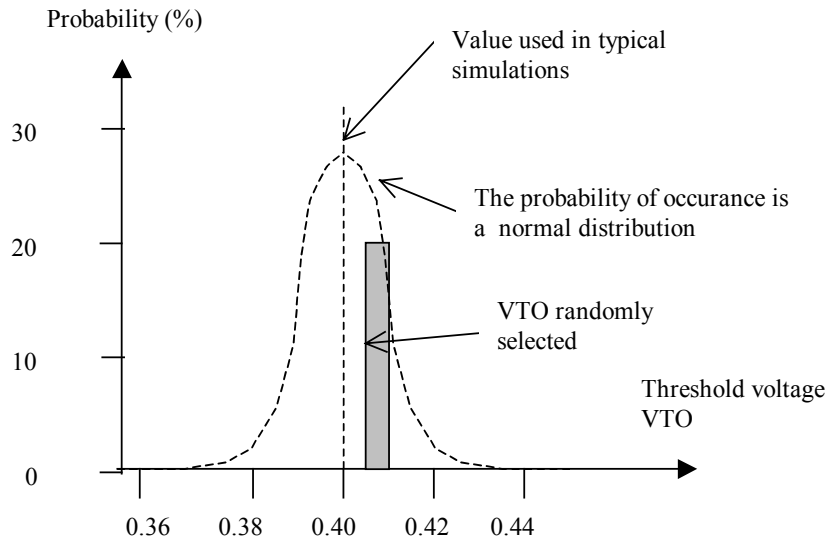


Fig. 4-52: Random selection of Vt, with a normal probability

The simulations of the transient response may be cumulated by a press of the **Reset** button. A new button **Memory** appears in the simulation window, at the right lower corner. Press this button to draw all simulations together without refreshing the grid. Each time the Reset button is activated, a new set of threshold and mobility parameters is used to conduct the simulation. The accumulation of ten successive transient simulations is represented in figure 4-53.

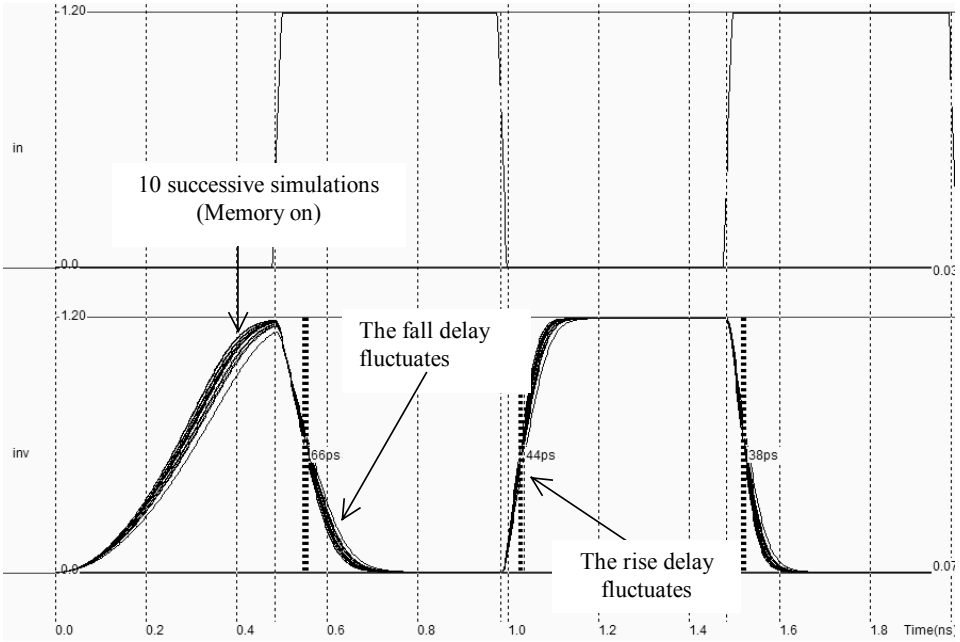


Fig. 4-53: The Monte-Carlo simulation of the inverter transient characteristics, using random VTO and UO parameters (Inv.MSK).

The inverter has a strong probability to behave close to the typical value. In some rare cases, the switching performances vary significantly. The min/max simulation is also very interesting to simulate the inverter in extreme situations.

8. The Inverter as a library cell

Generally speaking, the integrated circuit design relies on a library of basic cells. In this library, each basic cell is described in a very detailed way. The layout information and several static and dynamic aspects are usually included. Such details are important to choose the appropriate cell, to evaluate the circuit size, standby parasitic current and switching performances.

The data-sheet of the inverter usually looks like figure 4-54. Firstly, the header gives the cell name. The mask level file and symbol files are also listed. The truth table recalls the logic behavior of the cell. The symbol is also provided. In the case of complex cells such as latches, where numerous versions and options co-exist beyond the same name, the truth-table is of key importance. The node capacitance is useful for propagation delay prediction, as the switching performance is linked with the capacitance load.

The operating point recalls the value of the supply with which the characterization has been conducted. Some information is also given for low supply voltage (See also the switching characteristics at 0.9V).

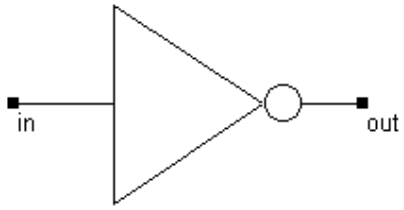
Name: INVERTER Technology: 0.12µm CMOS Layout: INV.MSK Symbol: NOT.SYM

Operating point: VDD=1.2V, Temperature=25°C

TruthTable:

In	Out
0	1
1	0

Symbol:



Capacitance:

- Input: 0.5fF
- Output 0.5fF

Drive: 1x

Cell Area : 1.26µmx4.3µm (5.14µm^2)

Power consumption : 1.02µW/MHz typical

Standby current: 100pA

Inverter	Rise time (ps)				Fall time (ps)			
Input slope	0.01ns (fast)		0.1ns (slow)		0.01ns (fast)		0.1ns (slow)	
Load (fF)	10fF	100fF	10fF	100fF	10fF	100fF	10fF	100fF
Delay In→Out	42	340	61	416	35	288	49	338
Delay In→Out (VDD=0.9V)			86				65	
Delay In→Out (max, -40°)			70				50	
Delay In→Out (min, 120°C)			122				98	

Inverter	Peak current (µA)			
Input slope	0.01ns (fast)		0.1ns (slow)	
Load (fF)	10fF	100fF	10fF	100fF
Peak current (typ)			138	
Peak current (max, -40°)			189	
Peak current (min, 120°C)			105	
Peak current (typ,VDD=0.9V)			79	

Fig. 4-54: The library information for the basic inverter (Inv.MSK).

The power consumption is usually described in µW/MHz. To characterize this value, a 1MHz clock is connected to the input and the total power consumption is computed from the integral of the current. In Microwind, we preferably use a 1GHz clock, and consequently divide the power estimation by 1000. The cell consumption increase linearly with frequency. The standby current is a key information in low-power circuits, where the standby parasitic current should be as small as possible. Depending on the MOS option (normal, high-speed, low leakage), the standby current may vary in a very significant way.

The keyword "1x" refers to the inverter strength. A cell with 1x strength is designed with small output MOS devices, usually close to the minimum length and width. A cell with 2x has medium size MOS devices, a cell with drive 4x is used for high speed signals. Cells with 8x drive or even 16x drive may exist, to propagate very fast signals such as clocks and bus. However, using cells with high drive means a high power consumption and high risks of signal integrity problems.

The delay between signals *in* and *out* is strongly dependant on the slope of the input signal, the capacitance connected to the output signal, the temperature, the power supply and the process variations. The goal of the switching delay table is to summarize the delay in typical conditions as well as in extreme conditions. Several design tools such as the timing analyzer and the power consumption extractor will use these data to guess all possible cases of loading conditions, temperature variation, etc.

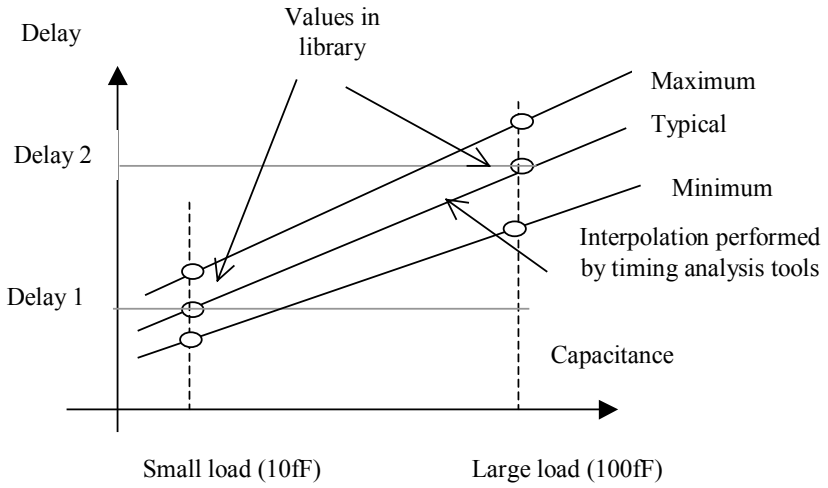


Fig. 4-55: Delay parameters are used by timing analysis tools to predict the cell switching performances for any capacitance

The current peak details are used to evaluate the power consumption of the circuit. The value of the current changes significantly depending on the loading conditions, temperature and supply voltage, as expected.

9. 3-State Inverter

Until now all the symbols produced the value logic ‘0’ and logic ‘1’. However, if several inverters share the same node, such as bus structures (Figure 4-56), conflicts will rise. In order to avoid multiple access at the same time, specific circuits called 3-state inverters are used, featuring the possibility to remain in a ‘high impedance’ state when access is not required.

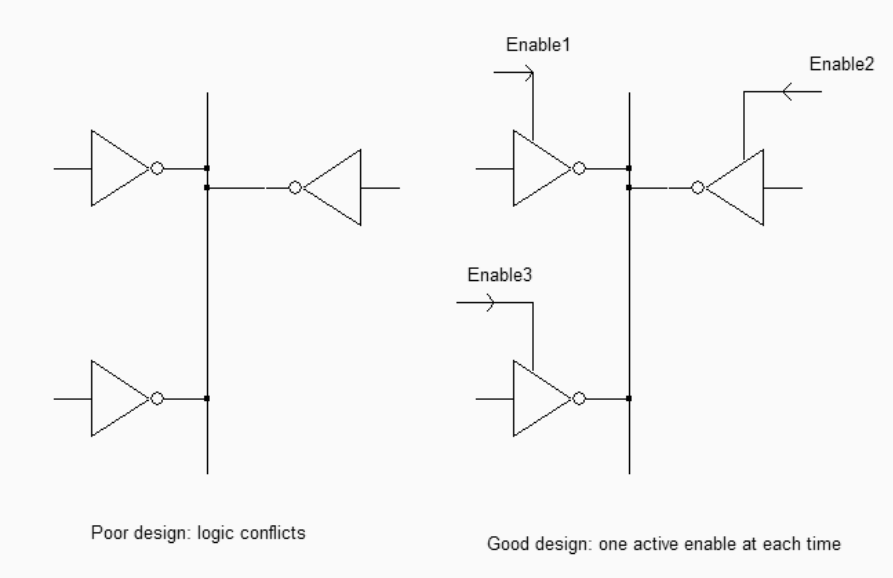


Figure 4-56: If multiple access is required on a single node, 3-state inverters are used for interfacing (Inv3state.SCH)

The 3-state inverter symbol consists of the logic inverter and an enable control circuit. The output remains in ‘high impedance’ (Logic symbol 'X') as long as the enable *En* is set to level ‘0’. The truth table is reported below.

NOTIF1

In	En	Out
0	0	X
0	1	1
1	0	X
1	1	0
x	0 or 1	X
0 or 1	X	X

The internal structure of the 3-state inverter is shown in figure 4-57. The basic CMOS inverter is no more connected to the supply lines VDD and VSS directly. In contrary, pass nMOS and pMOS devices are inserted to disconnect the inverter when the cell is disabled.

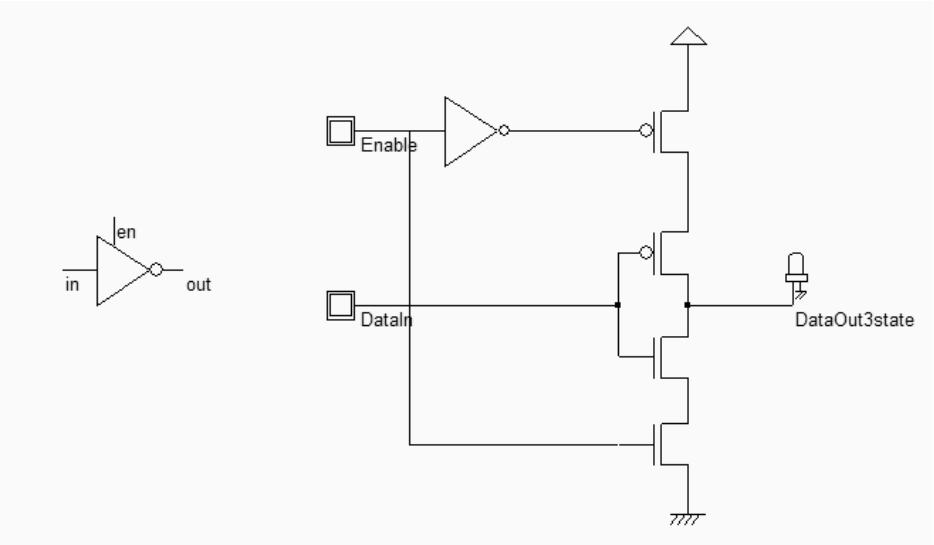


Figure 4-57: Schematic diagram and logic symbol for the 3-state inverter (CmosInv3State.SCH)

Unfortunately, a supplementary inverter is needed to generate the /enable signal required to control the pMOS device. The logic simulation reported in figure 4-58 illustrates two basic situations: one where *enable* is inactive, and the output is in high-impedance state <glossary> as no path exists to VDD or VSS, the other where the circuit is equivalent to an inverter, as the upper and lower pass transistors are enabled.

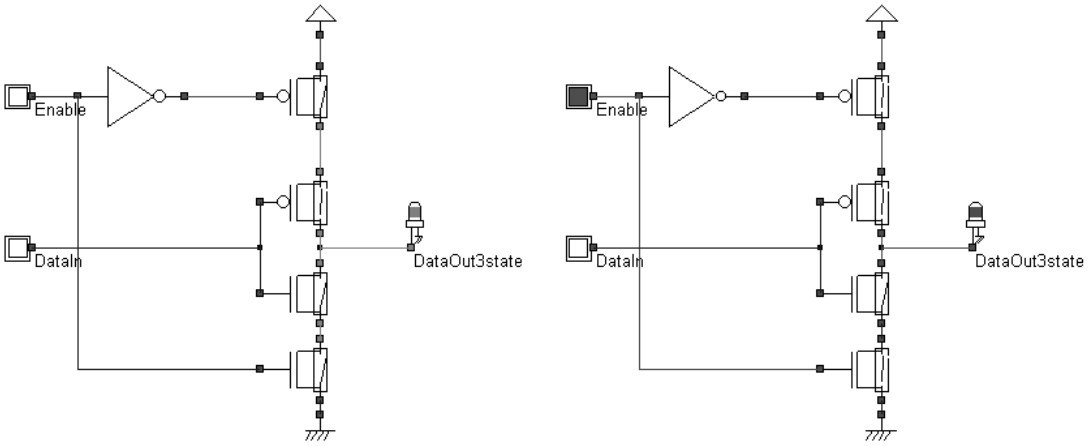


Figure 4-58: Simulation of the 3-state inverter (CmosInv3State.SCH)

Two versions of layout are proposed in figure 4-59, and they correspond to the same design. The cell situated on the left is the direct implementation of the schematic diagram of the 3-state inverter. The layout implementation is not optimal as we loose some silicon area due to severe diffusion design rules which require a 4 lambda spacing. The new arrangement, shown on the right of the figure, is significantly more compact, thanks to horizontal flip of the *Enable* inverter, and the sharing of the ground and supply contacts, as illustrated in figure 4-60. Continuous diffusions always lead to more compact and faster designs.

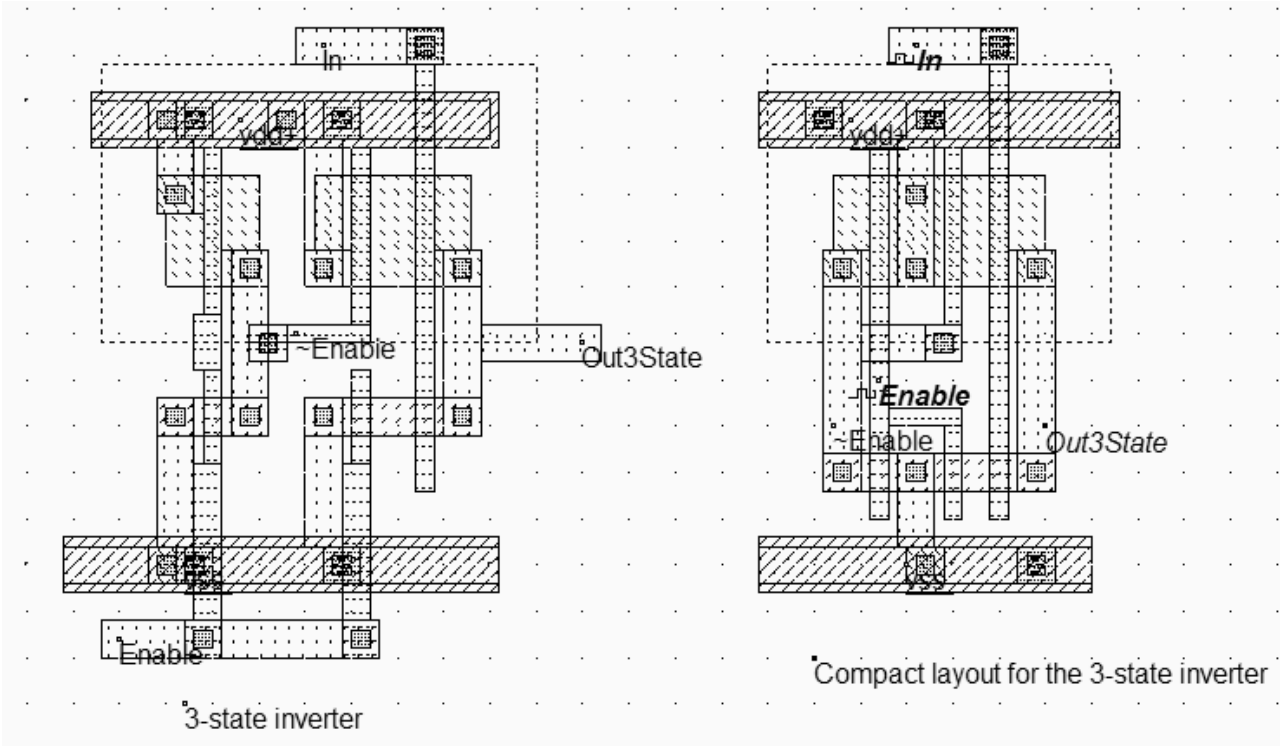


Figure 4-59: The layout of the 3-state inverter (Inv3State.MSK)

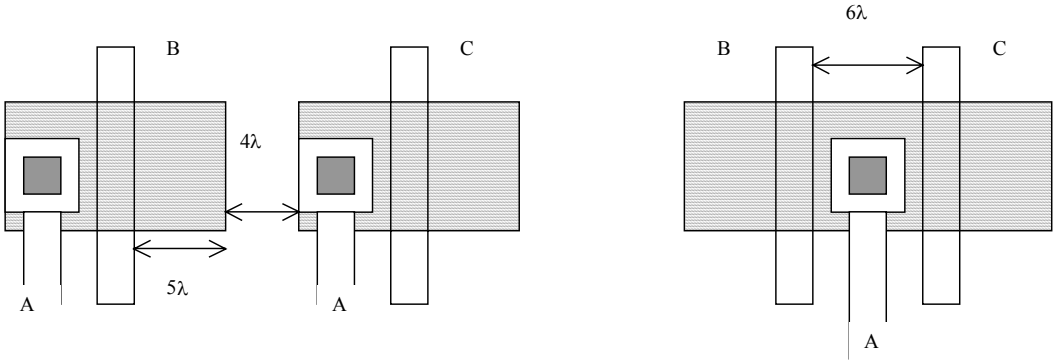


Figure 4-60: A permutation technique to achieve more compact layout

The analog simulation reported in figure 4-61 gives an interesting view of the high impedance state. From the chronograms, we see that when *Enable*=1 the cell acts as a regular CMOS inverter, while when *Enable*=0 the output "floats" in an unpredictable voltage value, which tends to fluctuate at the switching of the input, mainly due to parasitic leakage and couplings.

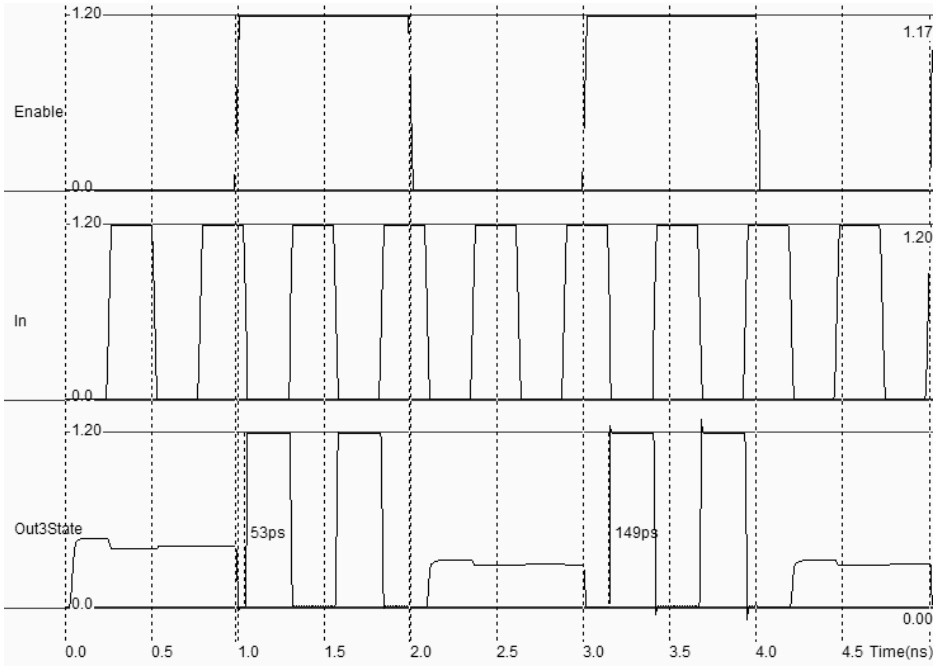


Figure 4-61: Analog simulation of the 3-state inverter (INV3STATE.MSK)

10. All nMOS Inverters

Several other circuits exist to build the logic inverter function [Baker]. One popular inverter is shown in figure 4-62. It consists of a normal n-channel MOS device *N1* and of another n-channel MOS device *N2* connected as a simple load. Due to the permanent connection of the gate to VDD, the nMOS device *N2* is equivalent to a resistance Ron_N2. When *Clock*=0, a path exists to rise the output through the resistance. The final value *Vhigh* is *VDD-Vtn*, where *Vtn* is the threshold of *N2*. When *clock*=1, the circuit is equivalent to a voltage divider where *N2* still conducts, and *N1* creates a path to ground. An approximation of *Vlow* is given by equation 4-7.

$$V_{low} = VDD \frac{R_{on\_N2}}{R_{on\_N1} + R_{on\_N2}} \quad \text{(Equ. 4-7)}$$

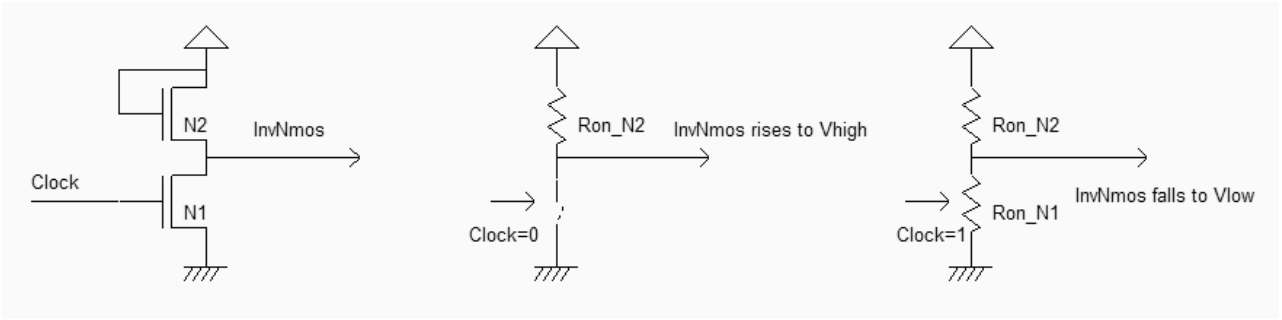


Figure 4-62: An inverter only made with nMOS devices (InvNmos.SCH)

The simulation waveforms given in figure 4-63 are quite unusual as the low state (*Clock*=1) of the output leads to a stand-by current which had not appeared until now in CMOS circuits. This DC power waste is a major drawback for this kind of design. Furthermore, the logic level 0 corresponds to 0.3V while the logic level 1 corresponds to 0.8V. The switching is slow, specifically from 0 to 1, due to a weak nMOS device. However, no pMOS device is required, which simplifies both the design and the process. The device N2 is sized with a large length and a small width to increase the resistance *Ron_N2*, to lower the output voltage when *clock*=1. All n-MOS inverters were used before CMOS technology was made available.

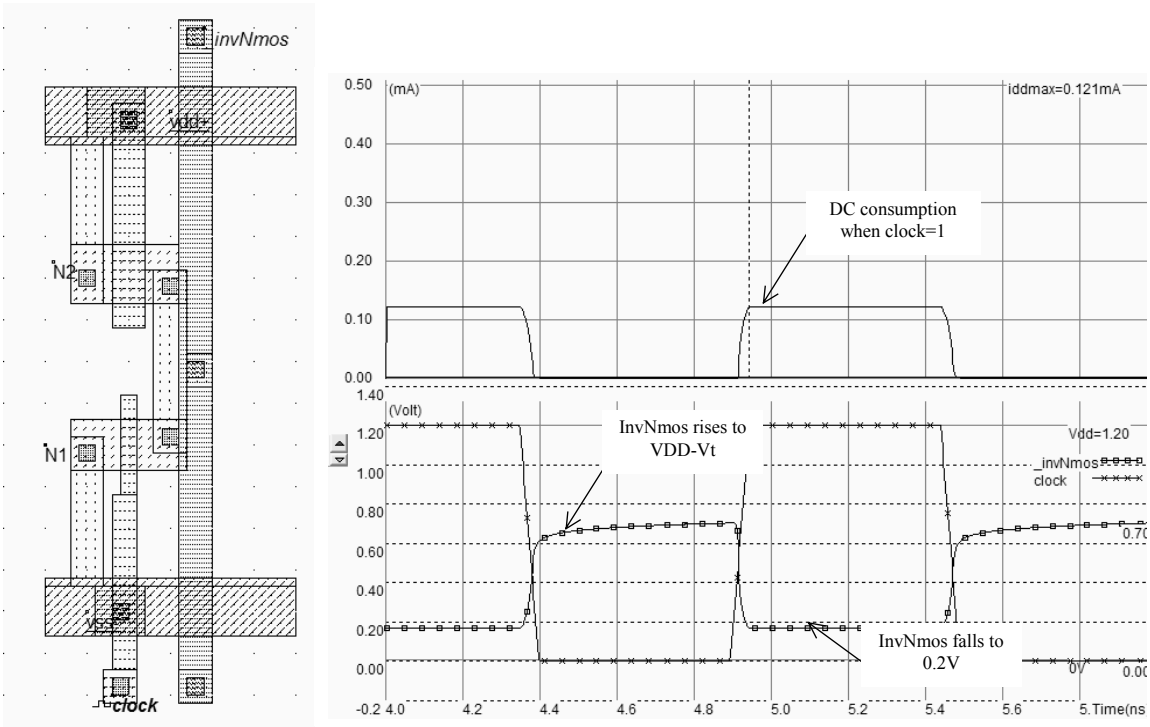
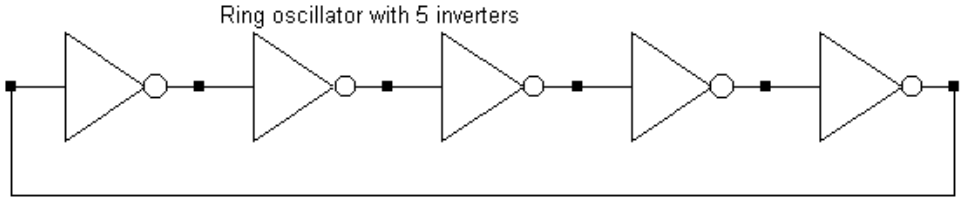


Figure 4-63: All n-MOS inverter(INVNMOS.MSK)

11. Ring Oscillator

The ring oscillator made from 5 inverters has the property of oscillating naturally. We observe in the circuit of figure 4-64 the oscillating outputs and measure their corresponding frequency.



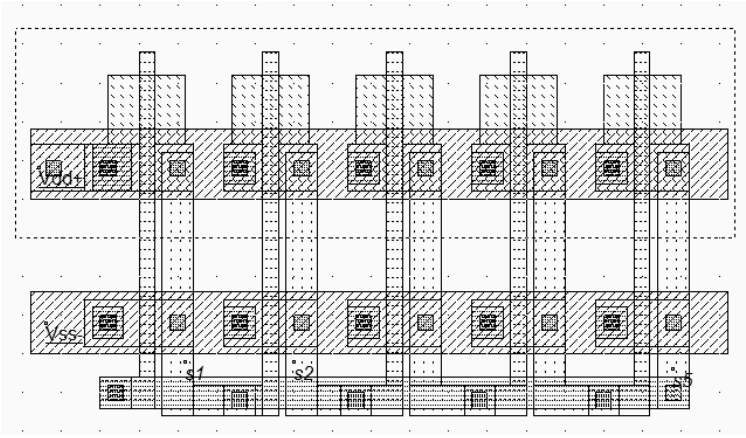


Figure 4-64: Schematic diagram and layout of the ring oscillator used for simulation (INV5.MSK)

The ring oscillator circuit can be simulated easily at layout level with Microwind using various technologies. The time-domain waveform of the output is reported in figure 4-65 for 0.8, 0.12µm and 70nm technologies. Although the supply voltage (VDD) has been reduced (VDD is 5V in 0.8µm, 1.2V in 0.12µm, and 0.7V in 70nm), the gain in frequency improvement is significant.

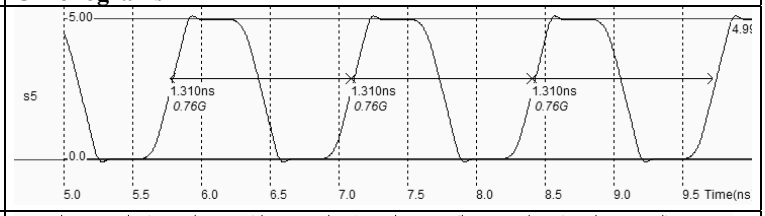
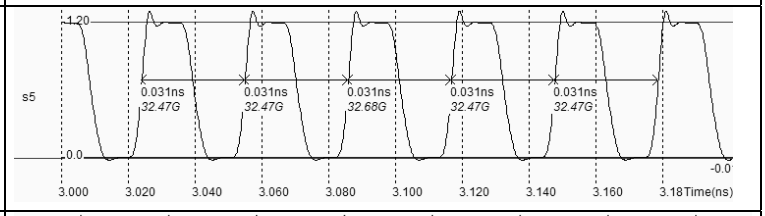
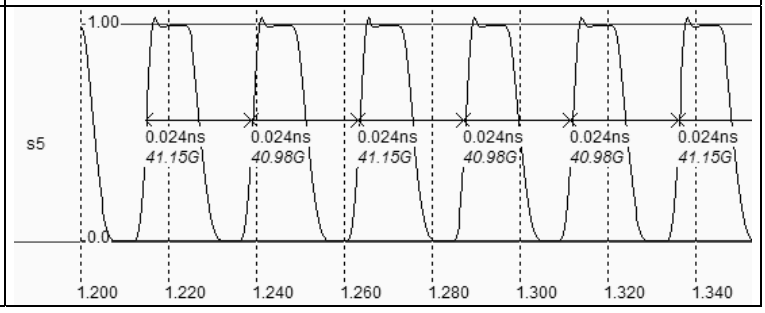
Technology	Supply	Oscillation	Chronograms
0.8 µm	5V	0.76GHz	
0.12 µm	1.2V	32GHz	
90nm	1.0V	41GHz	

Fig. 4-65: Oscillation frequency improvement with the technology scale down (Inv5.MSK)

By default the software is configured with 0.12µm technology. Use the command **File → Select Foundry** to change the configuring technology. For example, select **cmos08.RUL** which corresponds to the CMOS 0.8µm technology, or the file **cmos90nm.RUL** which configures Microwind to the CMOS 90nm technology. When you run again the simulation, you may observe the change of VDD and the significant change in oscillating frequency.

High Speed vs. Low leakage

Let us consider the ring oscillator with an enable circuit, where one inverter has been replaced by a NAND gate to enable or disable oscillation (Inv5Enable.MSK). The schematic diagram is shown in figure 4-66, as well as its layout implementation. We analyze the switching performances in high speed and low leakage mode, by changing the properties of the option layer which surrounds all devices.

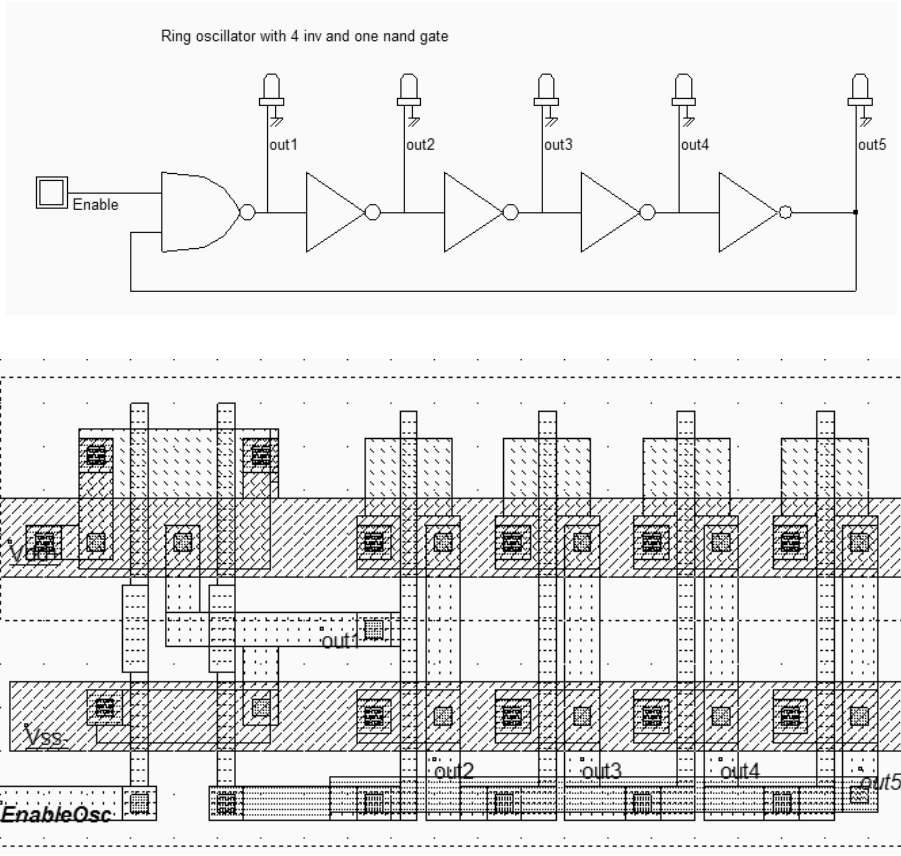


Fig. 4-66 The schematic diagram and layout of the ring oscillator used to compare the analog performances in high speed and low leakage mode (INV5Enable.MSK)

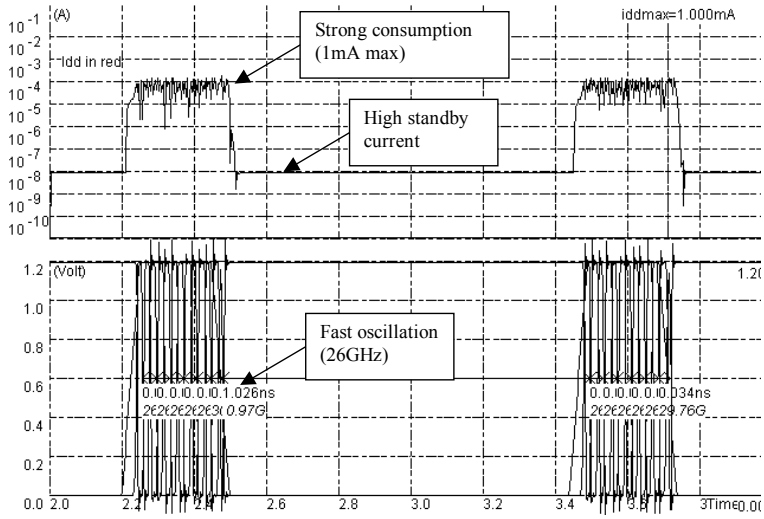


Fig. 4-67: Simulation of the ring oscillator in high speed mode, using BSIM4 model. The oscillating frequency is fast but the standby current is high (Inv5Enable.MSK)

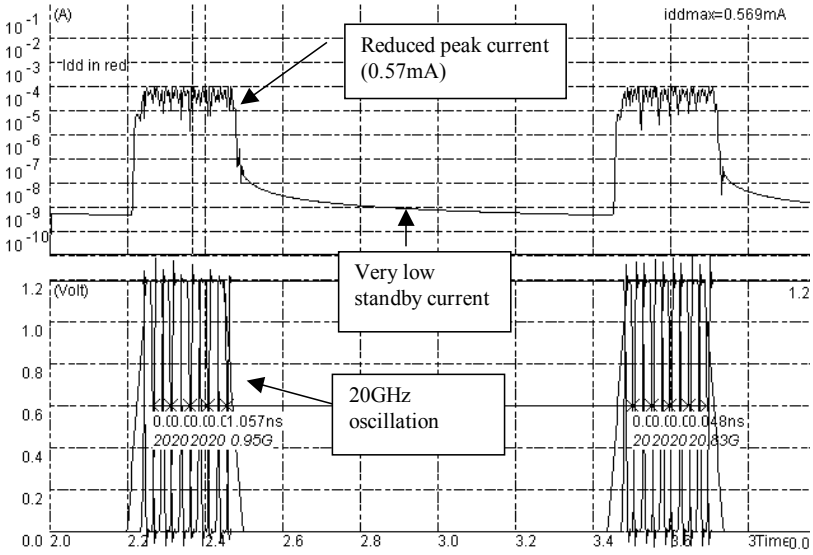


Fig. 4-68: Simulation of the ring oscillator in low voltage mode, using BSIM4 model. The oscillating frequency is slower but the standby current is very low (Inv5Enable.MSK)

Parameter	**Low leakage mode**	**High Speed mode**
Imax	0.6 mA	1.0mA
I standby	<1nA	>10nA
Oscillating frequency	20GHz	26GHz

Table 4-4: Comparative performances of the ring oscillator (Inv5Enable.MSK)

The option layer which surrounds the oscillator is set to high speed mode by a double click inside that box. In high speed mode, the circuit works fast (26GHz) but consumes a lot of power (1mA) when on, and a significant standby

current when off (10nA), as shown in the simulation of the voltage and current given figure 4-66. Notice the tick in front of "Scale I in log" to display the current in logarithmic scale.
In contrast, the low leakage MOS features slower oscillation (20GHz in figure 4-67, that is approximately a 25% speed reduction) , but with 40% less current when ON, and more than one decade less standby current when off (1nA). In summary, low leakage MOS devices should be used whenever possible. High speed MOS should be used only when speed is critical, such as communication bus, critical path, etc.. The analog performances are summarized in table 4-4.

Temperature effects

The main consequence of temperature increase is a decreasing mobility of the electrons and holes of the MOS channel, leading to slower transient performances. Thus, the propagation delay due to the logic gate is increased, as illustrated in figure 4-68 which concerns the switching characteristics of the 5-inverter ring oscillator. In Microwind2, you can get access to temperature using the command **Simulate → Simulation Parameters**. The temperature is given in °C.

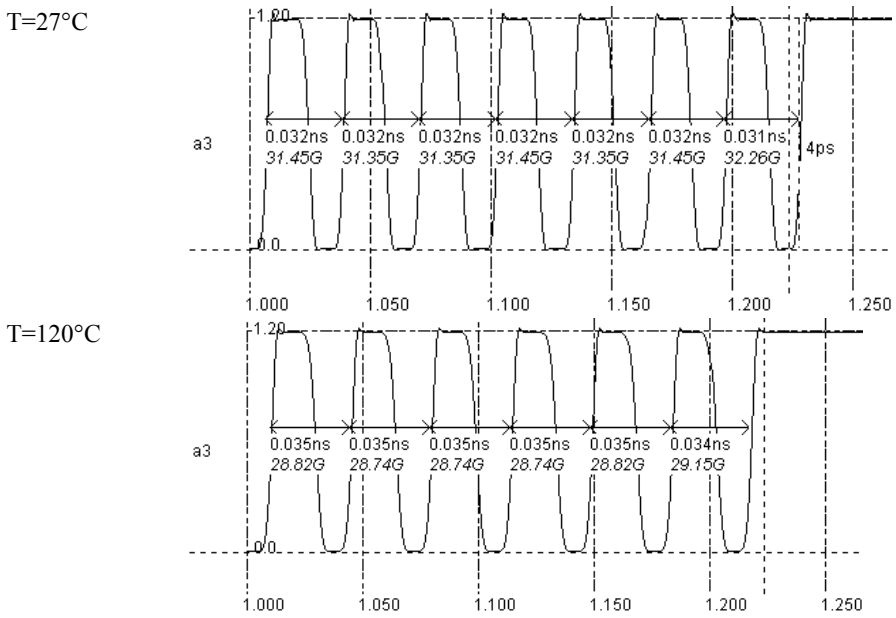


Fig. 4-69. Propagation delay increases with temperature (Inv5Enable.MSK)

In the simulation of figure 4-69, we used the BSIM4 model for a temperature set to 25°C and 120°C. We can observe a 10% decrease of switching speed, which finds its origin in the mobility degradation, which is computed by the following formulation.

$$U0 = U0_{(T=27)}\left(\frac{T+273}{300}\right)^{-1.8} \qquad \text{(eq. 4-4)}$$

We may conduct the parametric analysis of the temperature influence on the oscillating frequency, in order to obtain the results reported in figure 4-70. It may be seen that the frequency variation from -100°C to +100°C is kept below

15%. The reason for this reduced dependence is that the mobility reduction is compensated by the threshold voltage decrease, also strongly dependent on the temperature, which tends to limit the overall effects of temperature variations.

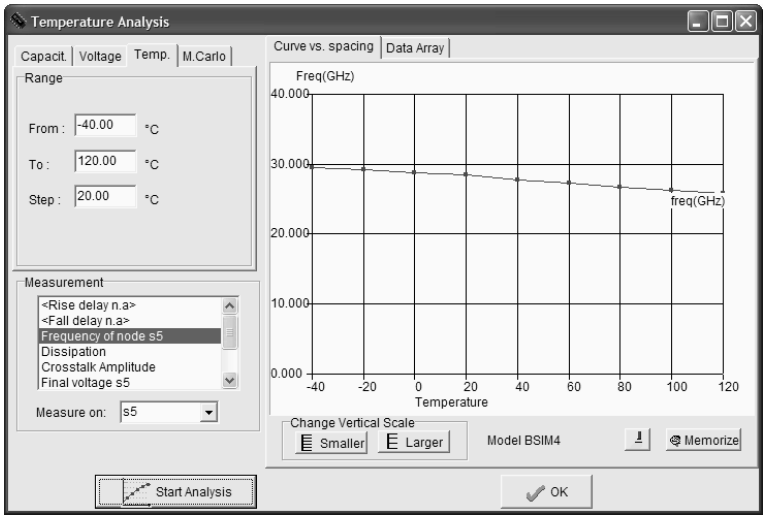


Fig. 4-70: Performances of the ring oscillator versus temperature increase (Inv5Enable.MSK)

A 2.5GHz ring oscillator

The previous ring oscillator operated around 30GHz, which is of no practical use. In contrast, the 2.5GHz frequency is widely used for a variety of wireless network applications. In this paragraph, we investigate several possibilities to slow the oscillator frequency down to 2.5GHz. One immediate idea consists in designing a ring oscillator with more inverter stages (Around 70). This is a power consuming and silicon area consuming approach. A more attractive solution consists in the reduction of the MOS current capabilities. Then a new question rises: how should we proceed, as we may increase the channel length, decrease the channel width, or add parasitic capacitance in each switching node (Figure 4-70)?

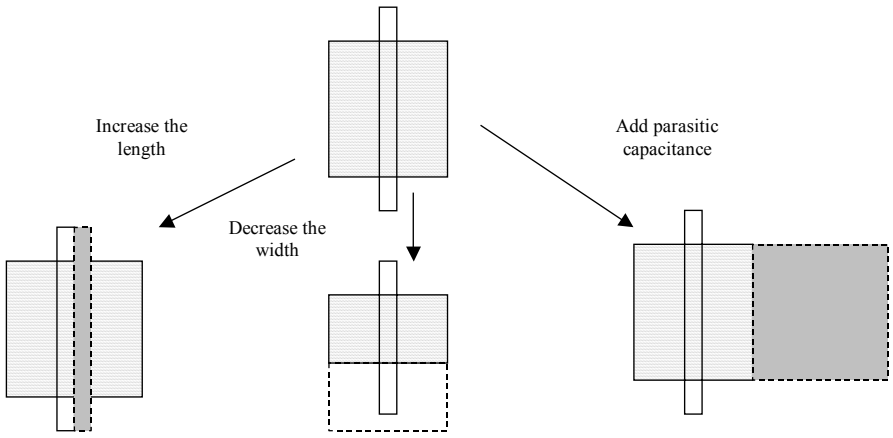


Figure 4-71: Reducing the current of the MOS device may be performed by increasing the length or decreasing the width

One solution is proposed in figure 4-72. It combines the channel length increase, the width decrease to its minimum value, and the enlarging of drain areas whenever possible to increase the parasitic junction surface, and consequently its parasitic capacitance. All these layout modification have a sufficient impact to reduce the oscillating frequency to around 2.5GHz. Notice that this frequency is very sensitive to process parameters, temperature, and supply voltage variation.

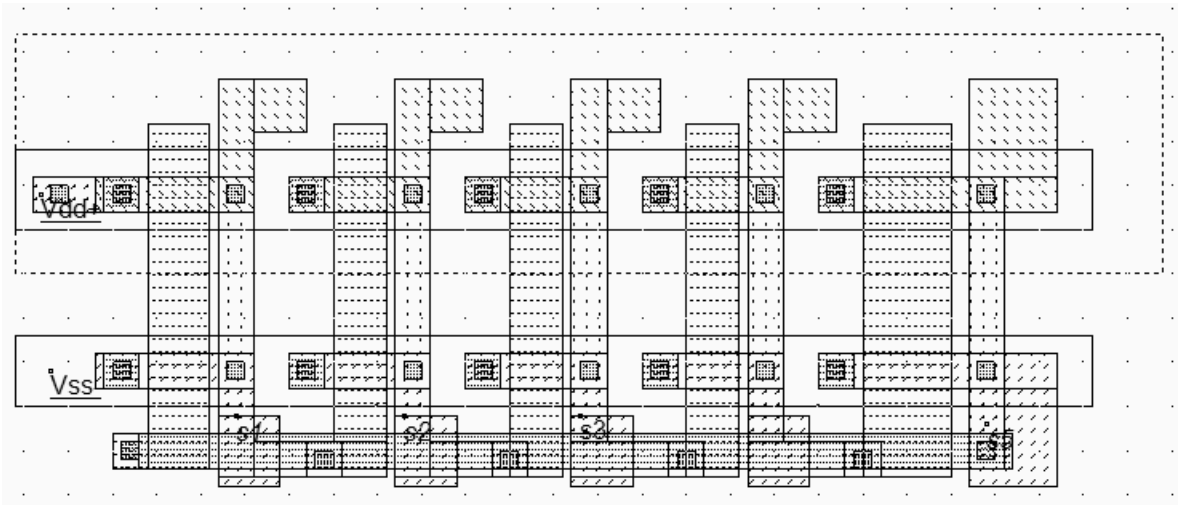


Figure 4-72: The 5-inverter oscillator tuned to 2.5GHz (Inv2,5GHz.MSK)

12. Latch-up effect

The latch-up effect is a parasitic shortcut between VDD and VSS that can lead to the destruction of the integrated circuits. The origin of latch-up is the activation of a parasitic N/P/N/P device (Also called thyristor) appearing in the vertical cross-section of the nMOS and pMOS structures as reported in figure 4-73.

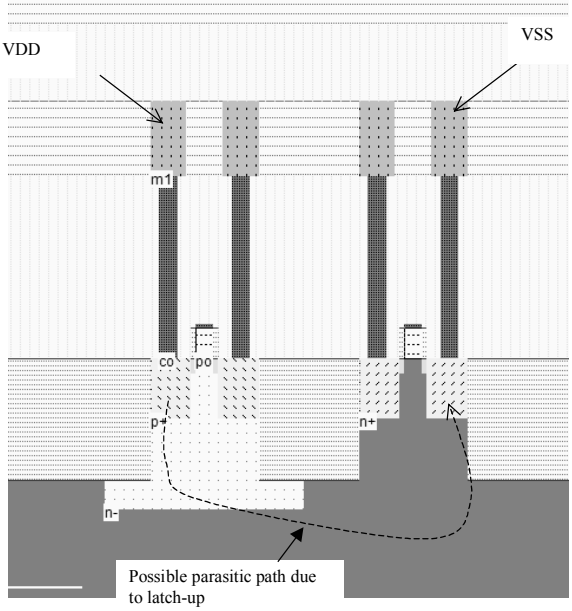


Fig. 4-73. Origin of latch-up

Limiting the latch-up effect

The latch-up effect is almost eliminated if the substrate is locally polarized to ground, and the n-well is locally polarized to VDD (Figure 4-74). In the upper layout (Figure 4-74a), the situation is extremely dangerous as the n-well region is floating. If the n-well potential drops around VDD/2 and the local substrate voltage rises to VDD/2, the latch-up phenomenon is initiated. Most layout tools alert the designer in the case of floating n-well regions. The good approach consists in inserting a polarization diode N+/N-well and stuck it to the highest possible potential, typically VDD.

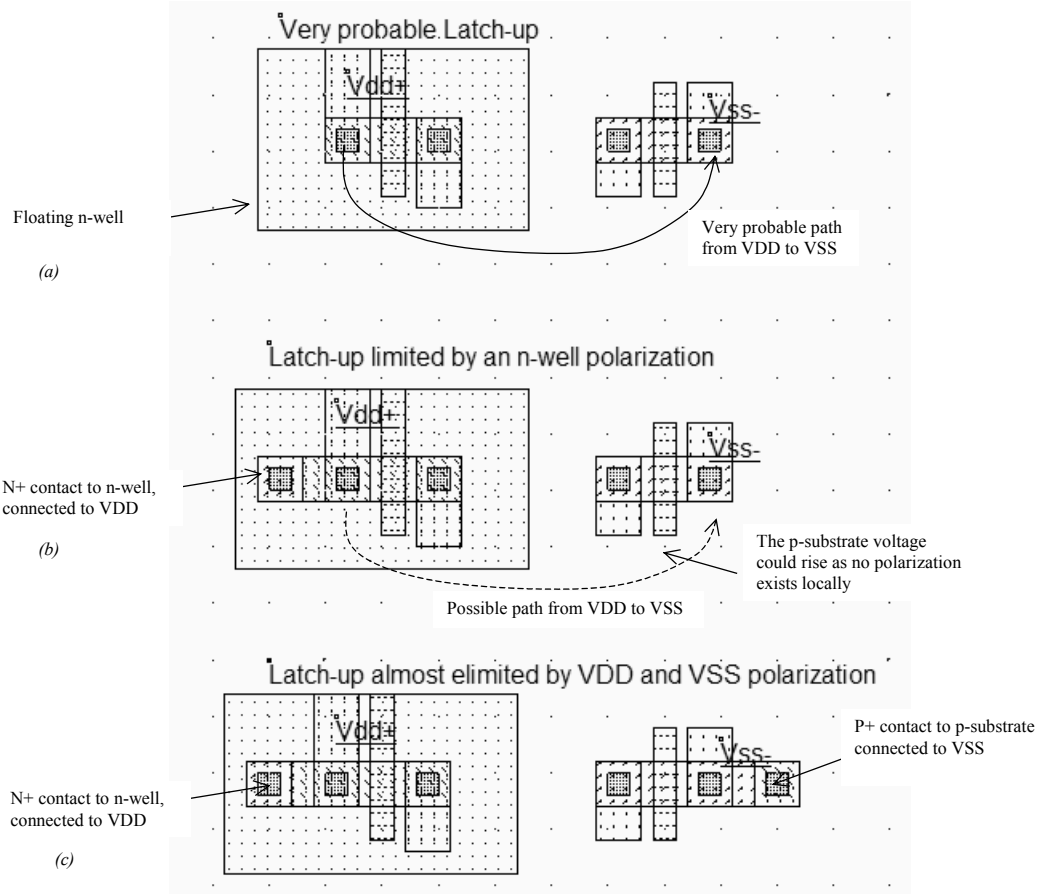


Fig. 4-74 Limiting the latch-up effect by polarization diodes

Many designers consider that there exists an « automatic » polarization of the substrate to ground and forget to add a local P+/P-substrate contact to ground, near the nMOS device (Figure 4-74b). This might be a dangerous assumption which can cause latch-up: in 0.12µm technologies, several manufacturers use a highly resistive p-doped substrate. In that case, the electrical link between the physical ground (Back of the IC) and the local nMOS area is equivalent to a resistor of several Kohm. Consequently, what is supposed to be a good 0V reference is a very weak 0V, that can easily fluctuate and turn on the N/P/N/P device, which may lead to latch-up and possible destruction. This is why it is highly recommended to add also a P+/P-substrate polarization to ground, which protects the logic cell from latch-up (Figure 4-74c).

13. CONCLUSION

This chapter has described the CMOS inverter, from a logic and analog point of view. The mobility difference between electrons and holes has been counterbalanced at layout level to obtain symmetrical static and dynamic characteristics. The effect of MOS model and temperature on the simulation results have also been investigated. The 3-state inverter, all n-MOS inverter and ring-oscillator circuits have been designed and simulated. Finally, we have presented the basic polarization techniques to avoid the parasitic latchup effect.

REFERENCES

[Weste] N. Weste, K. Eshraghian "Principles of CMOS VLSI design", Addison Wesley, ISBN 0-201-53376-6, 1993

[Baker] R.J. Baker, H. W. Li, D.E. Boyce "CMOS circuit design, layout and simulation", IEEE Press, ISBN 0-7803-3416-7, 1998

EXERCISES

4.1 Create the layout and compare the static characteristics of the three following inverters:

- Wn<Wp
- Wn=Wp
- Wn>Wp

Which one seems to be well balanced ? Justify your answer.

Answer: The most symmetrical behavior is obtained for Wp~2.Wn

4.2 We consider the two inverters of figure 4-75. We define t_{PLH1} as the delay from a low to high value of the output *inv1* (Figure 4-75). We define t_{PLH2} as the delay from a low to high value of the output *inv2*. Find the relation between the propagation delays t_{PLH1} and t_{PLH2}.

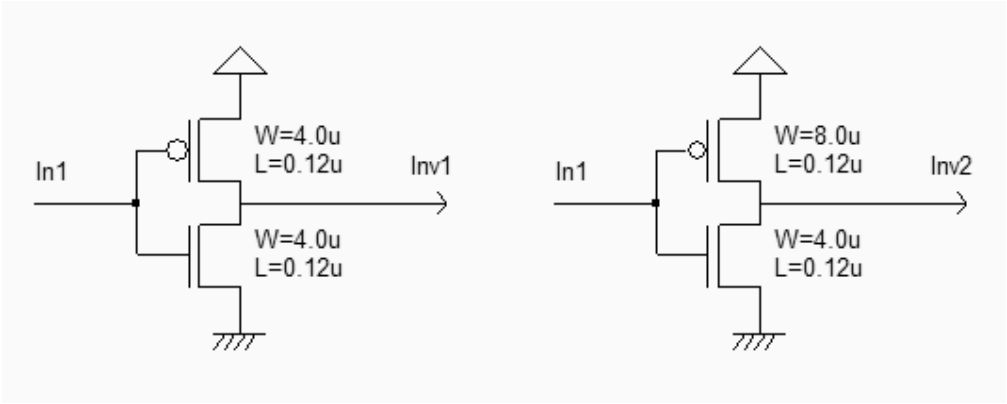


Figure 4-75: Compared performances of two inverters with different sizing (ch42.sch)

Answer: $t_{PLH2}=2/3 * t_{PLH1}$

4.3 Using Microwind in 0.12µm, draw an inverter (W_{PMOS}=2µm, W_{NMOS}=1µm) connected to a 100fF capacitor. Find *RON* and *ROFF* of each transistor and calculate t_{PHL} and t_{PLH}. Compare their value to the simulated results.

Answer: RON=, ROFF=, t_{PHL}= , t_{PLH}= <Sonia>

4.4 Configure Microwind in 90nm and design a ring oscillator using an odd number of inverters (For example 11). Based on the analog simulation using BSIM4, find the inverter propagation delay (t_p) and the oscillator frequency (f_{osc}). Extract t_{PHL} and t_{PLH} and deduce the theoretical oscillator frequency f_{osc_theory}. Compare it to the simulation (f_{osc}). Playing with the available MOS options in 90nm technology, analyze the variation of f_{osc}.

Answer: tp=, fosc=, fosc_therory= ,fosc_lowleakage=,fosc_highspeed,fosc_ultrahigh= <Sonia>

4.5 Using Microwind, design 2 inverters: INV1 ($L_{min,}$ $WN_{min,}$ WP_{min}), INV2 ($L_{min,}$ 4 x $WN_{min,}$ 4 x WP_{min}). What is the input capacitance of INV1? Simulate the 4 following configurations using the same input clock (clock switching: *tr*=*tf*=10ps) and extract the switching delays. Would the switching delay be different with a larger *tr* and *tf*?

- INV1 alone
- INV1 connected to INV1
- INV1 connected to INV2
- INV1 connected to a 10fF load

Answer: Cin_inv1=, td1=,td2=,td3=,td4=, when tr>xxxps, the delay starts to increase with tr <Sonia>

4.6 Using Microwind in 0.12µm, draw an inverter (L=0.12µm, W_{PMOS}=0.6µm, W_{NMOS}=0,3µm).

- Simulate the PMOS characteristics to find its I_{ON} current.
- Use the time domain simulation in mode **voltage and current** to compare I_{CCmax} to I_{ON}. Extract the power dissipation.
- Add a capacitor on the inverter output. For the two following values (1fF, 100fF) compare I_{Ccmax} and the power dissipation.
- Design a new inverter (L=0.12µm, W_{PMOS}=6µm, W_{NMOS}=3µm) with a 100fF load. What is the minimum number of diffusion contacts necessary to avoid current overstress in the inverter?

Answer: Ion=, Iccmax=, pow=,iccmax1f=,iccmax100f=,contacts=<Sonia>

4.7 Analyze the variation of frequency versus the technological parameter variation, for the 5-inverter ring oscillator (Inv5.MSK). Use the command **Analysis → Parametric analysis** for this study.

Answer: The variation is around