1 Introduction

The evolution of integrated circuit (IC) fabrication techniques is a unique fact in the history of modern industry. There have been steady improvements in terms of speed, density and cost for more than 30 years. In this chapter, we present some information illustrating the technology scale down.

1. GENERAL TRENDS

Inside general purpose electronics systems such as personal computers or cellular phones, we may find numerous integrated circuits (IC), placed together with discrete components on a printed circuit board (PCB), as shown in figure 1-1. The integrated circuits appearing in this figure have various sizes and complexity. The main core consists of a microprocessor, considered as the heart of the system, that includes several millions of transistors on a single chip. The push for smaller size, reduced power supply consumption and enhancement of services, has resulted in continuous technological advances, with possibility for ever higher integration.

Figure 1-1: Photograph of the internal parts of a cellular phone <Etienne: Or automotive>

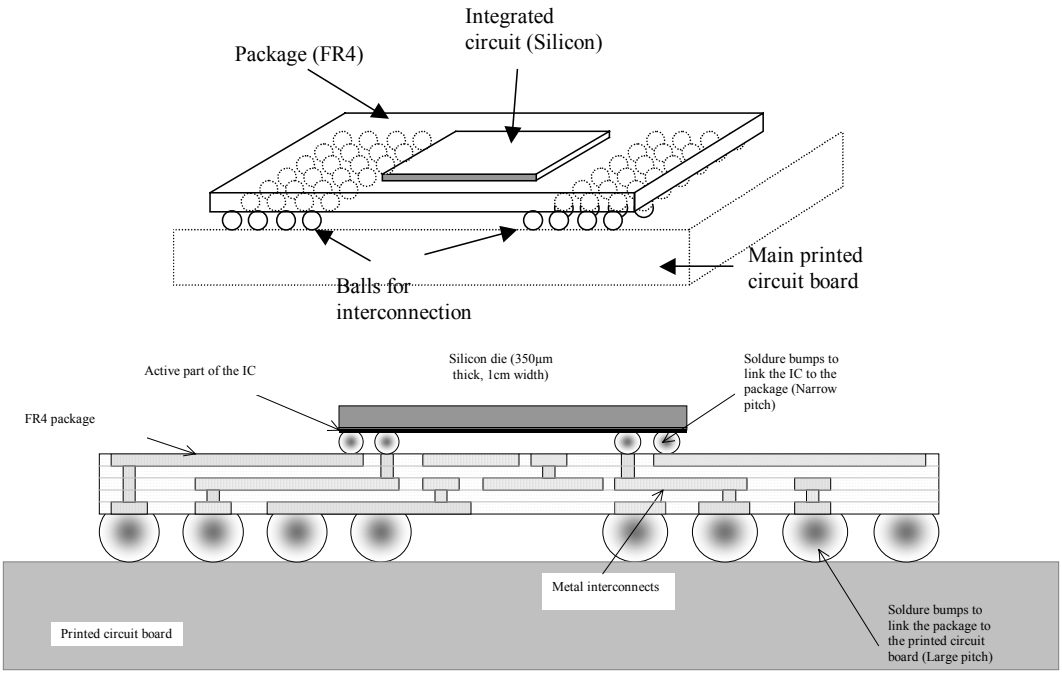
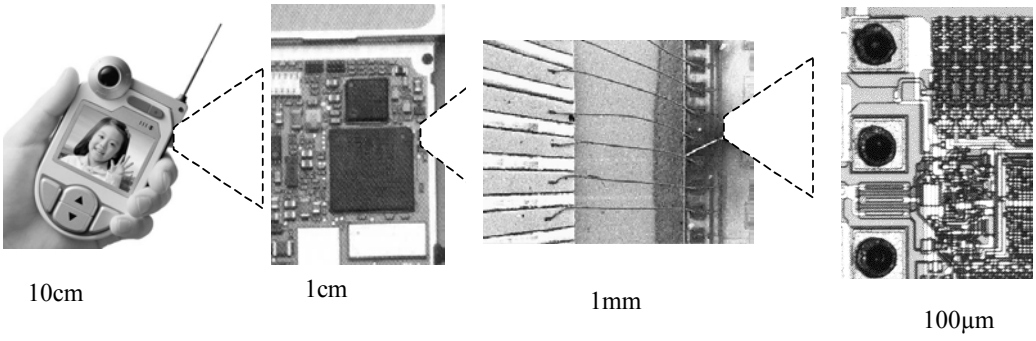


Figure 1-2: Typical structure of an integrated circuit

The integrated circuit consists of a silicon die <Glossary>, with a size usually around 1cmx1cm in the case of microprocessors and memories. The integrated circuit is mounted on a package (Figure 1-2), which is placed on a printed circuit board. The active part of the integrated circuit is only a very thin portion of the silicon die. At the border of the chip, small solder bumps serve as electrical connections between the integrated circuit and the package. The package itself is a sandwich of metal and insulator materials, that convey the electrical signals to large solder bumps, which interface with the printed circuit board.



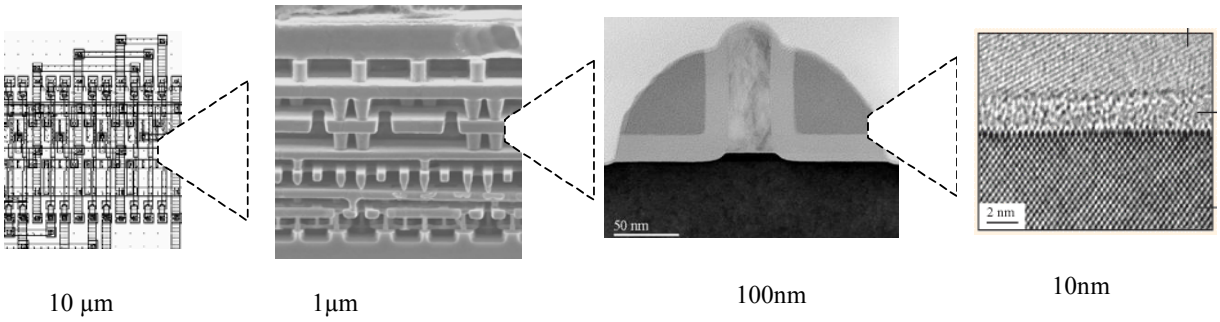


Figure 1-3: Patterns representative of each scale decade from 10cm to 10nm (Courtesy IBM, Fujitsu)

Around eight decades separate the user's equipment (Such as a mobile phone in figure 1-3) and the basic electrical phenomenon, consisting in the attraction of electrons through an oxide. Inside the electronic equipment, we may see integrated circuits and passive elements sharing the same printed circuit board (1 cm scale), wire connections between package and the die (1mm scale), input/output structures of the integrated circuit (100µm scale), the integrated circuit layout (10µm), a vertical cross-section of the process, revealing a complex stack of layers and insulators (1µm scale), the active device itself, called MOS transistor (which stands for Metal oxide semiconductor<glossary>).

Figure 1-4 describes the evolution of the complexity of Intel ® microprocessors in terms of number of devices on the chip [Intel]. The Pentium IV processor produced in 2003 included about 50,000,000 MOS devices integrated on a single piece of silicon no larger than 2x2 cm.

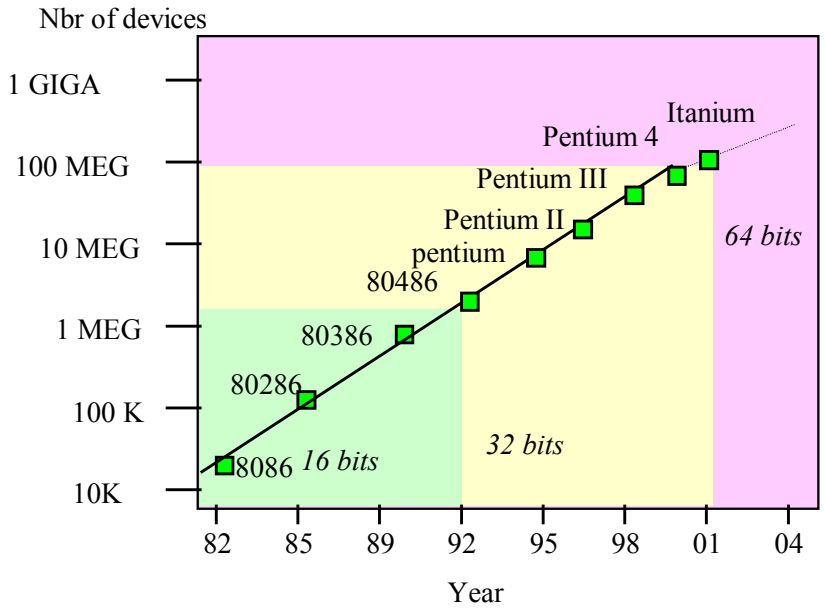


Figure 1-4: Evolution of microprocessors [Intel]

Since the 1 Kilo-byte (Kb) memory produced by Intel in 1971, semiconductor memories have improved both in density and performances, with the production of the 256 Mega-bit (Mb) dynamic memories (DRAM) in 2000, and 1Giga-bit (Gb) memories in 2004 (Figure 1-5). In other words, within around 30 years, the number of memory cells integrated on a single die has been increased by 1,000,000. An other type of memory chip called Flash memory has become very popular, due to its capabilities to retain the information without supply voltage (Non voltaile memories are described in chapter 9). According to the international technology roadmap for semiconductors [Itrs], the DRAM memory complexity is expected to increase up to 16 Giga-byte (Gb) in 2008.

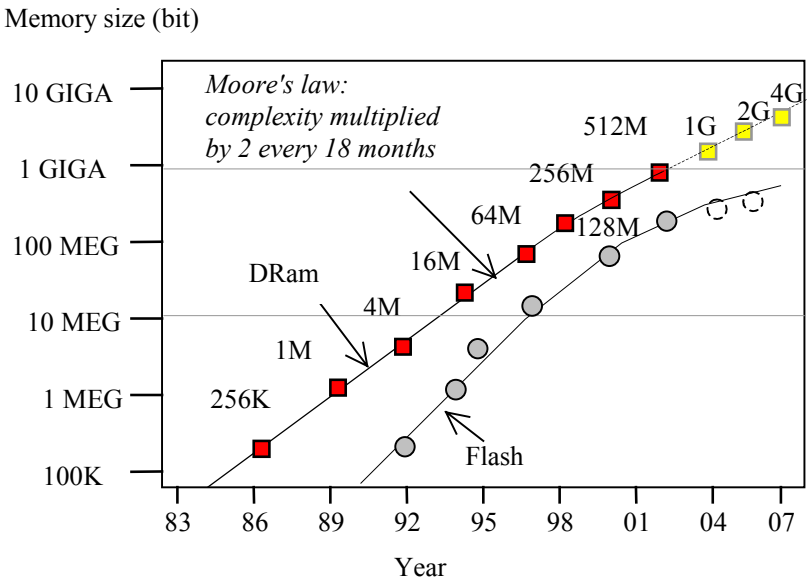


Fig. 1-5: Evolution of Dynamic RAM and Flash semiconductor memories [Itrs][Itoh01]

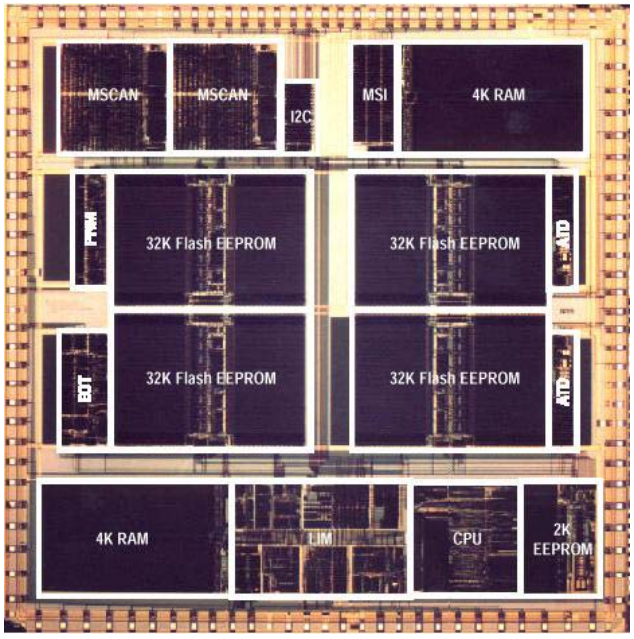


Figure 1-6: Bird's view of a micro-controller die (Courtesy of Motorola Semiconductors)

The layout aspect of the die of an industrial micro-controller is shown in figure 1-6 [Motorola]. This circuit is fabricated in several millions of samples for automotive applications. The micro-controller core is the central process unit (CPU), which uses several types of memory: the Electrically erasable Read-Only Memory (EEPROM), the FLASH memory (Rapidaly erasable Read-Only Memory) and the RAM memory (Random Access Memory). Some controllers are also embedded in the same die: the Control Area Network (MSCAN), the debug interface (MSI), and other functionnal cores (ATD, ETD <Etienne: ask for details to Motorola>).

2. THE DEVICE SCALE DOWN

We consider four main generations of integrated circuit technologies: micron, submicron, deep submicron and ultra deep submicron technologies., as illustrated in figure 1-7. The sub-micron era started in 1990 with the 0.8µm technology. The deep submicron technology started in 1995 with the introduction of lithography better than 0.3µm. Ultra deep submicron technology concerns lithography below 0.1µm. In figure 1-7, it is shown that research has always kept around 5 years ahead of mass production. It can also be seen that the trend towards smaller dimensions has been accelerated since 1996. In 2007, the lithography is expected to decrease down to 0.07µm. The lithography expressed in µm corresponds to the smallest patterns that can be implemented on the surface of the integrated circuit.

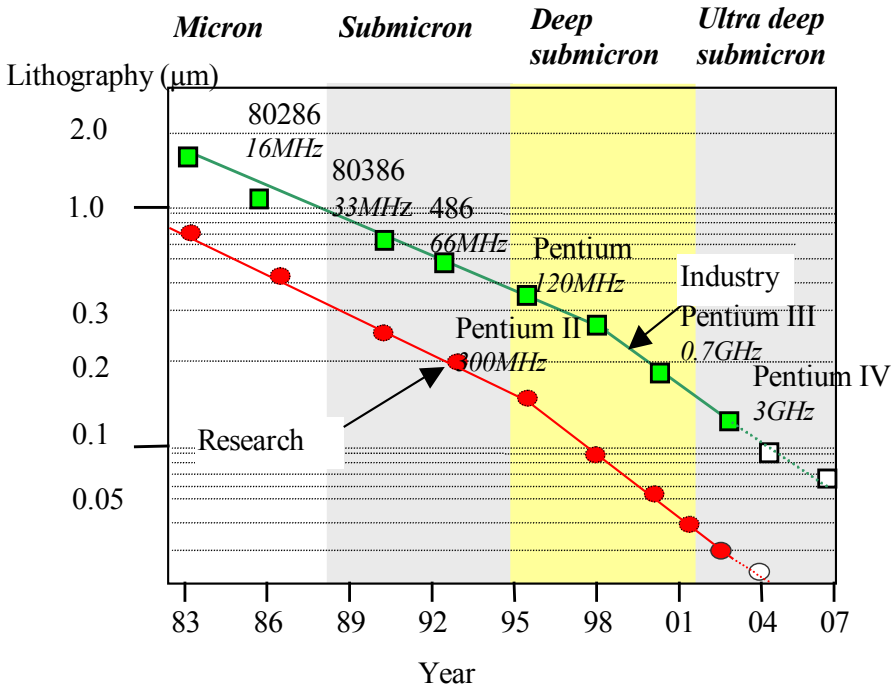


Figure 1-7: Evolution of lithography

3. FREQUENCY IMPROVEMENT

Figure 1-8 illustrates the clock frequency increase for high-performance microprocessors and industrial micro-controllers with the technology scale down. The microprocessor roadmap is based on Intel processors used for personal computers [Intel], while the micro-controllers roadmap is based on Motorola micro-controllers [Motorola] used for high performance automotive industry applications. The PC industry requires microprocessors running at the highest frequencies, which entails very high power consumption (30 Watts for the Pentium IV generation). The automotive industry requires embedded controllers with more and more sophisticated on-chip functionalities, larger embedded memories and interfacing protocols. The operating frequency follows a similar trend to that of PC processors, but with a significant shift.

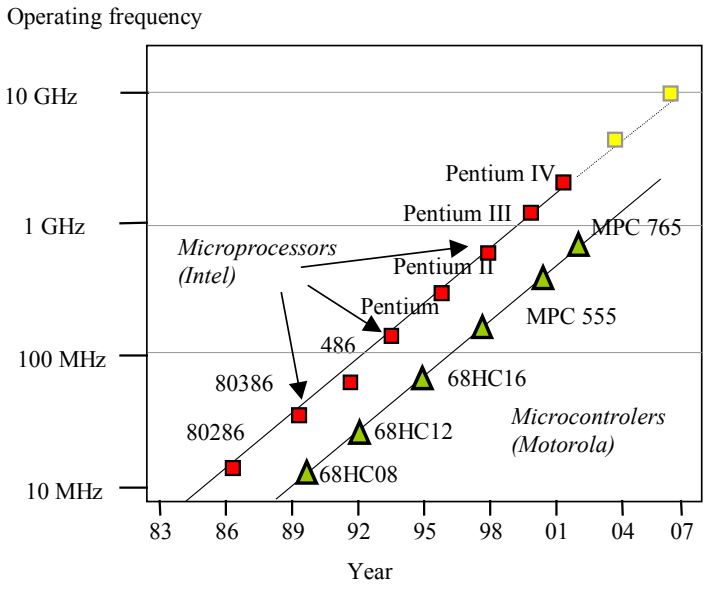


Figure 1-8: Increased operating frequency of microprocessors and micro-controllers

4. LAYERS

The table below lists a set of key parameters, and their evolution with the technology. Worth of interest is the increased number of metal interconnects, the reduction of the power supply VDD and the reduction of the gate oxide down to atomic scale values. Notice also the increase of the size of the die and the increasing number of input/output pads available on a single die.

Lithography	***Year***	***Metal layers***	***Core supply (V)***	***Core Oxide (nm)***	***Chip size (mm)***	***Input/output pads***	***Microwind2 rule file***
1.2µm	1986	2	5.0	25	5x5	250	Cmos12.rul

0.7µm	1988	2	5.0	20	7x7	350	Cmos08.rul
0.5µm	1992	3	3.3	12	10x10	600	Cmos06.rul
0.35µm	1994	5	3.3	7	15x15	800	Cmos035.rul
0.25µm	1996	6	2.5	5	17x17	1000	Cmos025.rul
0.18µm	1998	6	1.8	3	20x20	1500	Cmos018.rul
0.12µm	2001	6-8	1.2	2	22x20	1800	Cmos012.rul
90nm	2003	6-10	1.0	1.8	25x20	2000	Cmos90n.rul
65nm	2005	6-12	0.8	1.6	25x20	3000	Cmos70n.rul

Table 1-1: Evolution of key parameters with the technology scale down [ITRS]

The 1.2µm CMOS process features n-channel and p-channel MOS devices with a minimum channel length of 0.8µm. The Microwind tool may be configured in CMOS 1.2µm technology using the command **File→ Select Foundry**, and choosing **cmos12.rul** in the list. Metal interconnects are 2µm wide. The MOS diffusions are around 1µm deep. The two dimensional aspect of this technology is shown in figure 1-9.

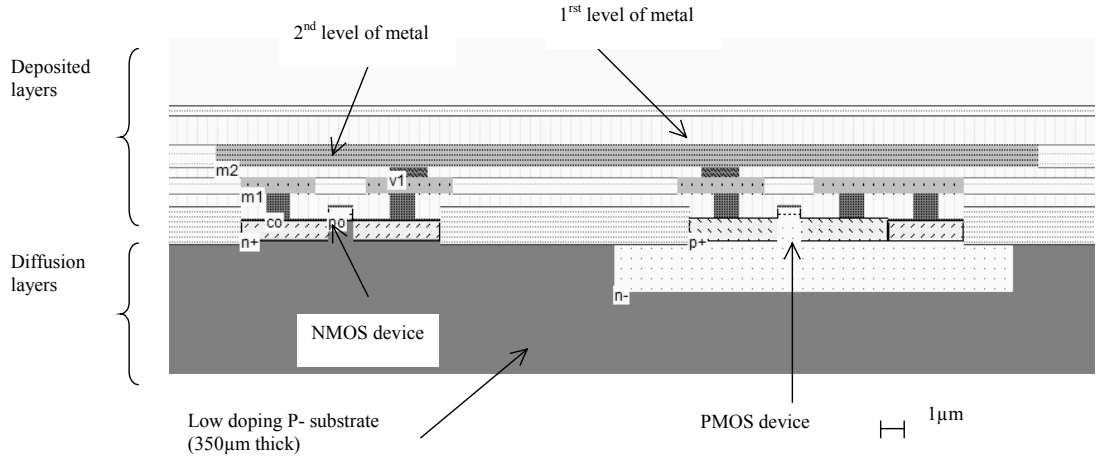


Figure 1-9: Cross-section of the 1.2µm CMOS technology (CMOS.MSK)

The 0.35µm CMOS technology is a five-metal layer process with a minimal MOS device length of 0.35µm. The MOS device includes lateral drain diffusions, with shallow trench oxide isolations. The Microwind tool may be configured in CMOS 0.35µm technology using the command **File→ Select Foundry**, and choosing "cmos035.rul" in the list. Metal interconnects are less than 1µm wide. The MOS diffusions are less than 0.5µm deep. The two dimensional aspect of this technology is shown in figure 1-10, using the layout **INV3.MSK**.

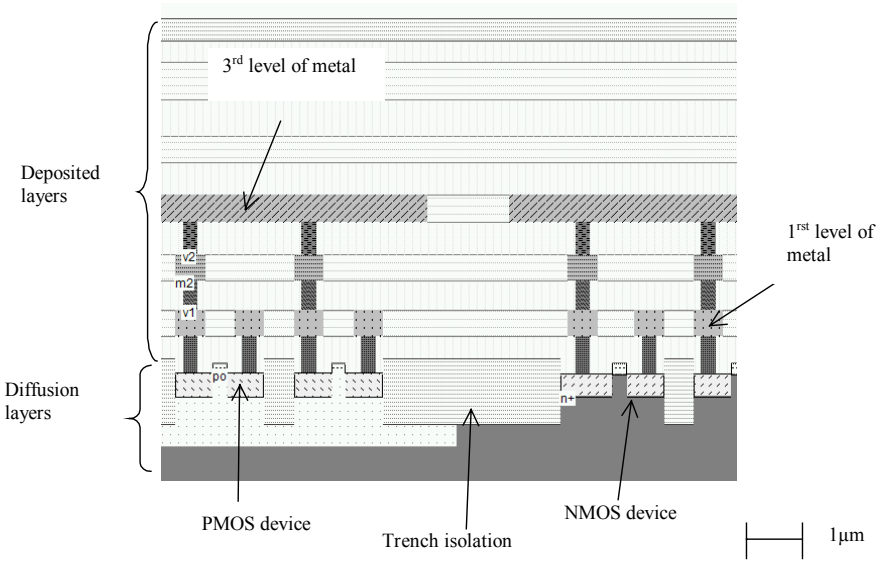


Figure 1-10: Cross-section of the 0.35µm CMOS technology (INV3.MSK)

The Microwind and Dsch tools are configured by default in a CMOS 0.12µm six-metal layer process with a minimal MOS device length of 0.12µm. The metal interconnects are very narrow, around 0.2µm, separated by 0.2µm (Figure 1-11). The MOS device appears very small, below the stacked layers of metal sandwiched between oxides.

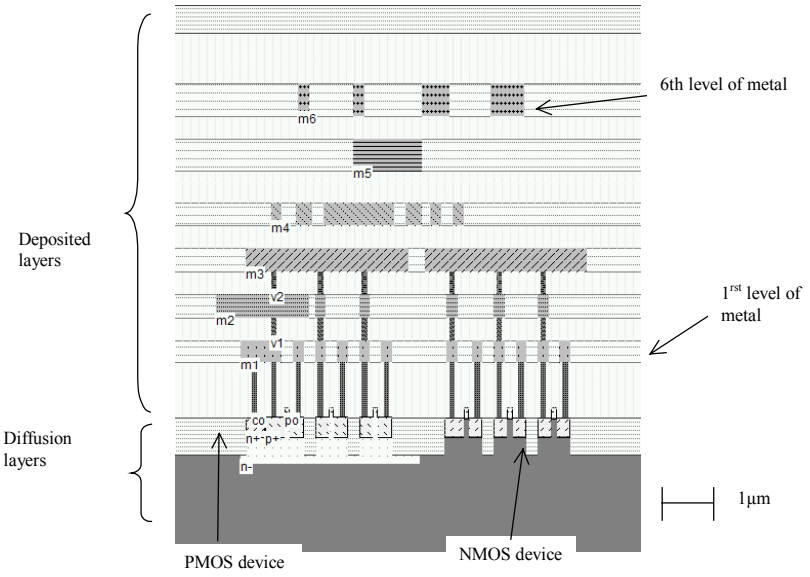


Figure 1-11: 2D View of the 0.12µm process

5. DENSITY

The main consequence of improved lithography is the ability to implement an identical function in an ever smaller silicon area. Consequently, more functions can be integrated in the same space. Moreover, the number

of metal layers used for interconnects has been continuously increasing in the course of the past ten years. More layers for routing means a more efficient use of the silicon surface, as for printed circuit boards. Active areas, i.e MOS devices can be placed closer to each other if many routing layers are provided (Figure 1-12).

The increased density provides two significant improvements: the reduction of the silicon area goes together with a decrease of parasitic capacitance of junctions and interconnects, thus increasing the switching speed of cells. Secondly, the shorter dimensions of the device itself speeds up the switching, which leads to further operating clock improvements.

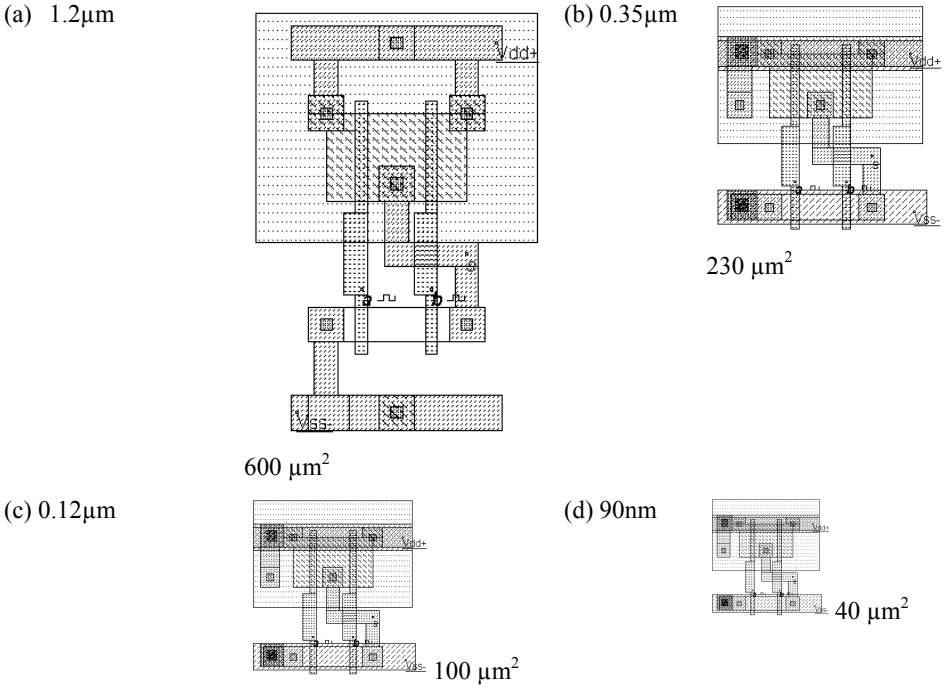


Figure 1-12: The evolution of the silicon area used to implement a NAND gate, which represents 20% of logic gates used in application specific integrated circuits

Meanwhile, the silicon wafer, on which the chips are manufactured, has constantly increased in size, with the technological advances. A larger diameter means more chips fabricated at the same time, but requires ultra-high cost equipments able to manipulate and process these wafers with an atomic-scale precision. This trend is illustrated in figure 1-13. The wafer diameter for 0.12µm technology is 8 inches or 20cm (One inch is equal to 2.54 cm). Twelve inches wafers (30cm) have been introduced for the 90nm technology generation. The thickness of the wafer varies from 300 to 600µm.

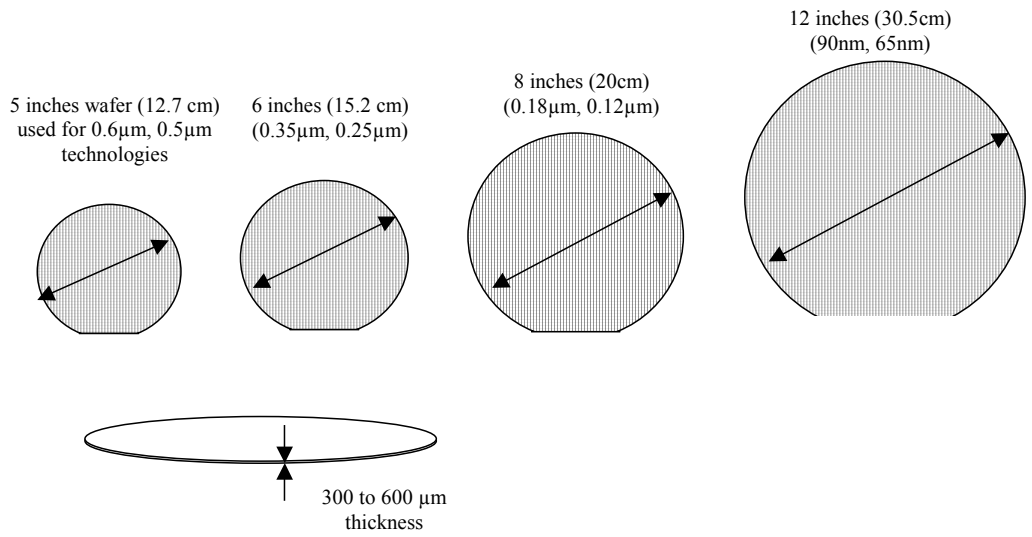


Figure 1-13: The silicon wafer used for patterning the integrated circuits

6. Design Trends

Originally, integrated circuits were designed at layout level, with the help of logic design tools, to achieve design complexities of around 10,000 transistors. The Microwind layout tool works at the lowest level of design, while DSCH operates at logic level.

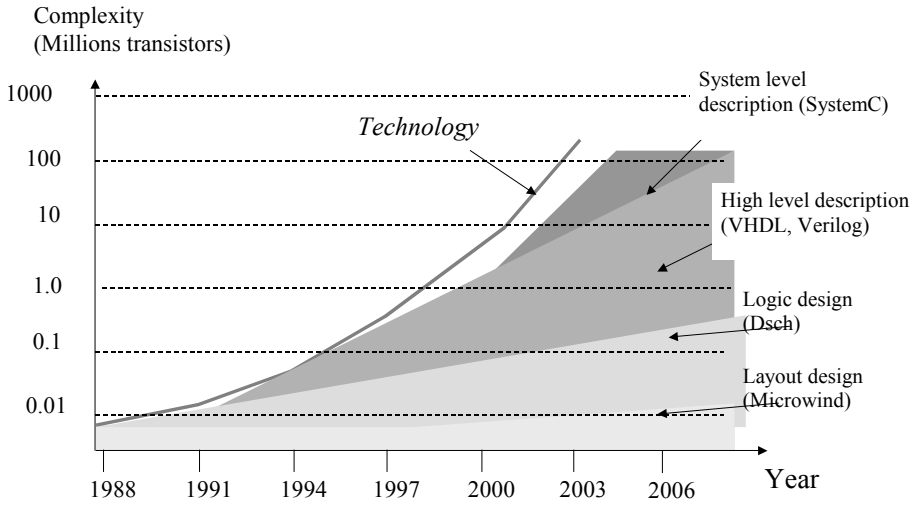


Figure 1-14: The evolution of integrated circuit design techniques, from layout level to system level

The introduction of high level description languages such as VHDL and Verilog [Verilog] have made possible the design of complete systems on a chip (SoC), with complexities ranging from 1million to 10 million transistors (Figure 1-14). Recently, languages for specifying circuit behavior such as SystemC [SystemC] have been made available, which correspond to design complexity between 100 and 1000 million transistors. Notice

that the technology has always been ahead of design capabilities, thanks to tremendous advances in process integration and circuit performances.

7. Market

Since the early days of microelectronics, the market has grown exponentially, representing more than 100 billion € in the beginning of the 21st century. The average growth in a long term trend is approximately 15%. Recently, two periods of negative growth have been observed: one in 1997-1999, the second one in 2002. Cycles of very high profits (1993-1995) have been followed by violent recession periods.

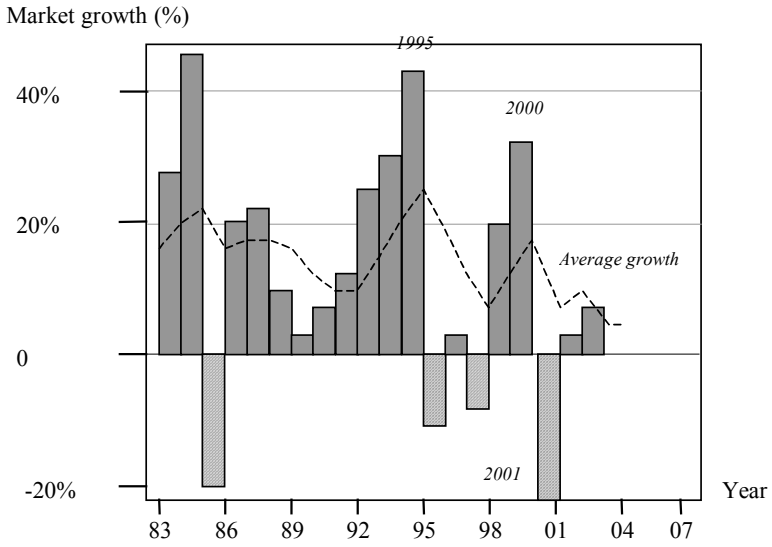


Figure 1-15: The percentage of market growth over the recent years shows a long term growth of 15%

Conclusion

This chapter has briefly illustrated the technology scale down, the evolution of the microprocessor and micro-controller complexity, as well as some general information about CMOS technology, trends and market. The position of the Microwind layout design tool and Dsch logic design tool has been also described.

References

[Moore] G.E Moore, "VLSI: some fundamental challenges", IEEE Spectrum, N° 16 Vol 4, pp 30, 1975

[SIA] <add web site>

[Verilog] <add ref>

[VHDL] <add ref>

[SystemC] <add ref>

[Intel] <add link>
[Motorola] <add link micro-controller division>
[ITRS] <add link>
[Itoh] K. Itoh "VLSI Memory Chip Design" Springler-Verlag, 2001

EXERCISES

1. Plot the frequency improvement versus the technology for the CMOSxx technology family, using the 3-inverter ring oscillator. Can you guess the performances of the 35nm technology?

2. Does the 3-inverter frequency performance represent the microprocessor frequency correctly? Use date of figure 1-3 to build your answer.

3. From the 2D comparative aspect of 0.8µm and 0.25µm technologies (Figure 6), what may be the rising problems of using multiple metallization layers?

4. With the technology scale down, the silicon area decreases for the same device (see figure 1.8), but the chip size increases (table 1.1). Can you explain this contradiction?

Partial answers are provided in Appendix F.