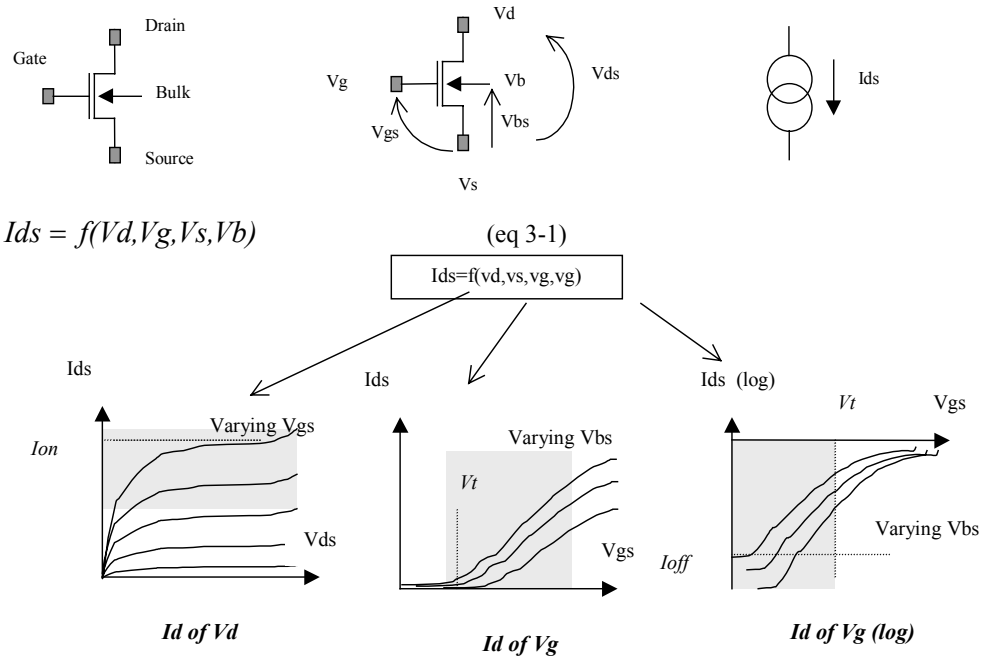
3 The MOS modeling

This chapter introduces the CMOS transistor modeling. The static characteristics of n-channel and p-channel MOS devices are shown, with details on the maximum current and its relationship with the sizing, the threshold voltage and various 2nd order effects. Three generations of MOS device models are introduced. Firstly, the original MOS model 1 is presented, as it was proposed in the early versions of SPICE simulator developed by the University of Berkeley, California. We demonstrate the inaccuracies of this model. Secondly, we introduce the semi-empirical model 3, which is still in use for MOS device simulation with a channel length greater than 1µm. Thirdly, we present a simplified version of the BSMI4 models, developed by the University of Berkeley for MOS devices with channel length down to 90nm.
Details on model parameters are provided for all models. The effects of temperature on the MOS performances are then presented. Finally, the three different MOS that may be found in 0.12µm are introduced: low threshold voltage, high speed and high voltage.

1. Introduction to modeling

Modeling the MOS device consists in writing a set of equations that link voltages and currents, in order to simulate and predict the behavior of the single device [Shockley] and consequently the behavior of a complete circuit. A considerable research and development effort has been dedicated in the past years to modeling MOS devices in an accurate way. Many books have been published over the years about the semiconductor physics and semiconductor device modeling. The most common references are [Tsividis], [Sze], [Lee] and recently [Liu]. For MOS devices, one of the key objectives of the model is to evaluate the current Ids which flows between the drain and the source, depending on the supply voltages Vd,Vg,Vs and Vb.



$$Ids = f(Vd,Vg,Vs,Vb) \qquad \text{(eq 3-1)}$$

Figure 3-1: Useful representations of the MOS device characteristics

From the equation (3-1), we may represent the variation of the current *Ids* versus voltages in three different ways, as illustrated in figure 3-1. The graphs are usually called *Id/Vd*, *Id/Vg*, and *Id(log)/Vg*. For simplicity's sake, we consider that the voltage *Vs* is grounded.

In the *Id/Vd* curve, the current Ids is plotted for varying gate voltage *Vgs*, from 0 to VDD. The parameter *Ion* gives the maximum available current, corresponding to maximum voltage *Vds* and *Vgs*. *Ion* is a very important parameter for signal switching, for example in logic gates.

In the *Id/Vg* curve, we extract the threshold voltage. In the previous chapter we observed the parasitic effects due to this threshold. Analog design is much concerned by an accurate prediction of the threshold voltage.

Then, the curve *Id(log)/Vg* is convenient to illustrate the current *Ids* for small values of the gate control. One of the most important parameters is the Ioff current, when *Vg*=0, that has a direct impact on standby power consumption.

A second objective of MOS models is to estimate the value of parasitic capacitances, mainly *Cgs, Cgd* and *Cgb* (Figure 3-2). Those capacitance prove to vary with the voltage *Vs,Vd,Vg* and *Vb*. Although not considered in the static simulations *Id/Vd* and *Id/Vg*, the variation of the capacitance must be computed at each iteration of the analog simulation, for accurate prediction of the switching delay.

$$Cgs = f_1(Vd,Vg,Vs,Vb) \qquad \text{(eq 3-2)}$$

$$Cgd = f_2(Vd,Vg,Vs,Vb) \qquad \text{(eq 3-3)}$$

$$Cgb = f3(Vd,Vg,Vs,Vb) \qquad \text{(eq 3-4)}$$

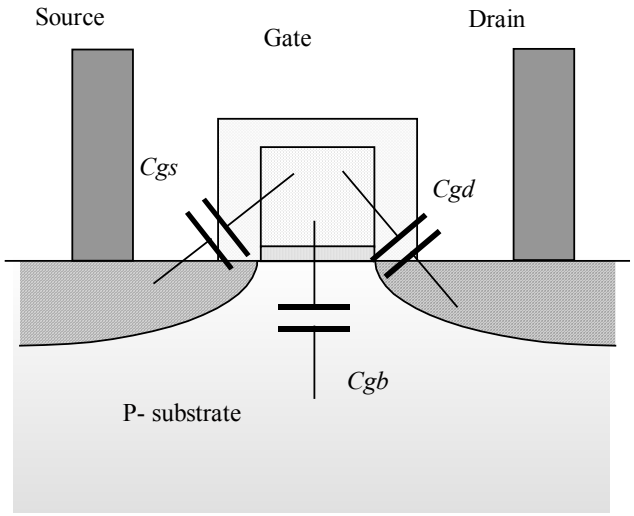


Figure 3-2: Capacitance between the gate and the source, drain, or substrate

A long list of MOS models have been developed for analog simulators. We choose to implement in Microwind2 three of those: the model 1, the model 3 and the model BSIM4. Details on those three models and their physical basis are provided in the next paragraphs.

The complete set of parameters for a given technology is called the model card. The procedure to build an accurate MOS model is quite complex, as it is based on a large set of measurements and sophisticated optimization procedures. The experimental data concerning a MOS device with large width and large length is used first, to fix basic parameters. Then the MOS model is tuned for small channel device measurements, and then for several sizes.

2. MOS Model 1

Equations

Historically, the MOS model 1 was the first to be proposed by Shockley, in 1952 [Shockley]. The equations of the MOS level 1 are provided in the next paragraphs. The evaluation of the current **Ids** between the drain and the source as a function of *Vd,Vg* and *Vs* is summarized in equations 3-5,3-6 and 3-7. The model parameters appearing in the user interface of Microwind2 are written using `COURRIER` font. The device operation is divided into three regions: cut-off, linear and saturated.

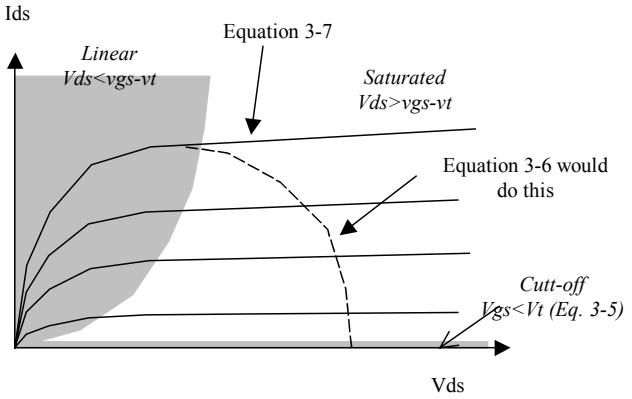


Figure 3-3: Two main domains are considered in the model: the linear area and the saturated area.

IF V_{gs}<0, the device is in cut-off mode.

$$Ids = 0 \tag{3-5}$$

IF V_{ds}<V_{gs}-VTO, the device is in linear mode

$$Ids = \mathrm{UO}\frac{\varepsilon_0\varepsilon_r}{\mathrm{TOX}}\cdot\frac{\mathrm{W}}{\mathrm{L}}((V_{gs}-vt).V_{ds}-\frac{(V_{ds})^2}{2})) \tag{3-6}$$

IF V_{ds}>V_{gs}-VTO, the device is in saturated mode:

$$Ids = \mathrm{UO}\frac{\varepsilon_0\varepsilon_r}{\mathrm{TOX}}\cdot\frac{\mathrm{W}}{\mathrm{L}}(V_{gs}-vt)^2 \tag{3-7}$$

With:

$$vt = \mathrm{VTO} + \mathrm{GAMMA}(\sqrt{(\mathrm{PHI}-vbs)}-\sqrt{\mathrm{PHI}}) \tag{3-8}$$

ε_0 = 8.85 10^{-12} F/m is the absolute permittivity

ε_r = relative permittivity, equal to 3.9 in the case of SiO2 (no unit)

Mos Model 1 parameters			
Parameter	Definition	Typical Value 0.12µm NMOS	PMOS
VTO	Theshold voltage	0.4V	-0.4V
U0	Carrier mobility	0.06m^2/V-s	0.02m^2/V-s
TOX	Gate oxide thickness	2nm	2nm
PHI	Surface potential at strong inversion	0.3V	0.3V
GAMMA	Bulk threshold parameter	0.4 $V^{0.5}$	0.4 $V^{0.5}$
W	MOS channel width	1µm	1µm
L	MOS channel length	0.12µm	0.12µm

Table 3-1: Parameters of MOS level 1 implemented into Microwind2

Implementation in Microwind

The static characteristics of the MOS model 1 may be obtained using the command **Simulate → Mos characteristics** available in the main menu of Microwind.

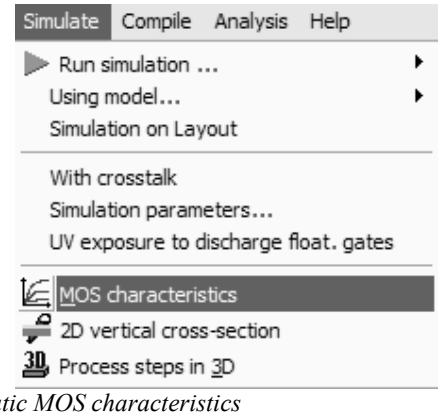


Figure 3-4: Access to the static MOS characteristics

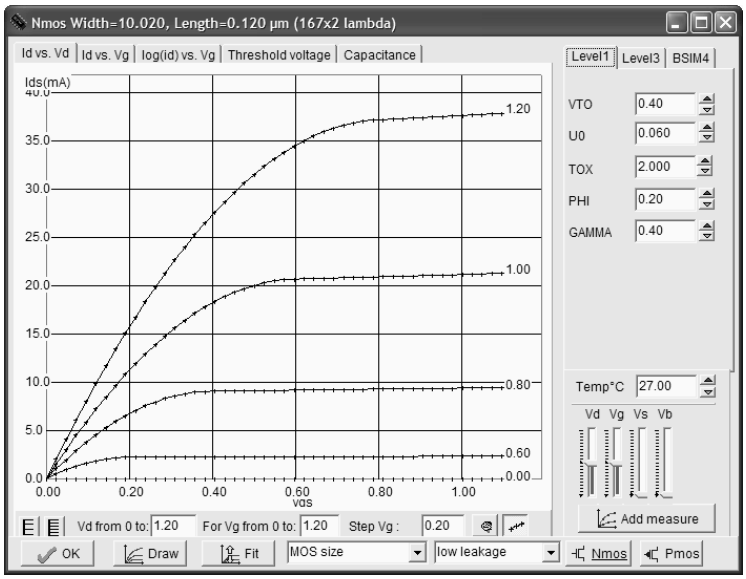


Figure 3-5: The screen used to simulate the static characteristics of the MOS with model 1 within Microwind2

In the top right part of the window, select the item "Level 1". The variation of *Ids* versus the voltage *Vds*, for varying gate voltage *Vgs*, is shown by default. The device width is 10µm by default, the channel length is 0.12µm. The parameters `VTO, U0, TOX`, `PHI` and `GAMMA` are listed in the right part of the window.

Mismatch between simulation and measurements

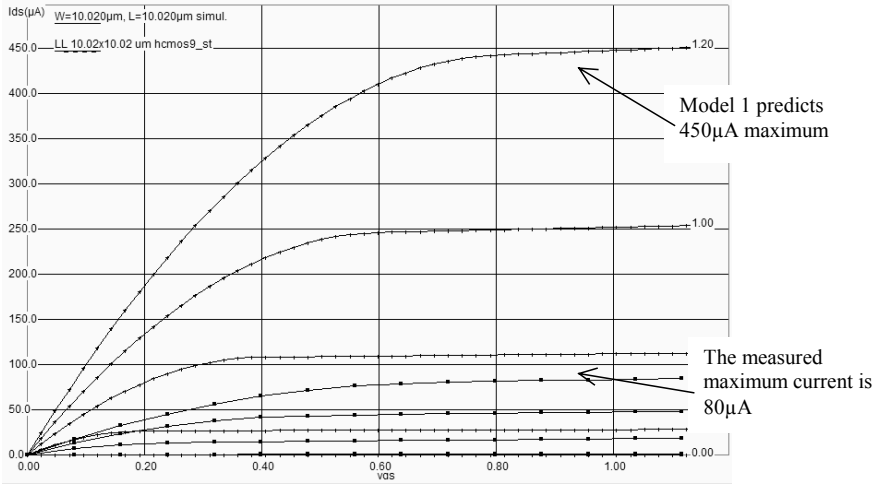


Figure 3-6: The model 1 predict a current 5 times higher than the measurement in the case of a large channel MOS device (L=10µm).

These old equations (1968, in [Shichman]) are not acceptable in 0.12µm. If we consider MOS devices with very long lengths (L>10µm), the mismatch between the simulation and the measurement is of the order of a factor of five. Let us compare the simulation and the measurement, for a device with a width W=10µm, and a long channel length L=10µm, fabricated in 0.12µm CMOS technology, as presented in figure 3-6. The measurement *Ne10x10.MES* was downloaded using the button **Load Measurement**. This measurement corresponds to an n-channel MOS device with a 10µm channel width and 10µm length, fabricated in CMOS 0.12µm from ST-microelectronics.

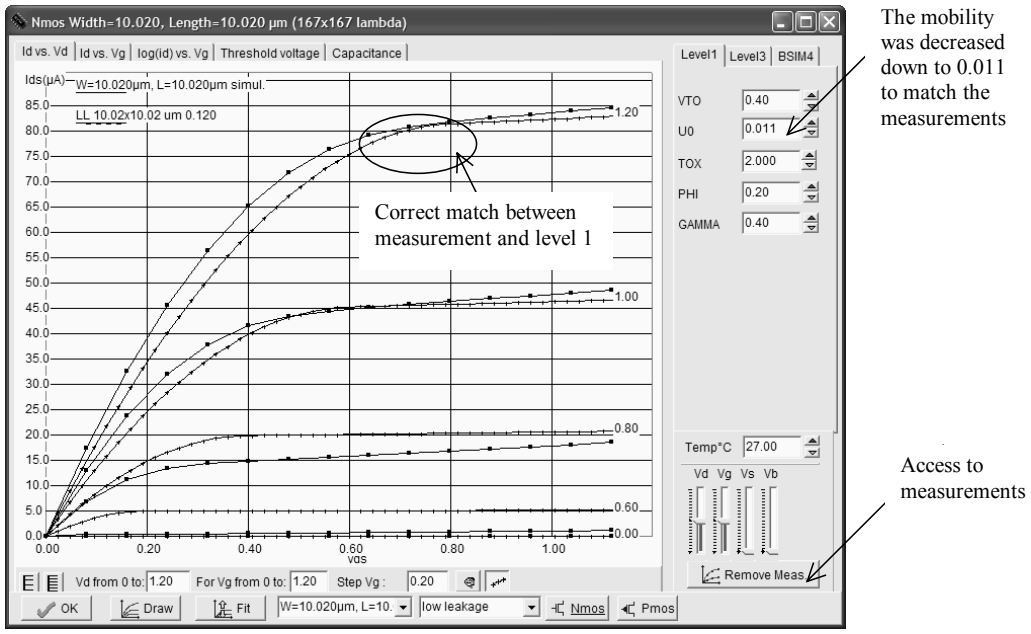


Figure 3-7: Comparing measured Id/Vd and level 1 simulations for a 10x10µm device result in a surprising similarity (Ne10x10.MES).

Initially, the simulation and measurement do not correspond at all. The mobility `U0` needs to be decreased from its initial value 0.06 down to 0.01. The curves are fitted at the price of an unrealistic change in the mobility parameter.

When dealing with sub-micron technology, the current predicted by model "Level 1" is several times higher than the real-case measurements. This means that several parasitic effects appeared with the technology scale down, most of them tending to reduce the effective current compared to the early modeling equations of model 1.

3. MOS Model 3

For the evaluation of the current *Ids* as a function of *Vd,Vg* and *Vs* between drain and source, we commonly use the following equations, close to SPICE model 3 formulations. The formulations are derived from model 1 and take into account a set of physical limitations in a semi-empirical way.

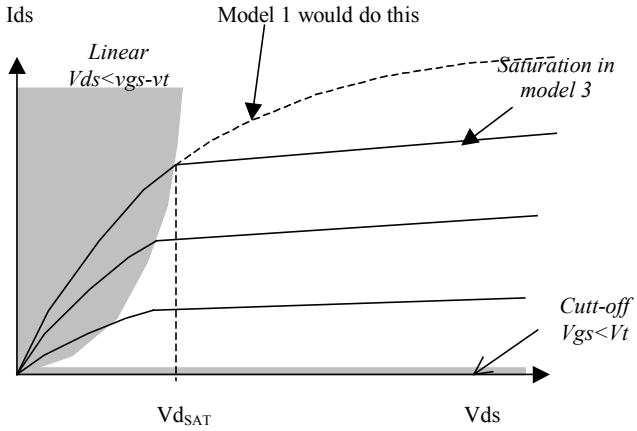


Figure 3-8: Introduction of the saturation voltage VdSat which truncates the equations issued from model 1

One of the most important change is the introduction of Vd_{SAT}, a saturation voltage from which the current saturates and do not rise as the LEVEL1 model would do. This saturation effect is significant for small channel length. The main LEVEL3 equations are listed below.

CUT-OFF MODE. Vgs<0

$$Ids = 0 \qquad (3\text{-}9)$$

NORMAL MODE. Vgs>Von

$$Ids = Keff \frac{\mathtt{W}}{Leff}(1 + \mathtt{KAPPA}.Vds)Vde((Vgs - Vth) - \frac{Vde}{2}) \qquad (3\text{-}10)$$

with

$$Von = 1.2Vth$$
$$Vth = \mathtt{VTO} + \mathtt{GAMMA}(\sqrt{\mathtt{PHI} - Vbs} - \sqrt{\mathtt{PHI}})$$
$$Vde = min(Vds, Vdsat)$$
$$Vdsat = Vc + Vsat - \sqrt{Vc^2 + Vsat^2}$$
$$Vdsat = Vgs - Vth$$
$$Vc = \mathtt{VMAX}\frac{Leff}{0.06}$$
$$Leff = L - 2LD$$

The formulation of the effective factor *Keff* (Equation 3-11) includes a mobility degradation factor THETA, which tends to reduce the mobility at high *Vgs*. The consequence is a reduction of the current Ids as compared to LEVEL1.

$$Keff = \frac{\varepsilon_0 \varepsilon_r}{TOX} \frac{UO}{(1 + THETA(vgs - vth))} \qquad (3\text{-}11)$$

In sub-threshold mode, that is for a gate voltage less than the threshold voltage, *Vds* is replaced by *Von* in the above equations. An exponential dependence of the current with *Vgs* is introduced by using the equation 3-12. Notice the temperature effect introduced in the denominator *nkT*.

Without any voltage applied to the gate, the current is no more equal to zero. The current of *Ids* for *Vgs*=0 is called the *Ioff* current (Figure 3-9). Its value in 0.12µm is around 10^{-10} A. In contrast, for *Vgs*=VDD, the maximum current *Ion* is of the order of several mA (10^{-3} A).

$$Ids = Ids(Von, Vds) exp(\frac{q(Vgs - Von)}{nkT}) \qquad (3\text{-}12)$$

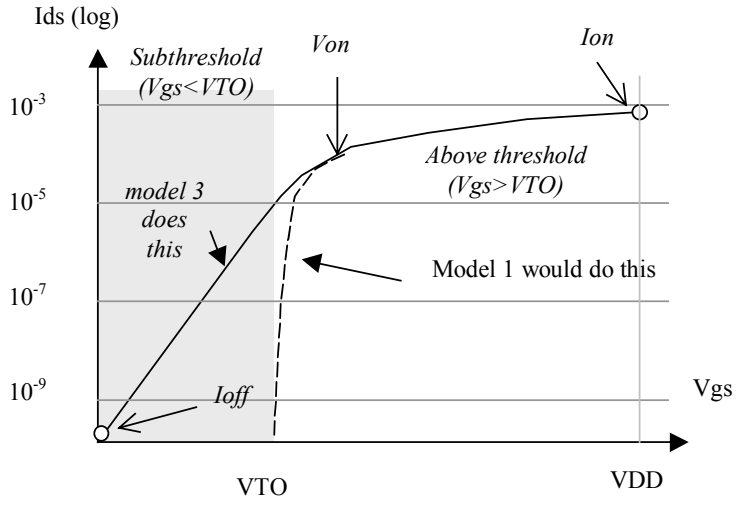


Figure 3-9: Introduction of an exponential law to model the sub-threshold behavior of the current

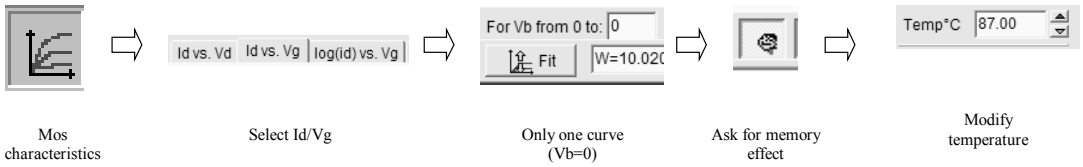
TEMPERATURE EFFECTS

The MOS device is sensitive to temperature. Three main parameters are concerned: the threshold voltage VTO, the mobility U0 and the slope in sub-threshold mode dependent on *kT/q*. Both VTO and U0 decrease when the temperature increases . The physical background is the degradation of the mobility of electrons

and holes when the temperature increase, due to a higher atomic volume of the crystal underneath the gate, and consequently less space for the current carriers. The modeling of the temperature effect is as follows:

$$U0 = U0_{(T=27)}\left(\frac{T+273}{300}\right)^{-1.5} \qquad \text{(eq. 3-13)}$$

$$VT = VT0_{(T=27)} - 0.002(T-300) \qquad \text{(eq. 3-14)}$$



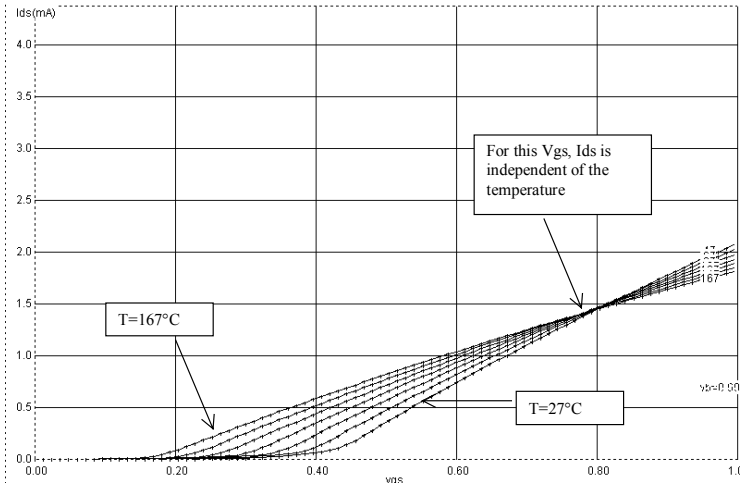


Figure 3-10 The effect of temperature on the MOS characteristics. In Id/Vg mode, a specific Vds makes the current independent of the temperature.

To obtain the curve of figure 3-10, click the icon MOS characteristics, select the curve *Id/Vg*, and enter the value "0" for the upper limit of *Vb*, so as to draw only one single curve. Enable the screen memory mode by a click on the icon **Enable Memory**. When you change the temperature, the change in the slope and the temperature-independent point appear, as shown in figure 3-10.

Mos Model 3 parameters			
Parameter	Definition	Typical Value 0.12µm NMOS	pMOS
VTO	Theshold voltage of a long channel device, at zero Vbs.	0.4V	-0.4V
U0	Carrier mobility	0.06 m^2/V.s	0.025 m^2/V.s
TOX	Gate oxide thickness	3 nm	3 nm
PHI	Surface potential at strong inversion	0.3V	0.3V

LD	Lateral diffusion into channel	0.01µm	0.01µm
GAMMA	Bulk threshold parameter	0.4 $V^{0.5}$	0.4 $V^{0.5}$
KAPPA	Saturation field factor	0.01 V^{-1}	0.01 V^{-1}
VMAX	Maximum drift velocity	150Km/s	100Km/s
THETA	Mobility degradation factor	0.3 V^{-1}	0.3 V^{-1}
NSS	Substhreshold factor	0.07 V^{-1}	0.07 V^{-1}
W	MOS channel width	0.5-20µm	0.5-40µm
L	MOS channel length	0.12µm	0.12µm

Table 3-xxx: list of parameters used in the implementation of the LEVEL3 model in Microwind2

Microwind User's Interface

You may understand the action of each parameter by using the screen reported in figure 3-11. Each parameter may be changed interactively using cursors, or by entering with the keyboard the appropriate value.

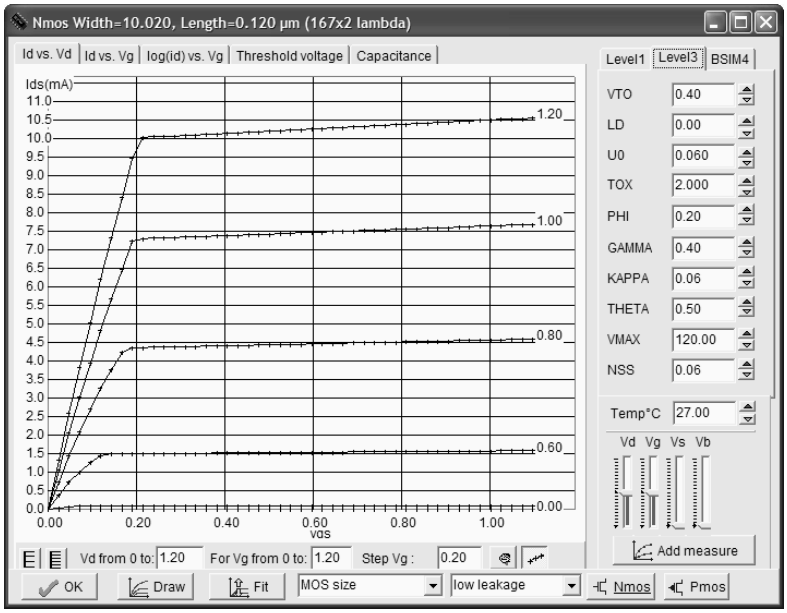


Fig. 3-11. The user interface to investigate the effect of each parameter on the current Ids (W=10µm, L=0.12µm)

Several screens may be proposed:

- *Id vs. Vd*, for varying *Vg*. This is the default screen. Its main interest is the characterization of the Ion current, the maximum current available in the device, for *Vd* and *Vg* set to VDD.
- *Id vs. Vg*, for varying *Vb*. In this screen, the threshold voltage *Vt* (VTO) is characterized, as well as its dependence on the bulk polarization.
- *Id vs. Vg*, in logarithmic scale. This screen is mandatory to characterize the MOS device in sub-threshold mode, that is for *Vgs<Vt*. Two of the important parameters are the slope of the current vs.

Vgs, and the *Ioff* current. The *Ioff* current is the standby current appearing between drain and source for *Vgs*=0.

- Threshold voltage *Vt vs. Length*. This screen has been added to illustrate advances in the modeling of deep-submicron effects. With LEVEL 3, *Vt* is constant for varying length, but is impacted by the bulk voltage.
- *Capacitance vs. Vds*. This screen illustrates the variation of *Cgs* and *Cgd* versus the drain-source voltage.

Current versus drain-source voltage

Using the display mode **Id vs. Vd,** you may see the effect of parameters `U0`, `TOX`, `KAPPA` and `VMAX`. Basically, the carrier mobility `U0` moves the whole curve, as it impacts the current *Ids* in an almost linear way. As `U0` is nearly a physical constant, a significant change of mobility has no physical meaning. The oxide thickness `TOX` does the same but in an opposite way.

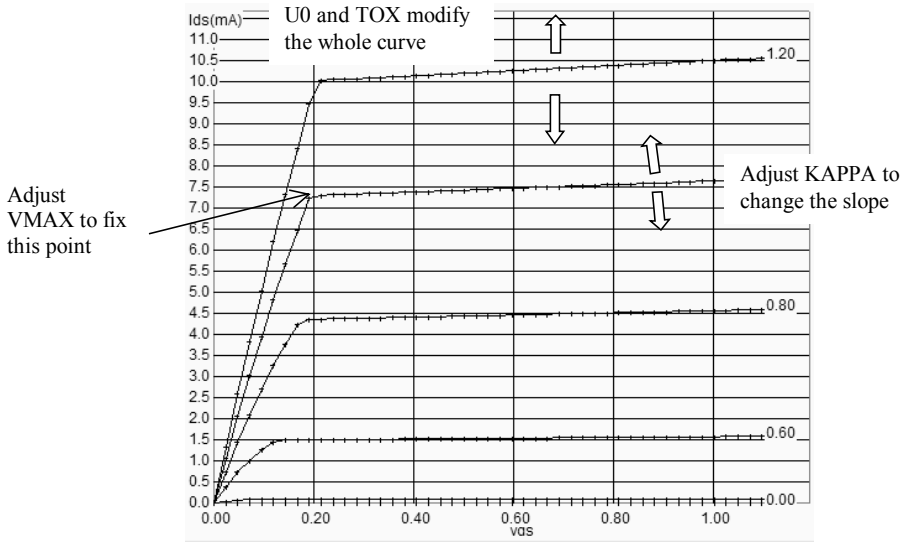


Fig. 3-12. Demonstration of the role of U0, KAPPA and VMAX in Id./Vd (W=10µm, L=0.12µm)

A `TOX` increase leads to a less efficient device, with less current. `KAPPA` changes the slope of the current when *Vds* is high, corresponding to the saturation region. Finally, `VMAX` truncates the curves for low values of *Vds*, to fit the transition point between the linear and the saturated region (Figure 3-12).

Current versus gate voltage

The role of VTO and GAMMA can be observed in the figure 3-13, using the display mode **Id vs. Vg**. If we use a long channel device, that is a length much greater than the minimum length, the second order effects are minimized. Act on VTO cursors in order to shift the curves right or left, and GAMMA to fit the spacing between curves. Parameters U0 and TOX also have a direct impact on the slope for high *Vgs*.

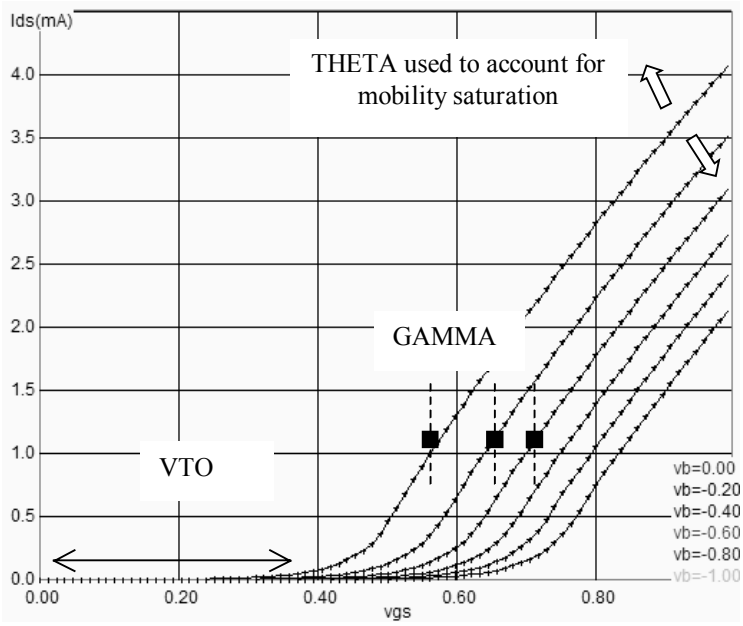


Fig. 3-13. The effects of VTO and GAMMA are illustrated in Id/Vg mode voltage (W=10µm, L=0.12µm)

Now we focus on a short channel MOS device, for example W=2µm, L=0.12µm. Using the same display mode **Id vs. Vg**, we obtain similar curves as for long-channel device. We observe that the shape of the current is bent. This modification is due to short channel parasitic effects. The parameter THETA is used to bend the current curves at high *Vgs*. The MOS model 3 do not provide parameters to account for the VTO dependence with length.

Current vs Vg in logarithmic scale

We finally illustrate the role of NSS in the display mode **Id(log)/Vg** (Figure 3-14). The parameter NSS has a direct impact on the slope in sub-threshold mode, that is for *Vgs*<*Vt*.

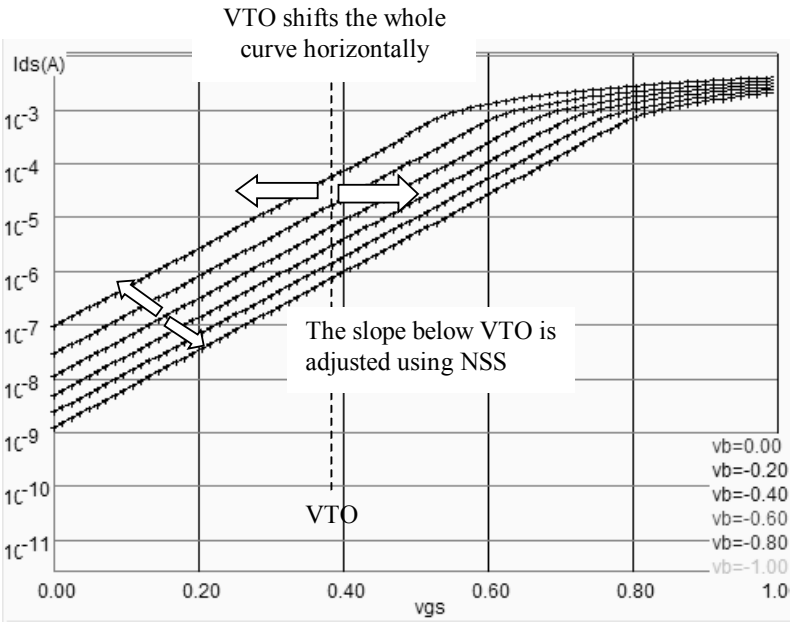


Figure 3-14. In sub-threshold region, the Id dependence on Vgs is exponential. The slope is tuned by parameter NSS. The whole curve is shifted using VTO voltage (W=10µm, L=0.12µm)

Capacitance vs. Vds

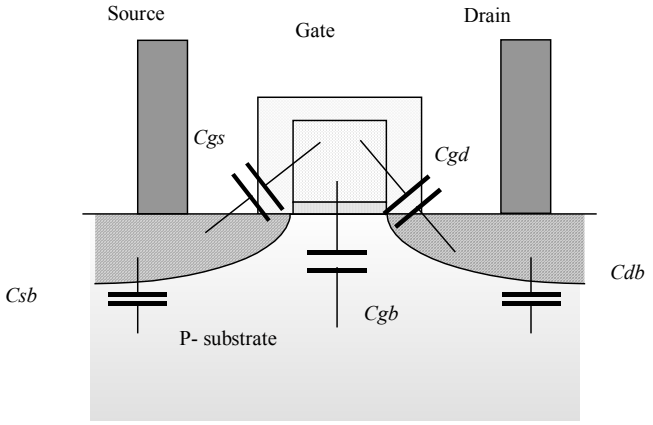


Figure 3-15: The MOS capacitance considered in MOS model 3

The five main capacitors considered in our implementation of MOS model 3 are the gate to bulk capacitance *Cgb*, the gate to source capacitance *Cgs*, the gate-to-drain capacitance *Cgd*, the junction capacitance between source and bulk *Csb* and the junction capacitance between drain and bulk *Cdb*.

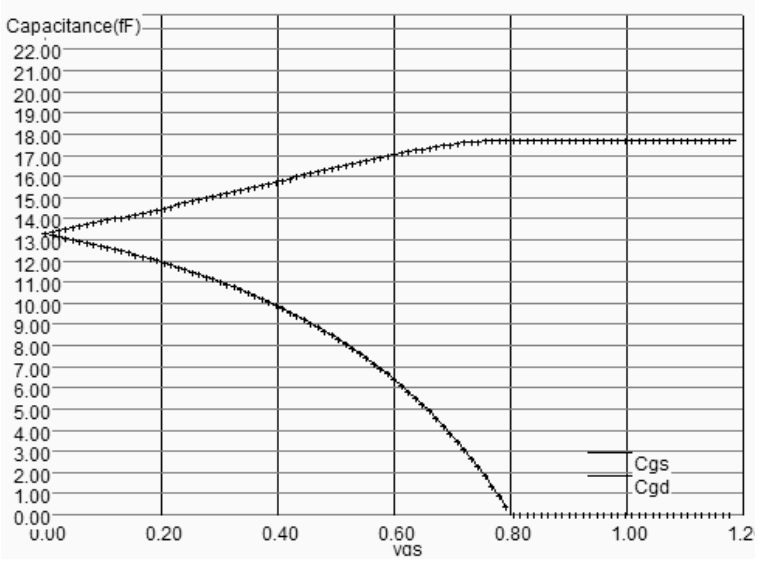


Figure 3-16: The evolution of MOS capacitance with the drain voltage (W=10µm, L=0.12µm)

The variation of the capacitance must be computed at each iteration of the analog simulation, for accurate prediction of the switching delay. In our implementation of MOS level 3, we use the following model, based on the formulations given in [Fjedly]. The parameter V_{dsat} was given by equation 3-10.

$$C_{GS} = \frac{2}{3} C_i \left[1 - \left(\frac{V_{GS} - V_t - V_{dsat}}{2(V_{GS} - V_t) - V_{dsat}} \right)^2 \right] \qquad (3\text{-}15)$$

$$C_{GD} = \frac{2}{3} C_i \left[1 - \left(\frac{V_{GS} - V_t}{2(V_{GS} - V_t) - V_{dsat}} \right)^2 \right] \qquad (3\text{-}16)$$

$$C_{GB} = 0 \qquad (3\text{-}17)$$

with

$$Ci = W.L.\frac{\varepsilon_0 \varepsilon_r}{\mathrm{TOX}} \qquad (3\text{-}18)$$

W = width of the MOS device (m)

L = length of the MOS device (m)

TOX = oxide thickness (m)

The two remaining capacitance C_{DB} and C_{SB} are junction capacitance. Their model is given by equations 3-19 and 3-20.

$$C_{DB} = W.L_{drain} \frac{\mathrm{CJ}}{\left(1 - \frac{V_{BD}}{\mathrm{PB}}\right)^{\mathrm{MJ}}} \qquad (3\text{-}19)$$

$$C_{SB} = W.L_{source}\frac{\mathrm{CJ}}{\left(1-\frac{V_{BS}}{\mathrm{PB}}\right)^{\mathrm{MJ}}} \qquad (3\text{-}20)$$

where

W is the channel width (m)

L_{drain} is the drain length, according to figure 3-17 (m)

CJ is around 3x10e-4 F/m2

PB is the built-in potential of the junction (around 0.8V)

MJ is the grading coefficient of the junction (around 0.5)

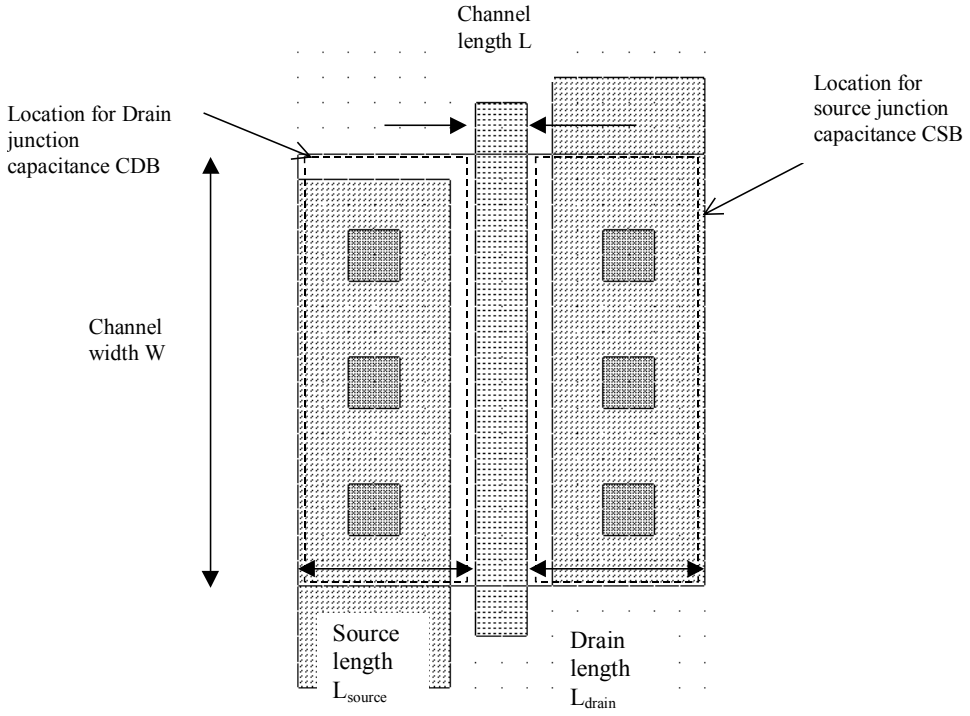


Figure 3-17: The junction capacitance for drain and source contributes significantly to the MOS capacitance

4. The BSIM4 MOS Model

A family of models has been developed at the University of Berkeley for the accurate simulation of sub-micron and deep submicron technologies. The Berkeley Short-channel IGFET Model (BSIM) exists in several versions (BSIM1, BSIM2, BSIM3). The BSIM3v3 version, promoted by the Electronic Industries Alliance (EIA) is an industry standard for deep-submicron device simulation [Eia].

A new MOS model, called BSIM4 [Bsim4], was introduced in 2000. A simplified version of this model is supported by Microwind2, and recommended for ultra-deep submicron technology simulation. The complete details on BSIM4 are provided in the excellent book [Liu]. BSIM4 still considers the operating regions described in MOS level 3 (linear for low *Vds*, saturated for high *Vds*, subthreshold for *Vgs<Vt*), but provides a perfect continuity between these regions. BSIM4 introduces a new region where the impact ionization effect is dominant (Figure 3-18). In that region, *Vds* is very high, over the nominal supply voltage VDD. One of the key features of BSIM4 is the use of one single equation to build the current, valid for all operating modes. Smoothing functions ensure a nice continuity between operating domains.

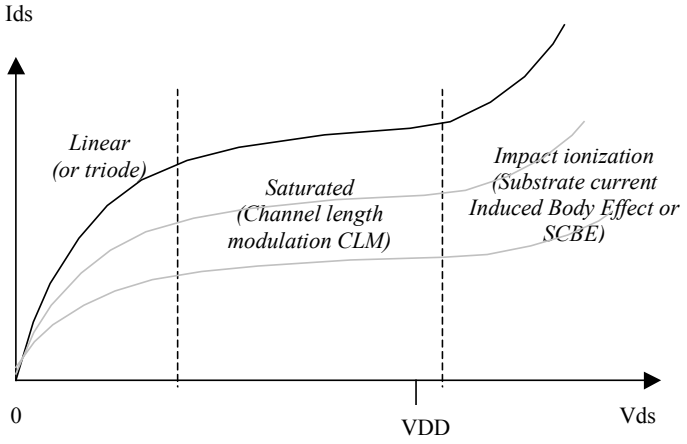


Figure 3-18: The three regions considered in our simplified version of BSIM4

The number of parameters specified in the official release of BSIM4 is as high as 300. A significant portion of these parameters is unused in our implementation. We concentrate on the most significant parameters, for educational purposes. The set of parameters is reduced to around 30.

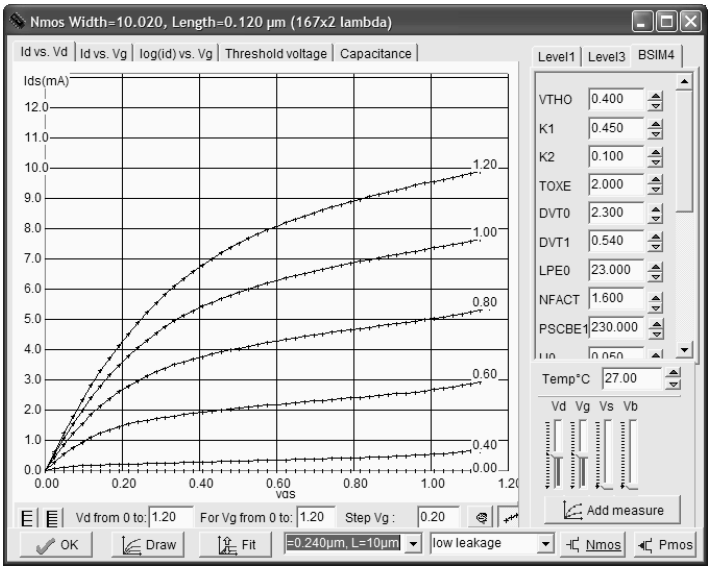


Figure 3-19: Implementation of BSIM4 within Microwind2, based on [Liu]

Effective Channel Length and Width

Once fabricated, the physical length L_{eff} and width W_{eff} of the MOS device do not correspond exactly to the initial length L and width W drawn using Microwind2 (Figure 3-20). The parameters `LINT` and `WINT` have been introduced for that purpose, with equations 3-21 and 3-22.

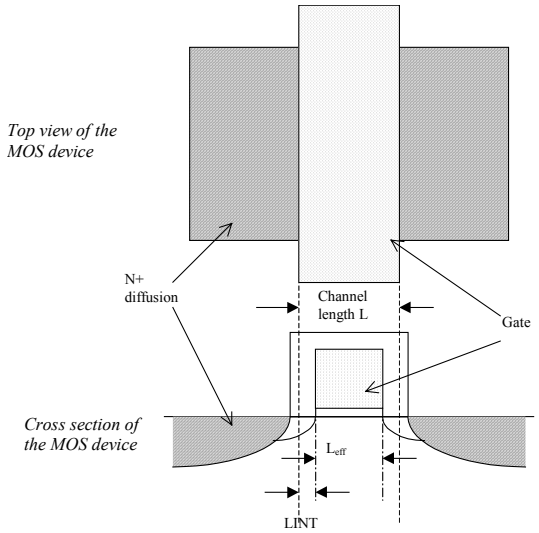


Figure 3-20: Illustration of the effective channel length Leff

$$Leff = L - 2.LINT \quad (3\text{-}21)$$

$$Weff = W - 2.WINT \quad (3\text{-}22)$$

Surface potential and junction depth

The surface potential Φs and junction depth are basic parameters taken into account in the evaluation of the threshold voltage and the global current. The surface potential Φs is defined by equation 3-23.

$$\Phi_s = 0.4 + vt.\ln(\frac{NDEP}{ni}) \quad (3\text{-}23)$$

where *vt* the thermal voltage given by equation 3-24, *NDEP* is the channel doping concentration for zero body bias (Around $10^{17}cm^{-3}$ in practice), and *ni* is the intrinsic carrier concentration of silicon (ni=1.02x$10^{10}cm^{-3}$ at 300°K). Consequently, the surface potential Φs in deep-submicron CMOS process is around 0.85V.

The thermal voltage is

$$vt = \frac{k_B T}{q} \quad (3\text{-}24)$$

k_B = Boldzmann constant = 1.38 x 10^{-23} J/K

T = temperature (300°K by default)

q = Electronic charge = 1.60 x 10^{-19} C

The built-in voltage of the source/drain junctions is given by equation 3-25.

$$V_{bi} = vt.\ln(\frac{NDEP.NSD}{ni^2}) \quad (3\text{-}25)$$

where *vt* the thermal voltage given by equation 3-24, *NDEP* is the channel doping concentration for zero body bias (Around $10^{17}cm^{-3}$ in practice), *NSD* is the source/drain doping concentration (Around $10^{20}cm^{-3}$ in practice), and *ni* is the intrinsic carrier concentration of silicon (ni=1.02x$10^{10}cm^{-3}$ at 300°K). Consequently, the built-in voltage *Vbi* in deep-submicron CMOS process is around 1.0V.

The depletion depth *Xdep* is computed by equation 3-26. It corresponds to the thickness of the region near the N+/P- junction interfaces, as illustrated in figure 3-21.

$$X_{dep} = \sqrt{\frac{2\varepsilon_{rsi}.\varepsilon_0(\Phi_s - Vbs)}{q.NDEP}} \quad (3\text{-}26)$$

where ε_{rsi} is the dielectric constant of silicon (11.7) ε_0 is the permittivity in vacuum ($8.854x10^{-12}$F/m), Φs is the surface potential given by equation 3-23, *NDEP* is the channel doping concentration for zero body bias, *q* is the electronic charge (1.60×10^{-19} C), and *vbs* is the bulk-source potential. The typical value of *Xdep* is 0.5µm (Figure 3-21).

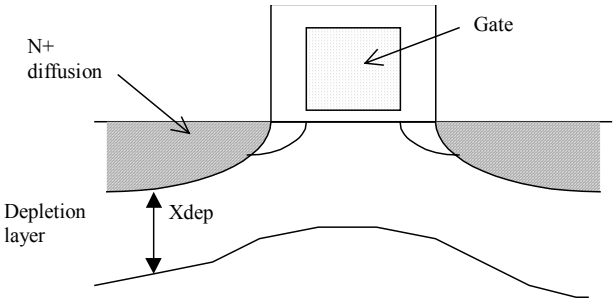


Figure 3-21: Illustration of the depletion depth Xdep

Threshold voltage

The main impact of the threshold voltage *Vt* is the *Ioff* parasitic current, that exhibits an exponential dependence with *1/Vt*. A high threshold voltage *Vt* leads to a small *Ioff* current, at the price of a low *Ion* current. Low threshold MOS devices consume a very high standby current, which impacts the power consumption of the whole circuit. An accurate prediction of the threshold voltage is a key issue for low power integrated circuit design. The general equation of the threshold voltage is presented in equation 3-27.

$$vth = VTHO + K1.\sqrt{(\Phi_s - Vbs} - \sqrt{\Phi_s}) - K2.Vbs + \Delta Vt_{SCE} + \Delta Vt_{NULD} + \Delta Vt_{DIBL} \qquad (3\text{-}27)$$

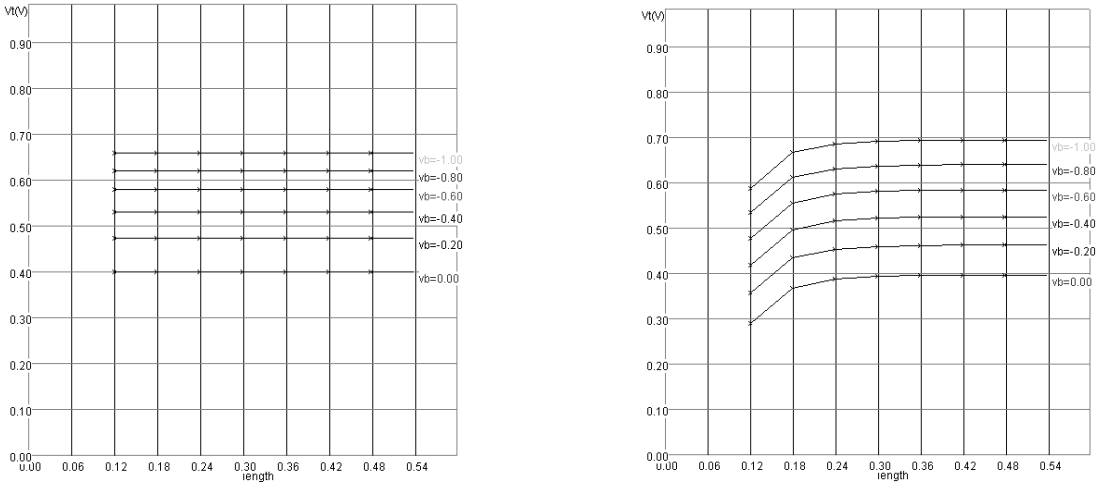
where `VTHO` is the long channel threshold voltage at *Vbs*=0 (Around 0.5V), `K1` is the first order body bias coefficient (0.5 $V^{1/2}$), Φs is the surface potential given by equation 3-23, *Vbs* is the bulk-source voltage, `K2` is the second order body bias coefficient, ΔVt_{SCE} is the short channel effect (SCE <gloss>) on *Vt* (Detailed in equation 3-28), ΔVt_{NULD} is the non-uniform lateral doping effect (NULD <gloss>) explained in equation 3-29, and ΔVt_{DIBL} is the drain-induced barrier lowering (DIBL <gloss>) effect of short channel on *Vt* (Detailed in equation 3-30).

Short channel effect

The threshold voltage is not the same for all MOS devices. There is a complex dependence between the threshold voltage and the effective length of the channel. For small channel, the threshold value tends to decrease. The equation 3-28 is proposed, based on an hyperbolic cosine function.

$$\Delta Vt_{SCE} = -\frac{0.5.DVT0}{\cosh(DVT1.\frac{Leff}{lt} - 1)}(Vbi - \Phi_s) \qquad (3\text{-}28)$$

where DVT0 is the first coefficient of short-channel effect on the threshold voltage (2.2 by default), DVT1 is the second coefficient of short-channel effect on the threshold voltage (0.53 by default), *Leff* is the effective channel length given in equation 3-21, and *lt* is the characteristic length, approximated in our implementation to 1/4 of the minimum channel length (0.03 µm for a 0.12µm), *Vbi* is defined in equation 3-25, and Φs is the surface potential given by equation 3-23.



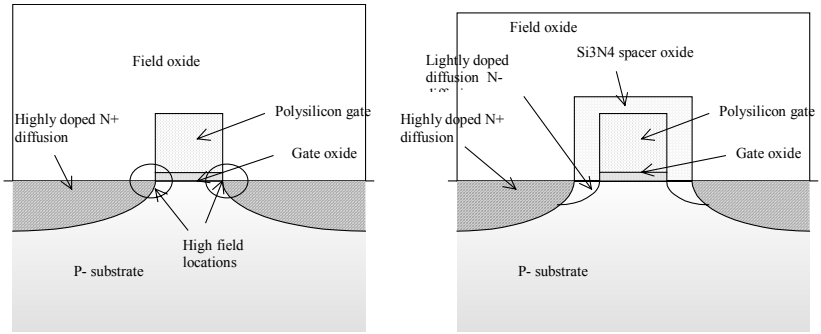
(a) No short channel effect (models 1&3) *(b) Short channel effect on Vt (Bsim4)*

Fig. 3-22: Short channel effect (SCE) on the threshold voltage

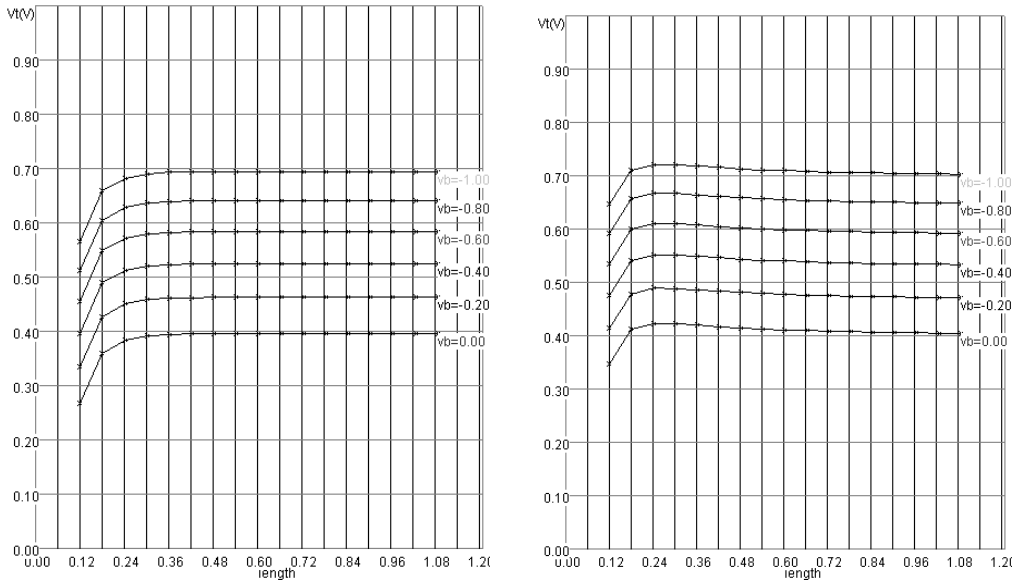
The illustration of the effect of ΔVt_{SCE} is proposed in figure 3-22. Without taking into account the short-channel effect, the threshold voltage is only dependent on *Vbs*. It can be seen that *Vt* increases when *Vbs* decreases. There is no dependence on the length. When we add the contribution of the short-channel effect expressed by equation 3-28, the threshold voltage is decreased significantly for small length values.

Non-uniform lateral doping

The lateral drain diffusion (LDD) is a technique introduced in recent technologies to reduce the peak channel fields in the MOS channel. The location for high-field parasitic effects is illustrated in the process section of figure 3-23 (a).



(a) MOS device without LDD structure *(b) MOS device with LDD structure*



(c) uniform lateral doping *(d) non-uniform lateral doping due to LDD*

Fig. 3-23: Effect of non-uniform lateral doping on the threshold dependence with the channel length

In the cross-section of figure 3-23 (b), the doping concentration at the corner of the gate is reduced thanks to a lightly doped N-type implantation. The Si3N4 spacer is grown over the gate before the N+ highly doped implantation is performed. Consequently, the high-filed effects are moderated. Unfortunately, the threshold voltage exhibits a complex dependence on the channel length, as illustrated in figure 3-23 (d), compared to (c). For a decreasing length, the threshold voltage tends to increase first (due to ΔVt_{NULD}), before decreasing rapidly due to the short channel effect ΔVt_{SCE} described in formula 3-28.

A simple formulation of the non-uniform lateral doping is ΔVt_{NULD} given below:

$$\Delta Vt_{NULD} = K1(\sqrt{1+\frac{LPE0}{L_{eff}}}-1).\sqrt{\Phi_s} \qquad (3\text{-}29)$$

Drain induced barrier lowering

When we apply a positive voltage on the drain of a long-channel n-MOS device, we observe no significant change in the value of *Vt*. When we do the same for a short-channel n-MOS device, we observe a decrease of the threshold voltage. The physical origin of DIBL is the increase of the depletion layer due to a high value of *Vds* that reduces the equivalent channel length, and consequently decreases the threshold voltage [Liu].

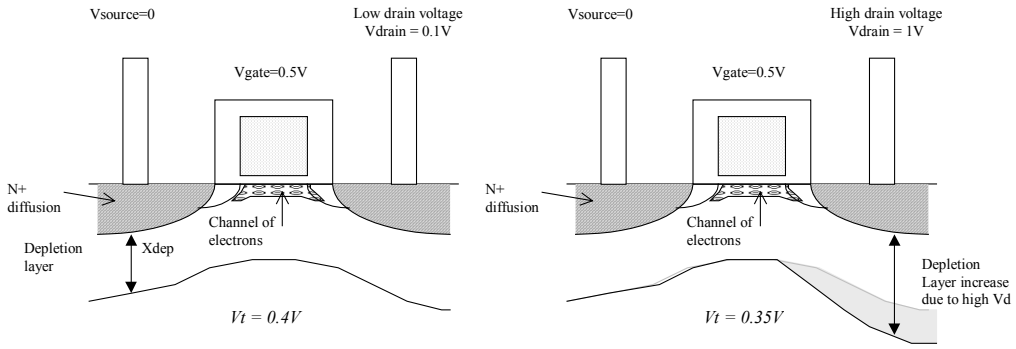


Fig. 3-24: Illustration of the depletion depth Xdep

$$\Delta Vt_{DIBL} = -0.5.ETA0.Vds \qquad (3\text{-}30)$$

A simplified model of the DIBL effect on the threshold voltage is proposed in equation 3-30. The parameter `ETA0` is the DIBL coefficient in sub-threshold region (default value 0.08), and *Vds* is the drain-source voltage.

Mobility

In this paragraph, we introduce the formulations for mobility of channel carriers. The generic parameter is `U0`, the mobility of electrons and holes. The effective mobility μ_{eff} is reduced due to several effects: the bulk polarization, and the gate voltage. The equation implemented in Microwind2 is one of the mobility models proposed in BSIM4 (Equation 3-31).

$$\mu_{eff} = \frac{\mathrm{U0}}{1+(\mathrm{UA}+\mathrm{UC}.\mathrm{V_{BS}})(\frac{\mathrm{V_{gsteff}}+2(\mathrm{VTH0}-\mathrm{V_{fb}}-\phi_s)}{\mathrm{TOXE}})^{\mathrm{EU}}} \qquad (3\text{-}31)$$

where

`U0` is the low field mobility, in m^2/V-s. Its default value is around 0.06 for n-channel MOS and 0.025 for p-channel MOS.

`UA` is the first order mobility degradation coefficient, in m/V. Its default value is around 10^{-15}.

`UC` is the body-effect coefficient of mobility degradation, in m/V^2. Its default value is -0.045×10^{-15}.

VFB is the flat band voltage, in V. It is computed using equation 3-32, where Φ_S is derived from equation 3-23. Its value is around 0.8V.

$$V_{FB} = \mathtt{VTO} - \Phi_S - \mathtt{K1}\sqrt{\Phi_S} \qquad (3\text{-}32)$$

TOXE is the oxide thickness, in m. A typical value for TOXE in 0.12µm is 2nm (2.10^{-9}m).

V_{BS} is the voltage difference between the bulk and the source (V).

EU is a coefficient equal to 1.67 for n-channel MOS, and 1.0 for p-channel MOS.

The parameter V_{gsteff} is a smoothing function, to ensure continuity between the subthreshold region and the linear region.

$$Vgst_{eff} = max(\mathtt{VOFF}, \frac{n.vt.ln(1+exp(\frac{(Vgs-Vth)}{n.vt}))}{1+n.exp(\frac{-(Vgs-Vth)}{n.vt})}) \qquad (3\text{-}33)$$

$$n = 1 + \mathtt{NFACTOR} \qquad (3\text{-}34)$$

A specific parameter VOFF is introduced to account for a specific effect appearing in short-channel device when *Vgs* is negative. Conventional models predict that the current decrease with an exponential law down to zero with decreasing *Vgs*. For *Vgs*<0, *Ids* is supposed to be 0.

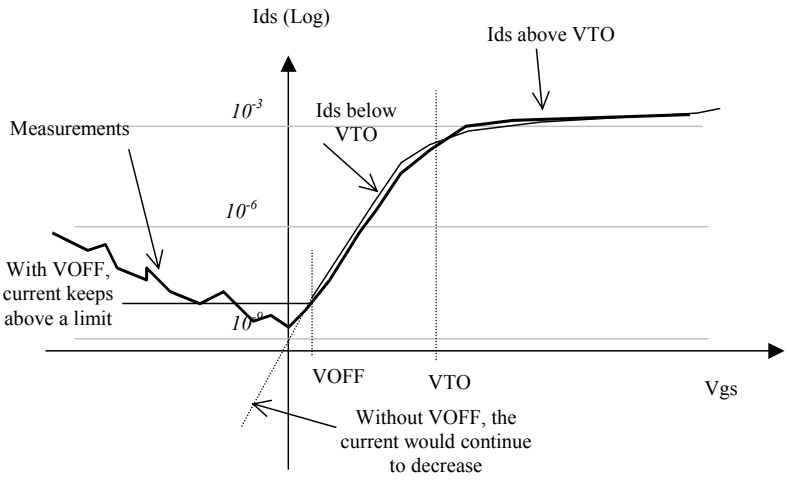


Figure 3-25: Illustration of the gate-induced drain leakage GIDL) for negative Vgs

In reality, *Ids* stops decreasing near zero *Vgs*, and then tends to increase with negative *Vgs* (Figure 3-25). This effect is called gate-induced drain leakage (GIDL). Consequently, the leakage current *Ioff* can be

significant when *Vgs* is negative (Quite frequent in logic cells). The `VOFF` parameter stops the *Ids* at a certain value, a simplified version of the BSIM4 modeling of the so-called gate-induced leakage current (More info may be found in [Liu]).

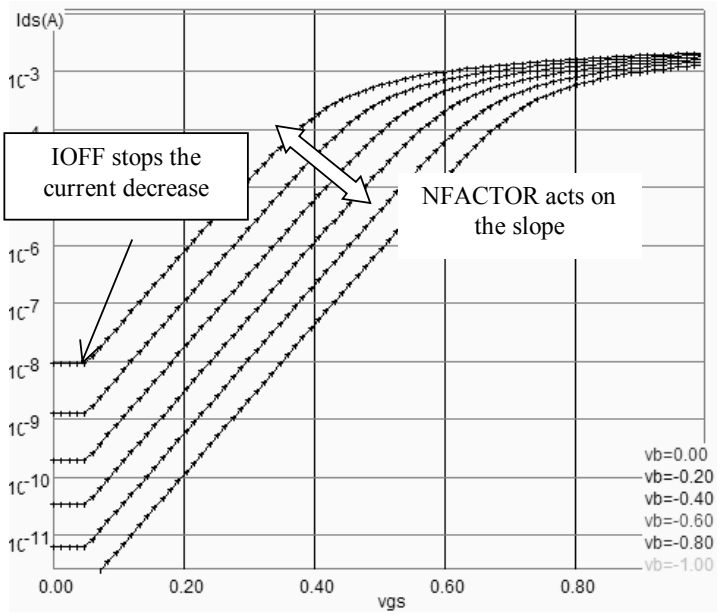


Figure 3-26: Illustration of the effects of IOFF and NFACTOR in sub-threshold mode

The parameter `NFACTOR` is usually close to 1, meaning that *n* is close from 2 (Equation 3-34). The effect on `NFACTOR` is illustrated in the display mode **Id. vs. Vg**, in logarithmic scale, as illustrated in figure 3-26.

$$Esat = 2\frac{Vsat}{\mu eff} \qquad (3\text{-}35)$$

$$Vdsat = Esat.\mathtt{L}\frac{(Vgsteff + 2.vt)}{(Esat.L + VgstEff + 2.vt)} \qquad (3\text{-}36)$$

Again, *VdsEff* is defined so as to smooth the evolution from *Vds* to the saturation voltage *Vdsat (*Equation 3-37*)*. The parameter *DELTA* is fixed to 0.01. The effect of *DELTA* is shown in figure 3-27. With a small value of DELTA (0.001 for example), the transition between linear and saturated region leads to a discontinuity. Experimental measurements show a gradual transition, that is well approximated when *DELTA*=0.01. A higher value of *DELTA* would lead to an *Ids* curve significantly lower than measurements.

$$Vdseff = Vdssat - 0.5(Vdsat - Vds - \delta + \sqrt{(Vdsat - Vds - \delta)^2 + 4\delta.Vdsat} \qquad (3\text{-}37)$$

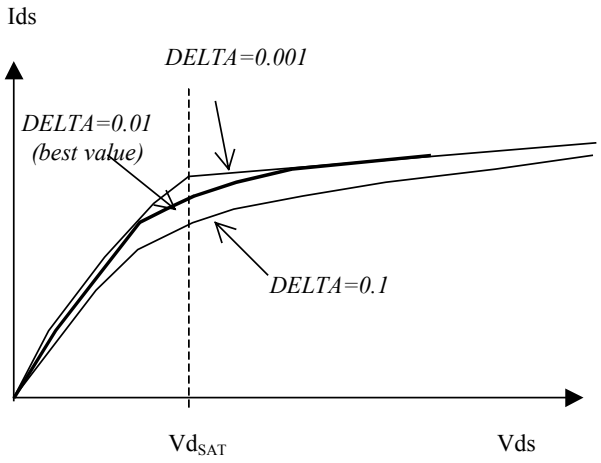


Figure 3-27: The smoothing function between linear and saturated regions can be modulated by DELTA. In Microwind2, DELTA is fixed to 0.01.

Current Ids

The current Ids is computed using one single equation, as described below.

$$Ids0 = \frac{Weff}{Leff}\mu eff\frac{\varepsilon_0\varepsilon_r}{\mathrm{TOXE}}V_{gsteff}\left(1-\frac{A_{bulk}V_{dseff}}{(2V_{gsteff}+4.vt)}\right)\frac{V_{dseff}}{\left(1+\frac{V_{dseff}}{\varepsilon_{sat}L_{eff}}\right)} \quad (3\text{-}38)$$

In our implementation of BSIM4 in Microwind, the parameter *Abulk* is fixed to 1. The final current *Ids* used in analog simulation is computed by equation 3-39:

$$Ids = Ids0\left(1+\frac{(V_{ds}-V_{dseff})}{V_{ascbe}}\right)\left(1+\frac{1}{\mathrm{C_{clm}}}ln\left(\frac{V_{ASAT}+\mathrm{V_{ACLM}}}{V_{ASAT}}\right)\right) \quad (3\text{-}39)$$

Two new terms appear after *Ids0*. The second term of the current equation accounts for impact ionization. It corresponds to a parasitic current at very high *Vds*, created by hot electrons and generating supplementary pairs or electrons and holes, when hitting the drain region after acquiring a high energy level inside the device channel. The parameter V_{ascbe} is a voltage below which the impact ionization becomes significant. If V_{ascbe} is large, *Ids* is almost equal to *Ids0*, meaning that there is no impact ionization effect. If V_{ascbe} is small, the shape of *Ids* is changed for high *Vds*, as illustrated in figure 3-28.

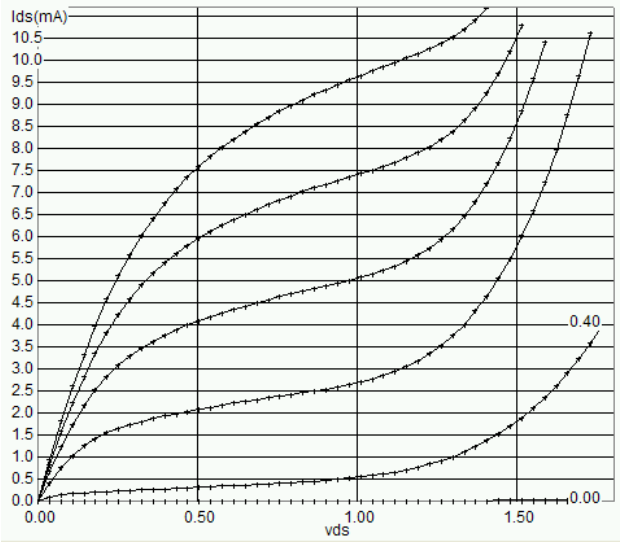


Figure 3-28: Effect of impact ionization at large Vds (W=10µm, L=0.12µm).

Two parameters affect the shape of the ionization current : `PSCBE1` and `PSCBE2`. The first parameter can be changed interactively on the screen. The voltage V_{asbe} is determined thanks to the following equations:

$$V_{ascbe} = \frac{L_{eff}}{\texttt{PSCBE2}} exp(\texttt{PSCBE1}\frac{litl}{(V_{ds} - V_{dseff})}) \qquad (3\text{-}40)$$

with

$$Litl = \sqrt{\texttt{XJ}\frac{\varepsilon_{rsi}}{\varepsilon_{rsiO2}}\texttt{TOXE}} \qquad (3\text{-}41)$$

XJ is the source/drain junction depth, around 0.1µm (10^{-7}m)

`TOXE` is the oxide thickness, in m (Around 3nm in 0.12µm)

ε_{rsi} = relative permittivity of silicon (11.7)

$\varepsilon_{rsi\ O2}$= relative permittivity of silicon oxide (3.9)

The third term of equation 3-39 accounts for the channel length modulation. An illustration of this phenomenon is provided in figure 3-29. It represents the *Ids* increase with large *Vds*. Graphically, V_{ACLM} is equivalent to an Early voltage, i.e. the value for which the *Ids* slope would cross the horizontal axis for negative *Vds*. For long channel devices (L=1µm for example), the effect of channel length modulation effect is small, so V_{ACLM} has a very high value (10V). For very short channels (0.12µm in the case of figure 3-30), a significant channel length modulation effect is observed, and V_{ACLM} is small.

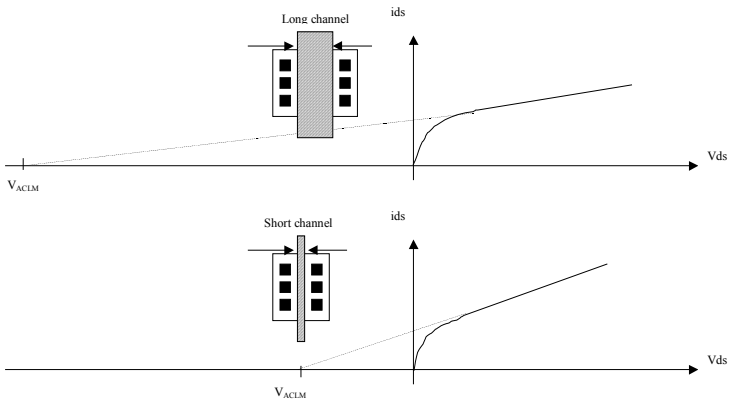


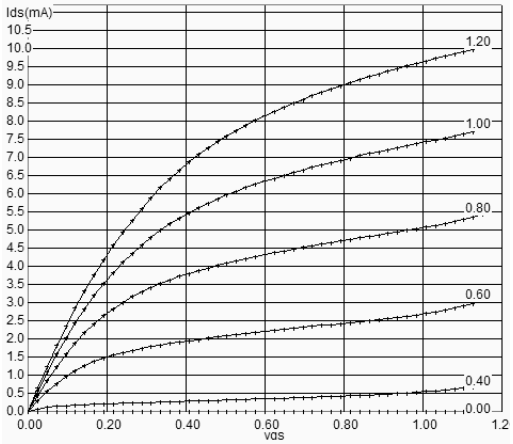
Figure 3-29: The channel length modulation is significant for short channel devices, and corresponds to the Ids increase at high Vds.

Only one new parameter, PCLM, is introduced in the equations. The parameters V_{ASAT} and V_{ACLM} are detailed below. The original equations from BSIM4 have been significantly simplified, and some fitting parameters have been ignored. See [Liu] for a description and relevant comments about the original equations.

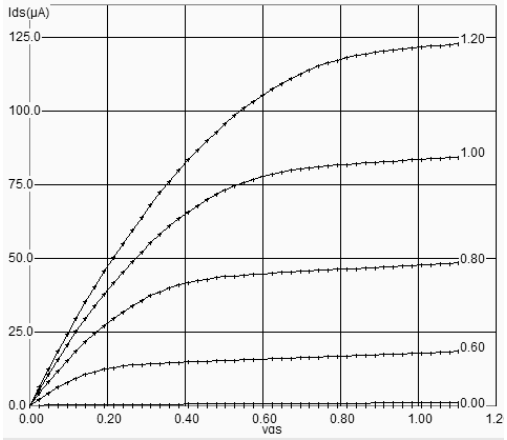
$$C_{clm} = \frac{1}{PCLM.litl}(l_{eff} + \frac{Vdsat}{\varepsilon_{sat}}) \qquad (3\text{-}42)$$

$$V_{ACLM} = C_{clm}(V_{ds} - V_{dseff}) \qquad (3\text{-}43)$$

$$V_{ASAT} = (\varepsilon_{sat}.l_{eff} + V_{DSSat})(1 - \frac{A_{bulk}V_{dsat}}{2(V_{gsteff} + 2Vt)}) \qquad (3\text{-}44)$$



(a) L=0.12µm, strong increase of Ids with Vds



(b) L=1µm small increase of Ids with Vds

Figure 3-30: The channel length modulation effect is significant for short channel devices in 0.12µm technology

Temperature Effects

Three main parameters are concerned by the sensitivity to temperature: the threshold voltage `VTO`, the mobility `U0` and the slope in sub-threshold mode. Both `VTO` and `U0` decrease when the temperature increases. The modeling of the temperature effect in BSIM4 is as follows. In Microwind2, `TNOM` is fixed to 300°K, equivalent to 27°C. `UTE` is negative, and set to -1.8 in 0.12µm CMOS technology, while `KT1` is set to -0.06 by default.

$$U0 = U0_{(T=27)}\left(\frac{T+273}{TNOM}\right)^{UTE} \quad (3\text{-}45)$$

$$VT = VT0_{(T=27)} + KT1\left(\frac{T+273}{TNOM} - 1\right) \quad (3\text{-}46)$$

A higher temperature leads to a reduced mobility, as `UTE` is negative. Consequently, at a higher temperature, the current *Ids* is lowered. This trend is clearly illustrated in figure 3-31. The reduction of the maximum current is 40% between -30°C and 100°C.

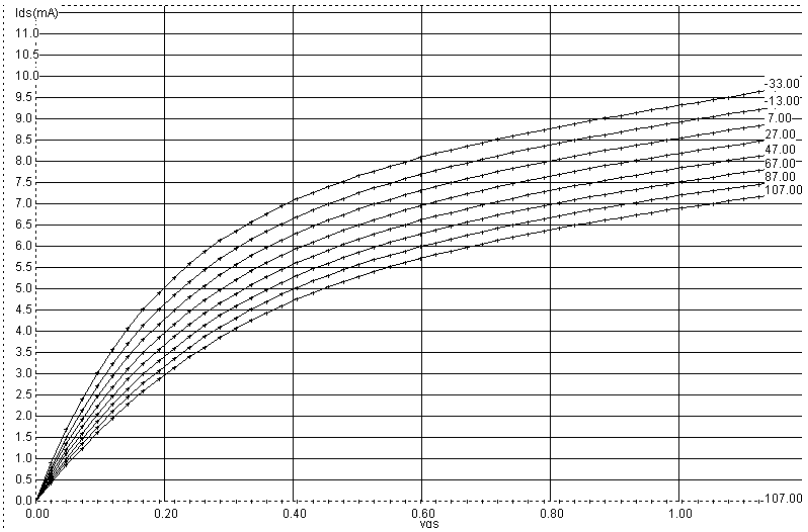


Figure 3-31: The effect of temperature on the peak Ids current, showing a degradation of current with rising temperature

For a short channel n-channel MOS device (L=0.12µm), the result of the parametric analysis illustrates the same trend (Figure 3-33).The parametric analysis is conducted as follows: the layout **MosTemperature.MSK** is loaded first. The MOS is polarized with a gate always on, the drain at VSS, and the source at VDD. The parametric analysis is launched. In the new window, select the temperature (Upper menu) and the maximum current (Lower menu). We observe in figure 3-33 a significant decrease of the Ion current with the temperature.

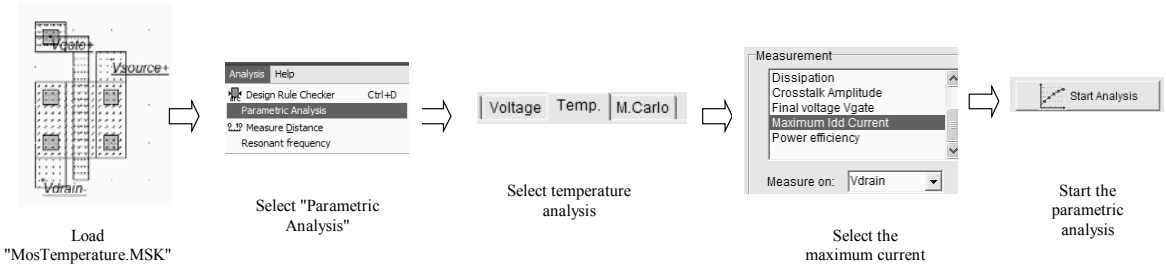


Figure 3-32: Configuring Microwind to display the variations of Ids vs. temperature

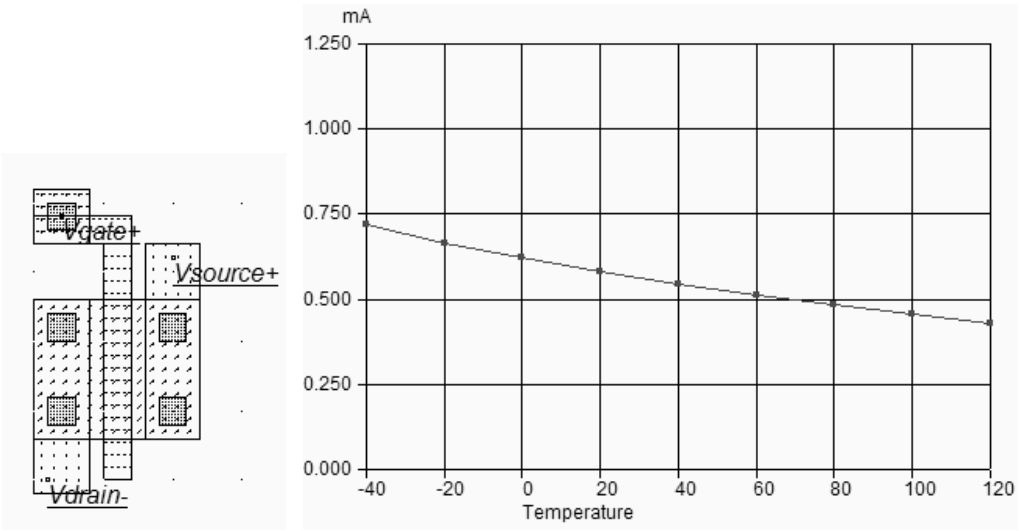


Figure 3-33: The parametric analysis reveals an important decrease of the maximum current Ids with temperature (MosTemperature.MSK)

Meanwhile, in an opposite trend, the threshold voltage is decreased, as `KT1` is negative (Figure 3-34). Therefore, there exists a remarkable operating point where the *Ids* current is almost constant and independent of temperature variation. In 0.12µm CMOS, the *Vds* voltage with zero temperature coefficient (ZTC) <Gloss> is around 0.9V, as shown in figure 3-34.

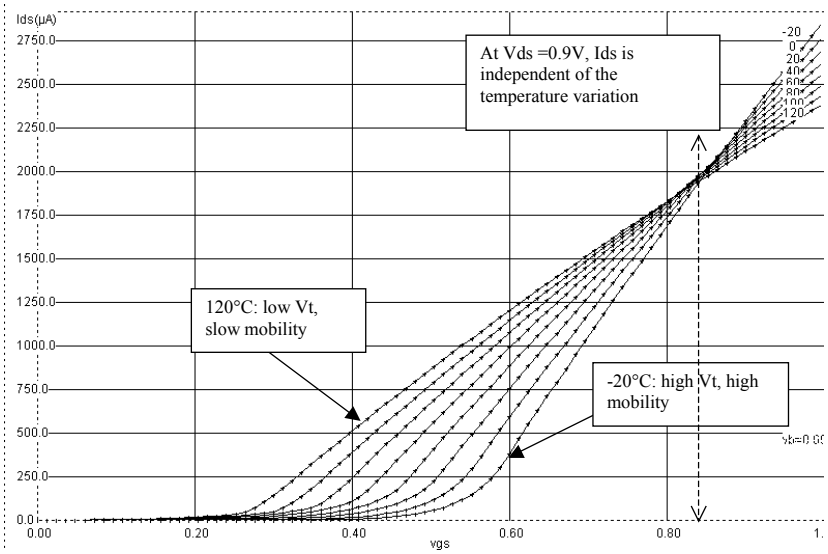


Figure 3-34: The effect of temperature on the Ids current, showing a zero temperature coefficient (ZTC) operating point

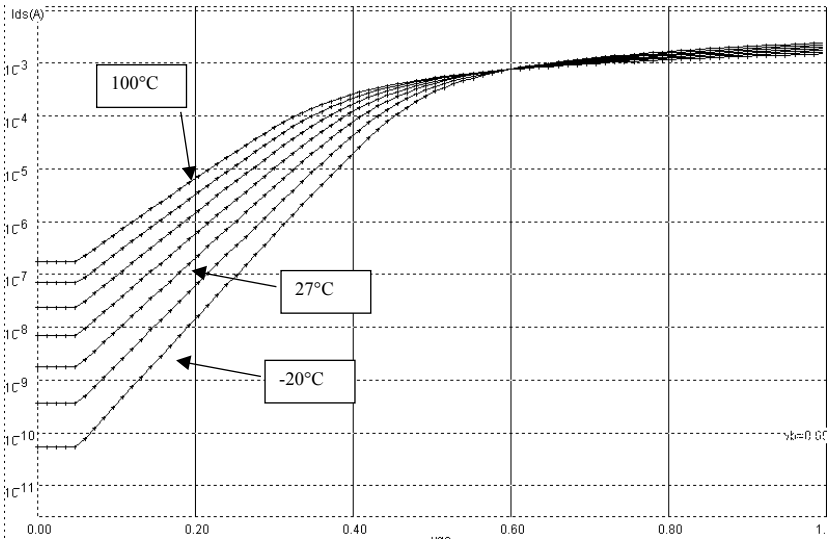


Figure 3-35 The effect of temperature on the MOS characteristics.

In the sub-threshold region, the impact of temperature is extremely important, as demonstrated in figure 3-35. At low temperature the current *Ids* decreased rapidly down to 10nA, corresponding to a small off leakage current. In contrast, at high temperature, not only the threshold voltage is reduced but the sub-threshold slope is flattened, which means an exponential increase of the *Ioff* leakage current (figure 3-35).

Parameter	Description	NMOS value in 0.12µm	NMOS value in 0.12µm	Name in RUL file
DVT0	First coefficient of short-channel effect on threshold voltage	2.2	2.2	B4D0VT
DVT1	Second coefficient of short-channel effect on Vth	0.53	0.53	B4D1VT
ETA0	Drain induced barrier lowering coefficient	0.08	0.08	B4ETA0
LINT	Channel-length offset parameter	0.01e-6µm	0.01e-6µm	B4LINT
LPE0	Lateral non-uniform doping parameter at Vbs = 0	2.3e-10	2.3e-10	B4LPE
NFACTOR	Sub-threshold turn-on swing factor. Controls the exponential increase of current with Vgs.	1	1	B4NFACTOR
PSCBE1	First substrate current induced body-effect mobility reduction	4.24e8 V/m	4.24e8 V/m	B4PSCBE1
PSCBE2	Second substrate current induced body-effect mobility reduction	4.24e8 V/m	4.24e8 V/m	B4PSCBE2
K1	First-order body bias coefficient	0.45 V1/2	0.45 V1/2	B4K1
K2	Second-order body bias coefficient	0.1	0.1	B4K2
KT1	Temperature coefficient of the threshold voltage.	-0.06V	-0.06V	B4KT1
NDEP	Channel doping concentration	1.7e17 cm-3	1.7e17 cm-3	B4NDEP
PCLM	Parameter for channel length modulation	1.2	1.2	B4PCLM
TOX	Gate oxide thickness	100nm	100nm	B4TOX
UA	Coefficient of first-order mobility degradation due to vertical field	11.0e-15 m/V	11.0e-15 m/V	B4UA
UC	Coefficient of mobility degradation due to body-bias effect	-0.04650e-15 V-1	-0.04650e-15 V-1	B4UC
U0	Low-field mobility	0.060 m2/Vs	0.025 m2/Vs	B4U0
UTE	Temperature coefficient for the zero-field mobility U0.	-1.8	-1.8	B4UTE
VFB	Flat-band voltage	-0.9	-0.9	B4VFB
VOFF	Offset voltage in subthreshold region.	-0.08V	-0.08V	B4VOFF
VSAT	Saturation velocity	8.0e4 m/s	8.0e4 m/s	B4VSAT
VTHO	Long channel threshold voltage at Vbs = 0V	0.3V	0.3V	B4VTHO
WINT	Channel-width offset parameter	0.01e-6µm	0.01e-6µm	B4WINT
XJ	Source/Drain junction depth	1.5e-7m	1.5e-7m	B4XJ

Table 3-4 List of user-accessible parameters in the BSIM4 implementation in Microwind.

5. Specific MOS devices

New kinds of MOS devices have been introduced in deep submicron technologies, starting the 0.18µm CMOS process generation. These MOS devices have specific characteristics which are described in this section.

Low leakage MOS

The main objective of the low leakage MOS is to reduce the *Ioff* current significantly, that is the small current that flows between drain and source with a zero gate voltage. The price to pay is a reduced Ion current. The designer has the possibility to use high speed MOS devices, which have high *Ioff* leakages but large *Ion* drive currents. The symbols of the low leakage MOS and the high speed MOS are given in figure 3-36.

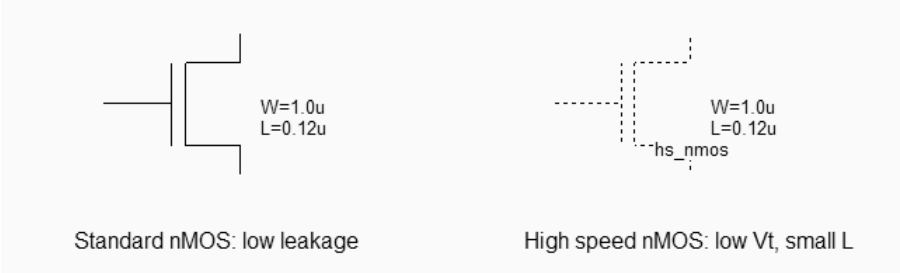


Figure 3-36: The low leakage MOS symbol (left) and the high speed MOS symbol (right) (MosOptions.SCH)

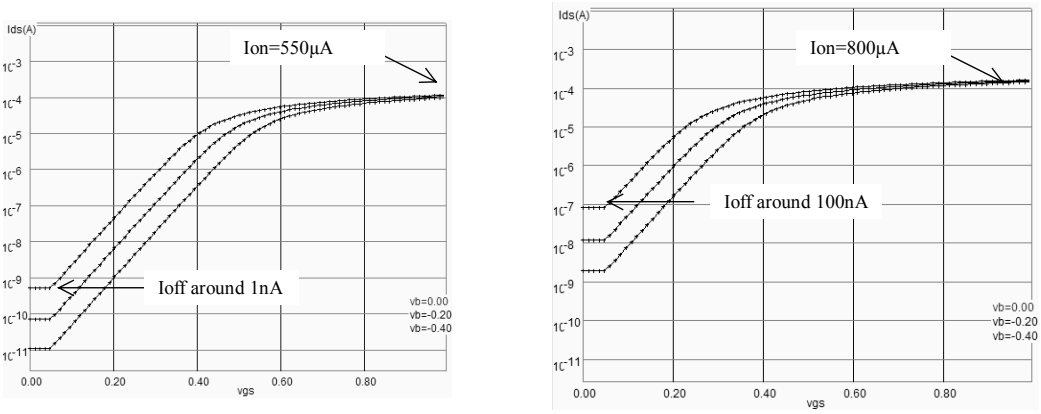


Fig. 3-37: The low leakage MOS offers a low Ioff current (1nA) but a reduced Ion current (550µA) as compared to the high speed MOS

In figure 3-37, the low leakage MOS device (left side) has an *Ioff* current reduced nearly by a factor 100, thanks to a higher threshold voltage (0.4V rather than 0.3V) and larger effective channel length (120nm) compared to the high speed MOS (100nm, see figure 3-30). By default, the MOS device is in low leakage option, to encourage low power design. The *Ion* difference is around 30%. This means that an high speed MOS device is 30% faster than the low leakage MOS. Its use is justified in circuits where speed is critical.

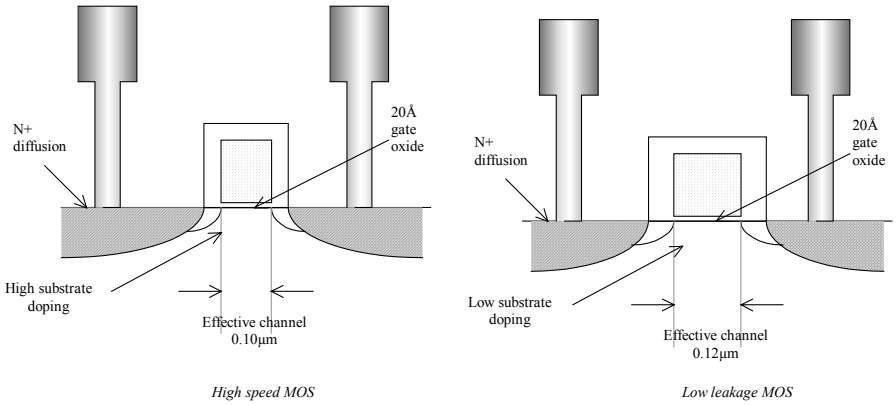


Fig. 3-38: Process section of the high speed (left) and low leakage (right) MOS devices

High speed MOS devices may be found in clock trees, data bus interfaces, central processing units, while low leakage MOS are used whenever possible, for all nodes where a maximum switching speed is not mandatory.

Mos options in Microwind

A specific layer, called option layer, is used to configure the MOS device option. The layer is situated in the upper part of the palette of layers. The bird's view of the standard MOS is identical to the high speed MOS, except for the added option layer which surrounds the MOS device. The p-channel MOS device includes an option layer together with the n-well layer, as seen in figure 3-39.

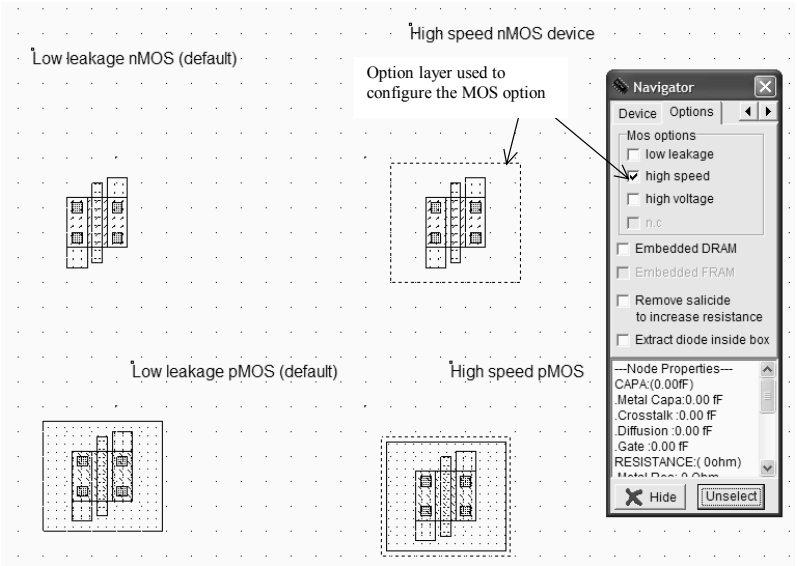


Fig. 3-39: High speed and Low leakage MOS layout. The only difference is the option layer configured for the low leakage option

An "Ultra-high speed" MOS has been introduced, together with the 90nm technology. This MOS device has a very narrow channel, nearly half of the technology, which increases significantly the Ion current at the price of a very high *Ioff* parasitic leakage current (Figure 3-40).

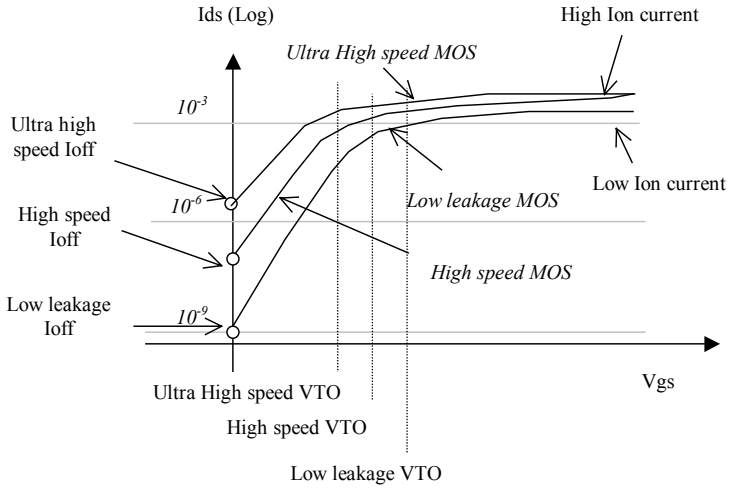


Fig. 3-40: Three types of MOS with different VTO threshold voltage are available in 90nm technology.

High Voltage MOS

Integrated circuits with low voltage internal supply and high voltage I/O interface are getting common in deep sub-micron technology. The internal logic of the integrated circuit operates at very low voltage (Typically 1.0V in 0.12µm), while the I/O devices operate in standard voltages (2.5, 3.3 or 5V).

Figure 3-41 shows the evolution of the supply voltage with the technology generation. The internal supply voltage is continuously decreasing. For compatibility reasons, the chip interface is kept at standard voltages, depending on the target application. Consequently, the input/output structures work at high voltage thanks to specific MOS devices with thick oxide called "High Voltage MOS", while the internal devices work at low voltage for optimum performances.

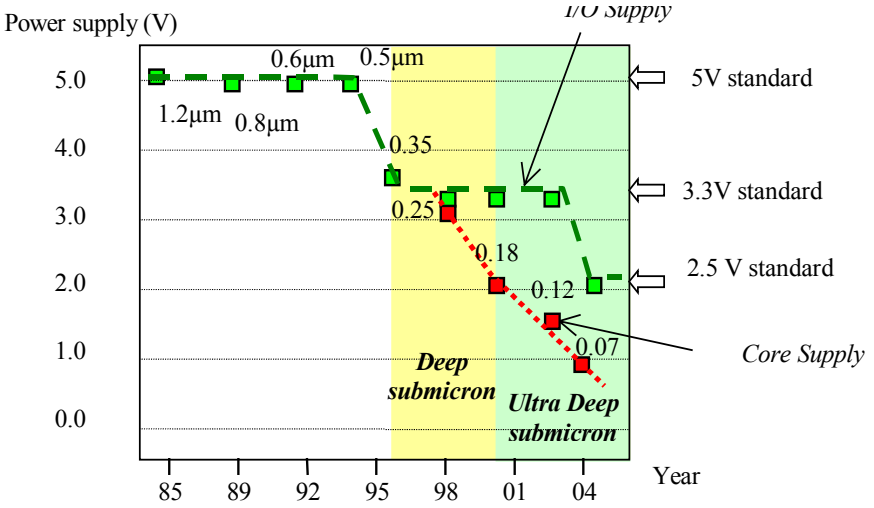


Fig. 3-41: The technology scale down leads to decreased core supply while keeping I/O interfacing compatible with 5V, 3.3V and 2.5V standards

For I/Os operating at high voltage, the high voltage MOS devices are commonly used. High-speed or low leakage devices would be dangerous to use because of their ultra-thin oxide: a 3V voltage applied to the gate of a core MOS device would damage the poly/substrate oxide. The high voltage MOS is built using a thick oxide, two to three times thicker than the low voltage MOS, to handle high voltages as required by the I/O interfaces (Figure 3-42). Furthermore, the length of the channel is 0.25µm minimum, that is twice the minimum length of core MOS. The cross-section of the three types of MOS (Low leakage, high speed and high voltage) is given in figure 3-43.

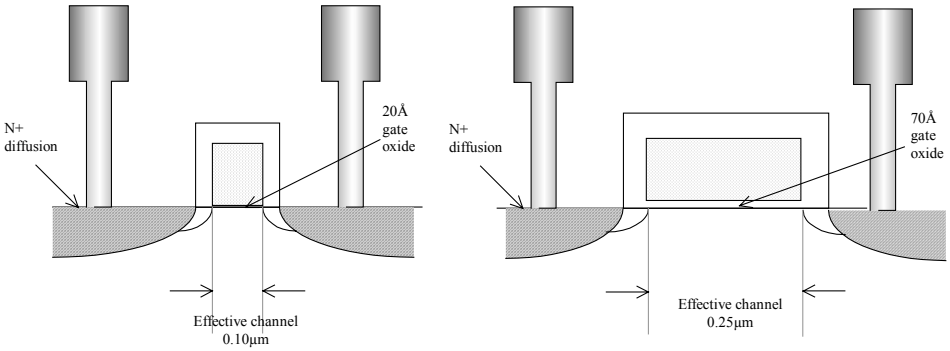


Fig. 3-42: Process section of the high speed and high voltage MOS devices

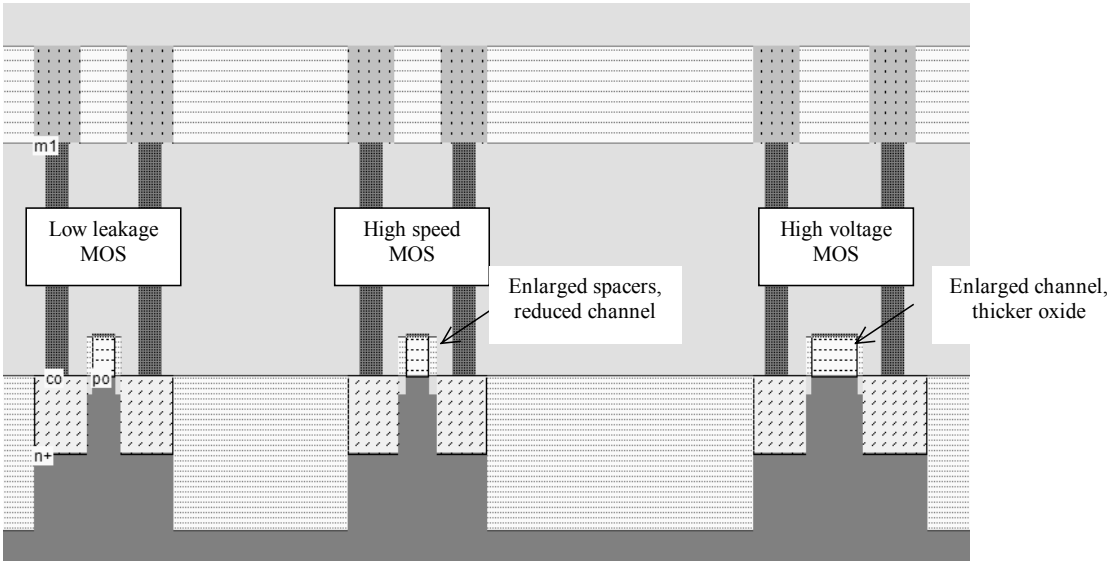


Fig. 3-43. The cross-section of the 3 n-channel MOS options: standard, high speed, and high voltage (lddExplain.MSK)

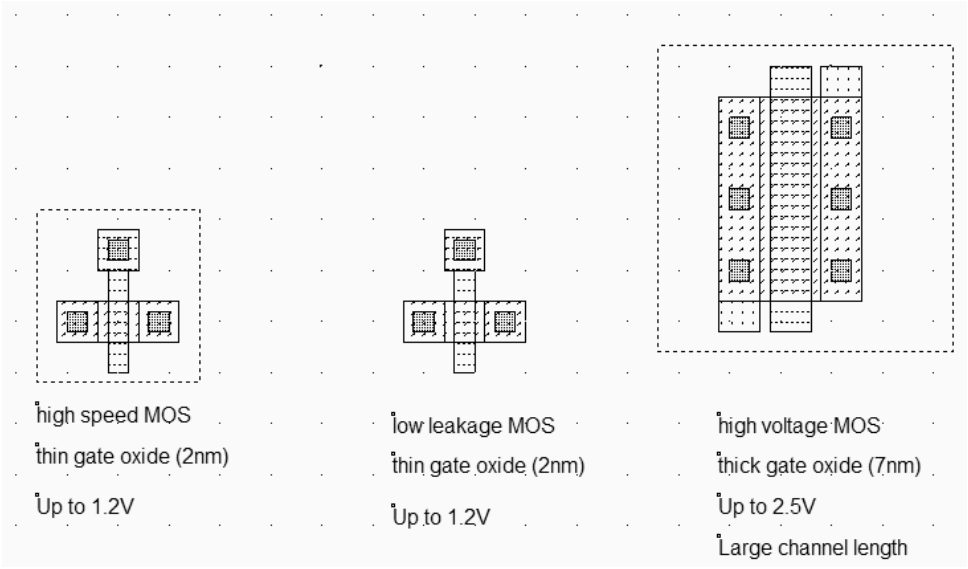


Fig. 3-44: High speed, low leakage and high voltage MOS (MosHighVoltage.MSK)

There is no difference between the high-speed MOS and the low leakage MOS from a layout point of view (Figure 3-44), expect the option layer for the high-speed option. The High voltage MOS has a significantly different layout, due to the enlarged channel length and width.

The I/V Characteristics of the high voltage MOS are plotted in figure 3-45, for *Vgs* and *Vds* up to 2.5V. The channel length is 0.25µm and the channel width is 1.2µm. Due to a large channel length, the current drive is less efficient.

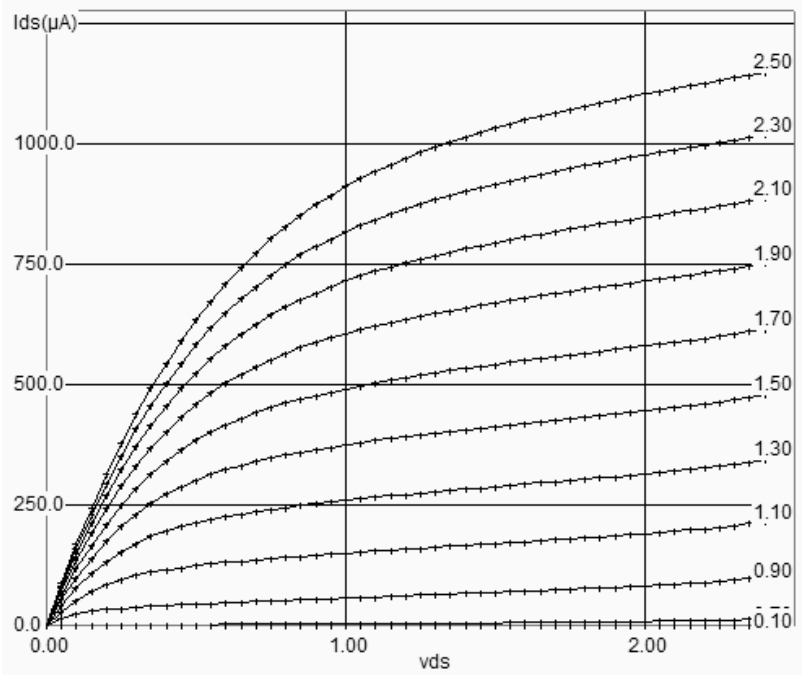


Fig. 3-45: Ids/Vds characteristics of the high voltage MOS.

There are two main reasons to keep a low-voltage supply for the core of the integrated circuit. The first one is low-power consumption, which is of key importance for integrated circuits used in cellular phones or any portable devices. Low supply strongly reduces power consumption by reducing the amplitude of signals, thus reducing the charge and discharge of each elementary node of the circuit. The equation 3-xxx gives an approximation of the power consumption. We deduce that even a small reduction of Vdd has a very positive impact on the reduction of the power consumption.

$$P = k.C.f.V_{DD}^{\ 2} \qquad (3\text{-}47)$$

where

P= power consumption (Watts)

K=technology factor, close to 0.5

C= total active capacitance of electrical nodes (F) (Not taking into account decoupling capacitance)

f=operational frequency of the integrated circuit (Hz)

Vdd= supply voltage (V)

Oxide Breakdown

The second reason for internal low voltage operation is the oxide breakdown. Increased switching performances have been achieved by a continuous reduction of the gate oxide thickness. In 0.12µm technology, the MOS device has an ultra thin gate oxide, around 0.002µm, that is 2nm or 20 Å,. Knowing that the molecular distance of SIO2 oxide is around 2Å, 20 Å means 10 atoms. The oxide may be destroyed by a voltage higher than a maximum limit *Vcrit*, called oxide breakdown voltage. A first order estimation is 0.1V/Å [Wang], which is expressed by equation 3-47.

$$Vcrit = \frac{K}{tox} \qquad (3\text{-}47)$$

With

K=breakdown coefficient (Close to 1 V.nm)

Tox = oxide thickness in nm

Vcrit=critical breakdown voltage (V)

Consequently, in 0.12µm, the breakdown voltage is around 2.0V, that is less than twice the nominal VDD (1.2V). An illustration of the breakdown voltage is proposed in figure 3-xxx. If we display the Id/Vd characteristics with Vg higher than VDD, (for example 2.5V instead of 1.2V), the oxide damage is represented by dotted lines (Here for Vg>2.0V). The MOS polarization should always be fixed in such a way that the gate voltage is lower than the breakdown voltage limit.

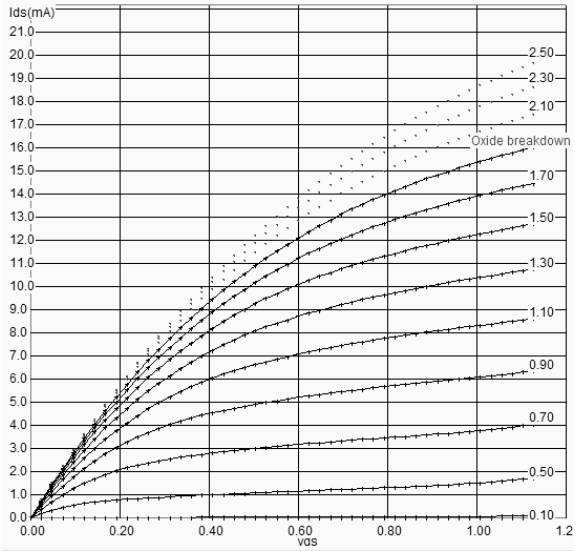


Fig. 3-46. Illustration of the breakdown voltage for a low leakage nMOS device, with a very high voltage applied on the gate

The oxide may be damaged by a 2V gate voltage. If the gate voltage is further increased, the physical destruction of the oxide may be observed, which usually results in a permanent conductive path between the gate and the source (Figure 3-47).

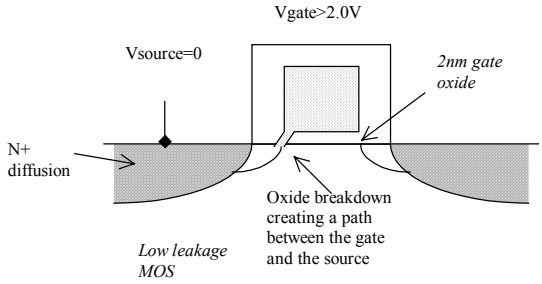


Fig. 3-47: oxide breakdown appears for gate voltage significantly higher than the nominal supply voltage

Microwind Configuration

A set of specific parameters are used for each MOS option to configure the BSIM4 and LEVEL3 models. The industrial approach usually consists in describing each MOS device in a completely separated set of model parameters. Consequently, MOS model cards may include several thousands of parameters. We aree trying to be as practical and didactic as possible, at the cost of a poor matching between measured and simulated MOS characteristics. In table 3-5, the list of the main varying parameters includes the gate oxide, the effective channel length parameter, and the threshold voltage.

Parameter	Description	NMOS value in 0.12µm	NMOS value in 0.12µm	Name in RUL file
TOX	Gate oxide thickness (low leakage) (high speed) (high voltage)	 20Å 20 70	 20Å 20 70	 B4TOX B4T2OX B4T3OX
LINT	Channel-length offset parameter (low leakage) (high speed) (high voltage)	 0.0 nm 10 0.0	 0.0 nm 10 0.0	 B4LINT B4L2INT B4L3INT
VTHO	Long channel threshold voltage (low leakage) (high speed) (high voltage)	 0.40 V 0.30 0.50	 0.40 V 0.30 0.50	 B4VTHO B4V2THO B4V3THO

Table 3-5: BSIM4 parameters variation depending on the MOS option

6. Process Variations

The simulated results should not be considered as absolute values. Due to unavoidable process variations during the hundreds of chemical steps for the fabrication of the integrated circuit, the MOS characteristics are never exactly identical from one device to another, and from one die to an other. It is very common to measure 5% to 20% electrical difference within the same die, and up to 30% difference between separate dies. One varying parameter is the effective channel length. In figure 3-48, although both devices have been designed with a drawn 2 lambda, the result is a 0.11µm length for the MOS situated on the left side, and 0.13µm for the MOS situated on the right side.

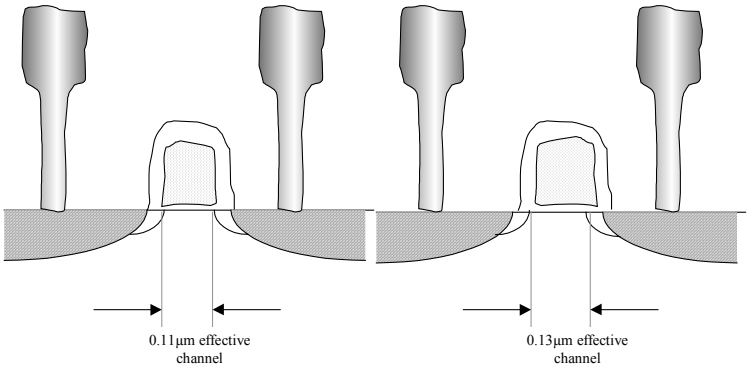


Fig. 3-48: The same MOS device may be fabricated with an important effective channel variation

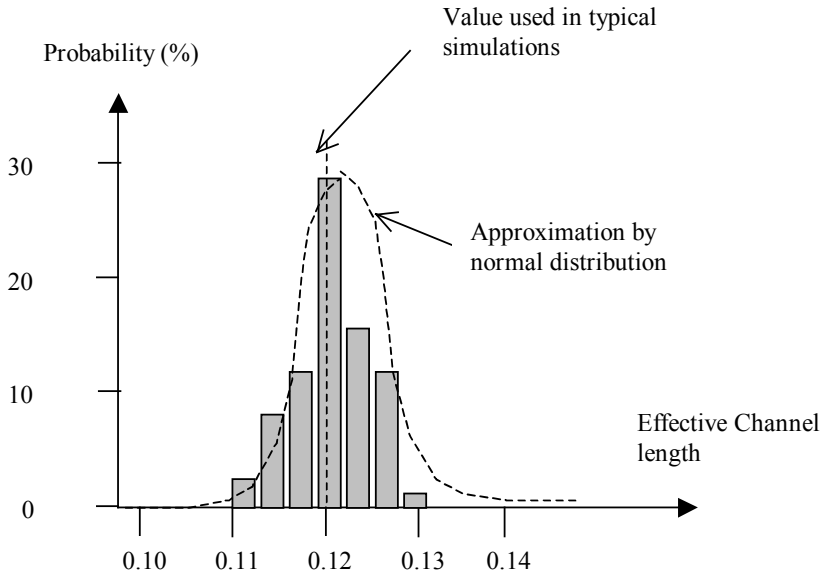


Fig. 3-49: The effective channel length may vary significantly with the process

If we cumulate several measurements on a wide number of devices, we can plot the probability of occurrence versus the measured effective length. The curve is usually a normal distribution with a center close to the default parameter given in the electrical rules (Figure 3-49).

Simulation with Microwind

The menu **Simulate → Simulation parameters** gives a simple access to minimum/typical/maximum parameter sets (Figure 3-50). The industrial approach usually consists in providing a separate set of model parameters for each case, which represents a huge amount of model parameters. In Microwind, the approach has consisted in altering two main parameters: the threshold voltage (20% variation) and the mobility (20% variation). All other parameters are supposed to be constant.

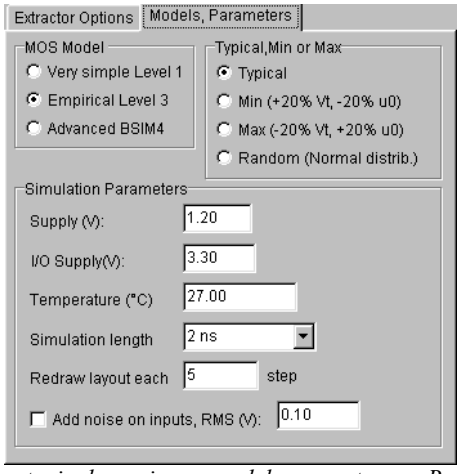


Fig. 3-50: Access to minimum, typical, maximum model parameters or Random simulation

A comparative simulation of the *Id/Vd* curve in typical, maximum and minimum scenarios shows a very large variation of performances (Figure 3-51). The user may automatically switch from one parameter set to an other by a press of a key ("M" for maximum, "m" for minimum,"t" for typical).

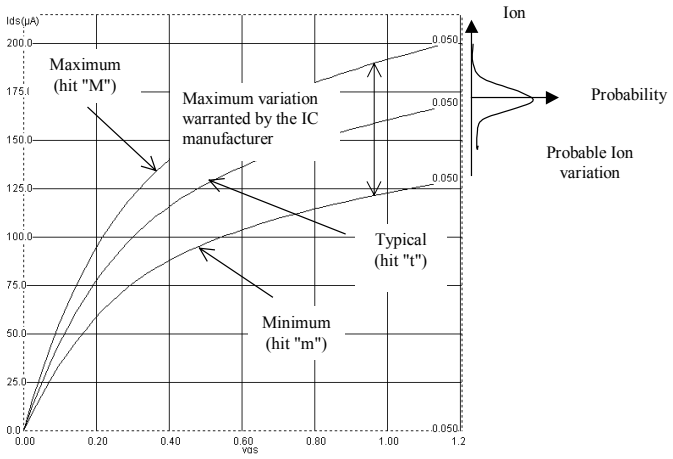


Fig. 3-51: The MOS Id/vd curve in Min,Typ,Max modes.

To superimpose the three curses, click the small brain icon (Enable Memory), and increase the **Step Vg** to 1.2 to draw only one curve for each mode. Notice the important variation between the minimum Ion and maximum Ion (From 125µA to 200µA). In reality, the MOS characteristics vary in a normal distribution around the typical case. Consequently, the Ion current of this MOS device is very likely to reach the typical value. The min/max simulation is very interesting to validate the design in extreme situations. The min/max simulation should also consider the temperature: the worst current is obtained at high temperature and with a minimum set of parameters, while the highest current is obtained at low temperature and with a maximum set of parameters.

7. Concluding remarks

The number of parameters required for various MOS models is reported in figure 3-52. It can be seen that the trend is to increase the number of parameters, in order to take into account various effects linked to the device scale down.

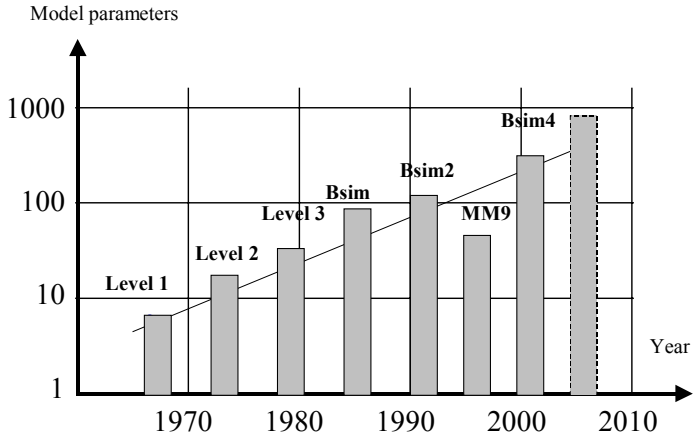


Fig. 3-52. Increased number of parameters in the MOS models

Even with advanced models, the resulting models may not fit well in all operating regions, for all device sizes. This is why the industrial approach for building model parameters is based on optimization mathematical algorithms. In deep submicron technology, the model parameters have a strong variation with the device size. For example the threshold voltage and mobility vary significantly with the device length, and the equations cannot always handle these dependencies properly. One solution is called binning. It consists in breaking the width-length space into several regions, as illustrated in figure 3-53. In each region, a specific set of model parameters is setup and optimized.

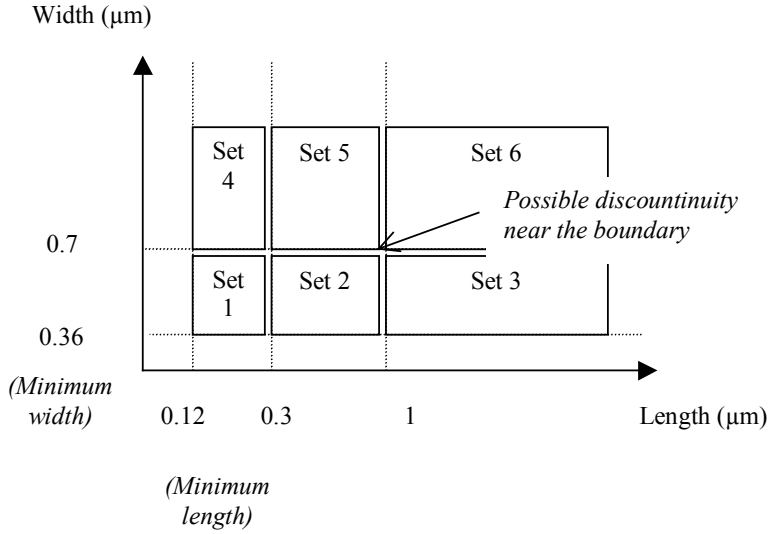


Figure 3-53: Using 6 sets of parameters to accurately cover the whole range of width and length

Binning severely complicates the process of parameters extraction. In the case of figure 3-xxx, 6 sets of parameters are required. Notice that set 1 covers small length and small width. Set n°2 covers a wider length

interval, while set n°3 is valid for any length greater than 1µm. This is because long length devices are easier to model than short length devices, where many second order effects appear. Binning is used in industry to increase the analog simulation accuracy, at the cost of several drawbacks: the simulation time cost due to model complexity, and discontinuities in the current prediction that may be observed at the boundary of two sets. These limitations are the fuel for constructing more complex models that fit well for the whole range of width and length. In the future, nano-scale technologies may require MOS models with up to 1000 parameters, requiring a degree of expertise never attained up to now.

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EXERCISES

3.1 Configure Microwind in 0.35µm technology (File **cmos035.RUL**) using the command **File → Select Foundry**. Compare simulation and measurement in 0.35µm for a nMOS device, W=10µm, L=0.4µm (File **Na10x0,4.MES**). Evaluate the mismatch between level 1, level 3 and BSIM4. In which domain is model 3 poorly fitted?

3.2 Configure Microwind in 0.18µm technology (File **cmos018.RUL**). Compare simulation and measurement in 0.18µm for a nMOS device, W=4µm, L=0.2µm, low leakage option (File **Nc4x0.2.mes**). Evaluate *Ron, Ion, Ioff*, and *Vt*. Perform the same evaluation for the high speed MOS, same size (File **NcHS4x0.2.mes**). Perform the same evaluation for the high voltage MOS, same size (File **NcHV4x0.2.mes**).

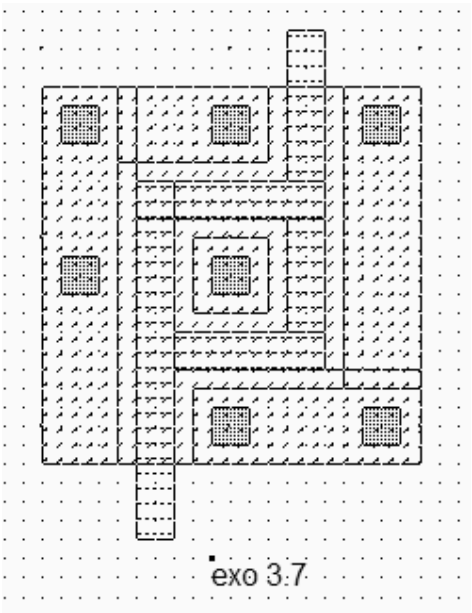
3.3 In low power applications, the n-well can be connected to a voltage *Vwell* different from VDD. This non usual polarization aims at modifying the threshold of the p-MOS transistor. Under which condition for *Vwell* the threshold of the PMOS transistor (Low Leakage option) is decreased to 0.2V in 0.12µm?

3.4 Design a MOS device with *Ion*=10mA, minimum gate length in 0.12µm. What is *Ioff*? How to obtain a MOS with *Ion*=10mA but twice less *Ioff*?

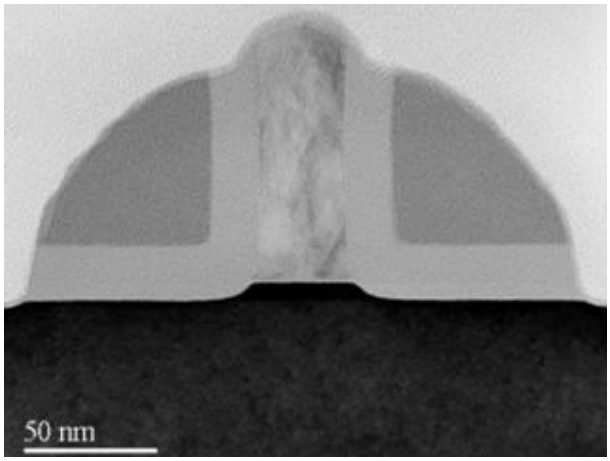
3.5 Compare the value of V_{GS_T0} (The value of *Vgs* for which *Ids* is independent of temperature) between MOS options in 0.12µm.

3.6 Show that four MOS devices (Wn,Ln) connected in parallel have approximately the same *Ion* than a single MOS device with a width equal to 4 Wn. What is the origin of the mismatch?

3.7 What is the channel size of the following MOS device? Does Microwind correctly extract the channel size of that device?



3.8 In the following picture of a 50nm MOS device, locate the gate, drain, and source, field oxide, gate oxide .


50 nm