14 Input Output Interfacing

This chapter is dedicated to the interfacing between the integrated circuit and the external word. After a brief justification of the power supply decrease, the input/output pads used to import and export signals are dealt with. Then, the input pad protections against electrostatic discharge and voltage overstress are described. The design of output buffers is also presented, with focus on current drive. Specific aspects of I/O floorplan, supply clamp and interfacing with packages are also introduced, followed by a short description of IBIS models for describing I/O behavior, and of the signal transport between integrated circuits.

1. Power Supply

The power supply of integrated circuits has continuously decreased with the progresses in process integration. Figure 14-1 shows the evolution of the supply voltage with the technology generation. A difference is made between the external supply and the internal supply. The external supply, usually 5V, 3.3V or 2.5V concerns the input/output interface. For compatibility reasons, the chip interface is kept at these high standard voltages, which eases the exchanges with other integrated circuits. The low internal supply concerns the core logic. Using a low voltage is attractive for low power applications and to prevent the very thin gate oxide for overstress and possible destruction. Classically, for reliable operations, the maximum voltage handled by the gate oxide is 0.7V/nm.

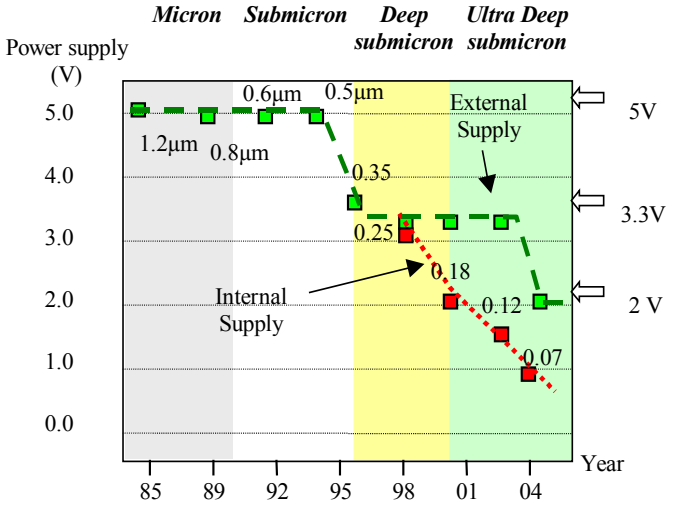


Figure 14-1: Power supply decrease with technology scale down

In 0.12µm CMOS technology, the external supply VDDH is 2.5V and the core supply VDD is 1.2V. The input/output structures work at high voltage by making extensive use of specific MOS devices with thick oxide, while the internal devices work at low voltage with optimum performances. Remember that the oxide thickness is 20 Å for the core MOS devices in 0.12µm, that the breakdown voltage for high quality SiO2 is around 0.1V/Å, which means that the device can handle up to 2V. Voltage translator ensures the bi-directional conversion between high and low voltage signals (Figure 14-2). In the die, several functions are supplied at high voltage, such as on-chip regulators, phase-lock-loops, ADC and DAC converters, or radio-frequency circuits and power amplifiers.

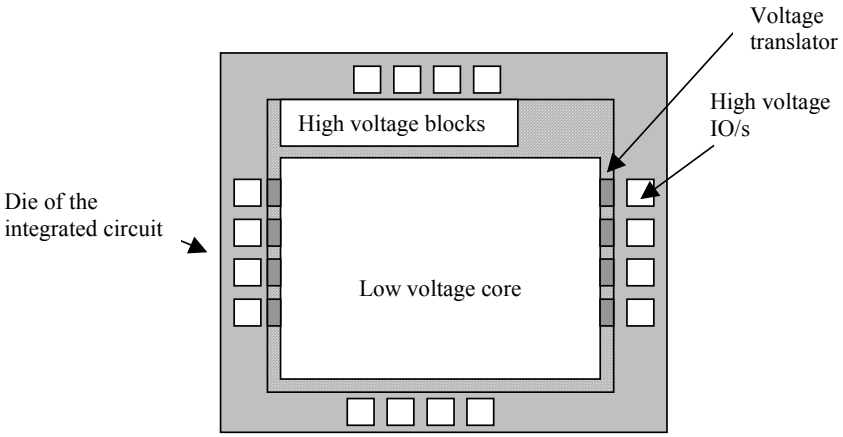


Figure 14-2: Multiple power supply in deep submicron technology

2. The Bonding Pad

The bonding pad is the interface between the integrated circuit die and the package. The pad has a very large surface (Almost giant compared to the size of logic cells) because it is the place where a connection wire is attached to build the electrical link to the outside word, as shown in figure 14-3.

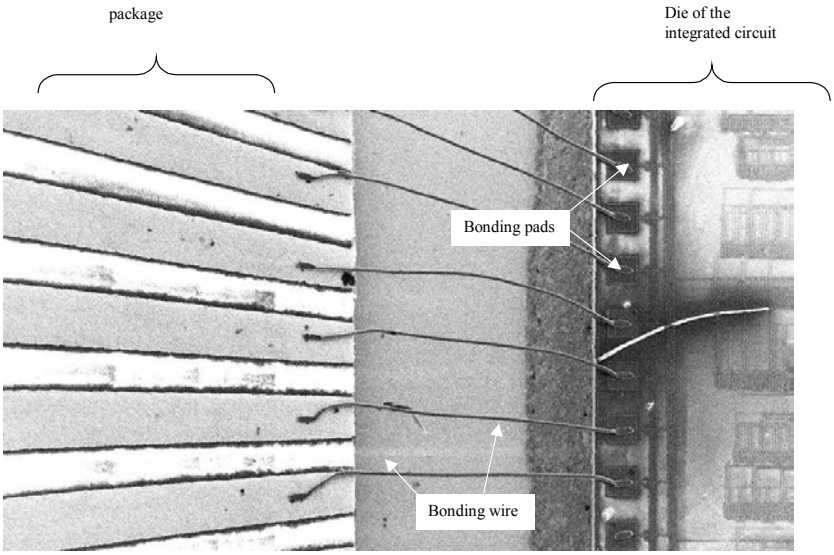


Figure 14-3: The bonding pad is used to connect a wire (called the bonding) which builds the electrical connection between the die and the package

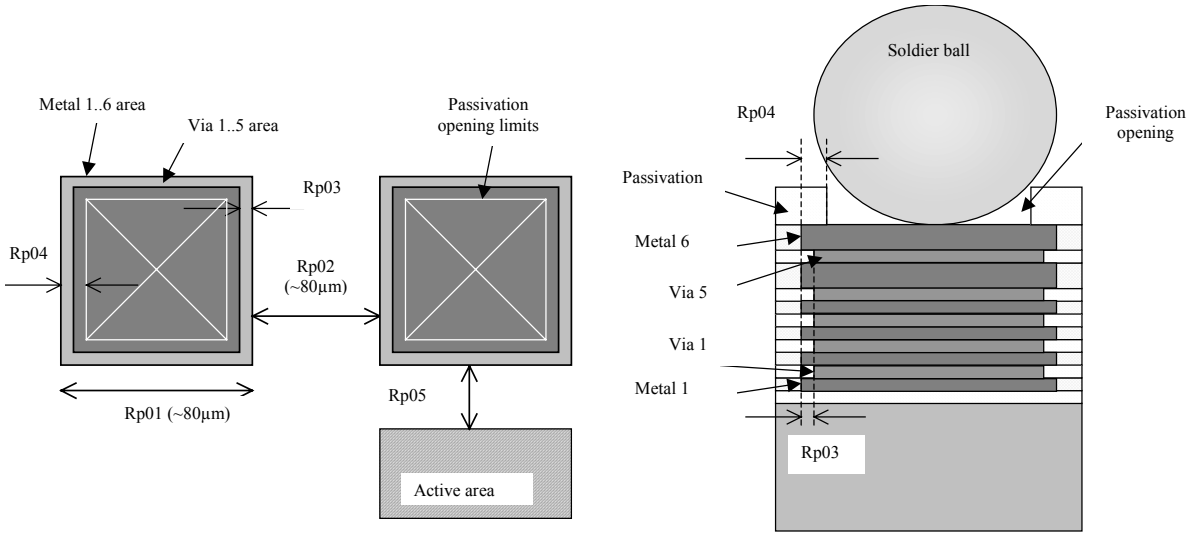


Figure 14-4: The bonding pad design rules

The pad size is approximately 80µm x 80µm. The basic design rules for the pad are shown in figure 14-4. The pad-to-pad spacing, (*Rp02*), is also around 80µm. New technologies such as 90nm enable the implementation of pad structures with 50x50µm openings.

The cross-section shown in figure 14-4 gives an illustration of the passivation opening and associated design rule *Rp04* on top of the metal and via stack. The thick oxide used for passivation is removed so that a bonding wire or a bonding ball can be connected by melting to the package.

Design rule	Description	Value in 0.12µm
rp01	Pad width:	80µm
rp02	Between two pads 100 µm	80µm
rp03	Border of via vs. Metal	2µm
rp04	Opening in passivation v.s last metal	5µm
rp05	Between pad and unrelated active area	20 µm

Table 14-1: The bonding pad design rules

The pad can be generated by Microwind using the command **Edit →Generate → I/O pads**. The menu shown in figure 14-5 gives access to a single pad, with a default size given by the technology (around 80µm in this case), or to a complete pad rind, as detailed later. Select the item **Single pad** and click **Generate**. Then give the location in the layout for the pad. As the pad is giant compared to the usual design scale, click **View All** to see the global pad layout.

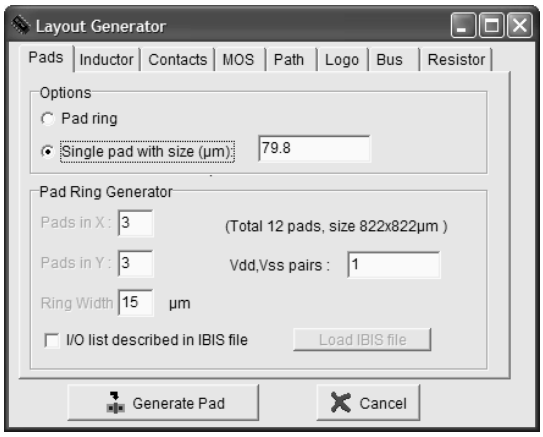


Figure 14-4: The bonding pad menu

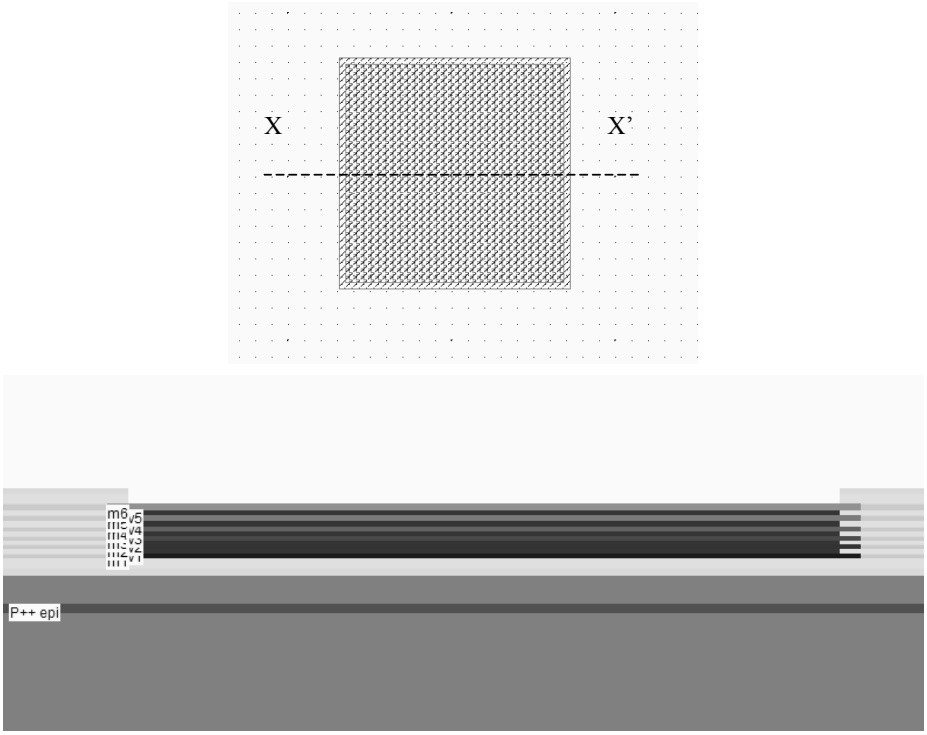


Figure 14-5: The bonding pad generated by Microwind and its cross-section. On top of metal6, the passivation has been removed (IOPad.MSK)

The cross-section of the pad is reported in figure 14-5. We see the stack of metal layers, the vias and the passivation opening for the bonding to the package. In some CMOS technologies, there may exist a constraint on the via size that forces the designer to split the large via surface into an array of elementary via with the 2 lambda size, 4 lambda spacing. This type of design rule has not been implemented in Microwind.

3. The Pad ring

The pad ring consists of several pads on each of the four sides of the integrated circuit, to interface with the outside world. The default menu for an automatic generation of a pad ring is shown in figure 14-6. The proposed architecture is based on 5 pads on each side, meaning a total of 20 pads.

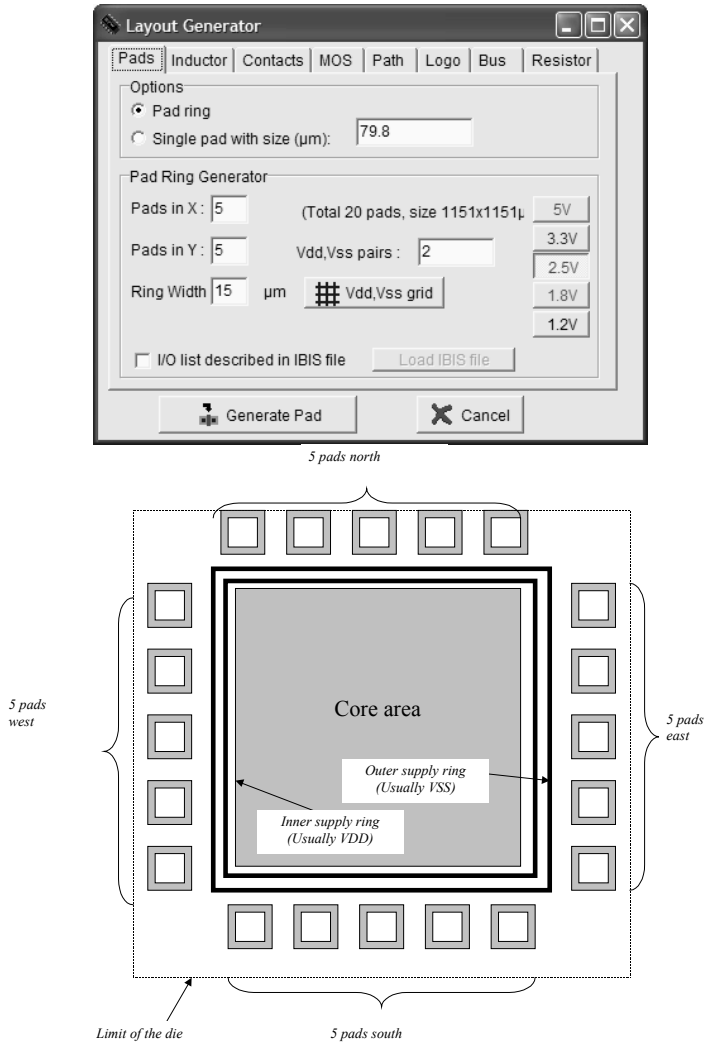


Figure 14-6: The menu for generating the pad ring and the corresponding architecture

The layout of the default pad ring generated in 0.12µm is shown in figure 14-7. Two pairs of supply VDD/VSS are automatically added to the pad structure. The first pair is fixed on the west side, the second pair on the east side. More VDD/VSS pairs may be generated. Usually one VDD/VSS pair is needed for 8-10 active input/output pads. Each I/O pad includes an over-voltage protection circuit based on two diodes which appear near the inner supply ring. These structures are justified and described later in this chapter.

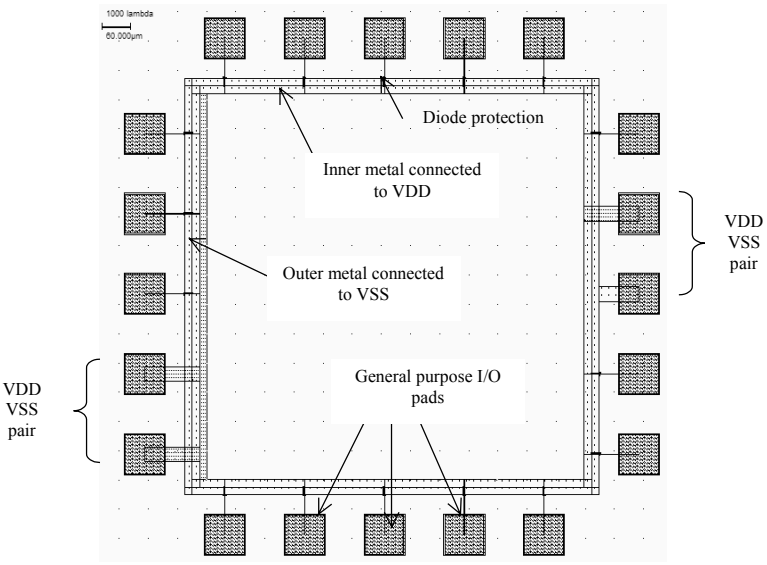


Figure 14-7: The default pad ring generated in 0.12µm, with 20 pads, including two pairs of VDD/VSS supply pins (padRing.MSK)

The way the supply pads are connected to the internal rings is detailed in figure 14-8. All VSS pads are connected to the outer ring, while the VDD pads are connected to the inner ring. The more the circuit needs power, the larger the number of supply pads. In a 800 I/O integrated circuit, nearly 100 pads are dedicated to the voltage supply, split equally between VSS and VDD supply pads.

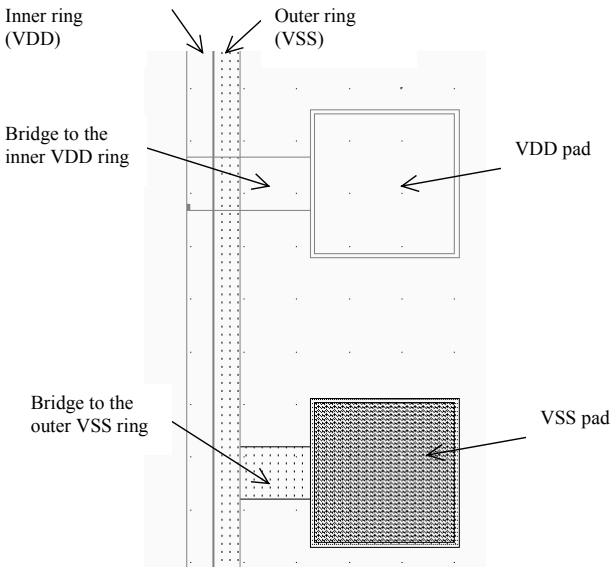


Figure 14-9: Connecting to the VSS and VDD internal ring (PadRing.MSK)

The supply rails

The supply voltage may be 5V, 3.3V, 2.5V, 1.8V or 1.2V. Most designs in 0.12µm use 1.2V for the internal core supply and 2.5V for the interfacing. This is because the logic circuits of the core operate at low voltage to reduce power consumption, and the I/O structures operate at high voltage for external compatibility and higher immunity to external perturbations. Usually, an on-chip voltage regulator converts the high voltage into an internal low voltage.
In most cases, the integrated circuit uses two separate supply pads, one for the high voltage, one for the low voltage. Consequently, the integrated circuit has four supply rings: VSS for I/Os (0.0V), VDD for I/Os (2.5V), VSS for the core (0.0V), VDD for the core (1.2V). An example of a four ring design is shown in figure 14-10.

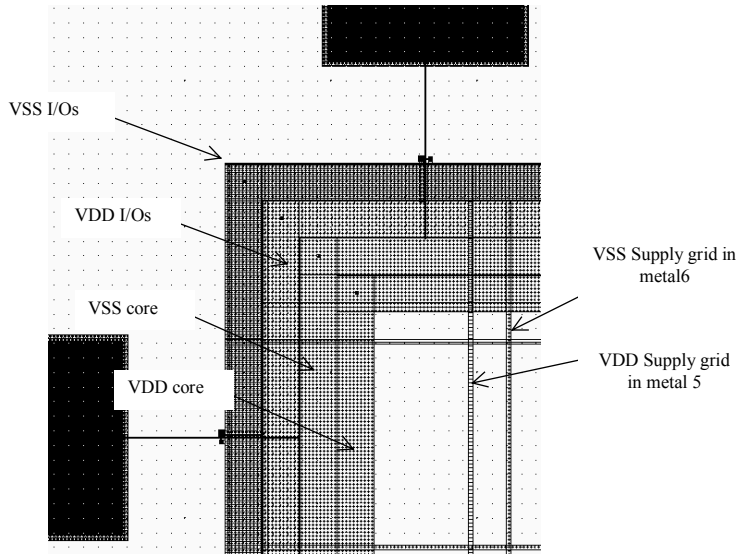


Figure 14-10: Zoom at the supply rings VSS, VDD for I/Os and core (PadRingDoubleGrid)

Supply rail design

A metal wire cannot drive an unlimited amount of current. When the average current density is higher than 2.10^9 A/m^2 [Hastings], the grains of the polycrystalline aluminum interconnect start to migrate (The phenomenon is called electro migration) and the conductor ultimately melts. To handle very high current density, the supply metal lines must be enlarged. A typical rule of thumb is 2mA/µm width for aluminum supply lines and 5mA/µm for copper, which means that a copper interconnect is superior to aluminum in sustaining large currents.

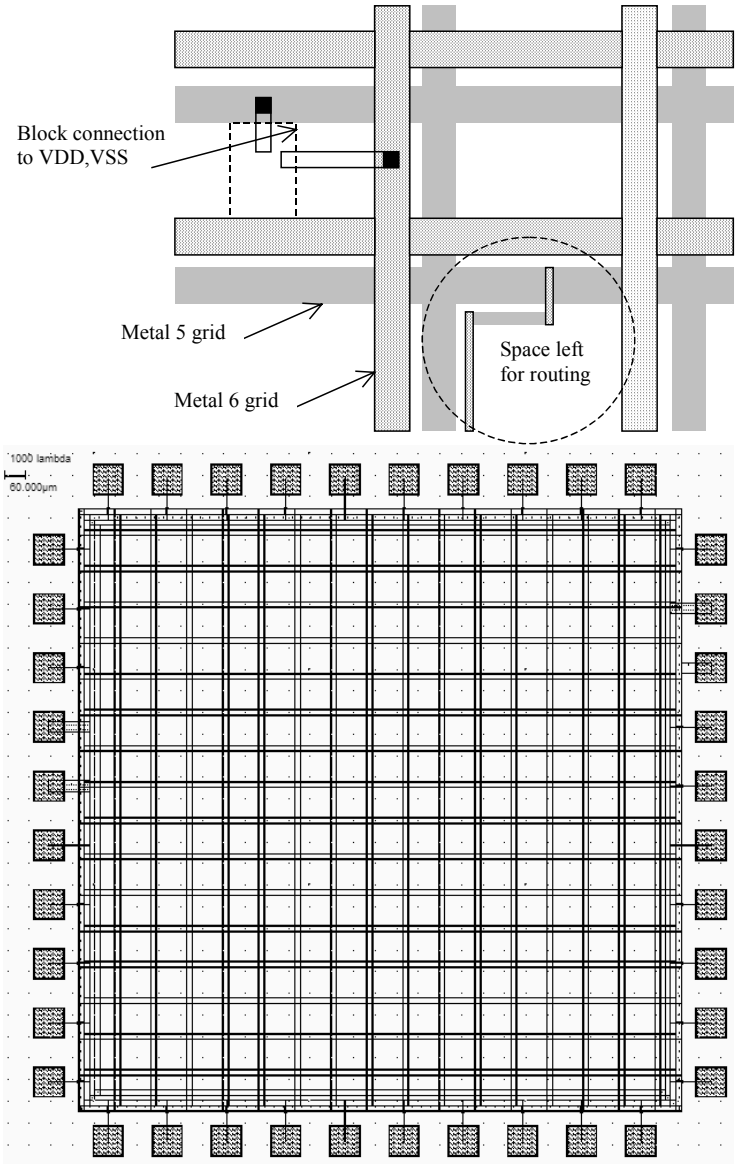


Figure 14-11: The supply rails are routed in metal5 and metal6 with a regular grid to provide power supply in all regions of the integrated circuit

A complex logic core may consume amperes of current. In that case, the supply lines must be enlarged in order to handle very large currents properly. The usually design approach consists in creating a regular grid structure, as illustrated in figure 14-11, which provides the supply current at all points of the integrated circuit. In that test circuit, the VDD supply is assigned to metal5, VSS to metal 6. These upper layers are thicker than lower metal layers and consequently can drive larger currents. The grid spacing is around 100µm, and each supply conductor width is around 5µm. Enlarging the supply width would reduce the routing area. Reducing the supply width would limit the current drive.

Metal Slit

Certain precautions should be taken when enlarging metal lines larger that 20µm. The coefficients of thermal expansion of SiO2 and metal are significantly different: 0.5 ppm/°K for SiO2, 2.8 for Silicon and 23 for aluminum. The stress accumulated during important temperature variations may break the large metal traces and crack oxides [Hastings][Shimokura]. Metal tracks less than 20µm width do no suffer such problems. The automatic layout generation tools in Microwind do not take this effect into account. The correct design in the case of large metal tracks is shown in figure 14-12. Holes in the metal are inserted regularly to split the box into parallel conductors to discourage delamination and oxide cracks.

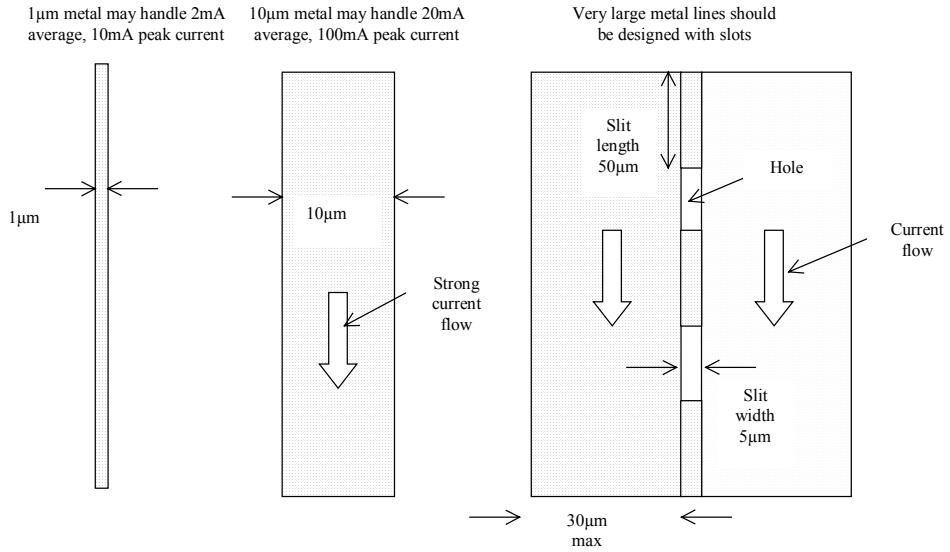


Figure 14-12: Very large metal lines are designed with slots to prevent the damages caused by thermal stress

Power line connection

The layout design of power line connections must be handled with care because of the strong current flow. An example of poor design is reported in figure 14-13 (a). Metal5 is connected to metal6 using via5. In (a), an unreliable connection is formed between metal5 and metal6 because the number of vias is too small regarding the amount of current. Remember that each via can only drive approximately 5mA average current. A better approach (b) consists in placing contacts on the border of the intersection area. The best approach (c) is to fill the crossing area with contacts. An in-depth study of power line design may be found [Clein].

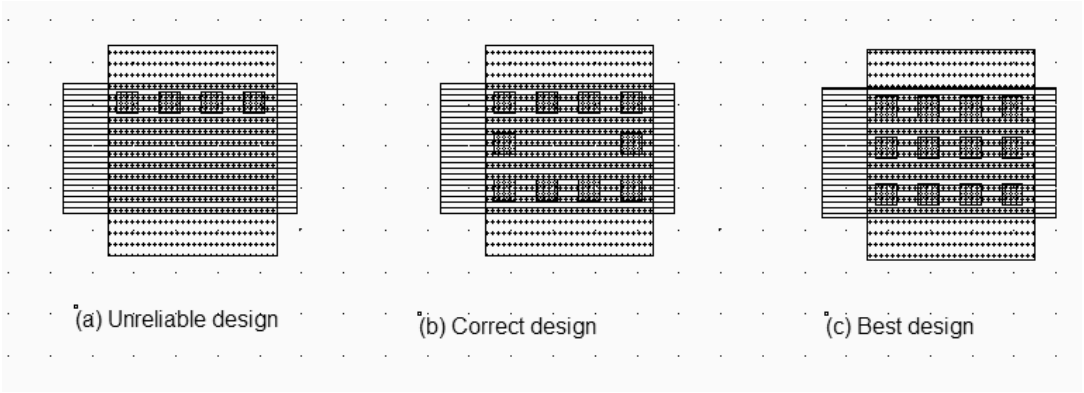


Figure 14-13: The interlayer connection using vias (ConnectLayers.MSK)

4. Input Structures

The input pad includes some over-voltage and under-voltage protections due to external voltage stress, electrostatic discharge (ESD <Glossary>), coupling with external electromagnetic sources, etc.. Such protections are required as the oxide of the gate connected to the input can easily be destroyed by over voltage. The electrostatic discharges may attain 1000 to 5000Volt, with a general shape similar to that of figure 14-14. The design of I/Os which may handle such a high voltage and which may dissipate such a high energy safely requires specific techniques which are introduced in the following sections.

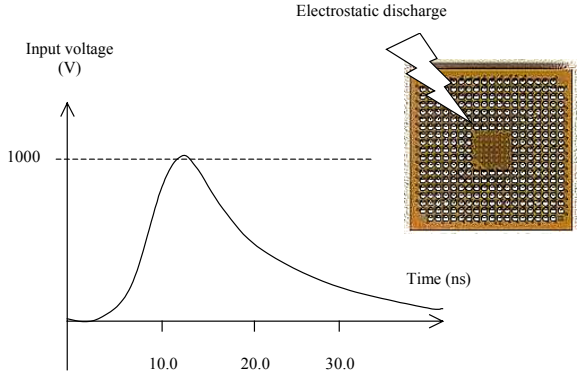


Figure 14-14: Example of electrostatic discharge on the input/output pin of an integrated circuit

One of the most simple ESD protections is made up of one resistance and two diodes (Fig. 14-15). The resistor helps to dissipate the parasitic energy and reduces the amplitude of the voltage overstress <Glossary>. One diode handles the negative voltage flowing inside the circuit (N+/P substrate diode), the other diode (P+/N well) handles the positive voltage. The combination of the serial resistor and the diode bridge represents an acceptable protection circuit against transient voltage overstress around +/-50V.

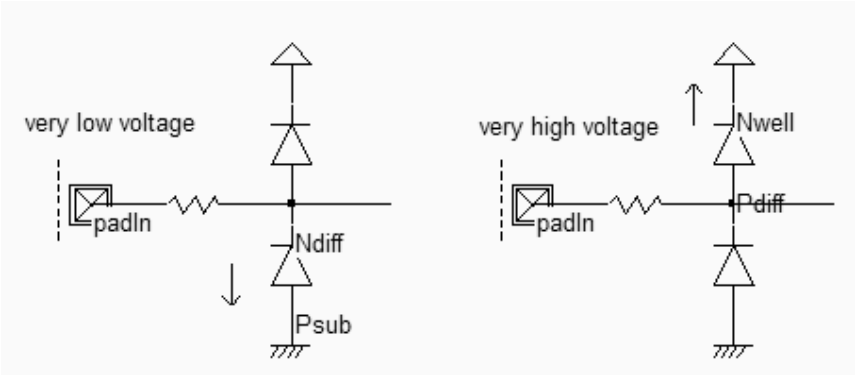


Figure 14-154: Input protection circuit (IOPadIn.SCH)

Resistor Design

Two types of resistors are available for ESD protection : polysilicon and N-well. The polysilicon resistor is completely embedded in oxide, and may therefore handle very high voltage stress. However the polysilicon is thin and its current capabilities are limited. The default salicidation of the polysilicon layer must be removed to obtain a high resistivity. The design of an ESD resistor is different from usual polysilicon resistors, mainly because of the high current, requiring an enlarged layer width and multiple contacts (Figure 14-16). The usual ESD resistance value ranges between 50 and 2000 ohm. In Microwind, the polysilicon resistor is generated by fixing the target resistance value, and enlarging the width to several µm to handle strong currents.

The major drawback of polysilicon resistor is the poor heat dissipation. The oxide has a positive role in isolating the polysilicon conductor from the rest of the circuit for over-voltages expressed in Kilo-volts. However, the same oxide plays a negative role by thermally isolating the polysilicon material which would ultimately melt because of overheating.

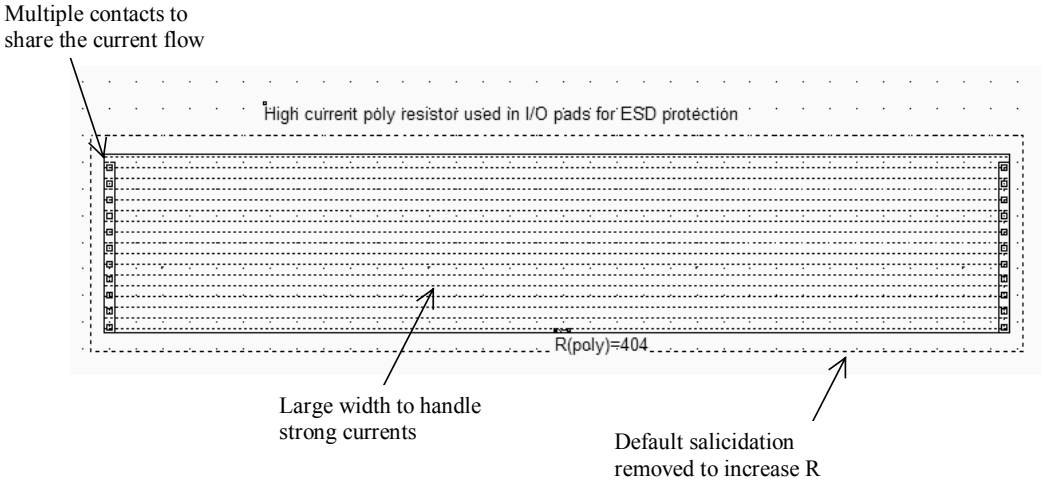


Figure 14-16: Polysilicon resistor used in input protection circuit (ResPoly.MSK)

An alternative solution consists in using the N-well as a resistor. In that case, N+ diffusion contacts are used for the electrical connection between the upper metal and the lower well area. The thermal conduction is excellent but the voltage isolation is limited by the breakdown of the junction between the N-well resistor and the P-substrate.

Diode Design

Diodes are essential parts of the ESD protection. Used since the infancy stage of microelectronics, the diodes are still widely used because of their efficiency and simplicity [Dabral]. The native diodes in CMOS technology consist of an N+ diffusion in the p-substrate and a P+ diffusion in the n-well, as shown in figure 14-17.

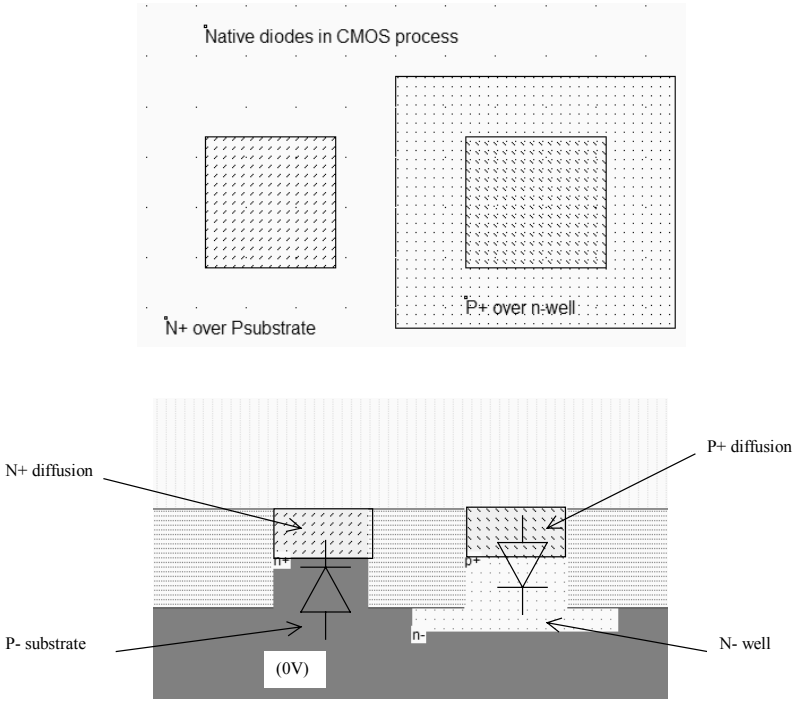


Figure 14-17: The most simple diodes in a CMOS process (Diode.MSK)

As the substrate is at 0V, the P-/N+ diode is turned on only if the N+ voltage is significantly negative (-0.5V). If the N+ voltage is higher than 0V (Which is the usual case), the diode has no effect, and can be considered as a parasitic capacitance. As the n-well is usually connected to a high voltage VDDH, the P+/Nwell diode is turned on only if the P+ voltage is higher than the I/O supply voltage VDDH (VDDH+ 0.5V, that is around 3V in 0.12µm).

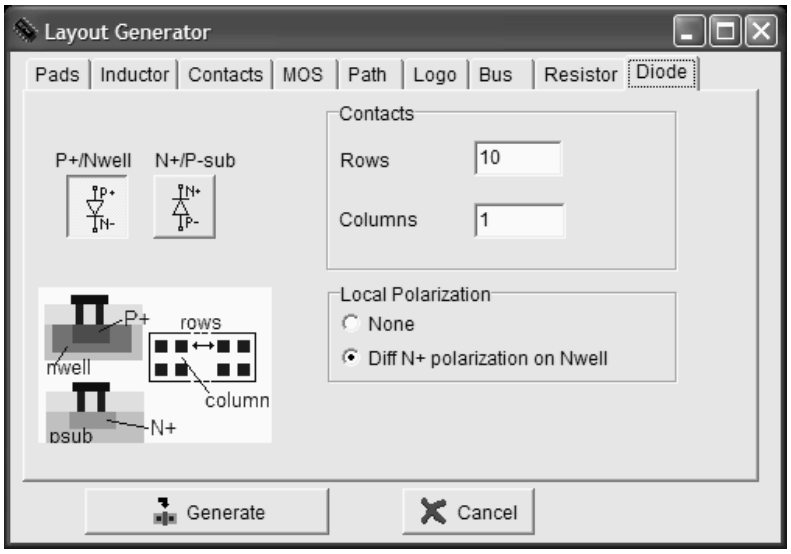


Figure 14-18: The diode generating menu in Microwind (By default a P+/well diode)

The command used to generate a protection diode in Microwind is **Edit →Generate →Diode**. Click either the P+/nwell diode or the N+/P substrate diode. By default, the diode is quite large, and connected to the upper metal by a row of 10 contacts. The N+ diode region is surrounded by a polarization ring made of P+ diffusion, as shown in figure 14-19. The large number of rows ensures a large current capability, which is very important in the case of ESD protection devices.

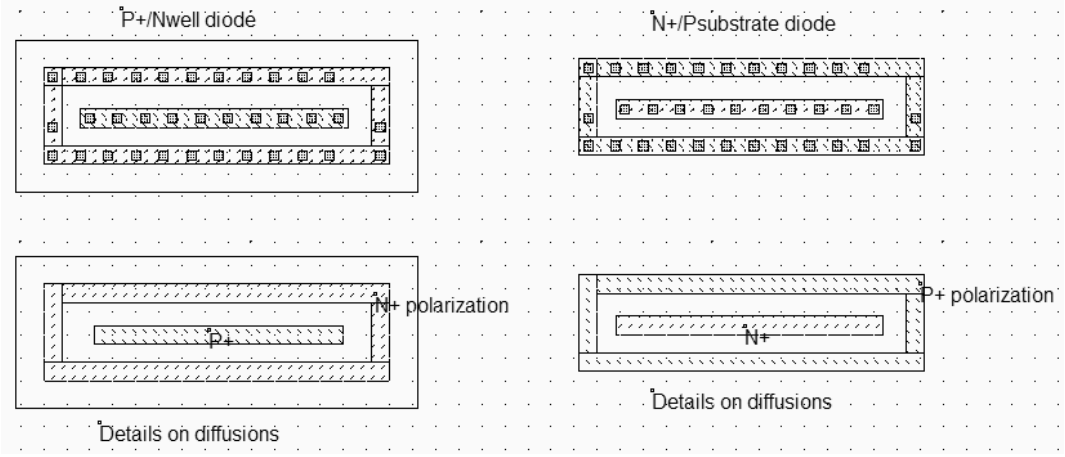
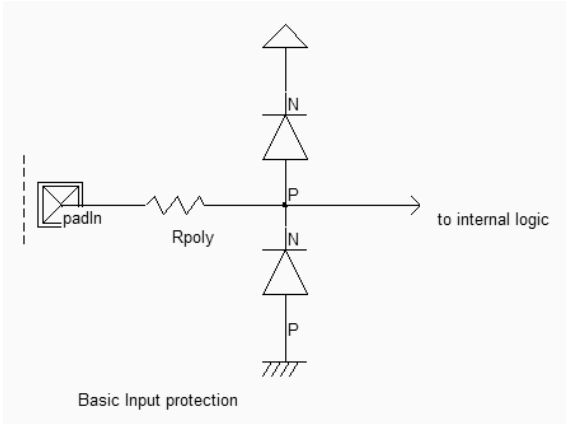


Figure 14-19: Generating a default protection diode (IODiode.MSK)



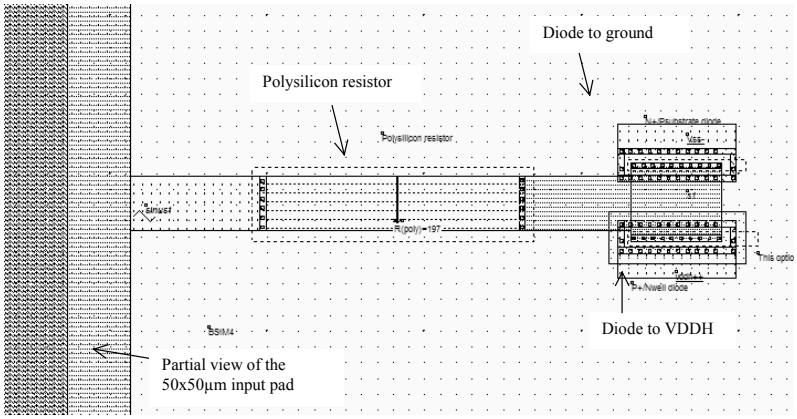


Figure 14-20: A test case to evaluate the role of diodes (IoPadIN.MSK)

A protection circuit example is given in figure 14-20. It consists of a pad 50x50µm, a serial resistor around 200 ohm and two diodes. When a very high sinusoidal waveform (+/- 10V) which corresponds to an electrical overstress is injected, the diodes exhibit a clamping effect both for the positive and negative overstress. The best simulation mode is **Voltage and Currents**. The voltage scale may be changed using the arrows on the left side of the lower voltage window. The internal voltage remains within the voltage range [0..VDDH] while the voltage near the pad is –10 to +10V wide. Notice that the current flowing in the diodes is around 1mA (Figure 14-21).

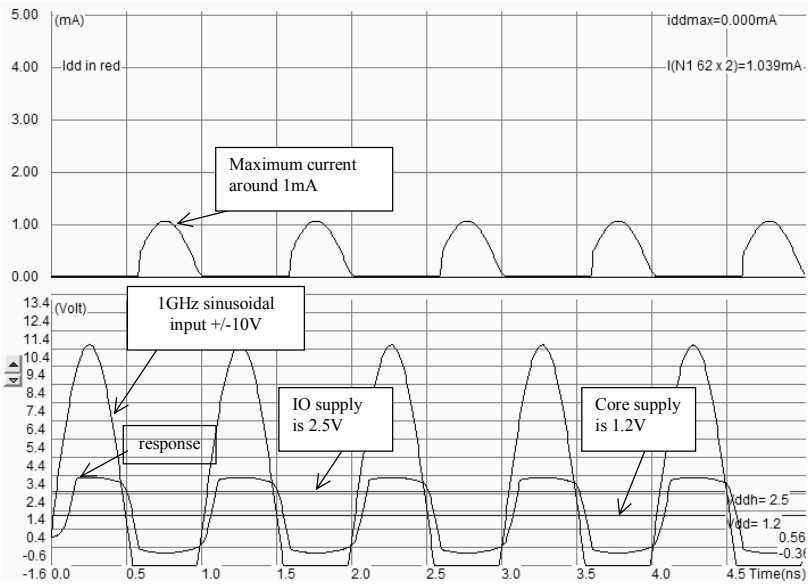


Figure 14-21: The diodes clamp the positive and negative overstress so that the internal voltage keeps close to the voltage range [0..VDDH] (IoPadIN.MSK)

Considering a real case electrostatic discharge, the voltage may rise to 1000V-5000V, which corresponds to a diode current more than 100 times larger, that is 100-500mA. Around 100 contacts would be needed for minimum reliability. In industrial case ESD protections, the diode length is approximately 50µm. Notice that the lateral surface of the diode is more important than its surface, as the current flows mainly horizontally. The design shown in figure 14-22 (b) should be preferred to the one of figure 14-22 (a) because the lateral surface is larger, meaning a better current efficiency.

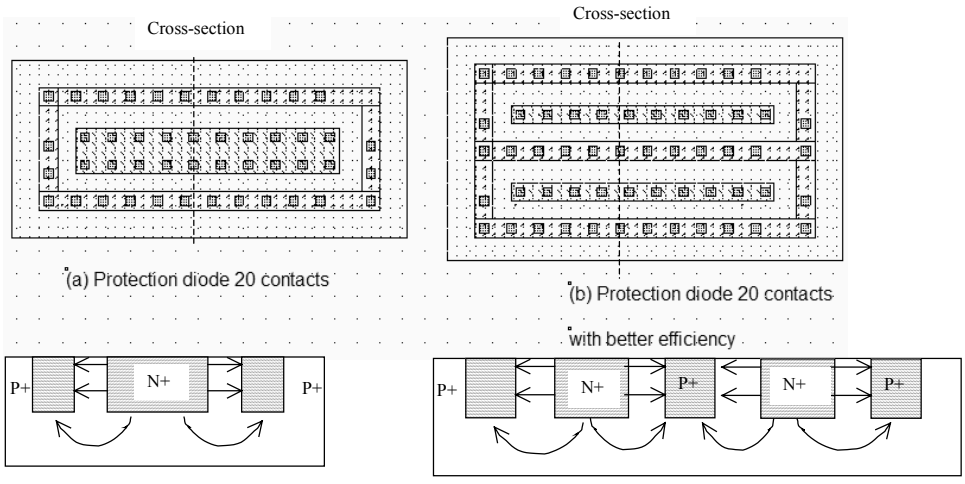


Figure 14-22: The lateral surface of the diode should be maximized for better efficiency (IODiodes2.MSK)

Clamp MOS Devices

An interesting device for electrostatic discharge prevention is described in [Dabral], called the gate-coupled NMOS. The schematic diagram of the circuit is shown in figure 14-23. It consists of two stages of protection, the first one which handles the majority of the current, and the second one which assists the first stage with relaxed stress constraints. Such protections can handle 5-7KV (Kilo-volt) ESD stress, with several design iterations and experimental testing.

The *C1-R1* circuit is a high pass filter. By default the voltage of node *Ng* is zero, due to the weak tie to VSS. A very sharp over-voltage such as the one created by an electrostatic discharge induces a positive voltage on node *Ng* which turns on the clamp MOS by capacitance coupling. A current path is established between the pad and the ground, until the voltage of *Ng* goes below the threshold voltage. Finally, the clamp is turned off and the ESD charges are eliminated. Note that a nominal rise edge from 0 to VDD should not turn on the clamp. Therefore, C1 and R1 must be chosen to eliminate the ESD pulse while keeping quiet in presence of logic edges.

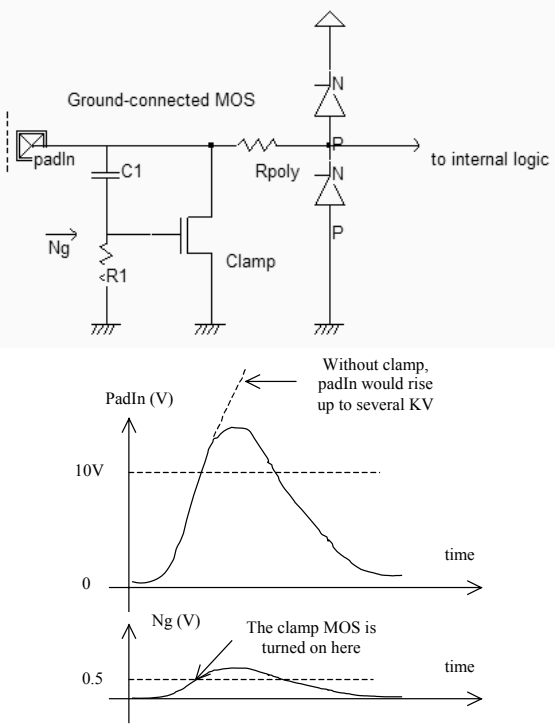


Figure 14-24: The ground-connected MOS turns on and short cuts the over voltage at a very sharp rise edge of the input voltage, such as in an ESD pulse (IOPadIn.SCH)

A lot of subtle layout issues rise with the implementation of high performance electrostatic discharge protections, as described in [Wang]. The clamp MOS is a good example of specific layout techniques for optimized behavior when faced to overstress. The driving idea is to keep the parasitic current flow straight from the input pad to the ground. A double oxide MOS device (See next section) is used to handle strong voltage stress. The diffusion connected to the pad is enlarged to create a small serial resistance which is used as a ballast (Figure 12-25). The salicidation of the drain and source is generally removed to increase this ballasting effect.

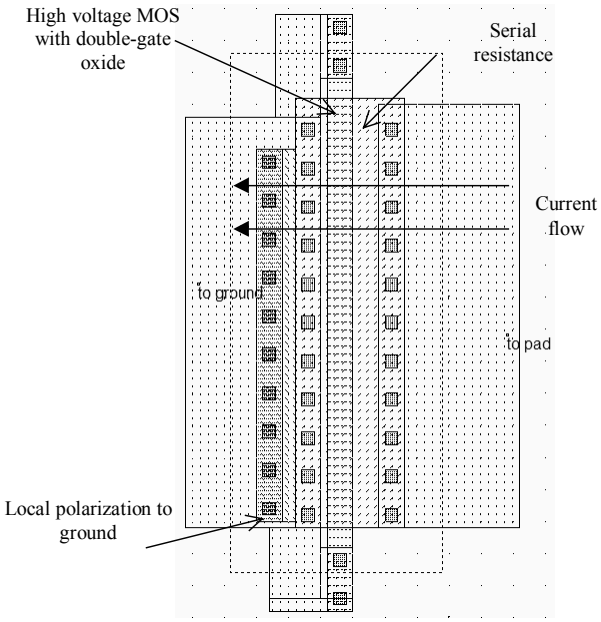


Figure 14-25: Specific layout of the gate-grounded MOS used in advanced input pads (ggMos.MSK)

Zener Diode

The Zener diode is equivalent to a normal diode, but has a particular behavior in invert mode, as it turns on for a very negative *VPN* voltage, that is a very high *padIn* voltage. The characteristics of the Zener diode are shown in figure 14-26. For positive *VPN*, the diode is in direct mode, for negative *VPN*, the diode is off. However, when *VPN* is strongly negative (Less than *VZ*), the diode is turned on again, with a so-called Zener effect. The diode layout is also shown in figure 14-26. An option layer configured to extract the diode surrounds the diode area (Dot rectangle in the layout). The diode model parameters are derived from the BSIM4 model, and are not accessible to the user. In contrast, the surface of the diode has a direct impact on its characteristics.

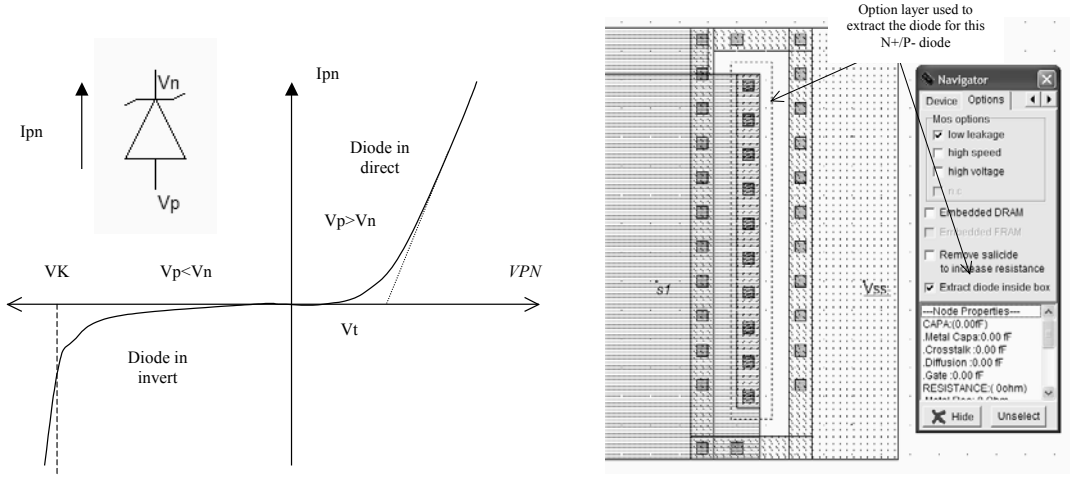


Figure 14-26: The Zener diode (IOPadZener.MSK)

Turning back to the input protection circuit, a significant increase of the pad voltage corresponds to a negative increase of *Vpn*. When passing the *VK* limit, the Zener diode is turned on and the charges start to flow through the substrate to the ground.

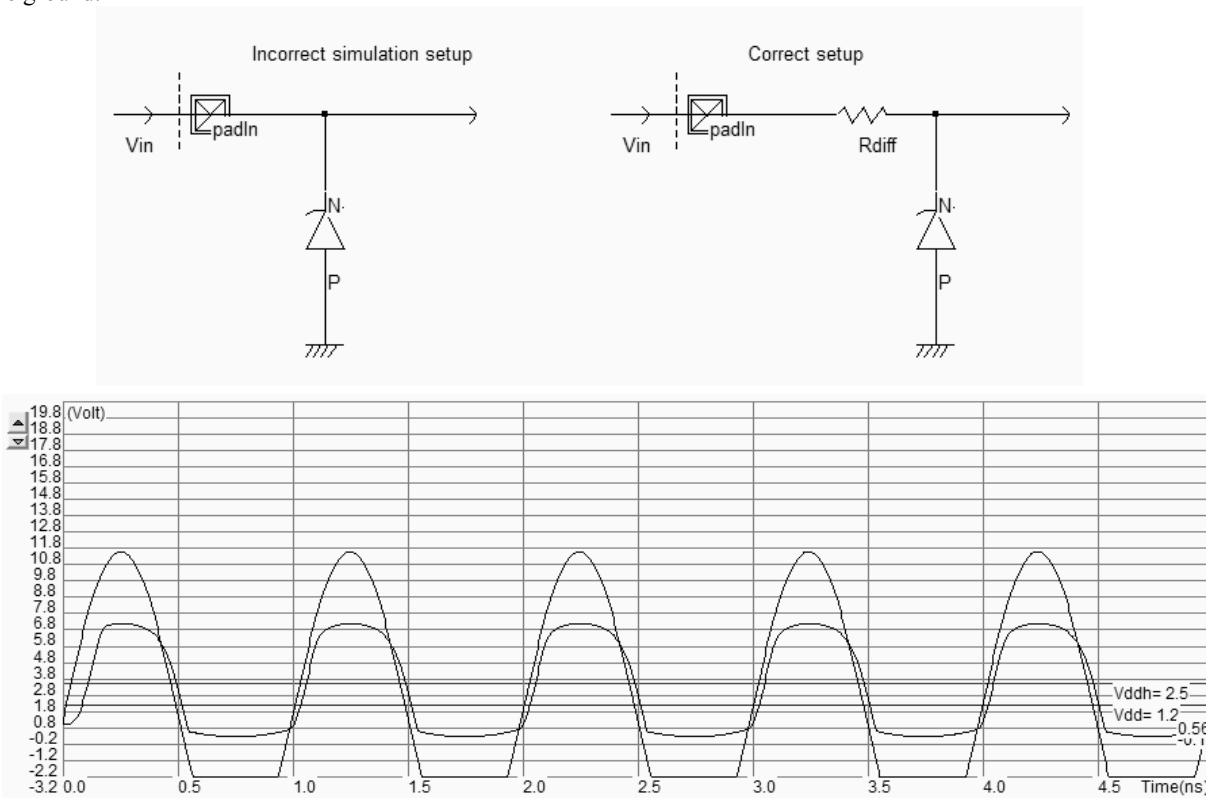


Figure 14-27: The Zener effect can be seen for positive overstress (IOPadZener.MSK)

The simulation of the Zener diode as a protection circuit is proposed with the schematic diagrams of figure 14-27. The simulation setup proposed on the left is incorrect as the direct connection of the voltage source to the Zener diode also forces the output voltage so that no clamp effect can be seen. In contrast, the serial resistor *Rdif* of the right figure creates the required impedance between the voltage source and the output to enable the observation of the Zener effect. The diode model used in Microwind includes the Zener effect if the simulation is performed in BSIM4 mode. In the simulation of figure 14-27, the large positive voltage provokes the necessary conditions for a negative *VPN* and consequently a Zener clamp. The diode in direct mode is observed for negative input values, which corresponds to positive *VPN*.

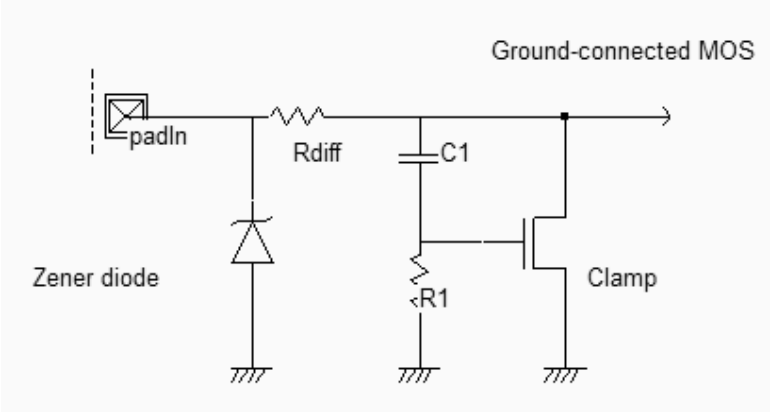


Figure 14-28: An input pad protected with a Zener diode and a diffusion resistor (IOPadIn.SCH)

An input protection circuit which combines the Zener diode as a primary protection circuit , the ground-connected MOS and a secondary protection circuit is proposed in figure 14-28. Such structures may handle severe ESD stress, as well as other parasitic transient pulses found in industrial applications.

High voltage MOS

The general diagram of an input structure is given in figure 14-29. A high voltage buffer is used to handle voltage overstress issued from electrostatic discharges. The logic signal is then converted into a low voltage signal to be used in the core logic. For interfacing with input/output, specific high voltage MOS are introduced. These MOS devices are called high voltage MOS. They use a double gate oxide to handle the high voltage of the I/Os. The thin oxide used for internal logic devices would be damaged by the high I/O voltage. In DSCH, the high voltage devices are drawn with a double line. The symbol *Vdd_HV* represents the I/O voltage, which is usually 2.5V in CMOS 0.12µm.

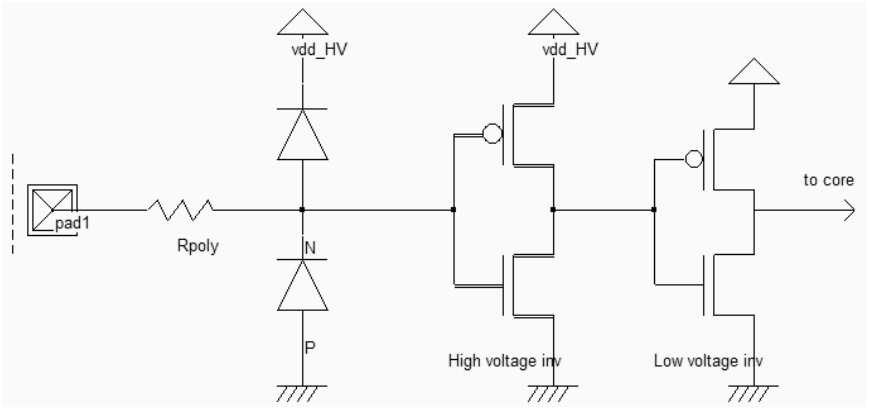


Figure 14-29: The basic principles for an input circuit, including the ESD protection and the voltage translator (IOPadIn.SCH)

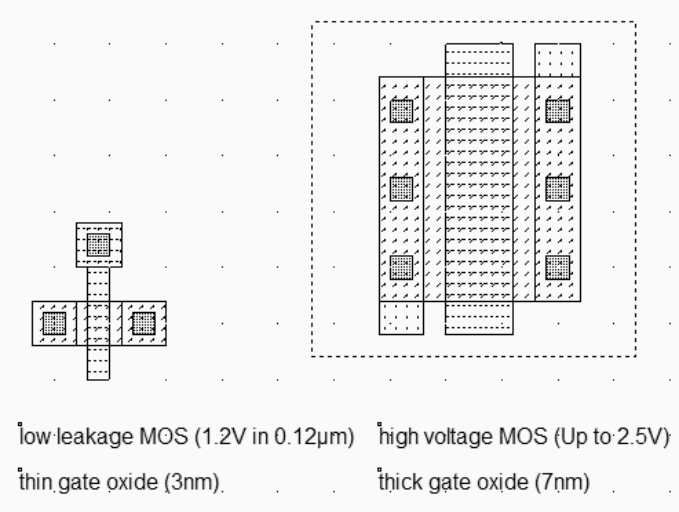


Figure 14-30: High voltage MOS device vs. normal MOS (MOSHighVoltage.MSK)

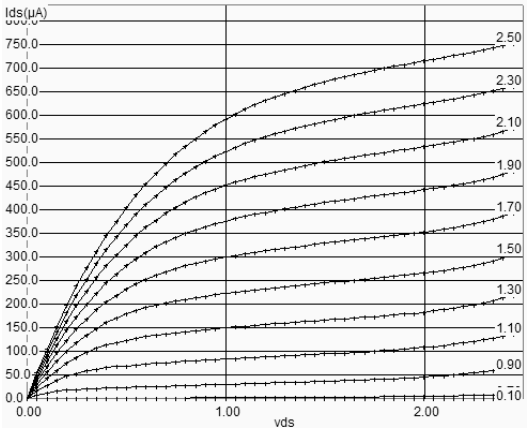


Figure 14-31: Static characteristics of the high voltage MOS (MOSHighVoltage.MSK)

The high voltage MOS layout differs slightly from the normal MOS, as shown in the comparative layout view of figure 14-30. The high voltage MOS uses a gate width which is much larger than that of the regular MOS. Usually, the lateral drain diffusion, which aims at limiting the hot-carrier effect at boosting the device lifetime, is removed in high voltage MOS devices. It has been shown that lateral drain diffusion degrades the ESD protection performances [Wang]. One reason is the lower efficiency of LDD devices in enabling strong currents to flow in the channel. Consequently, LDD device are slower to evacuate the parasitic energy. The gate oxide thickness is twice the oxide of the core logic. In 0.12µm, the gate oxide of the high voltage MOS is around 5nm, while the core MOS is 2nm.

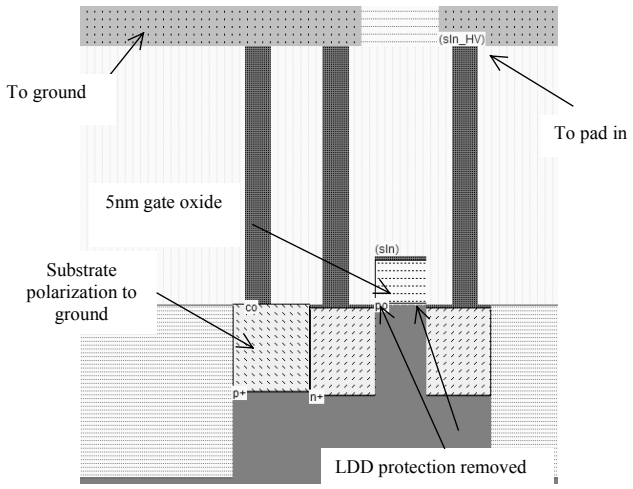


Figure 14-32: The particularities of MOS devices used in input pads: removed LDD and double gate oxide (IOPadMos.MSK)

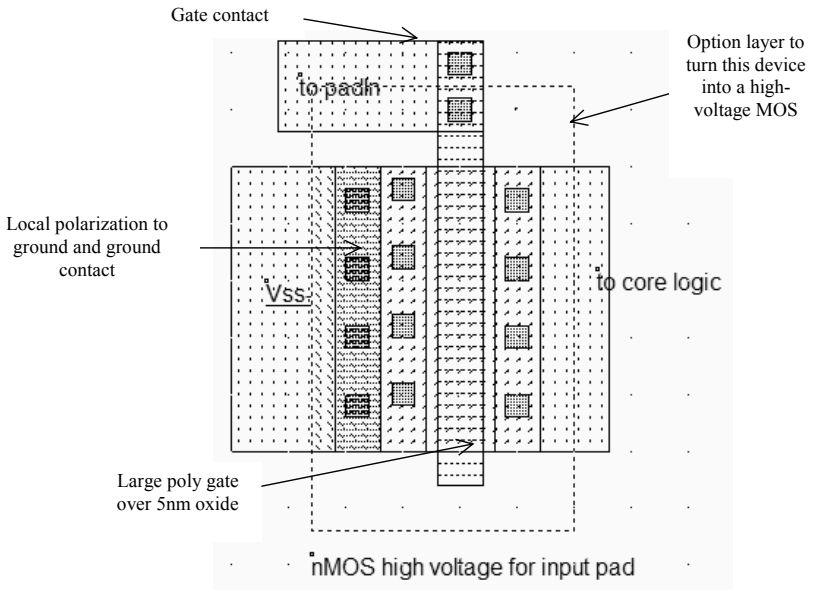


Figure 14-43: Layout of the input MOS device (IOPadMos.MSK)

The bird's view of the layout (Figure 14-43) reveals that the polysilicon gate is not the usual 2-lambda length. In the case of high voltage MOS devices, the minimum length is 4 lambda. The 2 lambda sizing is not compatible with the double gate oxide and the high voltage operation. The gate oxide is twice thicker than the low voltage MOS. The high voltage device performance corresponds approximately to a 0.25µm MOS device. To turn a normal MOS into a high voltage MOS, the designer must add an option layer (The dot rectangle in figure 14-43). The tick in front of **High voltage MOS** (Figure 14-44) assigns high voltage properties to the device : double oxide, removed LDD, different rules for minimum length, and different MOS model parameters.

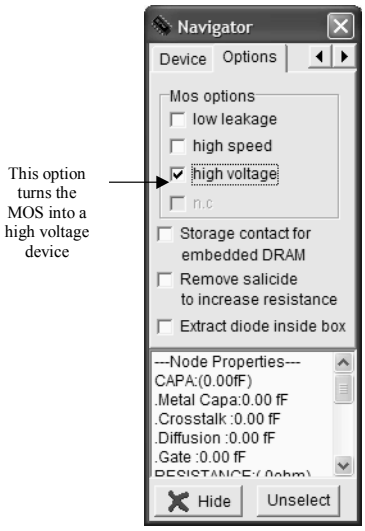


Figure 14-44: Handling the high voltage property through the option layer (IOPadMOS.MSK)

The simulation of the complete input pad is proposed with the schematic diagram of figure 14-45. A slow sinusoidal waveform *DataIn* (10MHz) is generated between 0 and 2.5V, with an additive noise. The noise is a random number mainly concentrated between –1 and +1 V, with a Gaussian distribution. The noise contains virtually all frequencies spread uniformly from very low to very high frequencies. The noise input passes through the serial polysilicon resistor of around 330Ω, then through the two diodes and serves as the input for the high voltage inverter. The output *SinHV* is connected to the low voltage inverter.

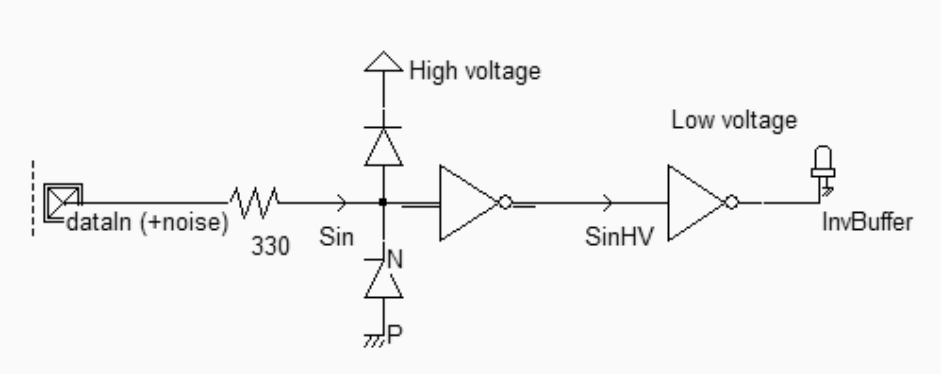


Figure 14-45: Simulation of an input structure with voltage translation from high to low voltage (IOPadIn.SCH)

Click **Add Noise** in the sinusoidal parameter window to activate the noise generation in addition to the desired signal. The Gaussian noise model gives a good approximation of ambient noise (Figure 14-46). The RMS amplitude is derived from an evaluation of the Root-Mean-Square of the noise sampled data *noise[n*]. The RMS voltage is given by equation 14-1. It gives a good indication of the envelope of the noise, as the exact amplitude may not be determined due to the random nature of the signal.

$$Vrms = \sqrt{\frac{\sum_{i=0}^{n} (noise[i])^2}{n}} \qquad \text{(Equ. 14-1)}$$

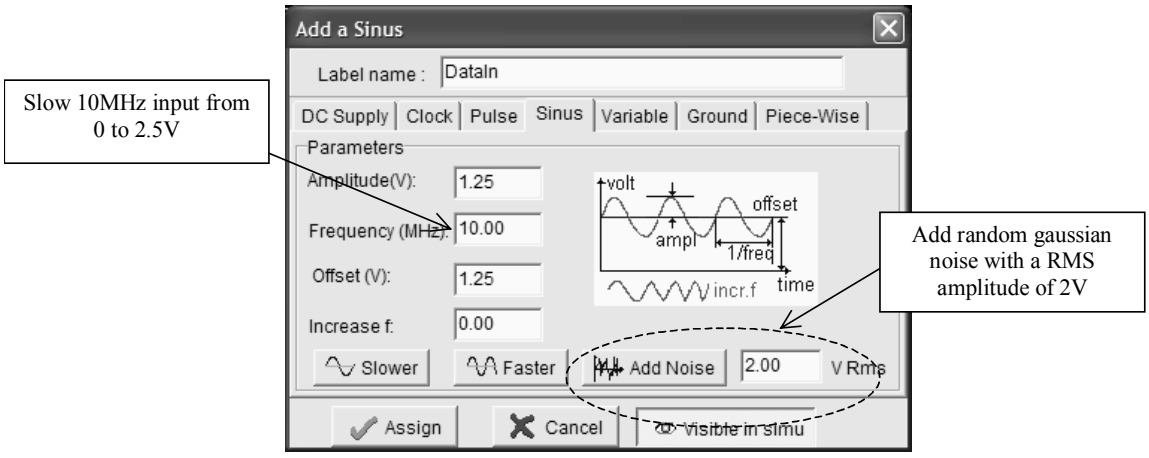


Figure 14-46: Handling the high voltage property through the option layer (IOPadMOS.MSK)

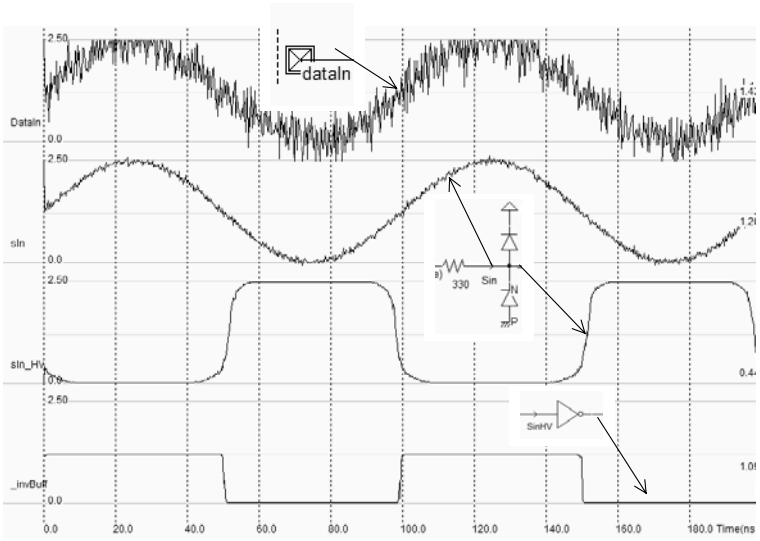


Figure 14-47: Simulation of a noisy input and the response of the input buffer (IOPadInInv.MSK)

The simulation shown in figure 14-47 gives an interesting insight of the signal propagation within the input pad. First, the noisy sinusoidal waveform is significantly filtered by the serial resistance and the parasitic diode capacitance. The noise amplitude of signal *Sin* is greatly reduced. However, due to the slow rise and fall of the input signal, a risk of parasitic glitch may appear. The signal Sin_HV gives a logic translation of the input voltage which is converted to a low swing signal *Inv_buff* by the low voltage inverter.

Input pad with Schmitt Trigger

Using a Schmitt trigger instead of an inverter helps to transform a very noisy input signal into a clean logic signal. The Schmitt trigger circuit switches at different thresholds, in order to increase the noise margin of the input buffer. The main difference between the inverter and the Schmitt trigger appears in the simulation shown in figure 14-48.

While the inverter may transform a noisy input into several glitches at the output near the commutation point of the inverter, the Schmitt trigger produces one single commutation.

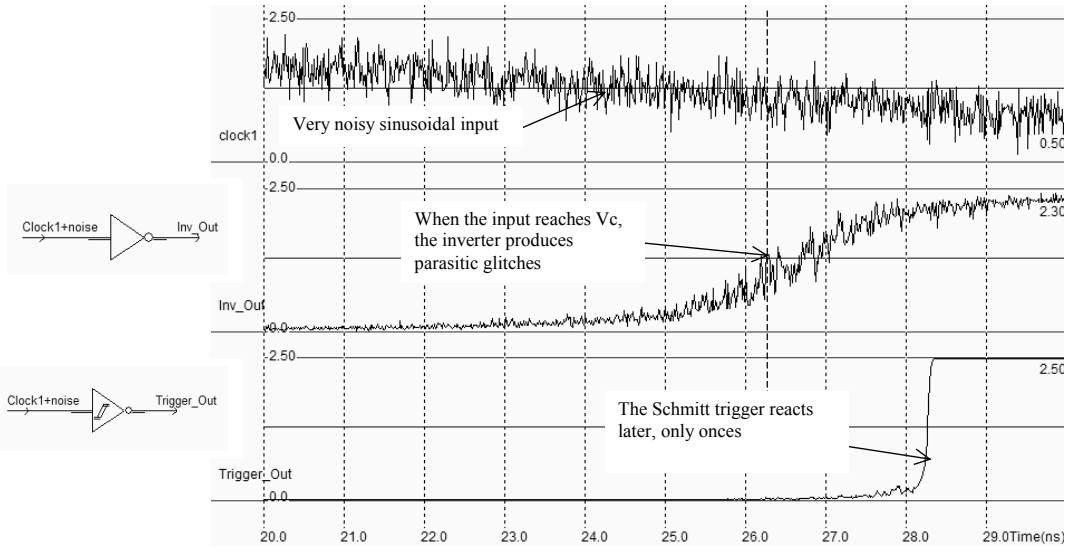
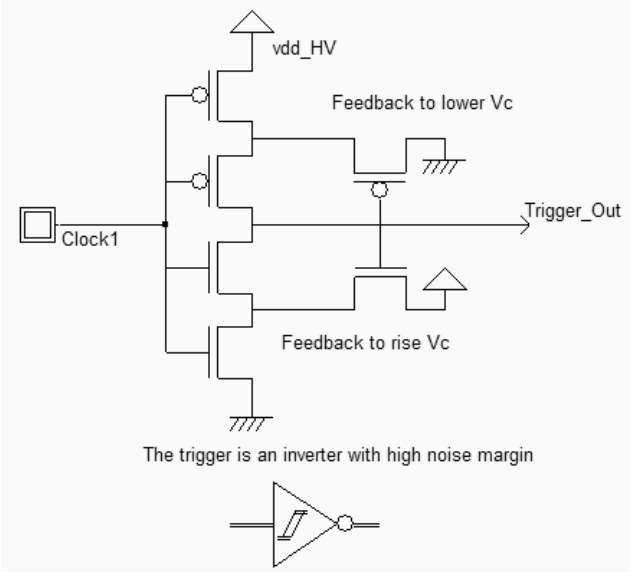


Figure 14-48: The filtering effect of the Schmitt trigger with a noisy input signal (TriggerCompInv.MSK)

The schematic diagram of the trigger is proposed in figure 14-49 [Bellaouar]. A brilliant idea lies beyond this circuit - it is based on a modification of the commutation point, thanks to feedback MOS devices. The pMOS feedback device adds a path to ground when *Trigger_Out* is low. Consequently, the threshold voltage is lowered to a commutation point *Vc_low*, lower than the commutation point of a regular inverter V_C. The nMOS feedback device adds a path to *VDD_HV* when *Trigger_Out* is high. Consequently, the threshold voltage has risen to *Vc_high*, higher than the commutation point V_C.



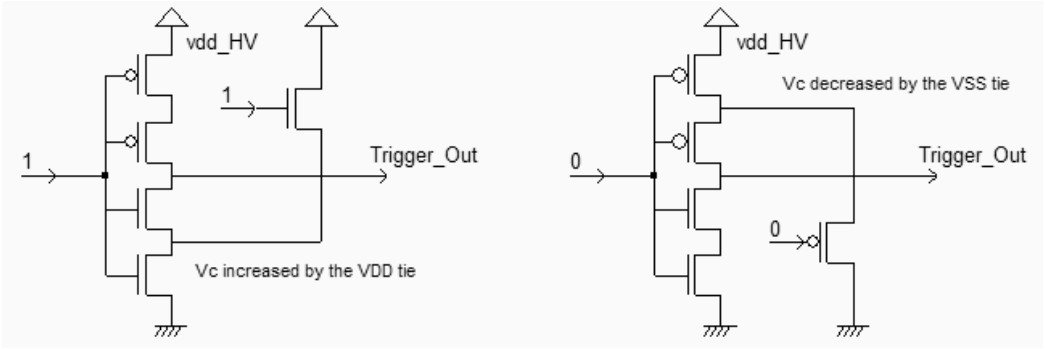


Figure 14-49. Schematic diagram of the trigger (Trigger.SCH)

The layout of the trigger is shown in figure 14-50. The feedback MOS devices are situated on the right of the trigger core. An inverter is added for comparison. The most demonstrative simulation is probably the compared static characteristics of the inverter and the trigger (Figure 14-51).

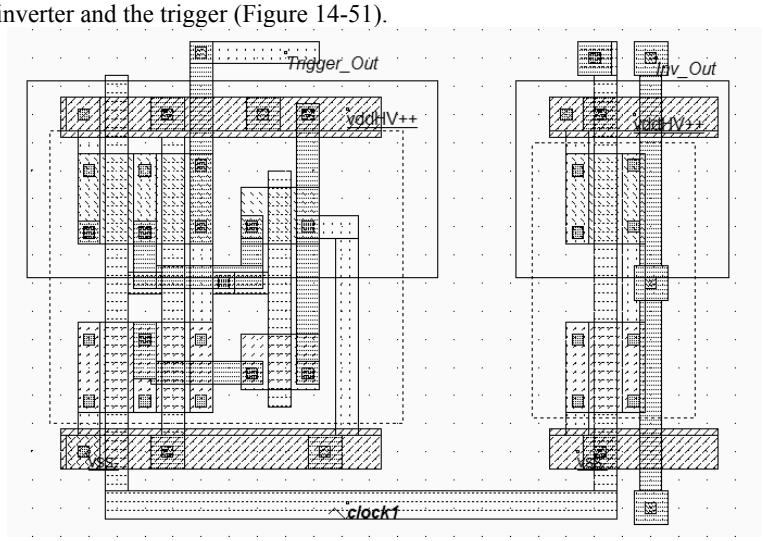


Figure 14-50. Layout of the trigger and the inverter, using high voltage MOS devices (TriggerCompInv.MSK)

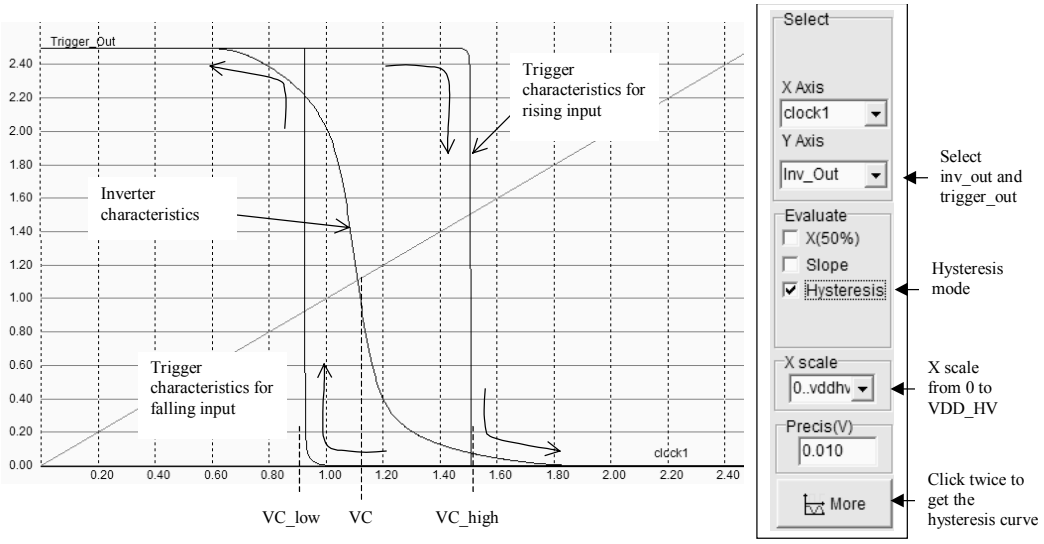


Figure 14-51. Static characteristics of the trigger compared to the inverter (Trigger.MSK)

The static simulation is available in **Voltage vs. voltage** mode. Firstly, the X scale must be adjusted to 0..*VDD_HV*. Secondly, the hysteresis mode must be activated: at each simulation, the input signal is either decreased or increased. Finally, the trigger characteristics may be added to the inverter by changing the selected output.

5. Digital Output Structures

The role of the output buffer is to ensure that the signal coming out of the integrated circuit (IC1 in figure 14-52) is propagated safely to the receiver which is usually the input of a second integrated circuit (IC2). The emitter signal comes from a low voltage inverter *Inv_out1*. In 0.12µm, the voltage range is [0..1,2V]. Most I/O interfaces operate at high voltage (2.5 or 3.3V) for compatibility and speed reasons, as well as robustness to parasitic interference as described in part 4. The signal is transformed into a high voltage signal through the inverter *Inv_Out2* [0..2,5V] which is directly connected to the pad and to the outside world. The signal goes through the package, the printed circuit board, and the the other package which is represented by a transmission line. At the far end of the transmission line, we find the input structure of a receiving integrated circuit IC2, consisting of an inverter *Inv_In1*, working at high voltage, and of *Inv_In2*, working at low voltage.

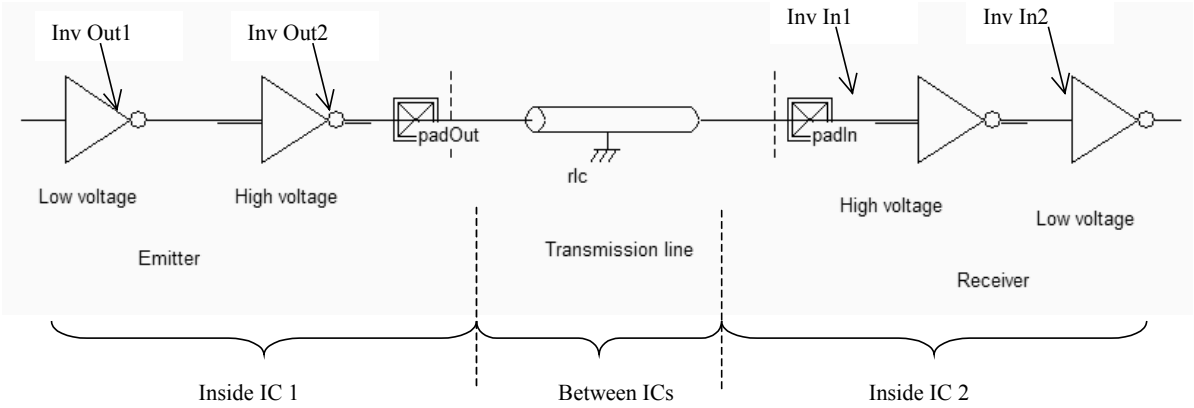


Figure 14-52: The signal propagation between integrated circuits IC1 and IC2

Output Buffer

The schematic diagram of the basic output buffer is given in figure 14-53. A very simple structure is used to protect the output buffer from electrostatic discharge, and more generally from any over or under voltage. A Zener diode may be used, or a set of two diodes, as for the input pad.

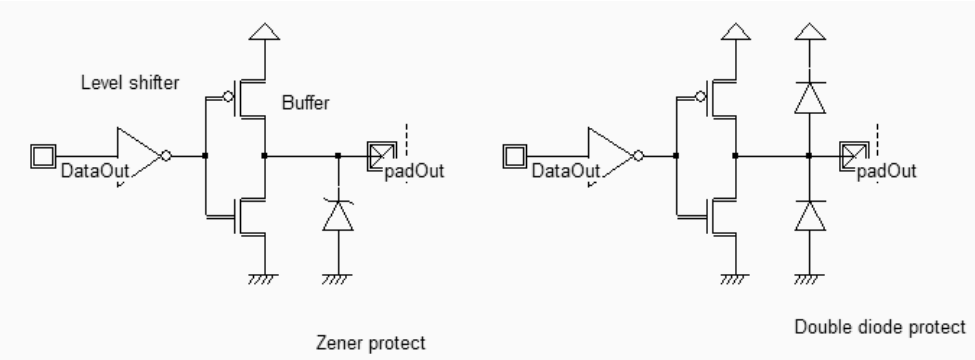


Figure 14-53: The output buffer design including the protection against electrostatic discharge (IOPadOut.SCH)

Level shifter

The role of the level shifter is to translate the low voltage logic signal *Data_Out* into a high voltage logic signal which controls the buffer devices. An immediate solution would consist in using a high voltage inverter as a level shifter. The signal *Data_Out* has a 1.2V voltage amplitude, as shown in figure 14-54.

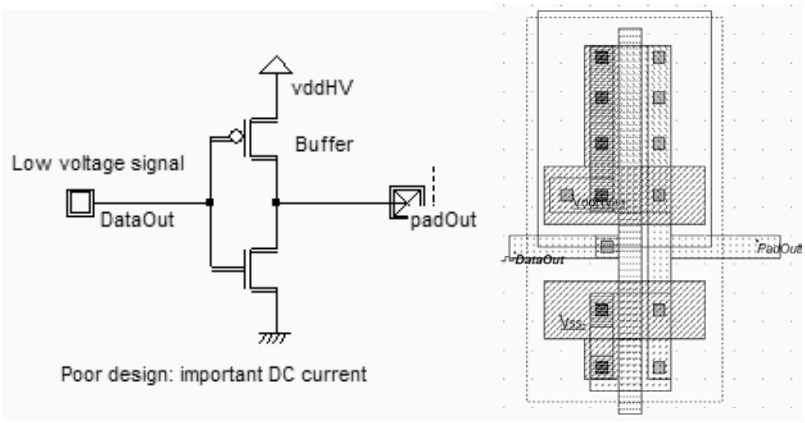


Figure 14-54: The inverter used as a level shifter (LevelShiftBad.MSK)

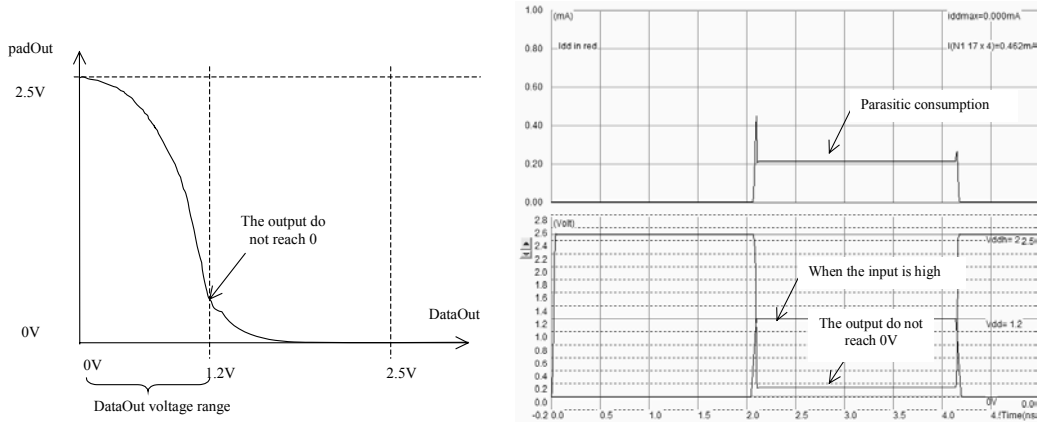


Figure 14-55: Analog simulation of the inverter showing the parasitic DC consumption (LevelShiftBad.MSK)

In the simulation shown in figure 14-55, the output signal *PadOut* is almost correct, except that the low level is not exactly zero. This is due to the input voltage limit to 1.2V. In the inverter characteristics (Figure 14-55 left), the input voltage 1.2V is not sufficient to obtain a "good" zero on the output. The important consequence of this incomplete switching is the large DC dissipation on a high level of *DataOut*, in the range of 200 micro-watts. Since this parasitic consumption appears at a low logic level, the sum of DC currents in the case of a 1000 pin integrated circuit would approach a fraction of ampere, which is not acceptable.

Figure 14-56 gives the schematic diagram of a level shifter circuit which has no problem of parasitic DC power dissipation. The circuit consists of a low voltage inverter, the level shifter itself and the buffer. The circuit has two power supplies: a low voltage *VDD* for the left-most inverter, and a high voltage V*ddHV* for the rest of the circuit.

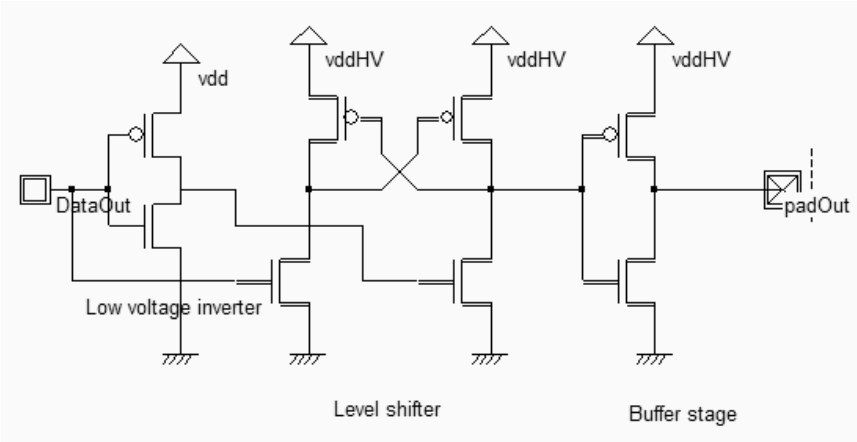
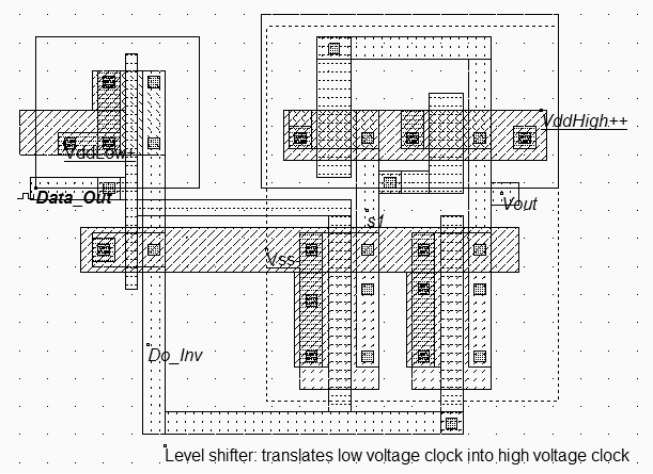


Figure 14-56: Schematic diagram of a level shifter (IOPadOut.SCH)

The layout of the level shifter is shown in figure 14-57. The left part works at low voltage 1.2V, the right part works with high-voltage MOS devices, at a supply of 2.5V (*VddHigh*). The data signal *Data_Out* has a 0-1.2V voltage swing. The output *Vout* has a 0-2.5V voltage swing. This time, no DC consumption appears except during transitions of the logic signals, as shown in the simulation of figure 14-57.



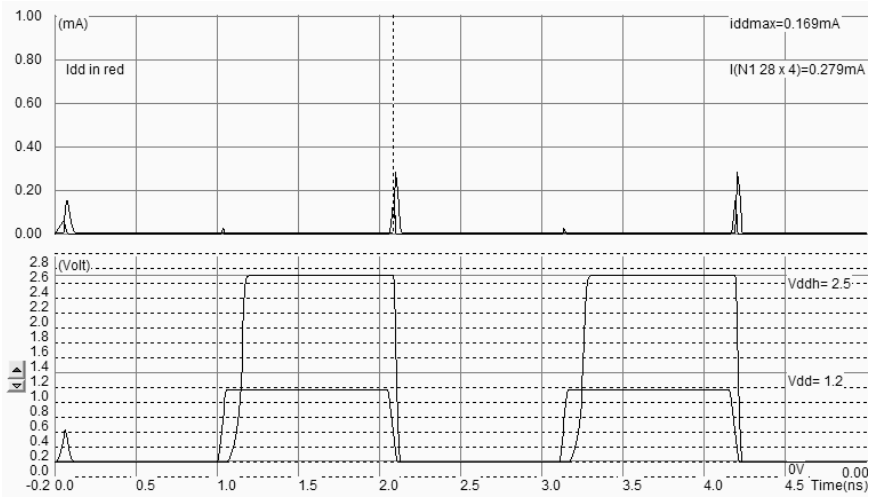


Figure 14-57: Layout and simulation of the level shifter (LevelShift.MSK)

Output MOS devices

The role of the output buffer is to amplify the logic signal generated by the level shifter in order to switch at the appropriate speed, which depends on the target application. Usually, the buffer stage is built from several MOS devices in parallel, in order to achieve maximum Ion current of 2,4,8 or 16mA.

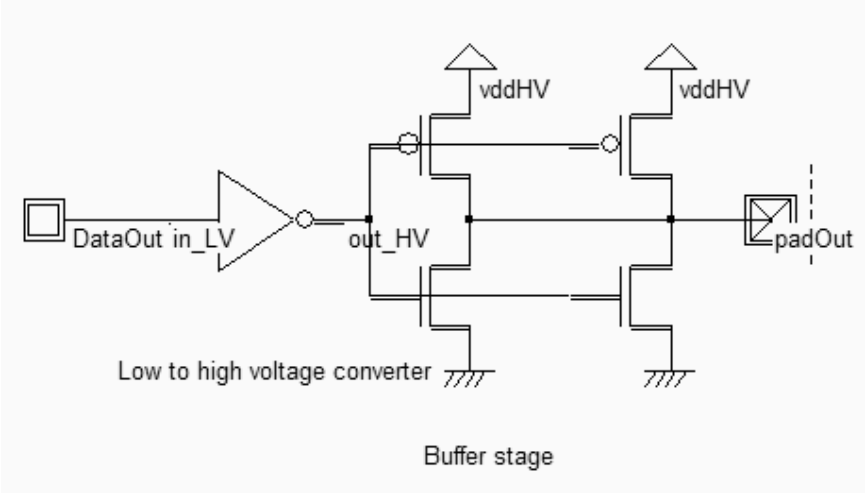


Figure 14-58: The schematic diagram of the buffer stage (IOPadOut.SCH)

The buffer stage is connected to the output of the high voltage inverter, called *Out_HV* in figure 14-58. Usually, several MOS devices are connected in parallel to achieve a large current flow in order to drive efficiently the large capacitance of the output node. The MOS devices with parallel fingers can be generated by Microwind, using the MOS generator shown in figure 14-59. Assuming that the target current is 4mA, what we need is 2 fingers, the high-voltage MOS option, the minimum length 0.24µm for this type of device, and a width adjusted to 2.5µm. Notice that Microwind also generates a set of polarization contacts, appearing on the left side of the MOS device, for a good connection to ground. The maximum current of typical MOS devices (High voltage option) is listed in table 14-1.

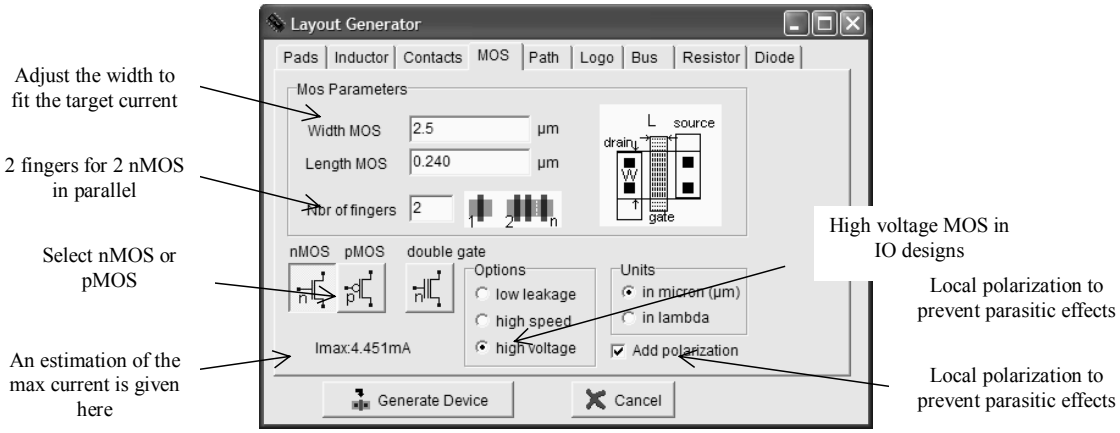


Figure 14-59: The MOS device generated for output pads is high-voltage, multiple fingers, and has a large width to produce the desired maximum current.

MOS width	MOS length	IonN (mA)	IonP (mA)
1.2µm	0.24µm	0.85	0.65
2µm	0.24µm	1.3	1.0
10µm	0.24µm	7.0	5.0
2µm	0.5µm	1.1	0.6
10µm	0.5µm	5.5	3.0

Table 14-1: Maximum current of basic nMOS and pMOS I/O devices (0.12µm CMOS)

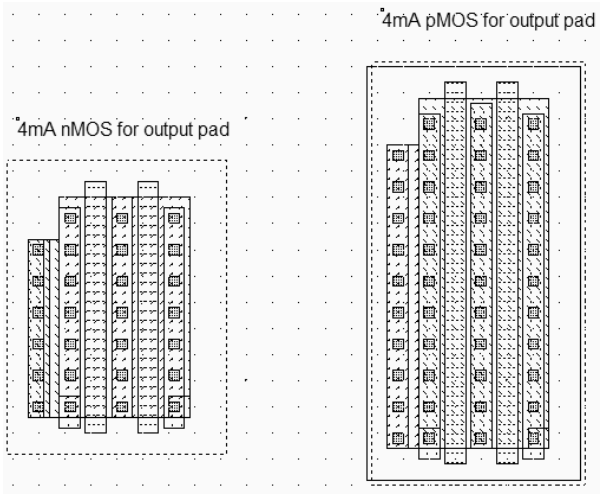


Figure 14-50: Generating multiple finger MOS devices for high current generation (IOPadMos.MSK)

The usual current drive of an output pad is 4mA. The nMOS and pMOS device that can switch 4mA are shown in figure 14-50. A high current drive is mandatory to ensure the rapid charge and discharge of the parasitic output node capacitance.

Output Buffer Simulation

Let us assume that the output pad structure drives a 5pF load, which is quite low. The *DataOut* signal is shifted again by the level shifter to a 0..2,5V signal, and serves as a command for the MOS devices in parallel, which ensures the charge and discharge of the load (Figure 14-51). The virtual capacitor of 5pF is added to the layout using the capacitor icon in the palette. The simulation reported in figure 14-52 shows a charge and discharge of this capacitor within around 3nS, which is sufficient in the case of low speed applications. In the case of a high speed signal transport, as in memory bus, the current drive must be increased.

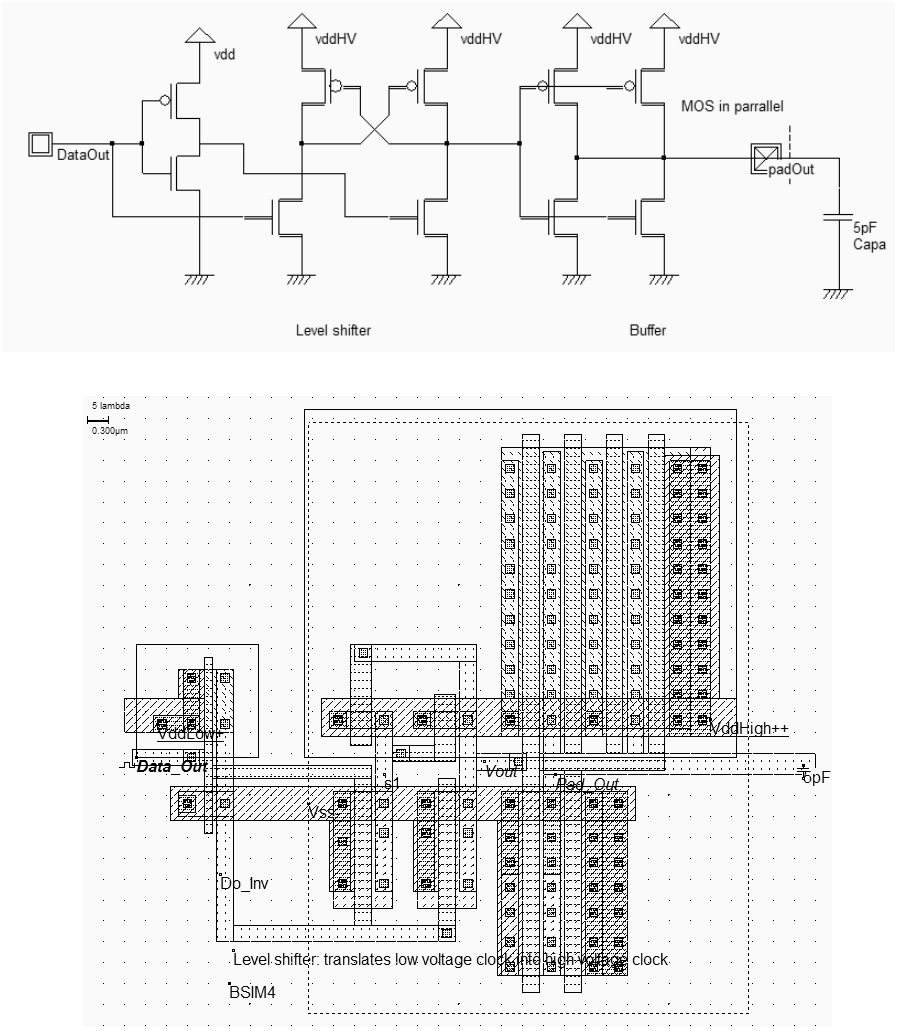


Figure 14-51: The schematic diagram of the output pad with the buffer stage, using MOS devices in parallel (LevelShiftBuff.MSK)

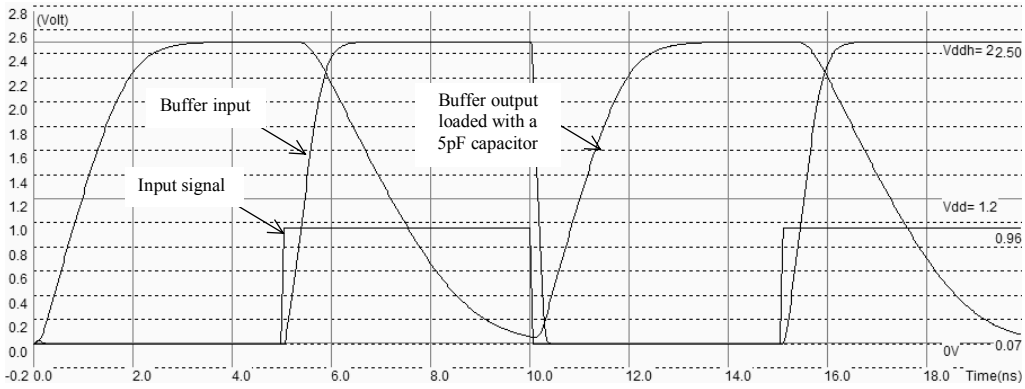


Figure 14-52: The analog simulation of the output pad loaded with 5pF (LevelShiftBuff.MSK)

Output MOS protection to ESD

To improve the robustness of the output structure to electrostatic discharge and voltage overstress, the MOS layout can be improved. Firstly, the salicidation of the drain should be removed to increase the sheet resistance from the channel to the output pad and to enhance the ballasting resistance effect which has a positive influence on ESD protection performance. The ballasting resistance is mainly used to dissipate over voltage. The salicidation of the gate and source have no impact on ESD protection. The only region that should be resistive is the drain diffusion area connected to the pad. A specific option layer is added in the MOS design of figure 14-53 to increase the serial resistance which aims at protecting the output MOS device from parasitic stress.

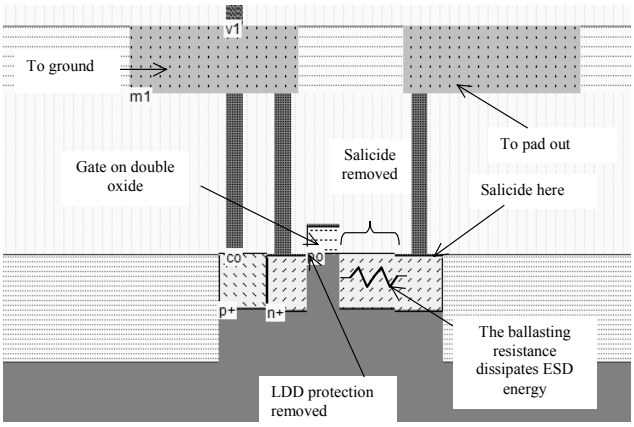


Figure 14-53: Cross-section of the MOS devices used in I/O pads (IOPadMos.MSK)

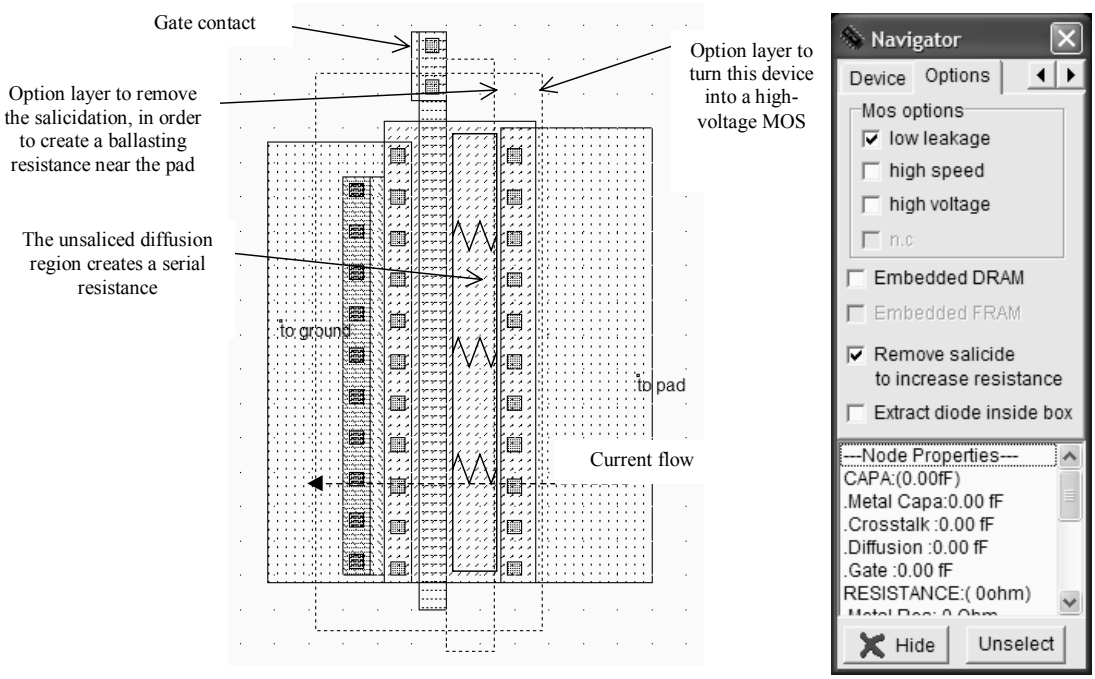


Figure 14-54: The particularities of MOS devices used in I/O pads: removed LDD, double gate oxide, and a ballast region (IOPadMos.MSK). Two option layers serve to declare the high-voltage and salicide removal options

The default salicidation causes a reduction by a factor of 10 of the serial drain resistance from the pad contact to the gate, resulting in significant protection degradation. An option layer is added to the layout covering the ballasting region, with the activation of the property **Remove Salicide** which blocks the titanium salicidation, and keeps the parasitic serial resistance intact.

3-state and Programmable Drive Buffer

The programmable drive buffer is used to adapt the current drive to the load, through a programming logic circuit. The circuit shown in figure 14-55 is able to switch the output signal *Pad_Out* with a 2mA, 4mA or 6mA current.

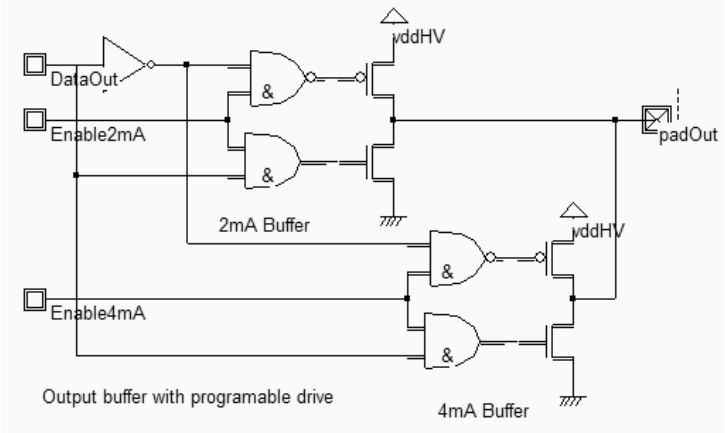


Figure 14-55: The programmable drive buffer (IOOutProgDrive.SCH)

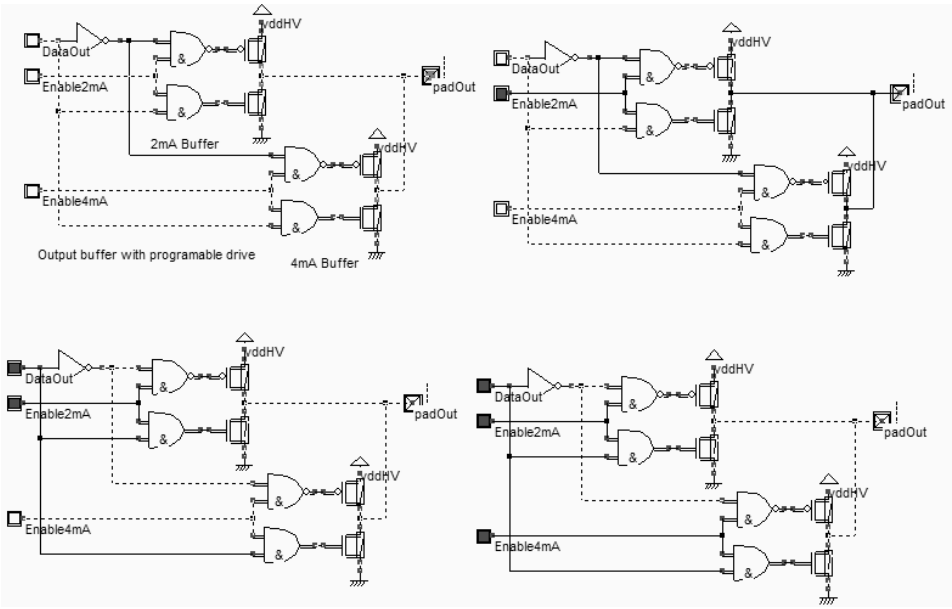


Figure 14-56: The simulation of the programmable drive buffer (IOOutProgDrive.SCH)

The nMOS and pMOS drivers are controlled independently. If all enables are inactive (Figure 14-56 top left)and all switches are off, the pad is in high impedance state. This is convenient to realize a 3-state buffer. If *Enable_2mA* is asserted, the 2mA buffer is activated (Top right, bottom left). When both *Enable_2mA* and *Enable_4mA* are active, both buffers work in parallel, adding their currents to a total of 6mA. These specifications are summarized in table 14-2.

Enable_4mA	Enable_2mA	PadOut current
&0	0	0mA (3-state)
0	1	2mA
1	0	4mA
1	1	6mA

Table 14-2: The output current depends on the enable signals (IOOutProgDrive.SCH)

6. Pull-up, pull-down

It might be interesting to add the possibility of a weak tie to a defined voltage, particularly in the case of shared data buses. The role of the pull-up resistor shown in the schematic design of figure 14-57 is to recall the output node to *VDD_HV* when the connection is floating. Using a MOS device as a 10KΩ switched resistance is efficient in terms of silicon area. The only drawback of this pull-up resistance is that the active logic level "0" is a little higher than 0.0V due to the leakage to *VDD_HV*, which leads to a non negligible DC current consumption. Similarly, a high resistance nMOS device may create a weak tie to ground, which is equivalent to a pull-down device.

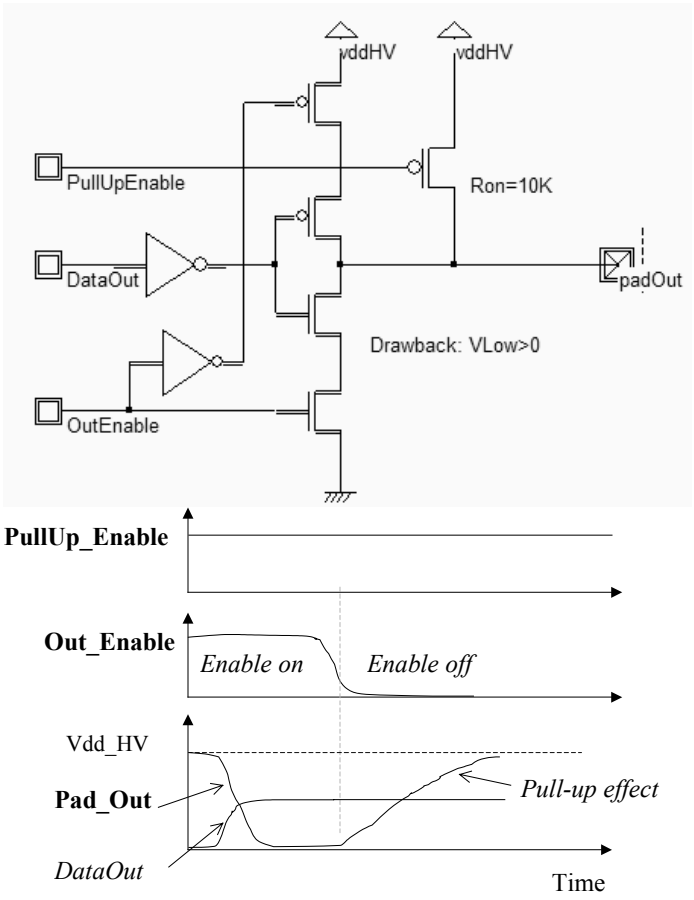


Figure 14-57: The 3-state output pad with a 10Kohm pull-up (IOPadOut.SCH)

I/O pad

The input-output pad structure is a combination of input and output pad structure. The input-output pad contains one input stage together with one output stage, usually with extensive programmable functionality. In figure 14-58, the output stage can be turned off when the signal *Out_Enable* is inactive. The pull up and pull down devices can be activated through *PullUp_Enable* and *PullDown_Enable* signals. More complex I/O pads may include programmable drives, as described previously.

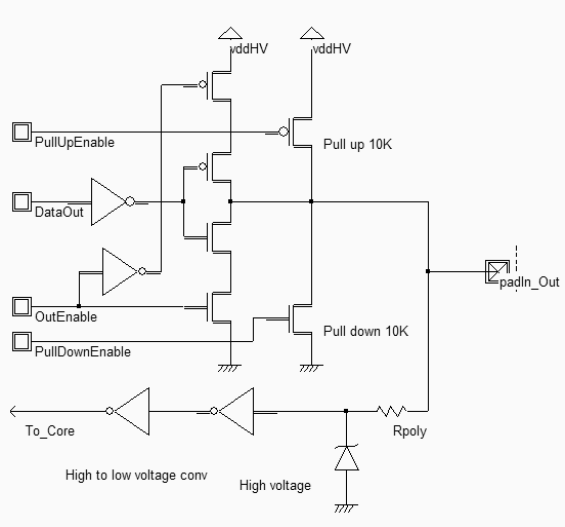


Figure 14-58. Design of an input-output pad (IOPad.MSK)

7. Low voltage differential swing

The main speed limitation in signal propagation is the time required to reach the logic state "1" or "0". Working at low supply voltage reduces the voltage swing and thus decreases the time required for the signal to reach the final logic area. Unfortunately, decreasing the logic cell supply also reduces the *Ion* current of the MOS devices which drives the output line. The differential swing logic circuit [Uyemura] uses two information signals *vin* and *~vin* instead of one, where *~vin* represents the logical complement of *vin*. The receiver works in differential mode, with signals that have a low swing amplitude.

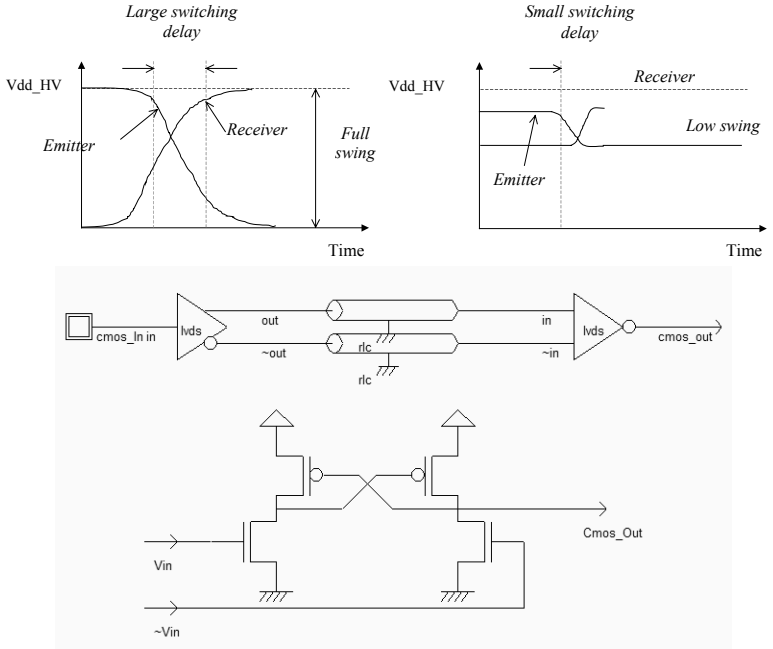


Figure 14-59: Low voltage differential swing logic to improve signal transport

Low voltage differential swing circuits operate at much higher frequencies than conventional CMOS drivers. However, LVDS circuits dissipate a significant amount of DC current, even when there is no switching activity. In the simulation of figure 14-60, a biasing current of 100µA appears in the upper window. Combined with the fact that LVDS circuits require two interconnects instead of one, differential circuits are limited to very high speed functions such as fast data buses.

From a layout design point of view, the sizing of n-MOS and p-MOS devices has a strong influence on the LVDS buffer operation. The specification of the LVDS signal has a direct impact on the width ratio between n-MOS and p-MOS devices. In the case of a voltage swing of 400mV, from 0.4V to 0.8V, the p-MOS should be significantly smaller than the n-MOS to ensure reliable working conditions.

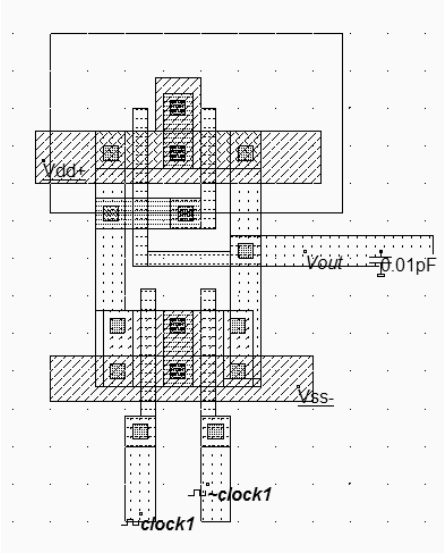


Figure 14-60: Low voltage differential swing layout (Lvds.MSK)

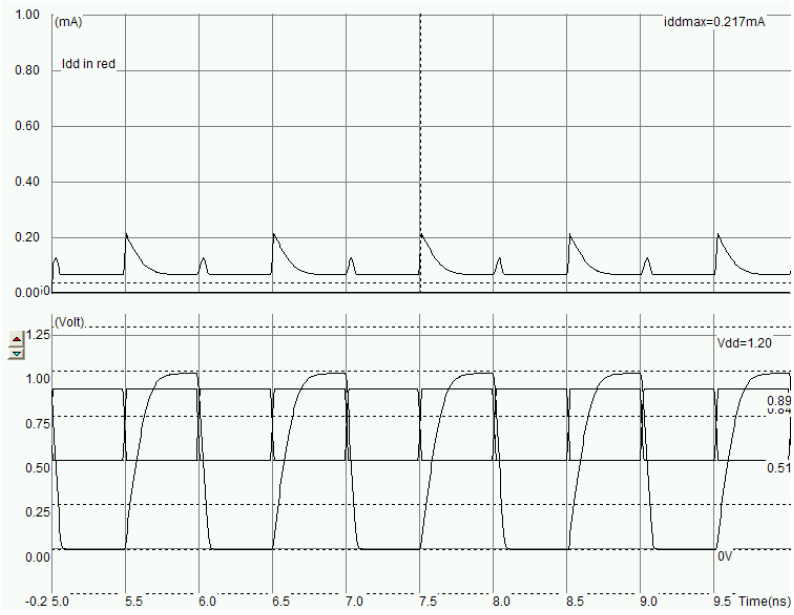


Figure 14-60: Low voltage differential swing simulation (Lvds.MSK)

8. Power Clamp

The power clamp is an efficient circuit that protect the logic core from oxide destruction, as a result of an electrostatic discharge appearing on the supply line. A simple circuit for this power clamp is proposed in figure 14-61, which has clear similarities with the ground gated MOS placed in input pads. The nMOS clamp is normally off, as *R1* ties the gate to a zero voltage, and *C1* is charged.

Assuming that an ESD pulse appears at the VDD supply, the nMOS transistor is turned on at a violent rise of VDD, which induces a positive voltage peak on *Vg* by capacitance coupling through *C1*. Consequently the MOS clamp is turned on, and the over voltage is limited. The MOS device width and the values for *R1* and *C1* are optimized to limit the core supply over-voltage below the gate oxide breakdown, without being sensitive to small VDD fluctuations. In 0.12µm, the oxide breakdown of the 2.5V logic is around 6V, but decreases to 3.0V for the 0.12µm devices.

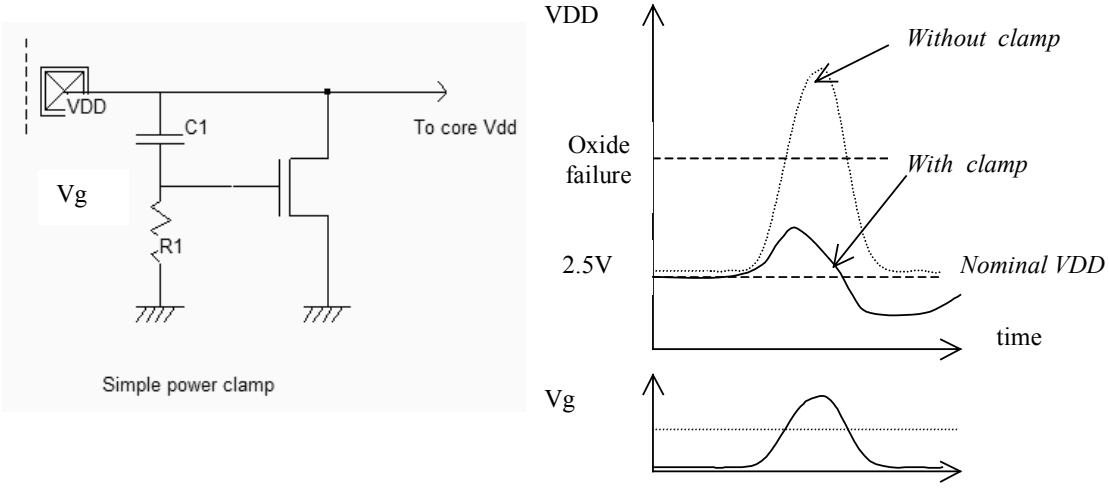


Figure 14-61. Design of a power clamp (PowerClamp.SCH)

9. CORE/PAD LIMITATION

When the active area of the chip is the main limiting factor, the pad structure may be designed in such a way that the width is large but the height is as small as possible. In that case, the oversize due to the pads is minimized. Protections are placed on both sides of the pad area. This situation is often called "Core Limited", and corresponds to the design shown in figure 14-62. In most pad libraries, the core limited structures have a minimum height, which often implies to place the protection circuits on both sides of the pad.

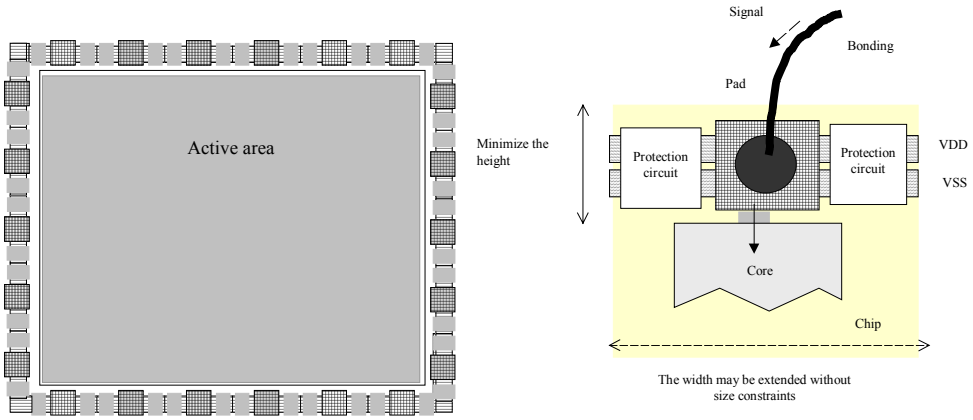


Figure 14-62 : Chip size fixed by the core

When the number of pads of the chip is the main limiting factor, the situation is called "Pad Limited", and corresponds to the design shown in figure 14-63. The pad structure may be designed in such a way that the width is small but the height is large. In that case, the oversize due to the pads is minimized. Protections are placed under the pad area.

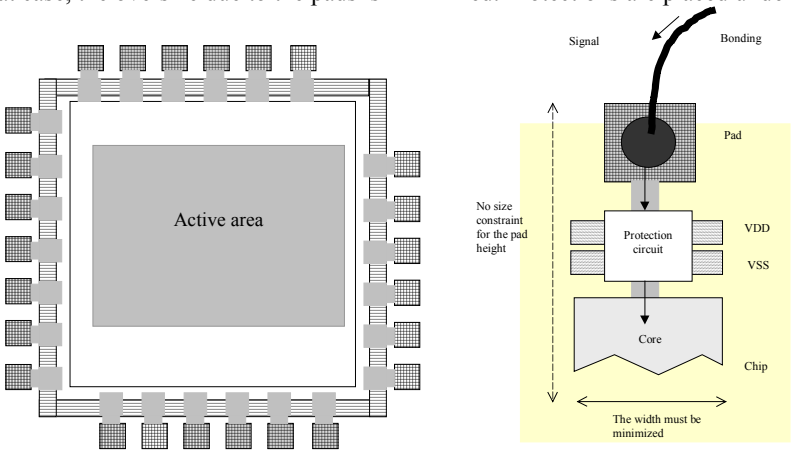


Figure 14-63. Chip size fixed by the number of pads

The spared silicon area may be avoided by using a double pair of I/O pads, as illustrated in figure 14-64. This attractive feature has been made available starting 0.25µm technology. An example of a test-chip using a double pad ring is reported in figure 14-64, which corresponds to a CMOS 0.18µm test-chip fabricated by ST-Microelectronics for research purposes. The pad pitch is significantly reduced thanks to the double row of bonding pads. The pad pitch for a single row is the sum of the minimum pad width *Rp01* and of the pad distance *Rp02*. In the double ring structure, the pad pitch is divided by a factor of 2.

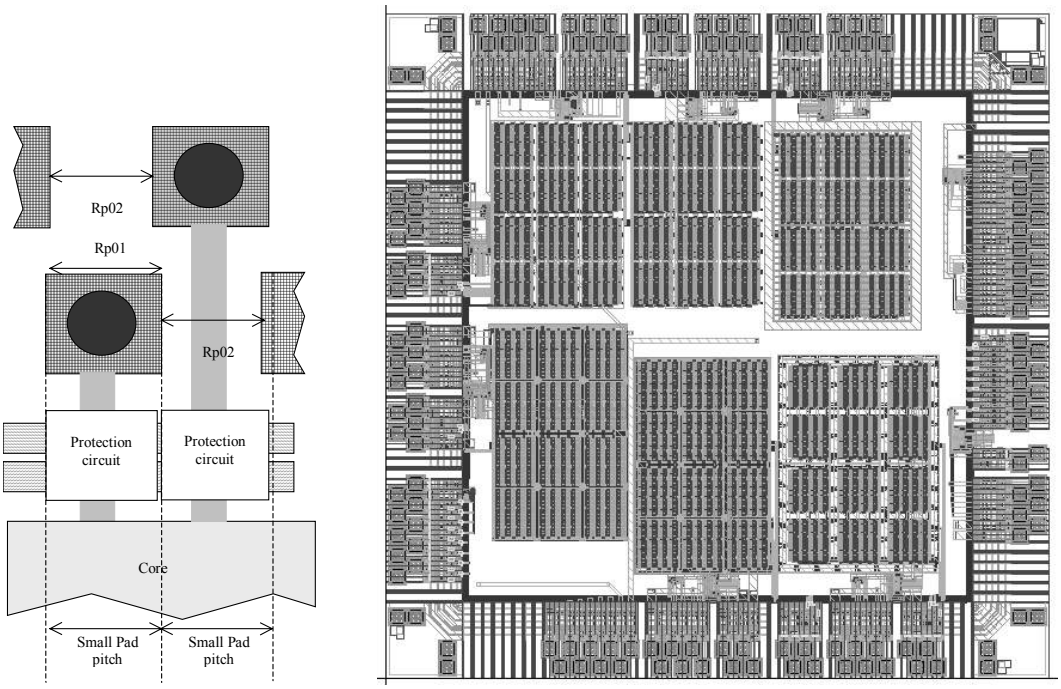


Figure 14-64. An example of a double ring test-chip in 0.18µm technology (Courtesy of ST-Microelectronics)

There exists possibilities to place three rows of bonding pads in some circuits, such as for some state-of-the art processors and micro-controllers. Future trends may include the use of matrix of bonding balls all over the surface of the chip. This technique, called chip-scale packing, is already in use for some low complexity integrated circuits.

10. I/O Pad description using Ibis

IBIS is a standard for electronic behavioral specifications of integrated circuit input/output analog characteristics. In order to enable an industry standard method to transport IBIS Modeling Data electronically between semiconductor vendors, simulation vendors, and end customers, a format has been proposed by the IBIS group [Ibis]. The version 3.2 of IBIS was finalized by a wide group of industry experts representing various companies and interests. A complete backup of slides and meeting notes for the latest IBIS open forum is available on the Ibis web site.

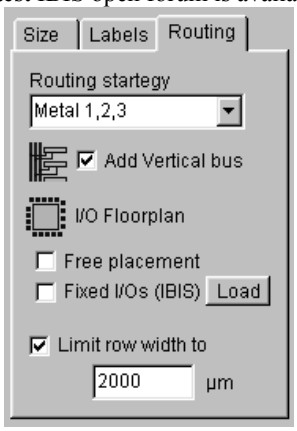


Figure 14-66. Controlling the I/O pin assignment by an IBIS description file

Microwind2 uses IBIS to pilot the generation of the I/O pads, when compiling a Verilog file. Click the button **Load** in front of the check box **Fixed I/Os**, in the Verilog menu. The default IBIS file is **default.IBS**. The screen shown in figure 14-67 appears.

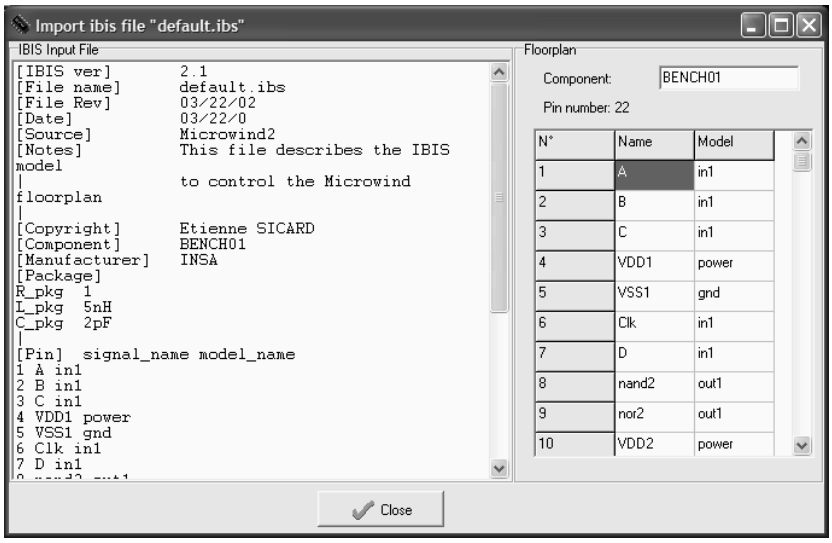


Figure 14-67. The IBIS description file loaded for controlling the pin assignment

It can be seen that IBIS is a text file, with a simple structure based on keywords. We only use a very reduced set of the available keywords, listed in table 14-3.

[IBIS Ver]	Specifies the IBIS template version. This keyword informs electronic parsers of the kinds of data types that are present in the file.
[File Rev]	Tracks the revision level of a particular .ibs file. Revision level is set at the discretion of the engineer defining the file.
[Component]	Marks the beginning of the IBIS description of the integrated circuit named after the keyword.
[Manufacturer]	Specifies the manufacturer's name of the component. Each manufacturer must use a consistent name in all .ibs files.
[Package]	Defines a range of values for the default packaging resistance, inductance, and capacitance of the component pins. Sub-Parameters are named R_pkg, L_pkg, C_pkg
[Pin]	Associates the component's I/O models to its various external pin names and signal names. Each line must contain either three or six columns. A pin line with three columns associates the pin's signal and model. Six columns can be used to override the default package values. In that case headers R_pin, L_pin, and C_pin appear.

Table 14-3. The IBIS keywords understood by Microwind

At a click on **Generate Pad**, the layout of figure 14-68 is created, which corresponds to the list of pins declared in the IBIS file, as appearing in figure 14-67.

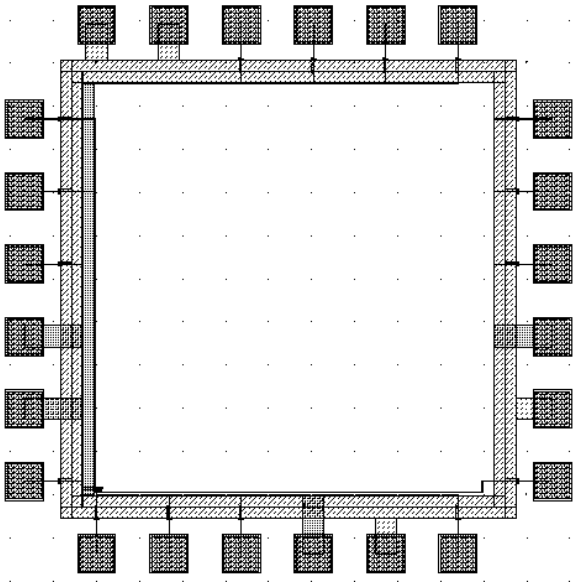


Figure 14-67. The I/O pad generation constructed using the IBIS file default.IBS

11. Connecting to the package

The integrated circuit is usually connected to the package by bonding wires or solder balls. In the first case, the bonding wires are made of gold, with a usual diameter of 25µm. The wires build the link between the pads and the package leads. An example of package connection using bonding wires is shown in figure 14-68.

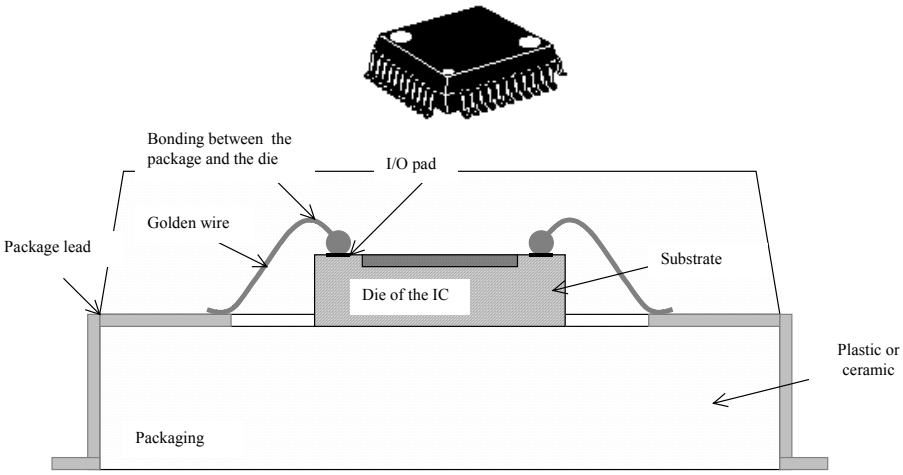


Figure 14-68: The structure of a Quad flat pack (QFP)

As the complexity of integrated circuits has constantly increased, a new type of link has been invented which creates in one single step all the connections between the die and the package. This technology, called ball grid array, was introduced some years ago and is now commonly used for integrated circuits with more than 200 pins. The cross-section of a ball-grid array and one integrated circuit example are proposed in figure 14-69. The die of the integrated circuit is flipped and connected using small solder balls to a specific package.

The package serves as a routing matrix from the IC pads (Pitch close to 100µm) to the ball gate array (Pitch between 500µm and 2mm). The package is a complex network of very thin copper conductors embedded in an insulator. The BGA substrate may include from 2 to 6 metal layers to achieve the routing of general purpose signals and the distribution of power supply.

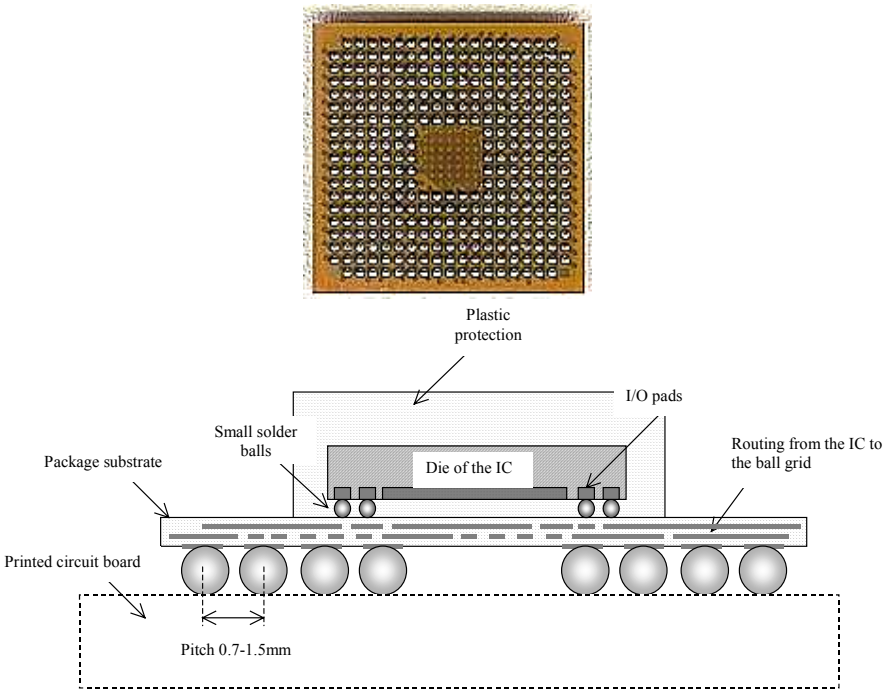
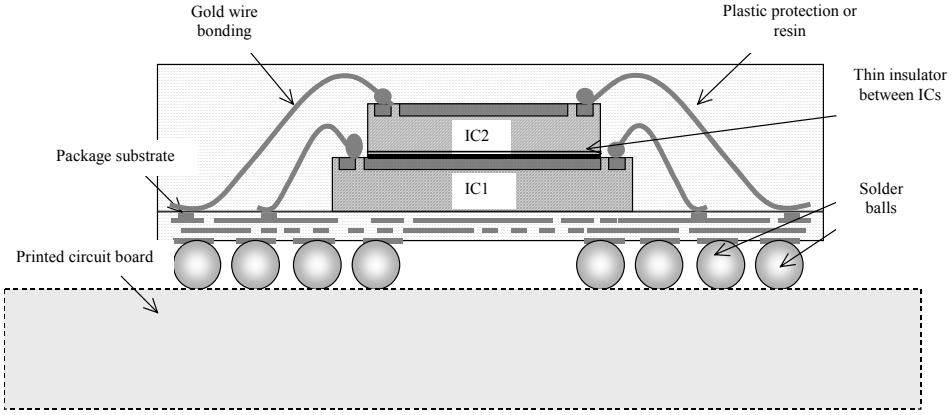


Figure 14-69: The assembly of the die to the package using micro balls

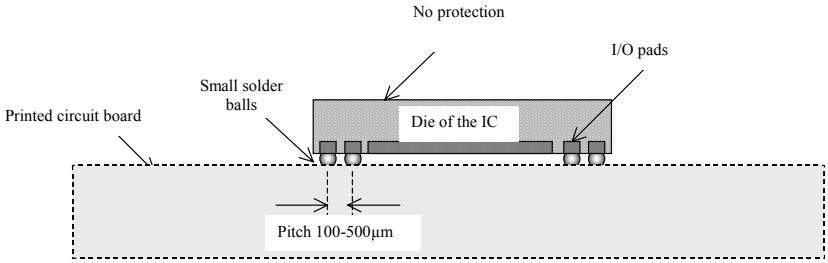
Stacked Integrated Circuits

To minimize the surface of the electronic systems, the trend is to stack integrated circuits within a single package, also called System in Package <Glossary>. The benefit of this technique is mainly a much more compact system, at the price of a much more complex assembly, reliability and thermal dissipation issues. One example of stacked integrated circuits is shown in figure 14-70-a. Stacked integrated circuits are particularly attractive when mixing processors, memories, power management, actuators, sensors and radio-frequency elements. Due to cost and reliability issues, the stacking of heterogeneous integrated circuits may be preferred to a single all-integrated die solution.

The chip scale packaging (CSP <Glossary>), shown in 14-70-b, consists in connecting directly the chip to the printed circuit board without any intermediate package substrate. The die is flipped and electrically connected to the board via solder balls. The routing constraints in the printed circuit board are very severe as the ball pitch may be as low as 200µm.



(a) Stacked integrated circuits



(b) Chip scale package

Figure 14-70: The stacking of two different dies in the same package (a) and the chip scale package (b)

12. Signal propagation between integrated circuits

The communication between two integrated circuits raises a set of issues that are briefly introduced in this paragraph. The emitter signal comes from a logic circuit *IC1* (figure 14-71). To be exported outside the integrated circuit, the signal is buffered by an inverter. The path between two integrated circuits is a conductor that can be a few millimeters to several meters long. Typically, the distance between two Ics in standard printed circuit boards is of the order of some centimeters. Finally, the signal enters a buffer of the receiver situated in *IC2*.

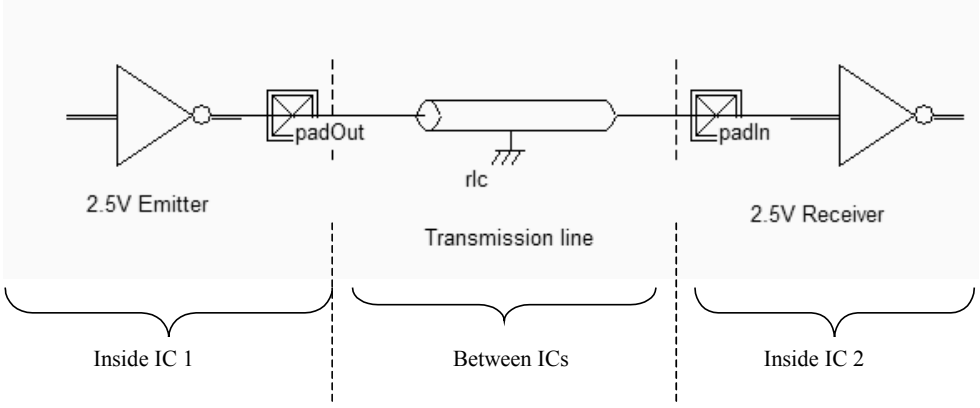


Figure 14-71: The signal propagation between integrated circuits

The transmission line effect can be seen in the simulation of figure 14-72. The original signal is quite clean and looks like a standard square waveform. However, the transport of the signal outside the integrated circuit, through the package, all the way along the interconnect and then inside the other integrated circuit has a significant impact on the shape of the resulting signal: propagation delay, overshoot and ringing. These effects are illustrated in figure 14-72

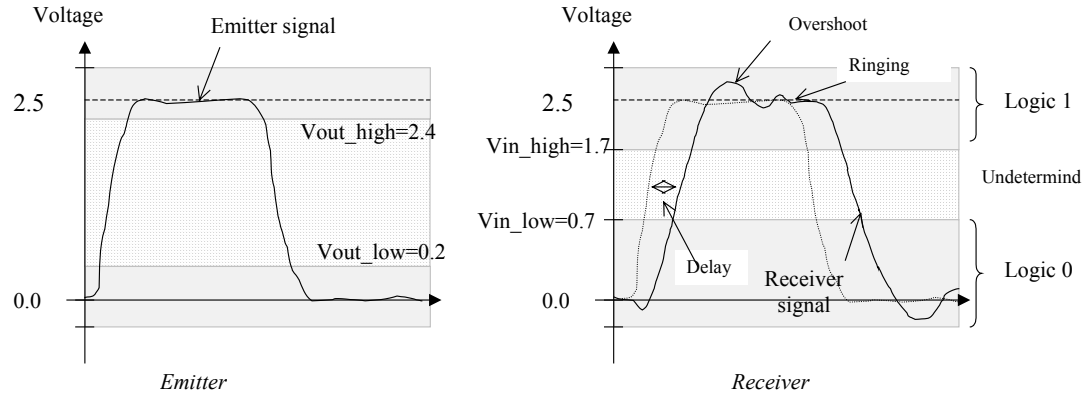


Figure 14-72: The signal is modified by the propagation within the package and interconnects.

Some limits are defined in figure 14-72 for low and high logic levels. These levels differ for the emitter and the receiver. The delay finds its origin in the flight time, linked to the light speed. In a normal epoxy printed circuit board (Also called FR4, with a permittivity of 4.2), the signal propagates according to equation 14-1 :

$$v = \frac{c}{\sqrt{\varepsilon_r}} \qquad \text{(Equation 14-1)}$$

The resulting propagation time is :

$$t_{prop} = \frac{\sqrt{\varepsilon_r}}{c} = \frac{2.1}{300{,}000 km/s} \cong 140 mm/ns$$

The overshoot and ringing are due to the inductive and capacitive behavior of the interconnection situated between the emitter and the receiver. The combination of C and L provokes resonance effects. As each portion of conductor has its own inductance and capacitance, several resonance effects may be observed at different frequencies.

There are various standards for input/output supply voltages, as shown in the table 14-3. The TTL standard and the low voltage TTL standard (LVTTL) work with non-symmetrical low and high levels. All CMOS standards are almost symmetrical.

Standard	VSS (V)	VDD(V)	Vin low	Vin high	Vout low	Vout high
TTL	0.0	5.0	0.8	2.0	0.4	2.4
LVTTL	0.0	3.3	0.8	2.0	0.4	2.4
LVCMOS2V5	0.0	2.5	0.7	1.7	0.2	2.1
LVCMOS1V8	0.0	1.8	0.63	1.17	0.45	1.35
LVCMOS1V2	0.0	1.2	0.43	0.78	0.30	0.9
LVCMOS1V0	0.0	1.0	0.35	0.65	0.25	0.75

Table 14-3: The format of some basic I/O standards in TTL and CMOS integrated circuits

The main limitation of a conventional I/O is the full swing of the voltage output, at the cost of a significant delay in the signal switching at the far end of the receiver. A very interesting idea consists in limiting the full voltage swing of the signal (Some volts) to only hundreds of mV. The flight time linked to the light speed remains unchanged but the charge and discharge time of the complete interconnect is significantly reduced.

Standard	VDD(V)	Vref (V)	Vin_low	Vin_high	Vout_low	Vin_high
SSTL3	3.3	1.65	Vref-0.2	Vref+0.2	0.90	2.10
SSTL2	2.5	1.25	Vref-0.15	Vref+0.15	0.65	1.85
SSTL18	1.8	0.9	Vref-0.125	Vref+0.125	0.40	1.30

Table 14-4: The format of high speed differential I/O standards used in recent CMOS integrated circuits

Details of small swing voltage standards (SSTL) are given in table 14-4. The SSTL circuit at work is illustrated for a 2.5V voltage supply (SSTL2), and a 1.25V voltage reference. A high speed bus using SSTL drivers is shown in 14-73. Notice the four SSTL drivers and receivers, plus the voltage reference *Vref*. The input data must be higher than *Vout_high* or lower than *Vout_low*, on the near end, close to the emitter.

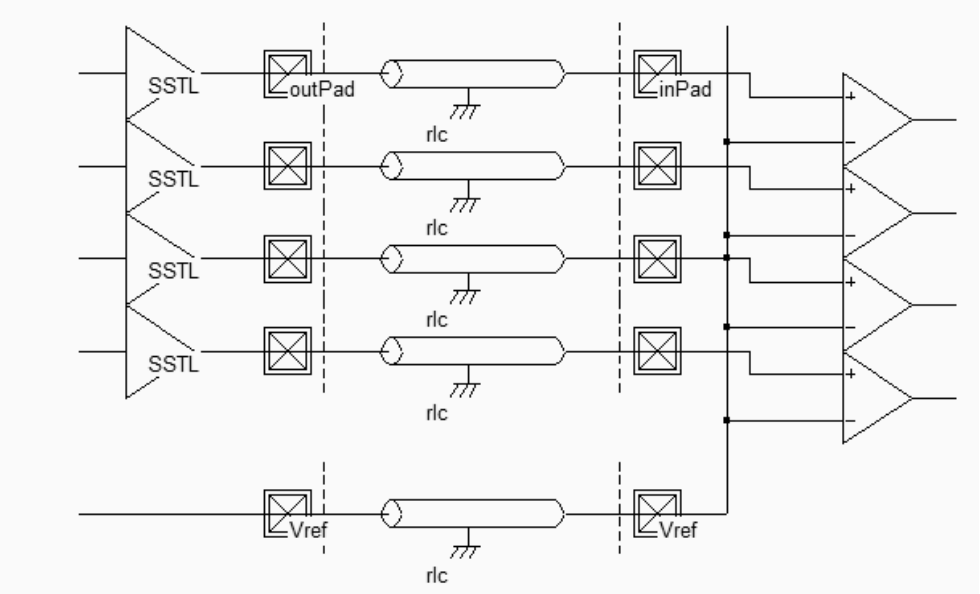


Figure 14-73: The SSTL bus used for double data rate RAM interfaces with high speed micro-processors (Iosstl.SCH)

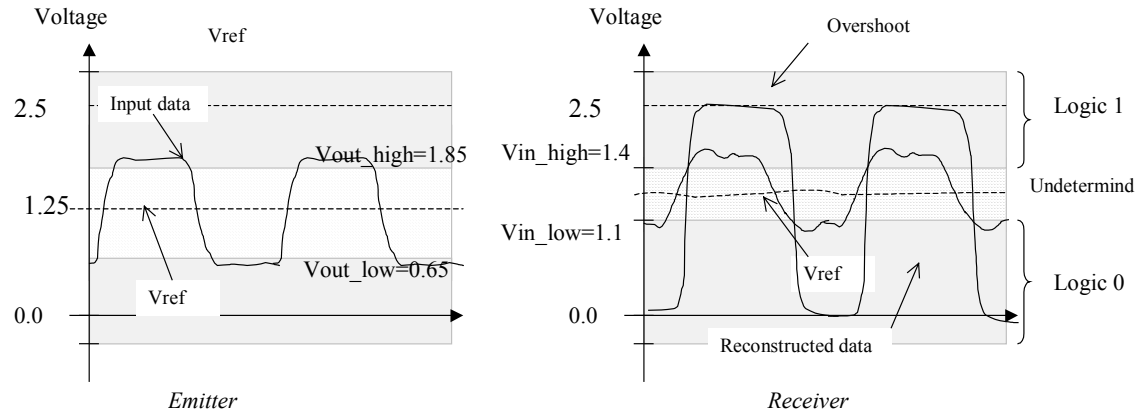


Figure 14-74: Typical waveforms for the SSTL2 emitter and receiver structure

The received signal is considered as a 1 if higher than *Vin_high* (Only 150mV higher than *Vref*), and considered as a 0 if lower than *Vin_low* (at least 150mV lower than *Vref*). These margins appear on the right of figure 14-74. The small voltage swing enables faster data rates: the SSTL2 input/outputs are used for double data rate memories with up to 800Mbit data rate.

13. Conclusion

This chapter has described the input/output interfacing of the integrated circuit. The power supply network has been described, with emphasis on metal grid strategy. Then, several aspects of the electrostatic discharge prevention have been addressed, and the basic elements for the input protection circuit have been detailed. Concerning the output structures, the buffer architecture, the 3-state option and programmable drive design principles have been presented. A brief presentation of IBIS has also been provided, followed by some insights in the connection between the integrated circuit and the external world. Quad flat pack, ball grid array, chip scale and stacked packages have also been described. Finally, the main standards for low voltage and small swing input/output signals have been listed.

Exercises

Exercise 14-1

Design a clamp circuit sensitive to a 100V pulse. The capacitor should be a coupling capacitor, and the simulation should be performed with the option "With crosstalk". Compare the performances of the clamp circuit and the Zener diode protection circuit proposed in this chapter.

Exercise 14-2

Design a programmable I/O pad, according to the schematic diagram of figure 14-57, with 2,4 or 6mA drive capabilities.

Exercise 14-3

Build a differential emitter/receiver circuit with a 2Gb/s bandwidth. What is the critical distance to perform the detection correctly?

Exercise 14-4

Evaluate the I/O density per mm^2 for QFP, BGA, µBGA and CSP.

Exercise 14-5

Build a SSTL bus transfer system for long interconnects on-chip. The interconnect may be routed in metal 6, and correspond to 10mm. Use the command **Edit → Generate → Metal** Bus to generate long bus lines automatically.

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