12 Radio-Frequency Circuits

Wireless communication systems require specific radio-frequency integrated circuits, which means optimum performances. The radio-frequency integrated circuits have to deal with traditional requirements such as low power consumption or high speed , but also with low process variation influence, power efficiency, linearity, low temperature influence, and low noise sensitivity. This chapter describes the general context of radio-frequency circuit design, integrated LC resonators, power amplifiers, high performance oscillators and frequency up/down converters.

1. Target Radio-Frequencies

Application	**GSM**	**DECT**	**UMTS**	**Bluetooth**	**IEEE 820.11a**	**IEEE 820.11b**
Description	Mobile phone 1st generation	Mobile phone 2nd generation	Mobile phone 3rd generation	Wireless network	Very high rate wireless networking	High rate wireless networking
Frequency (MHz)	890-915	1880-1900	1910-2200	2450	5200	2450
Data rate	12Kb/s	100Kb/s	0.1-2Mb/s	<Etienne>	6-18Mb/s	1-5Mb/s
Output Power	1-2 Watts	100mW	1 watt	100mW	0.1-1 Watt	0.1-1Watt

Table 12-1 : Main applications using radio-frequency Ics

Modern radio frequency equipments operate at frequency ranges officially called ultra-high frequencies (UHF) ranging from 300MHz to 3GHz, and super high frequencies (SHF) ranging from 3GHz to 30GHz. The “HF” bandwidth designates the bandwidth 3-30MHz. Mobiles phones and wireless networking have been the driving applications of radio-frequency integrated circuits, as described in figure 12-1.

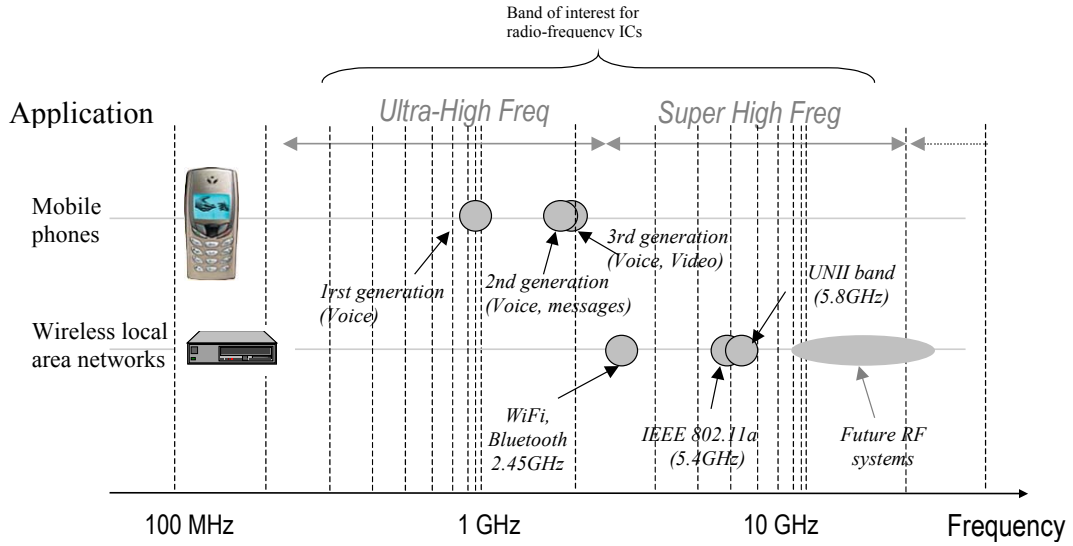


Figure 12-1. Some key radio-frequency applications

The general diagram of a mobile phone (Also called Universal Mobile Telecommunication System UMTS <Gloss>) is given in figure 12-2. The circuits detailed in this chapter refer mainly to the oscillators (VCO), the amplifiers and the filters.

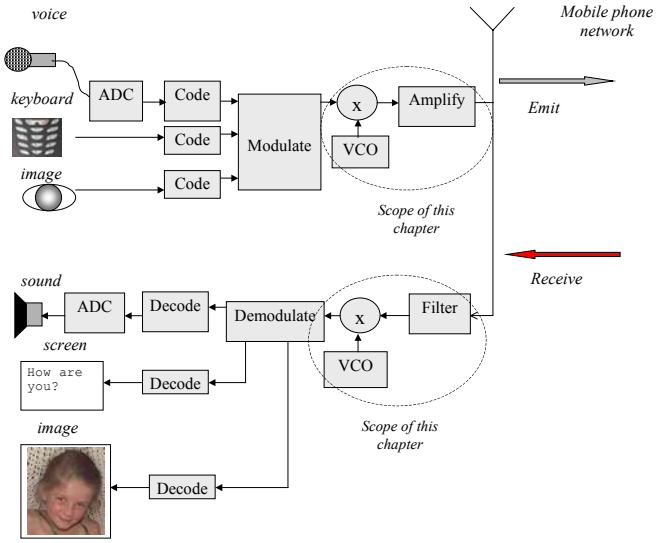


Figure 12-2. Generic diagram of the mobile phone structure

2. Inductor

Inductors are commonly used for filtering, amplifying, or for creating resonant circuits used in radio-frequency applications. The inductance symbol in DSCH and Microwind is as follows (Figure 12-3).

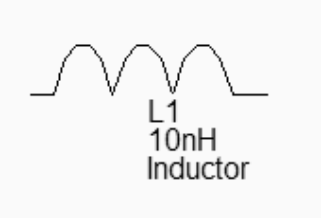


Figure 12-3. The inductance symbol

The layout of an on-chip inductor is typically a square spiral, since standard CMOS processes constrain all angles to be 90° (Figure 12-4). When possible, a polygon spiral using 45° tracks is used to increase the electrical performances of the inductor.

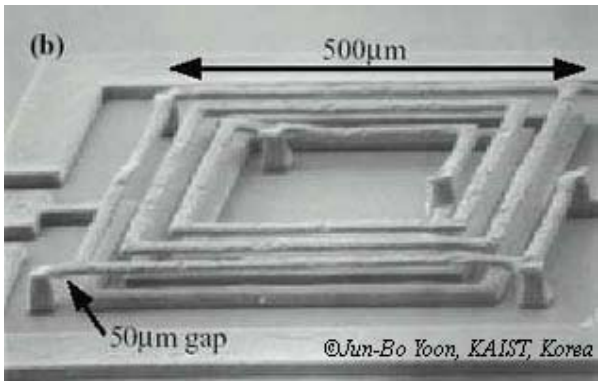


Figure 12-4. An integrated inductor

There exist a huge number of inductance calculation techniques, as detailed in the review from [Thompson]. A very interesting discussion about square planar spiral inductor may be found in [Lee]. The inductance formula used in Microwind (Equation 12-1) is one of the most widely known approximation, proposed as early as 1928 by [Wheeler], which is said to be still accurate for the evaluation of the on-chip inductor. With 5 turns, a conductor width of 20µm, a spacing of 5µm and a hollow of 100µm, we get L=11.6nH.

$$L = 37.5\mu_0 . \frac{n^2 . a^2}{(22.r - 14.a)} \qquad \text{(Equ. 12-1)}$$

with

$$r = n.(w + s)$$

$\mu 0 = 4\pi.10^{-7}$

n=number of turns

w= conductor width (m)

s=conductor spacing (m)

r=radius of the the coil (m)

a=square spiral's mean radius (m)

The quality factor Q is a very important metric to quantify the resonance effect. A high quality factor Q means low parasitic effects compared to the inductance. The formulation of the quality factor is not as easy as it could appear. An extensive discussion about the formulation of Q depending on the coil model is given in [Lee]. We consider the coil as a serial inductor L1, a parasitic serial resistor R1, and two parasitic capacitors C1 and C2 to the ground, as shown in figure 12-5. Consequently, the Q factor is approximately given by equation 12-2.

$$Q = \frac{\sqrt{\frac{L1}{(C1+C2)}}}{R1} \qquad \text{(Equ. 12-2)}$$

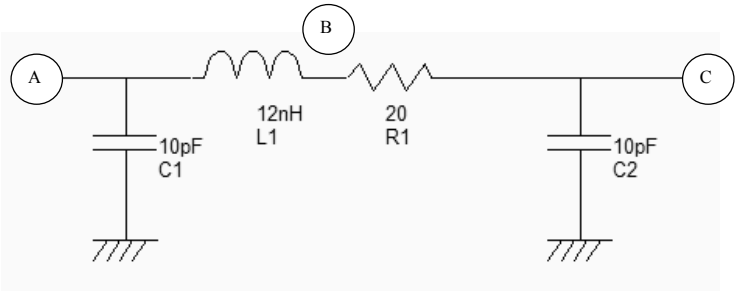


Figure 12-5. The equivalent model of the 12nH default coil and the approximation of the quality factor Q

Inductor Design in Microwind

We investigate here the design of a rectangular on-chip inductor, the layout options and the consequences on the inductor quality factor. The inductor can be generated automatically by Microwind using the command **Edit → Generate → Inductor**. The inductance value appears at the bottom of the window, as well as the parasitic resistance and the resulting quality factor Q.

Using the default parameters, the coil inductance approaches 12nH, with a quality factor of 1.15. The corresponding layout is shown in figure 12-6. Notice the virtual inductance (L1) and resistance (R1) symbols placed in the layout. These symbols indicate to the extraction that that three separate electrical nodes are requested (A,B and C), with a serial inductor between A and B and a serial resistance between B and C. If these symbols were omitted, the whole inductor would be considered as a single electrical node. Only the capacitance (C1, C2) would be properly extracted.

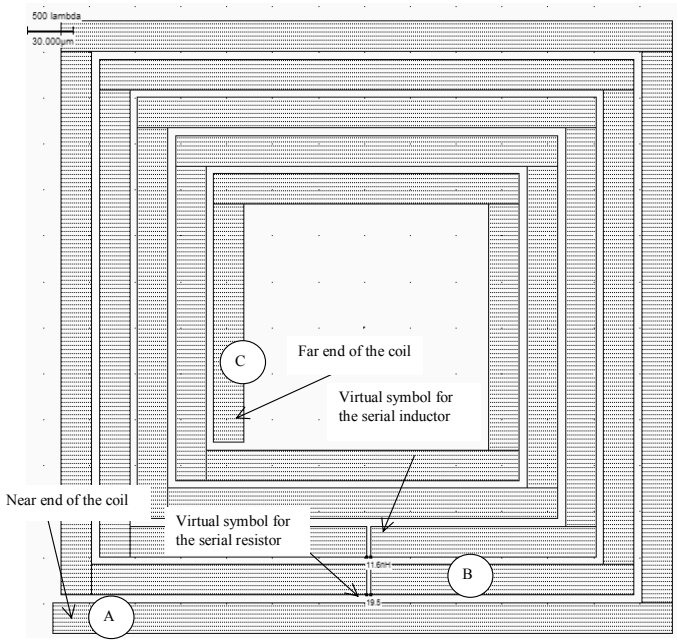


Figure 12-6. The inductor generated by default (inductor12nH.MSK)

Inductor Impedance

On-chip inductance has a typical value ranging from 1 to 100nH, which give an equivalent impedance between 10 and 1000 ohm, within the radio-frequency range 300MHz-3GHz (Figure 12-7), by applying the formulation of the impedance versus frequency.

$$Z_L = jL\omega \qquad \text{(Equ. 12-3)}$$

At frequencies lower than 100Hz, discrete off-chip are used because of the high inductor values (From 1to 100µH) to keep the impedance between 10 and 1000 Ohm. Such high inductances cannot be integrated in a reasonable silicon area. Around 1GHz, a 10nH on-chip inductor matches the standard 50Ω impedance of most input and output stages in very high frequency applications.

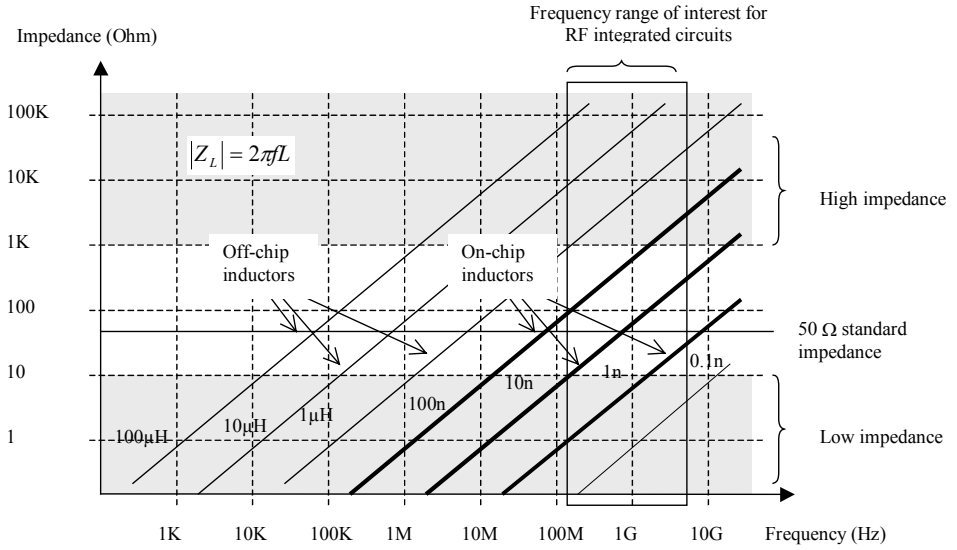
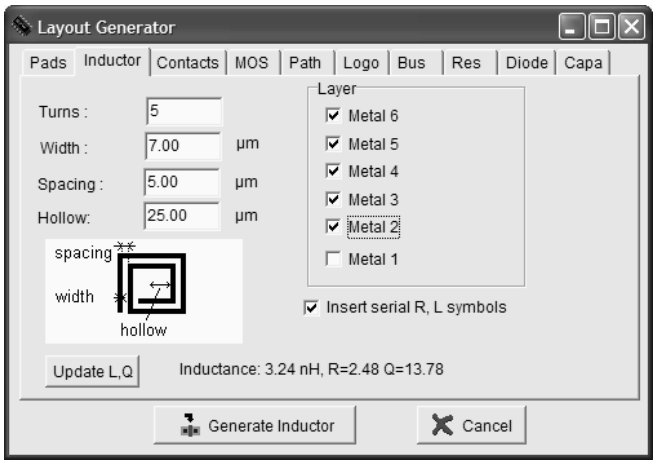


Figure 12-7. The inductor impedance versus frequency

High Quality Inductor

A high quality factor Q is attractive because it permits high voltage gain, and high selectivity in frequency domain. The usual value for Q is between 3 and 30. The main limiting factors for Q are the serial resistance *R1* of the wire and the substrate coupling capacitors *C1* and *C2*. From equation 12-2, it clearly appears that *R1,C1* and *C2* should be kept as low as possible to increase Q. There are several ways to improve the coil quality factor. The first one consists in using the upper metal layer (metal 6 in 0.12µm) which features a smaller sheet resistance together with a smaller capacitance. Unfortunately, the quality factor is only increased to 2.

A significant improvement consists in using metal layers in parallel (Figure 12-8). The selection of metal2, metal3, up to metal6 reduces the parasitic resistance of *R1* by a significant factor, while the capacitance of *C1* and *C2* is not changed significantly. The result is a quality factor near 13, for a 3nH inductor. Even when the conductor width is increased to further reduce *R1*, or if the number of turns and the coil shape are changed, the maximum *Q* is almost invariably below 20.



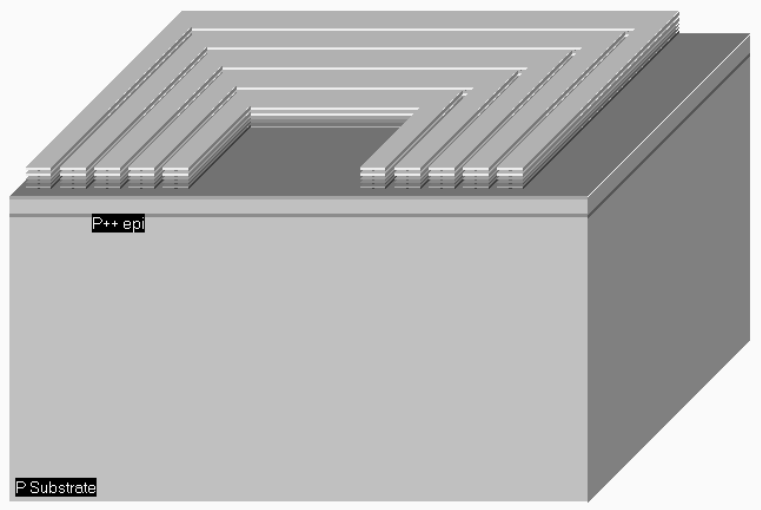


Figure 12-8: A 3D view of a high Q inductor using metal layers in parallel (Inductor3nHighQ.MSK)

Resonance

The coil can be considered as a RLC resonant circuit. At very low frequencies, the inductor is a short circuit, and the capacitor is an open circuit (Figure 12-9 left). This means that the voltage at node *C* is almost equal to *A*, if no load is connected to node *C*, as almost no current flows through *R1*. At very high frequencies, the inductor is an open circuit, the capacitor a short circuit (Figure 12-9 right). Consequently, the link between *C* and *A* tends towards an open circuit.

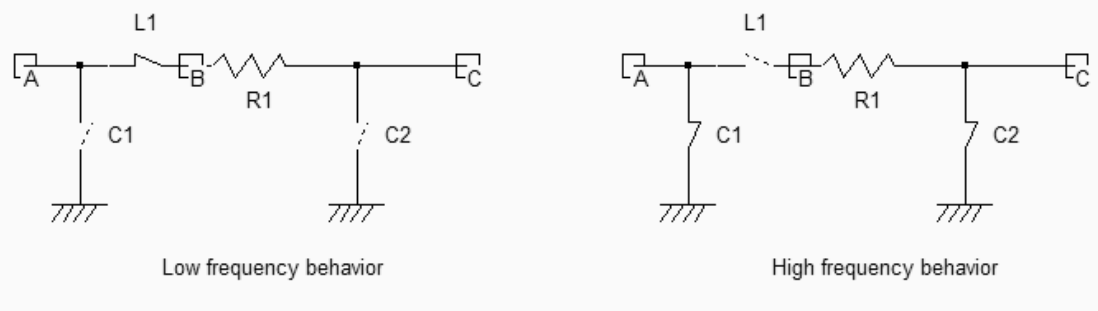


Figure 12-9. The behavior of a RLC circuit at low and high frequencies (Inductor.SCH)

At a very specific frequency the LC circuit features a resonance effect. The theoretical formulation of this frequency is given by equation 12-4.

$$f_r = \frac{1}{2\pi\sqrt{L1(C1+C2)}} \qquad \text{(Equ. 12-4)}$$

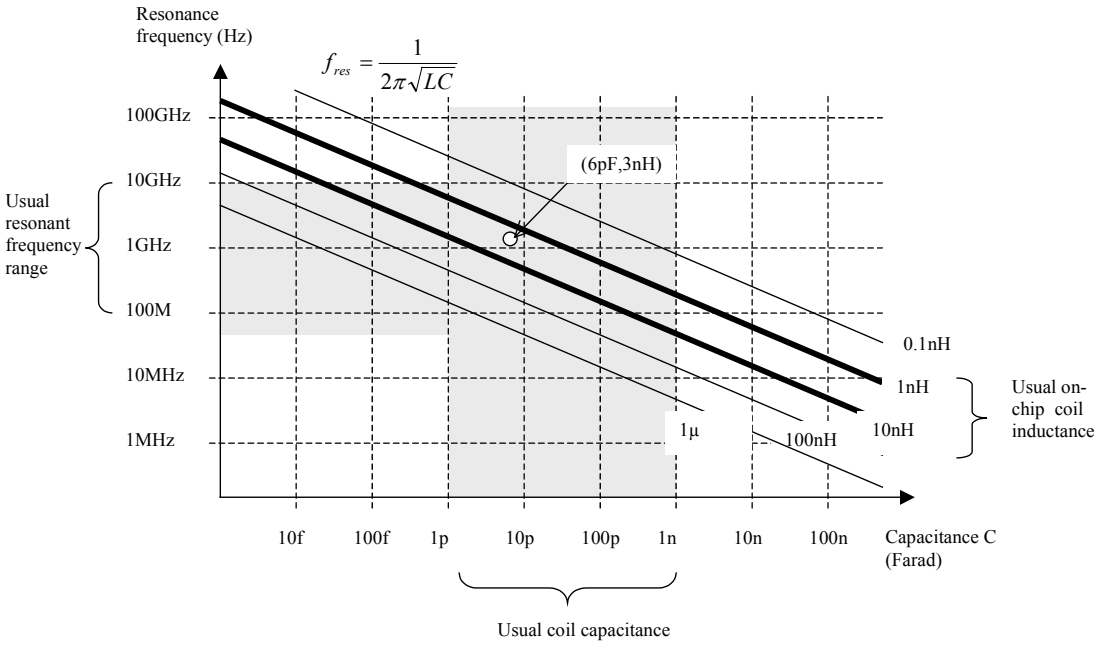


Figure 12-10. The resonance frequency depending on the capacitance and inductance

The variation of the resonant frequency with the capacitor and inductor is proposed in figure 12-8. On-chip coil inductances are within the range of 1 to 100nH. As the capacitance may vary from 1pF to 1nF, the range of the resonant frequency is around 100MHz to 10GHz, which includes most of the radio-frequency designs.

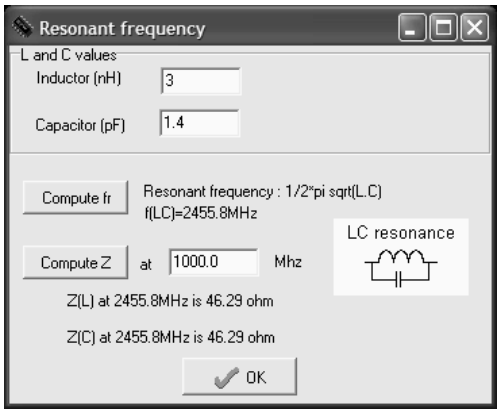


Figure 12-9. Microwind can compute the resonance frequency corresponding to user-defined L and C values

In the **Analysis** menu, the command **Resonance Frequency** includes a resonant frequency calculator, as shown in figure 12-9. For a given value of inductor and capacitor (3nH and 1.4pF in this example), the resonant frequency is directly computed in mega-hertz (MHz). For a target frequency of 2.45GHz, and a given inductor value of 3nH, we must choose a capacitor close to 1.4pF.

Simulation of the Coil

In the case of *L1*=3nH (Design corresponding to figure 12-6), the total capacitor is around 7pF. From the abacus given in figure 12-8, we obtain a resonant frequency around 1GHz. We may see the resonance effect of the coil and an illustration of the quality factor using the following procedure. The node *A* is controlled by a sinusoidal waveform with increased frequency (Also called "chirp" signal). We specify a very small amplitude (0.1V), and a zero offset. The resonance can be observed when the voltage at nodes *B* and *C* is higher than the input voltage *A*. The ratio between *B* and *A* is equal to the quality factor Q.

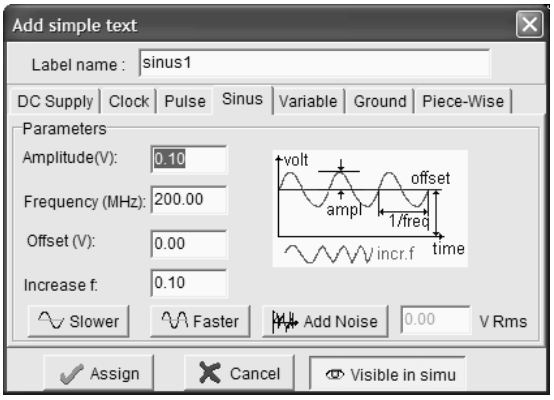


Figure 12-10. Using a sinusoidal waveform with increased frequency (Inductor3nHighQ.MSK)

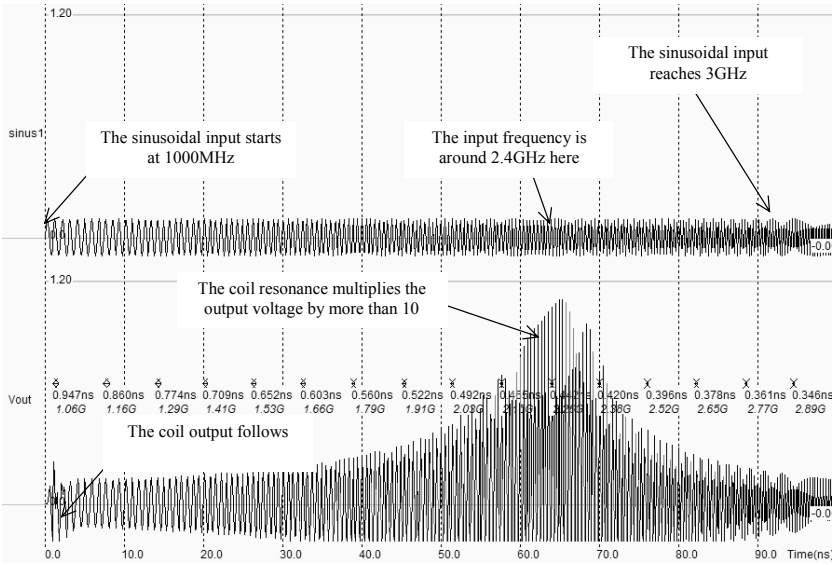
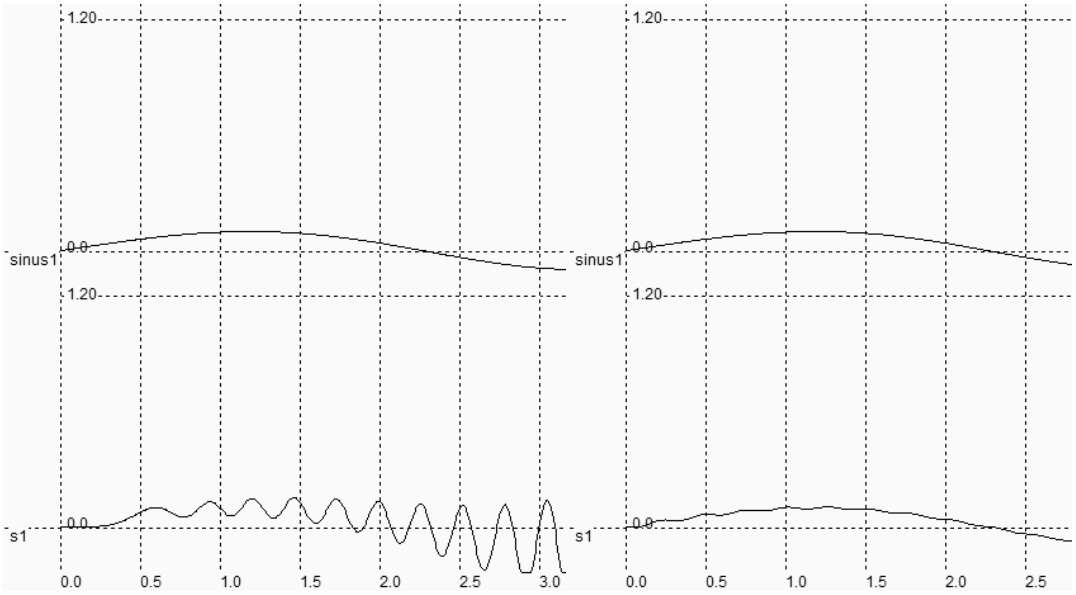


Figure 12-11. The behavior of a RLC circuit near resonance (Inductor3nHighQ.MSK)

The frequency corresponding to the resonance is around 2.4GHz, as predicted by the theoretical formulation. However, some mismatch between the prediction and the simulation may appear: first of all, the sinusoidal generator forces node *A* to a given voltage, which inhibits the role of capacitor *C1*. The resonance is only based on *L1*, *R1* and *C2*, which shifts the frequency to higher levels. Secondly, the simulation of the inductor effect requires a significant amount of computation, with a high precision, otherwise the simulation becomes unstable.

In 0.12µm, the simulation step is fixed to 0.3ps, which is a good compromise between accuracy and speed. However, when dealing with an inductor, this step should be reduced. IF we increase the step to 1ps (Figure 12-12-a), an important parasitic instability effect appears and the output tends to oscillate. With a small simulation step (0.1pS in the case of figure 12-12-b), the simulation converges but the computation is significantly slowed down.



(a) Simulation step 1ps – too large (b) Simulation step 0.1ps - correct

Figure 12-12: The numerical instability appears in the inductor simulation when using a large integration interval (1ps) which is removed when lowering this interval to 0.1ps.

3. Power Amplifier

The power amplifier is part of the radio-frequency transmitter, and is used to amplify the signal being transmitted to an antenna so that it can be received at the desired distance. A numerical or analog information is processed at low frequency, and converted to an appropriate sinusoidal waveform combined with a modulation. The high frequency converter transforms the low frequency signal f_{low} to a high frequency signal f_{high}. The shape of f_{high} is identical to f_{low} except that the frequency is one or two orders of magnitude higher. Details about this circuit are provided later in this chapter. The amplitude of f_{high} is usually small (10-100mV). A power amplifier is required to multiply the amplitude of the signal in order to transmit enough power to the emitting antenna.

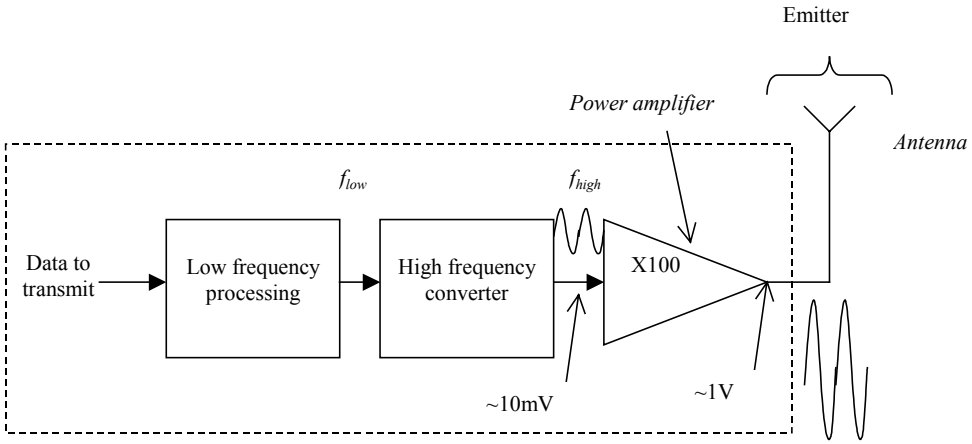


Figure 11-13: The power amplifier in a typical radio-frequency system

Antenna Model

We can consider an antenna as a load that, in the ideal case, will be a pure resistance. The antenna resistance *Ra* accounts for the power absorbed by the antenna. This power is mainly radiated by the antenna. Most mobile phone antennas are resonant monopoles [Macnamara] for which the antenna resistance *Ra* varies from 20 Ω (Ground plane width w=0) to 40 Ω (Infinite ground plane width). The monopole radiates mainly on X and Y directions (Figure 12-14). The length of the antenna is often chosen close to λ/4, where λ is the wavelength of the emitted signal. That length corresponds to the first maximum in the sinusoidal wave. From an electrical point of view, we can consider the antenna as a pure resistive load. The value of 50ohm is commonly used for *Ra* in simulations, as most equipments are "50 ohm adapted".

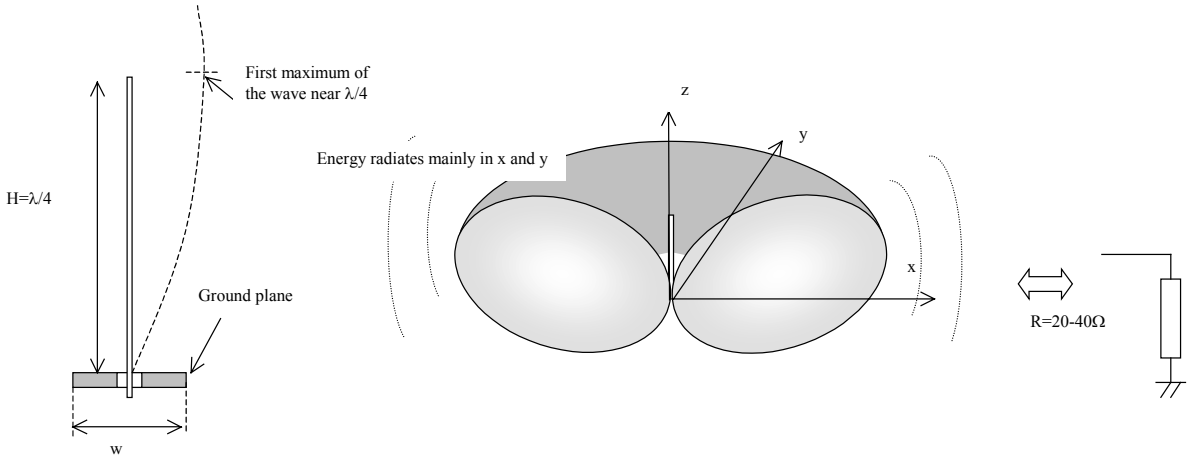


Figure 12-14. In first approximation, the antenna can be approximated as a load resistance around 30Ω.

Power Amplifier Principles

Most CMOS power amplifiers are based on a single MOS device, loaded with a "Radio-Frequency Choke" inductor L_{RFC}, as shown in figure 12-16. The inductor serves as a load for the MOS device (At a given frequency *f*, the inductor is equivalent to a resistance L.2π.*f*), with two significant advantages as compared to the resistor: the inductor do not consume DC power, and the combination of the inductor and the load capacitor C_L creates a resonance. The power is delivered to the load *RL*, which is often fixed to 50Ohm. This load is for example the antenna monopole, which can be assimilated to a radiation resistance, as described in the previous section. The resonance effect is obtained between L_{RFC} and C_L. The formulation for resonance is given below.

$$f_{resonance} = \frac{1}{2\pi\sqrt{L_{RFC}C_L}} \qquad \text{(Eq. 12-5)}$$

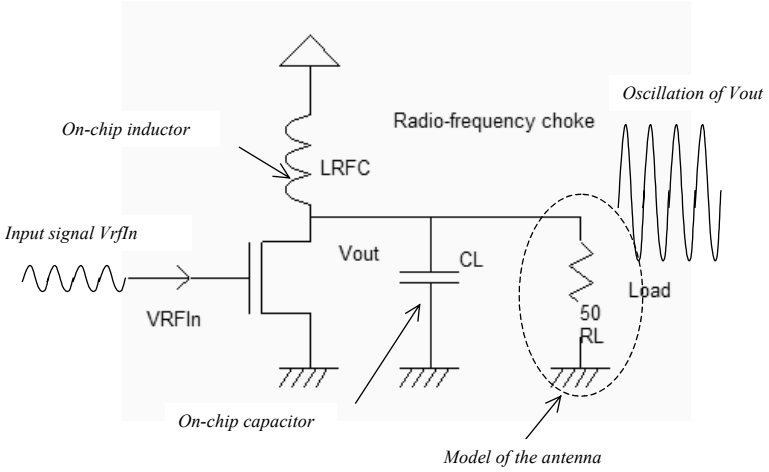


Figure 12-16: The basic diagram of a power amplifier (PowerAmp.SCH)

For example, a power amplifier designed for Bluetooth operation should resonate around 2.4GHz. If we assume that the inductance has a value of 3nH, the corresponding capacitor is around 1.5pF.

Power Amplifier MOS

The MOS devices used in power amplifier designs have very huge current capabilities to be able to deliver strong power on the load. This leads to very unusual constraints on the width of the transistor so that devices with a width larger than 1000µm are commonly implemented [Hella]. The radio frequency choke inductor has a resonant effect which induces an important voltage swing of node *Vout*. Consequently, high voltage MOS devices are used to handle large overvoltages. A MOS device with a very large width is not drawn directly, but is obtained by connecting medium size MOS devices in parallel. In Microwind, we generate multiple-finger MOS devices easily, thanks to the MOS generator command (Figure 12-17). The high voltage option is selected, and the number of fingers is fixed to 10.

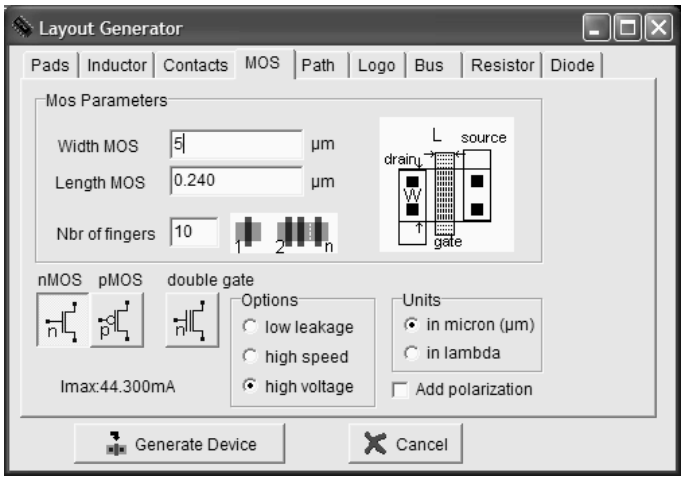


Figure 12-17. Generating a transistor with large current capabilities (PowerAmplifier.MSK)

The layout generated by Microwind is completed by adding a polarization ring to VSS, and metal2 contacts to the gate (Signal *VRF_In*) and the drain (Signal *Vout*). The result is shown in figure 12-18. The maximum current is close to 40mA. A convenient way of generating the polarization ring consists in using the Path generator command, and in selecting the option **Metal and p-diffusion**. Then the location for the polarization contacts must be drawn in order to complete the ring.

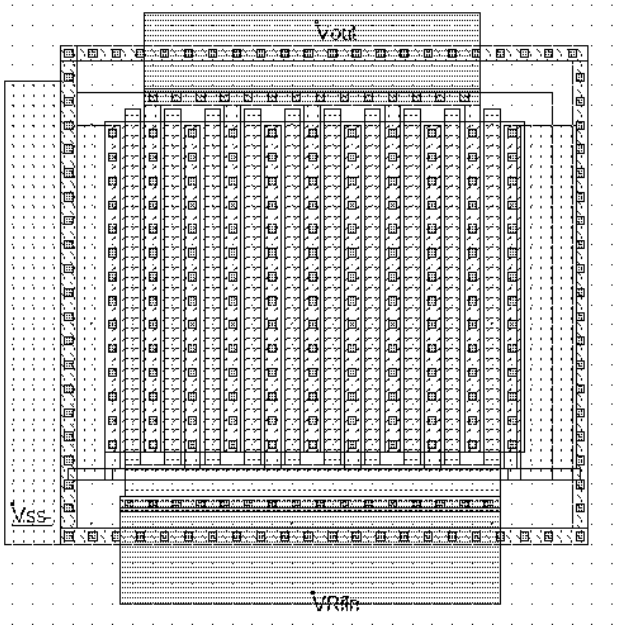


Figure 12-18. The layout of the power MOS also includes a polarization ring, and the contacts to metal2 connections to VRF_in and VOut (PowerAmplifier.MSK)

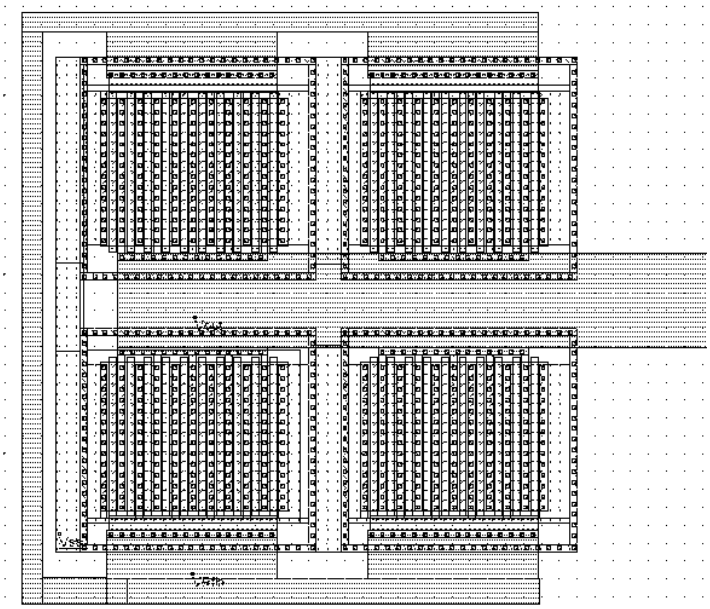


Figure 12-19: The layout of a 160mA power MOS using four large MOS in parallel (PowerAmplifierBig.MSK)

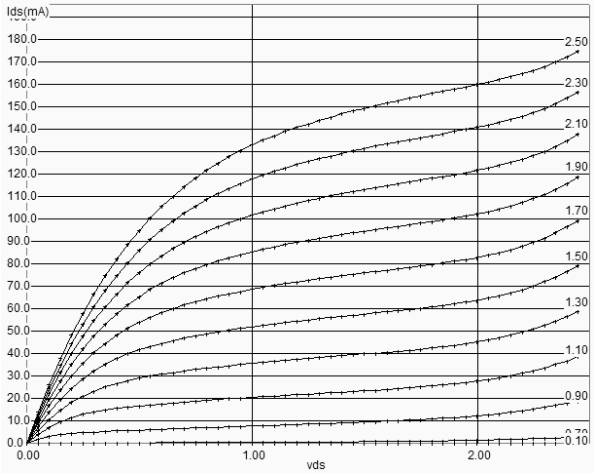


Figure 12-20. The static characteristics of the 160mA power MOS (PowerAmplifierBig.MSK)

An example of 160mA power device is shown in figure 12-19. Four devices are connected in parallel. The output node drives a large current and must be designed as wide as possible, with a short connection to the output pad to limit the serial resistance and parasitic capacitor to ground. The ESD protection is removed in some cases to enhance the power amplifier performances [Hella]. In the characteristics Id/Vd, the maximum *Ion* current is close to 170mA (Figure 12-20). The ground connection also drives a strong current and must be carefully connected to the ground supply.

Power Amplifier Efficiency

One of the most important characteristics of the power amplifier is the power efficiency, also called "drain efficiency" [Lee]. The definition of drain efficiency is given by equation 12-6.

The power efficiency is a ratio between the power delivered to the load and the supply power. The power efficiency (PE) is usually given in %. Typically, power efficiency *PE* ranges from 25 to 50%. The PE of CMOS power amplifiers is usually close to 30%. Higher efficiency is obtained with bipolar of GaAs semiconductors.

$$PE = \eta = \frac{P_{RF\_out}}{P_{DC}} \quad \text{(Equ 12-6)}$$

Where

P_{RF_out} is the RF output power (in watt)

P_{DC} is the total power delivered from the supply (in watt)

We may evaluate the power efficiency of the power amplifier with Microwind, using the following simulation procedure. The power amplifier is designed with a virtual load (*RL*=50 ohm in the case of figure 12-21). Notice that the connection of the *RL* virtual load is unusual: one end of the resistor is connected to VDD rather than VSS. Connecting *RL* to ground would add a very important standby DC current, flowing through *RL* even without RF input. In reality, the *RL* resistor represents the antenna radiation resistance which has no direct path to ground. To avoid the parasitic DC contribution, we connect one end of *RL* to VDD.

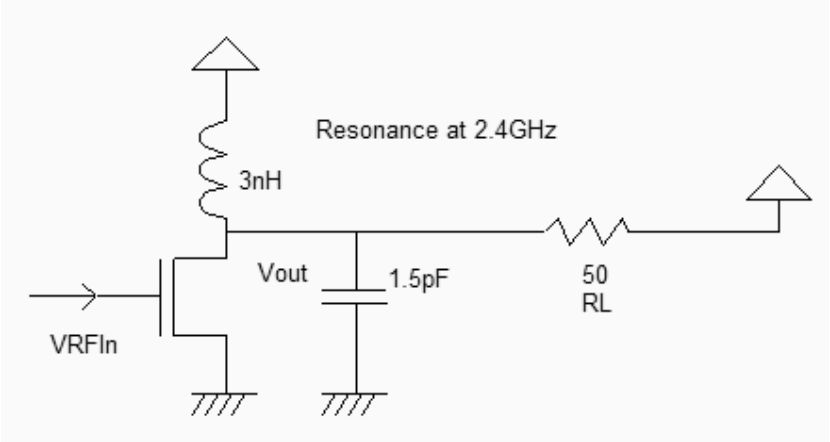


Figure 12-21. The evaluation of the power amplifier efficiency (PowerAmp.SCH)

The layout corresponding to the power amplifier is shown in figure 12-22. The inductor is virtual, as well as the 50ohm load. By default, the power P_{DC} is computed at each simulation and appears at the right lower corner of the simulation window of Microwind. In the simulation window corresponding to the mode **Current And Voltage vs. time**, we select the current flowing in R(50ohm). At the end of the simulation (Figure 12-23), the evaluation of the power efficiency is also displayed.

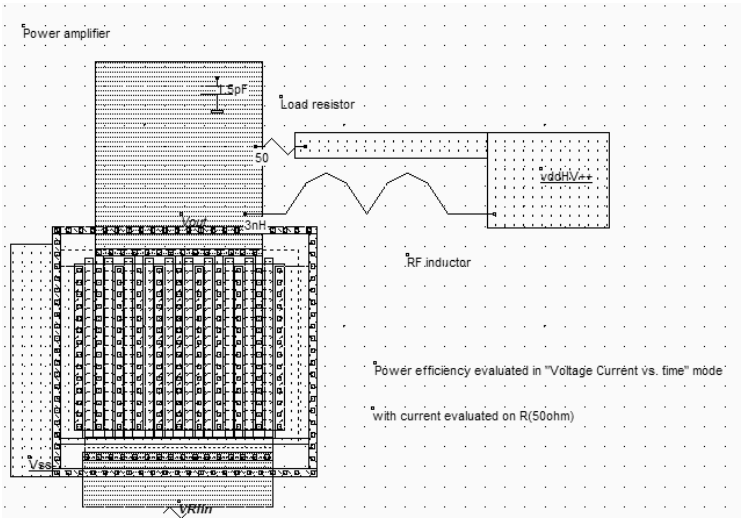


Figure 12-22. The evaluation of the power amplifier efficiency (PowerAmplifierEfficiency.MSK)

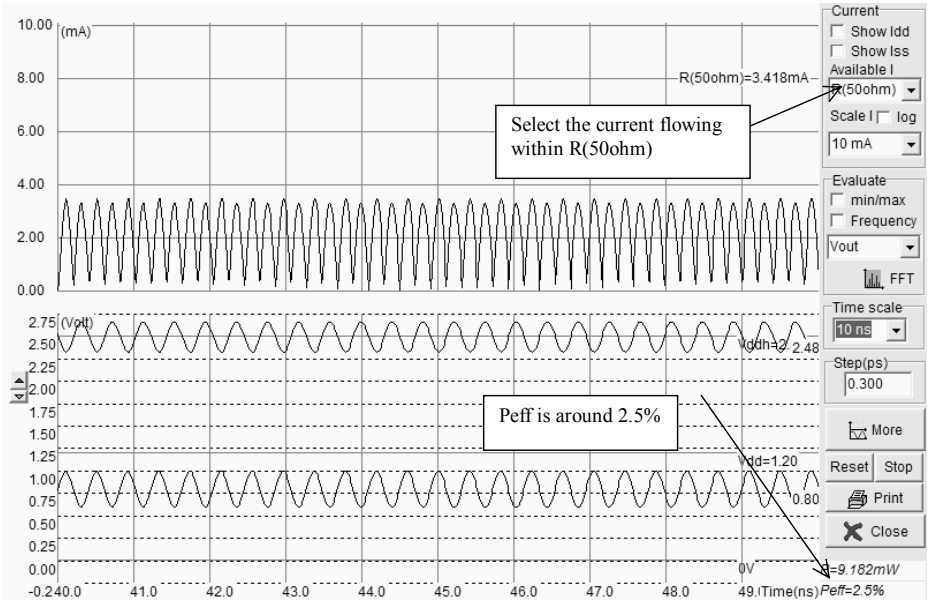


Figure 12-23. The evaluation of the power amplifier efficiency is accessible in the " Voltage and Current vs. Time " mode, by selecting the virtual load (PowerAmplifierEfficiency.MSK)

From the simulation of the simple power amplifier, we obtain a power efficiency of 2.5%, which is extremely low (Figure 12-23). In other words, 97.5% of the supply energy is dissipated and lost in the circuit, with only 2.5% delivered to the load. There are several techniques to improve the power efficiency: increasing the MOS size, modifing the amplitude of the input sinusoidal wave, and modifing the DC offset of the input sinusoidal wave.

An other metric for the power amplifier efficiency is the power added efficiency or PAE [Hella]. The PAE is very similar to equation 12-6. It includes the input power P_{RF_in} as given in equation 12-7. Microwind does not evaluate directly this parameter.

$$PAE = \left(\frac{P_{RF\_out} - P_{RF\_in}}{P_{DC}}\right) \qquad \text{(Equ 12-7)}$$

Where

P_{RF_out} is the RF output power (in watt)

P_{RF_in} is the RF input power (in watt)

P_{DC} is the total power delivered from the supply (in watt)

Class A Power Amplifier

The distinction between class A,B,AB, etc.. amplifiers is mainly given with the polarization of the input signal. A Class A amplifier is polarized in such a way that the transistor is always conducting. The MOS device operates almost linearly. An example of power amplifier polarized in class A is shown in figure 12-24. The power MOS is designed very big to improve the power efficiency.

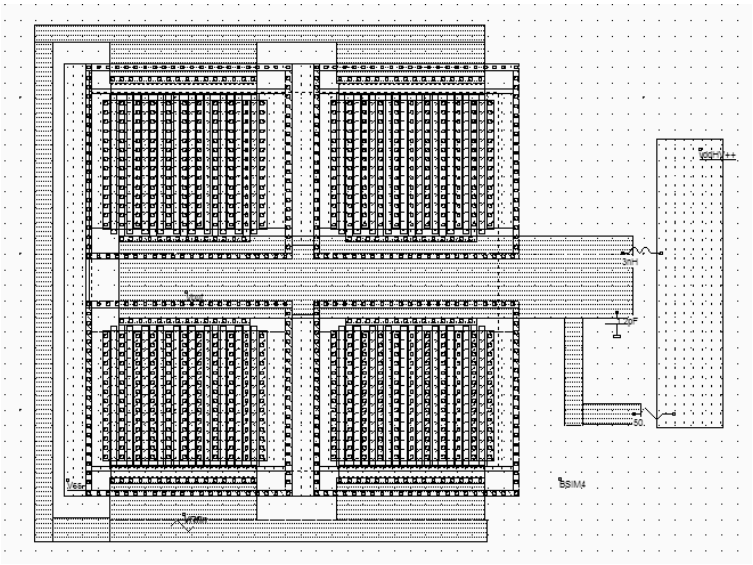


Figure 12-24. The class A amplifier design with a very large MOS device (PowerAmplifierClassA.MSK)

The sinusoidal input offset is 1.3V, the amplitude is 0.4V. The power MOS functional point trajectory is plotted in figure 12-25 and is obtained using the command **Simulate on Layout**. We see the evolution of the functional point with the voltage parameters: as *Vgs* varies from 0.9V to 1.7V, *Ids* fluctuates between 20mA to 70mA. The MOS device is always conducting, which corresponds to class A amplifiers.

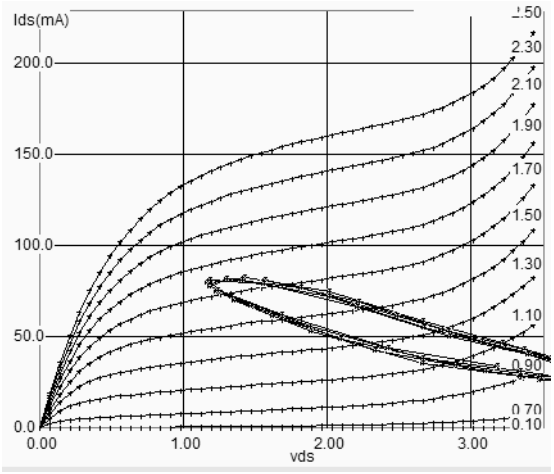


Figure 12-25. The class A amplifier has a sinusoidal input (PowerAmplifierClassA.MSK)

The main drawback of Class A amplifiers is the high bias current, leading to a poor efficiency. In other words, most of the power delivered by the supply is dissipated inefficiently. The power efficiency is around 11% in this layout. The main advantage is the amplifier linearity, which is illustrated by a quasi-sinusoidal output *Vout*, as seen in figure 12-26.

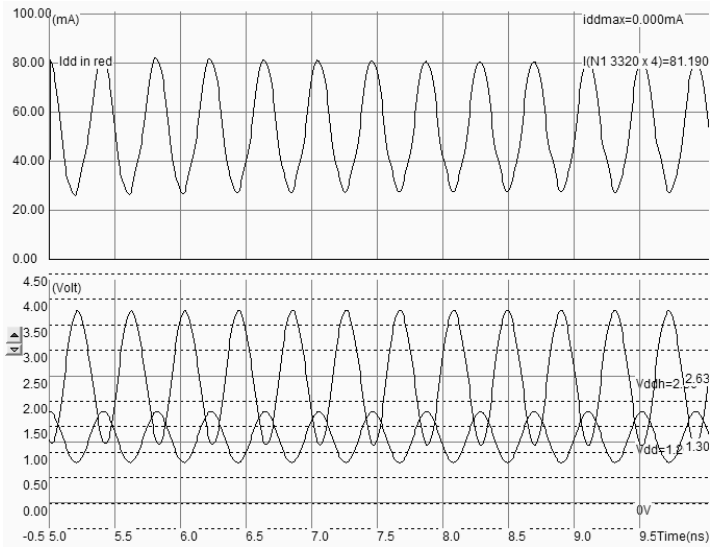


Figure 12-26. The Class A Amplifier simulation (PowerAmplifierClassA.MSK)

Class B Amplifier

In class B, the MOS device only conducts for half a cycle. The monitoring of the current flowing in the power MOS shows a peak of current over the first half of the input period. Over the other half, the power MOS is off, and the LC resonator transmits the power to the 50 ohm load. The power efficiency rises to 20%. The main drawback is the severe distortion of the output voltage, which was much less visible with the class A polarization. The intermediate class, called AB, corresponds to a conduction between half the cycle and the full cycle.

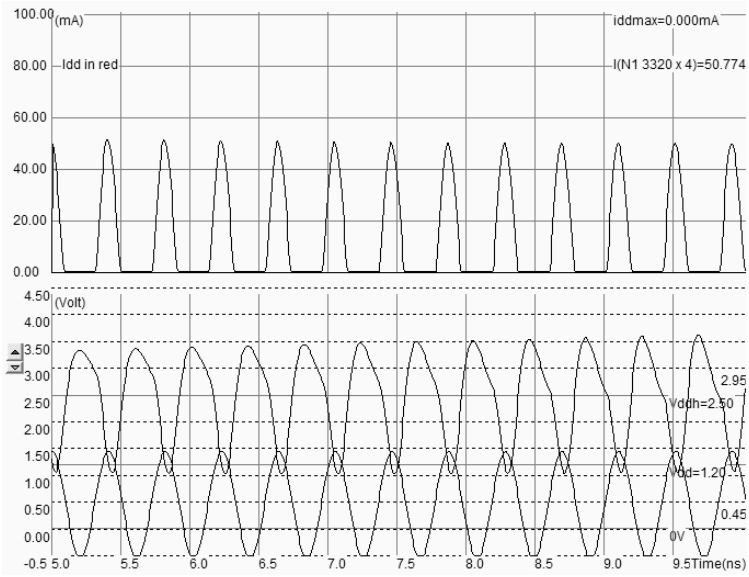


Figure 12-27. The class distinction for the power amplifier is linked to the DC value of the input signal

An evaluation of the spectral contents of the output node may be performed by the Fourier transform, with a plot in logarithmic scale. The Fourier transform is accessible on the simulation menu, through the button **FFT**. The fast Fourier transform translates the voltage waveform of the selected node into an evaluation of the energy of the signal versus its frequency. The energy plot shown in figure 12-28 reveals a peak near 2.5GHz. A noticeable energy is found on the second harmonic (*2xf0*=4900MHz) and third harmonics (*3xf0*). This is the consequence of a non-linear amplifier device.

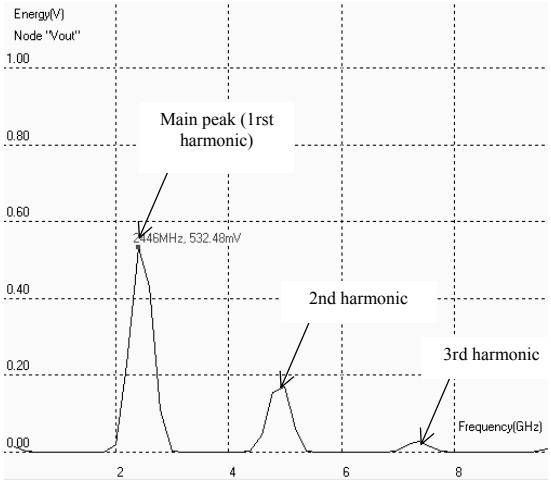


Figure 12-28: The class B amplifier is less linear than the class A amplifier (PowerAmplifierClassB.MSK)

Other classes

In class C, the conduction occurs for less than half the cycle. The increase of efficiency obtained by reducing the conduction period is achieved at the expense of a reduced output power delivered to the load. The class E amplifier schematic diagram is shown in figure 12-29.

A band pass filter (LHF, CHF) is added to the output stage and fitted to the *VRFin* input frequency. The effect of this passive circuit is to decrease the amplitude of the parasitic harmonics due to the non-linear nature of the amplifier, and to pass the desired frequency contribution. In some particular cases, the 3rd or even 5th harmonic is the desired one (Such as is 77GHz automotive radars for example, where the amplifier also serves as a frequency shifter).
The power stage is coupled to the resonator through a coupling capacitor *Cc.* The role of *Cc* is to transfer the energy to the load, without any DC path between the supply and the load. The MOS drain can reach very high values when the switch is OFF. Consequently, a high breakdown voltage transistor is required. The theoretical efficiency of class E amplifier is higher than 50%.

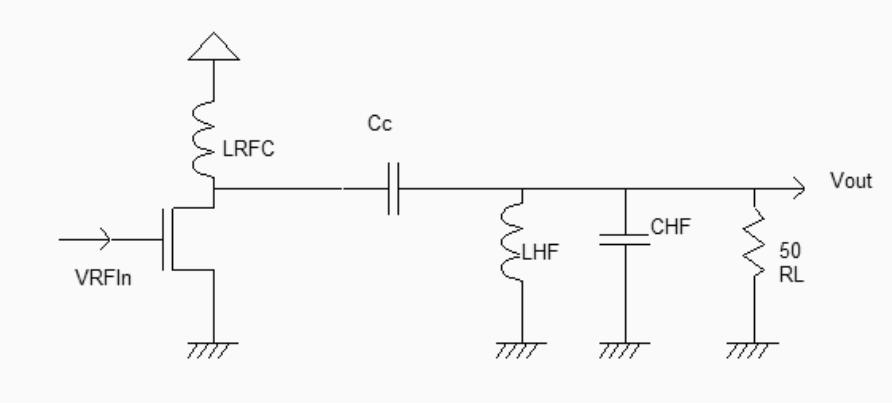


Figure 12-29: Class E amplifier (PowerAmpl.SCH)

Self Heating

Self heating refers to the temperature rise that can occur in power devices, due to excessive heat energy accumulated before being dissipated through the substrate, the package and ultimately through the air. The thermal time constant is the order of one micro-second. Simulations usually consider a typical temperature of 25°C. This is realistic in the case of low power dissipation (Some milli-watts). In the case of hundreds of milliwatts, the simulation should take into account a significant temperature rise near the device. For example, a temperature of 80°C is commonly considered in medium power devices (Below 1W). In some cases, the IC may operate up to 250°C. In Microwind, the operating temperature may be changed in the menu **Simulator Parameters** of the simulation menu. In the window shown in figure 12-30, the temperature is fixed to 85°C.

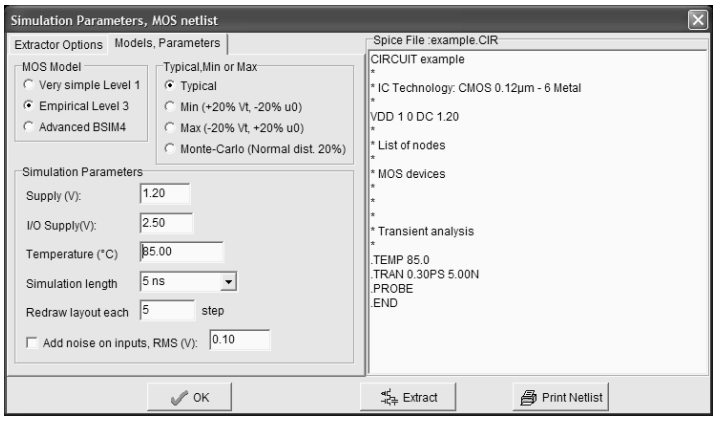


Figure 12-30: Setting up a high temperature for analog simulation

4. Oscillators

The role of oscillators is to create a periodic logic or analog signal with a stable and predictable frequency. Oscillators are required to generate the carrying signals for radio frequency transmission, but also the main clocks of processors.

Ring Oscillator

The ring oscillator is a very simple oscillator circuit, based on the switching delay existing between the input and output of an inverter. If we connect an odd chain of inverters, we obtain a natural oscillation, with a period which corresponds roughly to the number of elementary delays per gate. The fastest oscillation is obtained with 3 inverters (One single inverter connected to itself does not oscillate). The usual implementation consists in a series of five up to one hundred chained inverters. Usually, one inverter in the chain is replaced by a NAND gate to enable the oscillation (Figure 12-31).

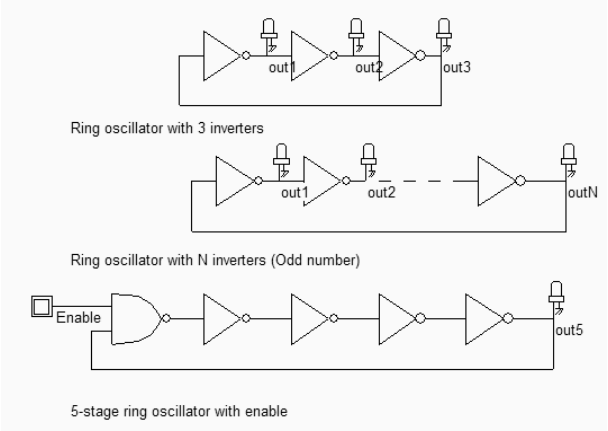


Figure 12-31: A ring oscillator is based on an odd number of inverters (Inv3.SCH)

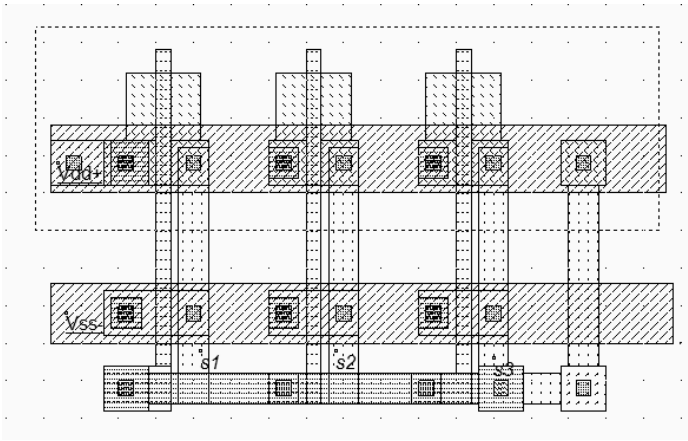


Figure 12-32: The implementation of a 3-inverter oscillator (Inv3.MSK)

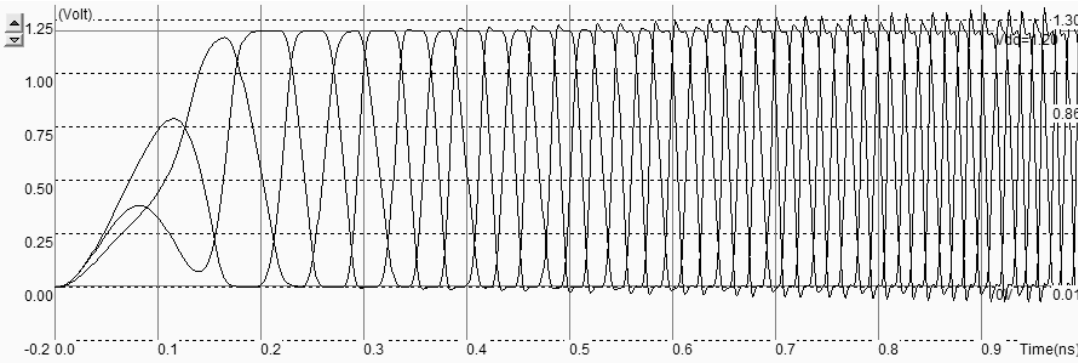


Figure 12-33: The simulation of the 3-inverter ring oscillator (Inv3.MSK)

The 3-inverter ring-oscillator layout is shown in figure 12-32. The right-most inverter output is connect the left-most inverter input by a metal bridge to create the desired feedback. Notice that no clock is assigned in this layout as the oscillation appears naturally, because of an intrinsic instability. The simulation of figure 12-33 shows the "warm-up" of the inverter circuit followed by a stable frequency oscillation.

The main problem of this type of oscillators is the very strong dependence of the output frequency on virtually all process parameters and operating conditions . As an example, the power supply voltage VDD has a very significant importance on the oscillating frequency. This dependency can be analyzed using the **parametric analysis** in the **Analysis** menu. Several simulations are performed with VDD varying from 0.8V to 1.4V with a 50mV step. We clearly observe a very important increase of the output frequency with VDD (Almost a factor of 2 between the lower and upper bounds). This means that any supply fluctuation has a significant impact on the oscillator frequency.

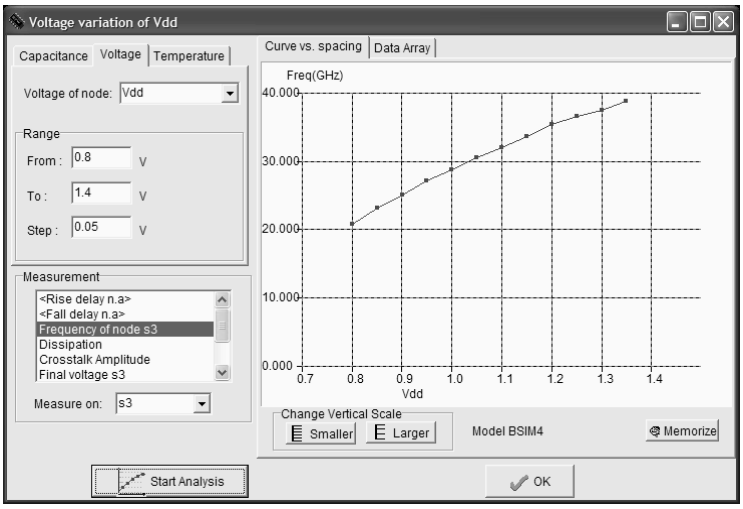


Figure 12-34: The oscillator frequency variation with the power supply (Inv3.MSK)

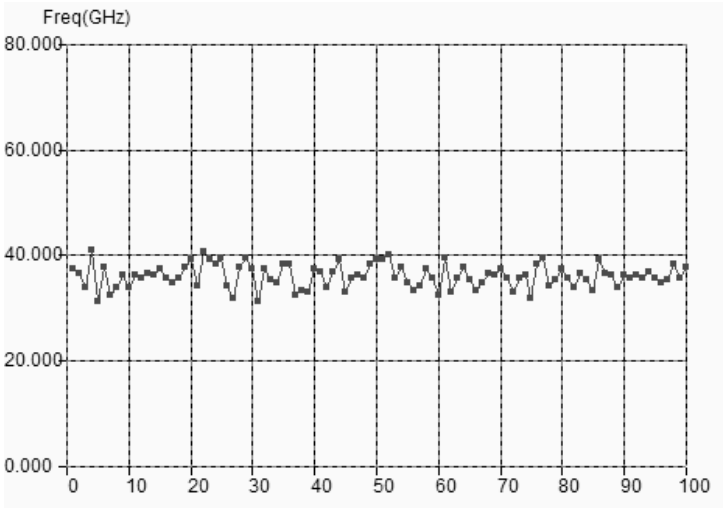


Figure 12-35: The process variations also have a direct impact on the switching frequency (Inv3.MSK)

The oscillation frequency of the ring oscillator is neither stable, nor controllable, and even not precisely predictable, as it is based on the switching characteristics of logic gates which may fluctuate +/-20%. A Monte Carlo analysis is performed in figure 12-35, to observe the technology variation influence on the oscillator frequency. The basic principle of this analysis is to sort a set of technological parameters in a random way, and to conduct the complete analog simulation for each random set. Each point in the X axis corresponds to one simulation, with a specific set of parameters.

There is no correlation between adjacent points, because of the random nature of all the different condition. We observe again the significant fluctuation of the oscillator frequency. As a conclusion, ring oscillators have poor performances, and may only be used in low performance clocking systems, or for a dynamic characterization of the technology. The design of several ring oscillators on CMOS test chips was also experienced to tune Microwind simulations with real-case ring oscillator measurements, and a good correlation between measured and simulated oscillator frequency was obtained.

Random simulation

In Microwind, the threshold and mobility parameters are varying with a *Normal* distribution <Gloss>, with a typical variation of 10%. The normal distribution of the threshold voltage *Vt* corresponds to a density of probability following the equation 12-8. The aspect of *f* versus *Vt* is given in figure 12-36.

$$f_{Vt} = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(Vt-Vt_0)^2}{2\sigma^2}} \qquad \text{(Equ. 12-8)}$$

where

f is the density of probability for a given value of the threshold voltage Vt(0 to 1)

σ=0.1 (Equivalent to 10% typical fluctuation of the parameter)

Vt0=typical threshold voltage (0.4V)

Vt= threshold value (V)

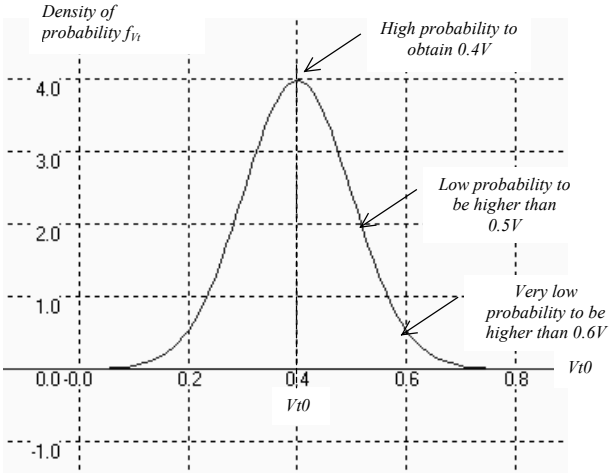


Figure 12-36: The normal distribution of Vt, with a typical variation of 10%

LC oscillator

The LC oscillator proposed in this paragraph is not based on the logic delay, as with the ring oscillator, but on the resonant effect of a passive inductor and capacitor circuit. In the schematic diagram of figure 12-37, the inductor *L1* resonates with the capacitor *C1* connected to S1, combined with *C2* connected to *S2*.

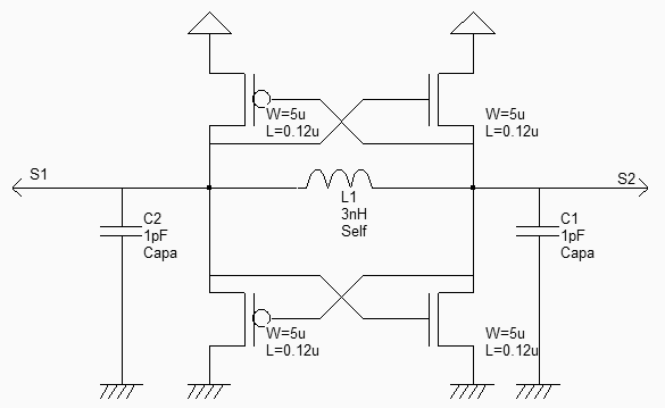


Figure 12-37: A differential oscillator using an inductor and companion capacitor (OscillatorDiff.SCH)

The layout implementation is performed using a 3nH virtual inductor and two 1pF capacitors (Figure 12-38). Notice the large width of active devices to ensure a sufficient current to charge and discharge the huge capacitance of the output node at the desired frequency. Using virtual capacitors instead of on-chip physical coils is recommended during the development phase. It allows an easy tuning of the inductor and capacitor elements in order to achieve the correct behavior. Once the circuit has been validated, the L and C symbols can be replaced by physical components. The time-domain simulation (Figure 12-39) shows a warm-up period around 1ns where the DC supply rises to its nominal value, and where the oscillator effect reaches a permanent state after some nano-seconds. The measured frequency approaches 3.75GHz with a 3nH inductor *L1* of and 1pF capacitors *C1* and *C2*.

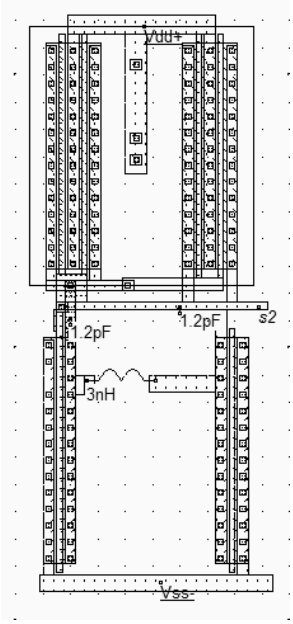


Figure 12-38: A differential oscillator using 3nH inductor (OscillatorDiff.MSK)

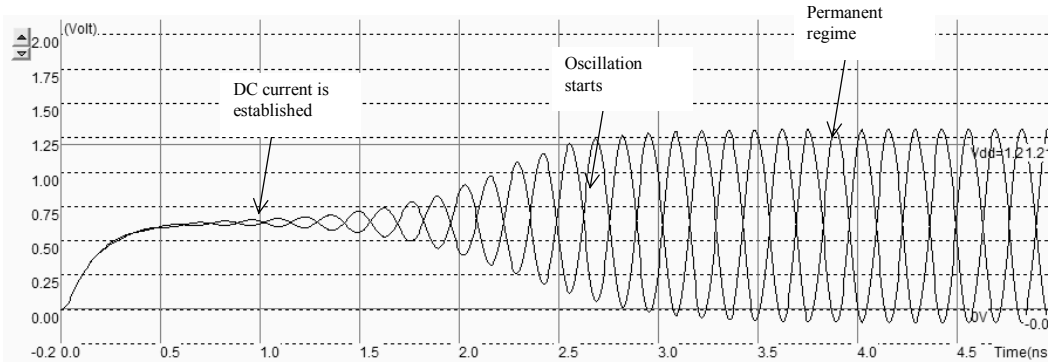


Figure 12-39: Simulation of the differential oscillator (OscillatorDiff.MSK)

The Fourier transform of the output *s1* reveals a main sinusoidal contribution at f0=3.725GHz as expected, and some harmonics at *2xf0* and *3xf0* (Figure 12-40). The remarkable property of this circuit is its ability to remain in a stable frequency even if we change the supply voltage or the temperature, which features a significant improvement as compared to the ring oscillator. Furthermore, the variations of the MOS model parameters have almost no effect on the frequency.

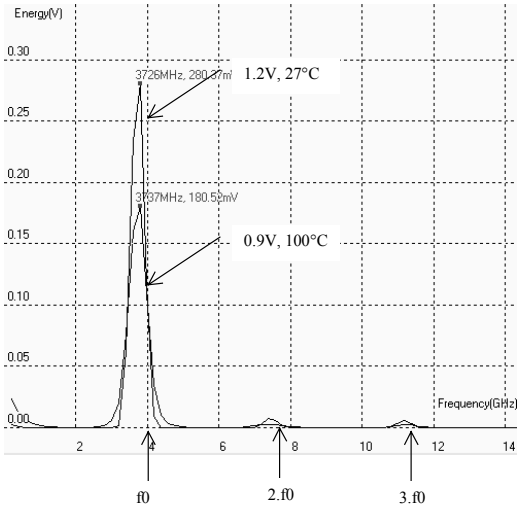


Figure 12-40: The frequency spectrum of the oscillator (OscillatorDiff.MSK)

For example, we may investigate the effect of VDD on the resonating frequency by lowering manually VDD from 1.2V down to 0.9V in the menu **Simulate→Simulation parameters**. The result is a significant increase of the warm-up phase, while the final oscillation frequency remains unchanged. A parametric analysis on VDD, from 0.7 to 1.4V, confirms that the LC oscillator performs much better than the ring-inverter oscillator, as it turns out to be almost immune to supply voltage fluctuations.

Unfortunately, the inductance of an on-chip coil is not perfectly constant, as the material resistance, conductor width and oxide thickness may vary by several %. The capacitance of a poly/poly2 structure, used for implementing the passive capacitor, may also vary due to the process fluctuation impact on the inter-layer oxide. The temperature also has an influence on the capacitance value [Reference].

In Microwind, the Monte-carlo simulation mode also impacts the value of all virtual elements in a similar way as for the threshold voltage and the mobility: before the simulation starts, the *L* and *C* values are assigned a value that fluctuates by +/-10% with a normal distribution around the user-defined impedance. The result is a significant variation of the oscillator frequency with the process parameters (Figure 12-41).

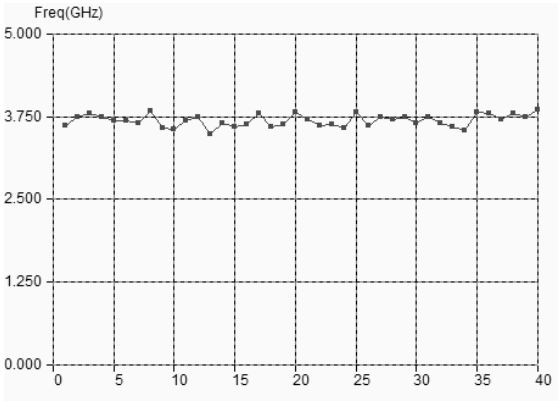


Figure 12-41: The frequency of the LC oscillator varies with the process parameters, mainly due to the capacitor and inductor process dependence (OscillatorDiff.MSK)

It can be concluded that a predictable and stable frequency oscillation is very hard to obtain on-chip, without any external high precision component. In radio-frequency applications, abase frequency is always delivered by a Quartz, which is the best discrete device to create an almost perfect oscillation circuit.

Voltage Controlled Oscillator

The voltage controlled oscillator (VCO) generates a clock with a controllable frequency. The VCO is commonly used for clock generation in phase lock loop circuits, as described later in this chapter. The clock may vary typically by +/-50% of its central frequency. A current-starved voltage controlled oscillator is shown in figure 12-42 [Weste] . The current-starved inverter chain uses a voltage control *Vcontrol* to modify the current that flows in the *N1*,*P1* branch. The current through *N1* is mirrored by *N2,N3* and *N4*. The same current flows in *P1*. The current through *P1* is mirrored by *P2*, *P2*, and *P4*. Consequently, the change in *Vcontrol* induces a global change in the inverter currents, and acts directly on the delay. Usually more than 3 inverters are in the loop. A higher odd number of stages is commonly implemented, depending on the target oscillating frequency and consumption constraints.

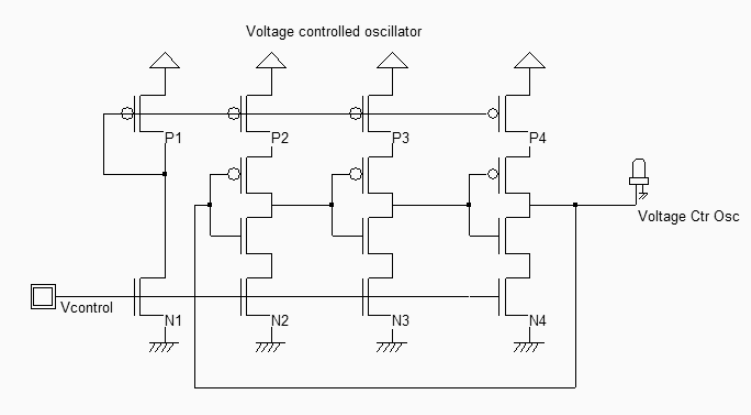


Figure 12-42: Schematic diagram of a voltage controlled oscillator (VCOMos.SCH)

The implementation of the current-starved VCO for a 5-inverter chain is given in figure 12-43. The current mirror is situated on the left. Five inverters have been designed to create the basic ring oscillator. Then a buffer inverter is situated on the right side of the layout.

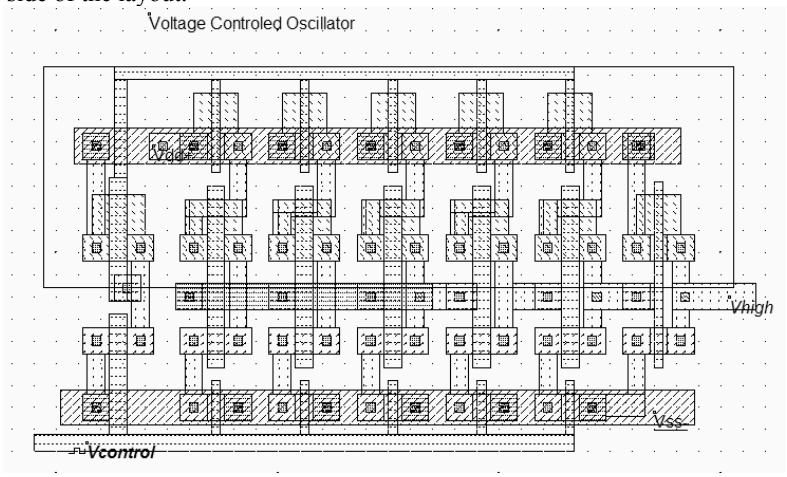


Figure 12-43. A VCO implementation using 5 chained inverters (VCO.MSK)

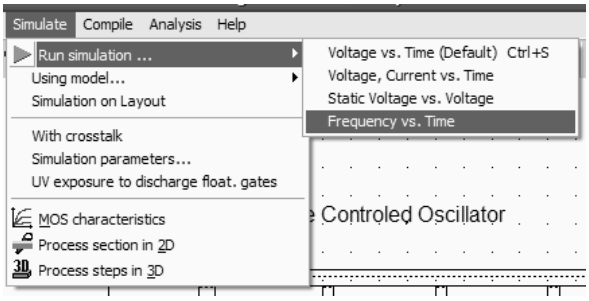


Figure 12-44. The access to Frequency vs. time simulation mode

The VCO circuit frequency variation with *Vcontrol* is accessed by using the layout shown in figure 12-43. A convenient simulation mode is directly accessible (figure 12-44), to display the frequency variations versus time together with the voltage variations. The frequency is evaluated on the selected node, which is the output node *Vhigh* in this case.

No oscillation is observed for an input voltage *Vcontrol* lower than 0.5V. Then the VCO starts to oscillate, but the frequency variation is clearly not linear. The maximum frequency is obtained for the highest value of *Vcontrol*, around 8.4GHz. By increasing the number of inverters and altering the size of the MOS current sources, we may modify the oscillating frequency easily.

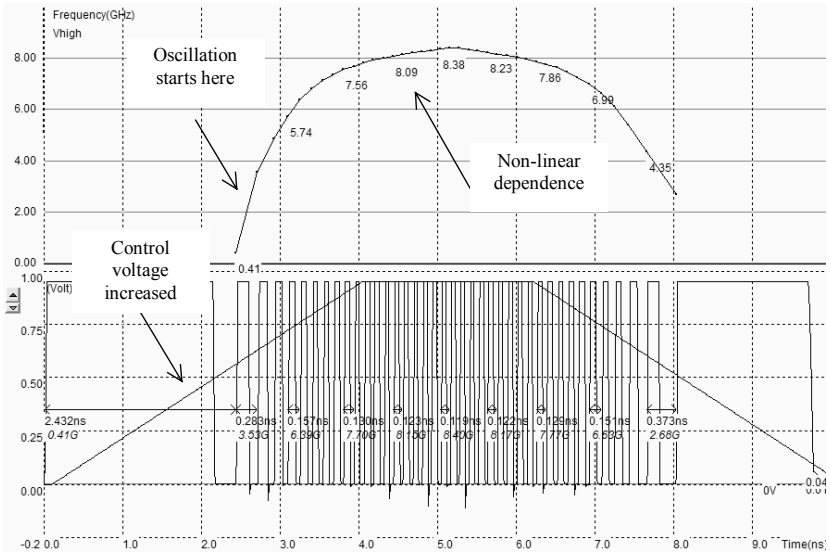


Figure 12-45. The frequency variations versus the control voltage show a non-linear dependence (VCO.MSK)

High Performance VCO

A voltage controlled oscillator with good linearity is shown in figure 12-46. This circuit has been implemented in several test-chips with successful results in 0.8, 0.35 down to 0.18µm technologies. The principle of this VCO is a delay cell with linear delay dependence on the control voltage [Bendhia]. The delay cell consists of a p-channel MOS in series, controlled by *Vcontrol* ,and a pull-down n-channel MOS, controlled by *Vplage*. The delay dependence on *Vcontrol* is almost linear for the fall edge. The key point is to design an inverter just after the delay cell with a very low commutation point *Vc*. The rise edge is almost unchanged. To delay both the rise and fall edge of the oscillator, two delay cells are connected, as shown in the schematic diagram.

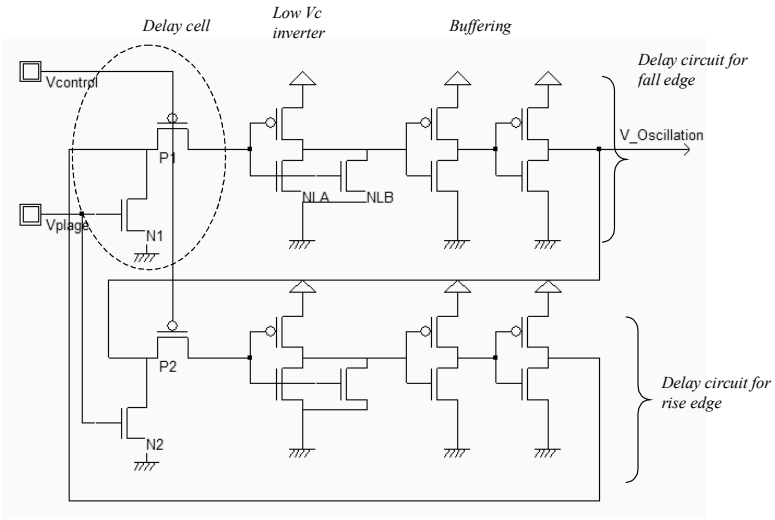


Figure 12-46: The layout implementation of a high performance VCO circuit (VCOLinear.MSK)

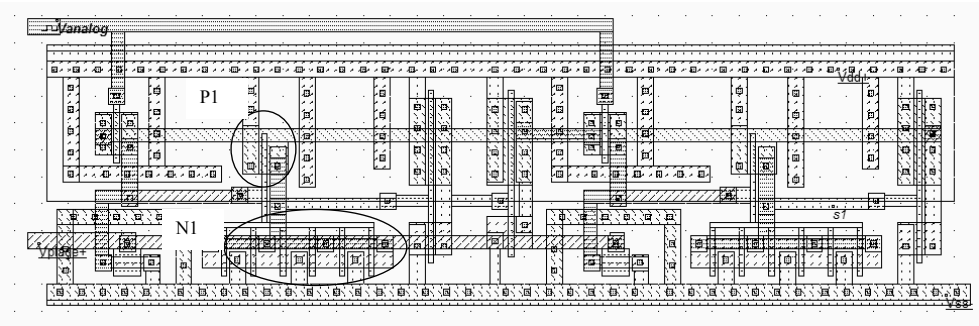


Figure 12-47: The layout implementation of a high performance VCO circuit (VCOLinear.MSK)

The layout of the VCO is a little unusual due to the needs for a very low commutation point for the inverter situated immediately after the delay cells. This is done by implementing a large n-channel MOS (N1 in figure 12-47) with high drive capabilities and a tiny p-channel MOS with low drive capabilities (P1 in figure 12-47).

The simulation of a high performance VCO circuit is given in figure 12-48. A quasi-linear dependence of the oscillating frequency on the input voltage control is observed within the range 0..0.6V. Although not displayed in the simulation, the voltage of *Vplage* has a strong influence on the oscillating frequency range. A high value of *Vplage* (Close to VDD) corresponds to a high frequency oscillation, while a low value (Close to the threshold voltage *Vt*) corresponds to a low frequency oscillation.

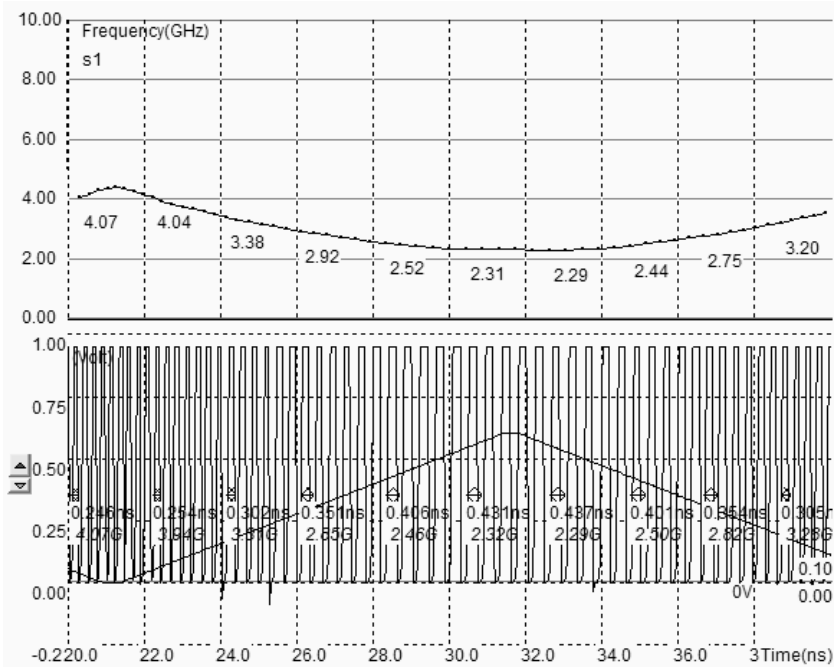


Figure 12-48: The simulation of a high performance VCO circuit (VCOLinear.MSK)

The main drawback of this type of oscillator is the great influence of temperature and VDD supply on the stability of the oscillation. If we change the temperature, the device current changes, and consequently the oscillation frequency is modified. Such oscillators are rarely used for high stability frequency generators.

5. Phase-Lock Loop

The phase-lock-loop (PLL<Gloss>) is commonly used in microprocessors to generate a clock at high frequency (F_{out}=2GHz for example) from an external clock at low frequency (F_{ref} = 100MHz for example). Clock signals in the range of 1GHz are very uneasy to import from outside the integrated circuit because of low pass effect of the printed circuit board tracks and package leads. The PLL is also used as a clock recovery circuit to generate a clock signal from a series of bits transmitted in serial without synchronization clock (Figure 12-49). The PLL may also be found in frequency demodulation circuits, to transform a frequency varying waveform into a voltage.

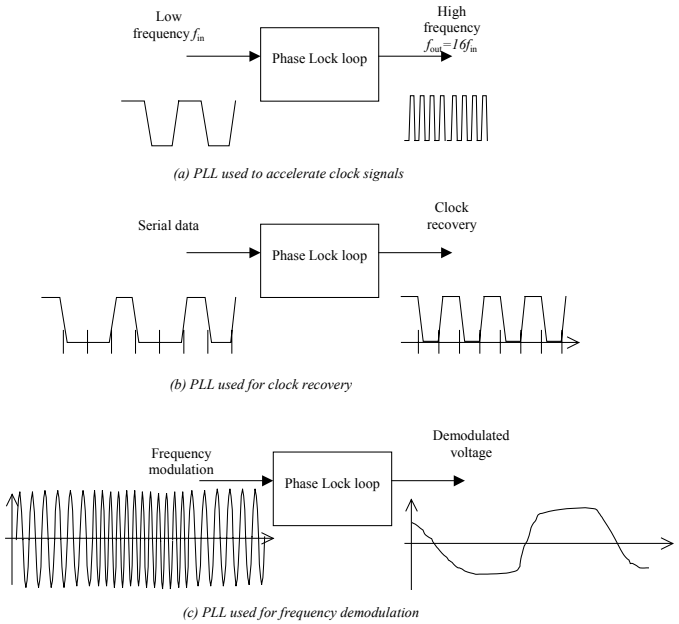


Figure 12-50. Principles of phase lock loops

The PLL uses a high frequency oscillator with varying speed, a counter, a phase detector and a filter (figure 12-51). The PLL includes a feedback loop which lines up the output clock *ClkOut* with the input clock *ClkIn* through a phase locking stabilization process. When locked, the high input frequency f_{out} is exactly $Nx\, f_{in}$. A variation of the input frequency f_{in} is transformed by the phase detector into a pulse signal which is converted into variation of the analog signal *Vc*. This signal changes the VCO frequency which is divided by the counter and changes *clkDiv* according to f_{in}.

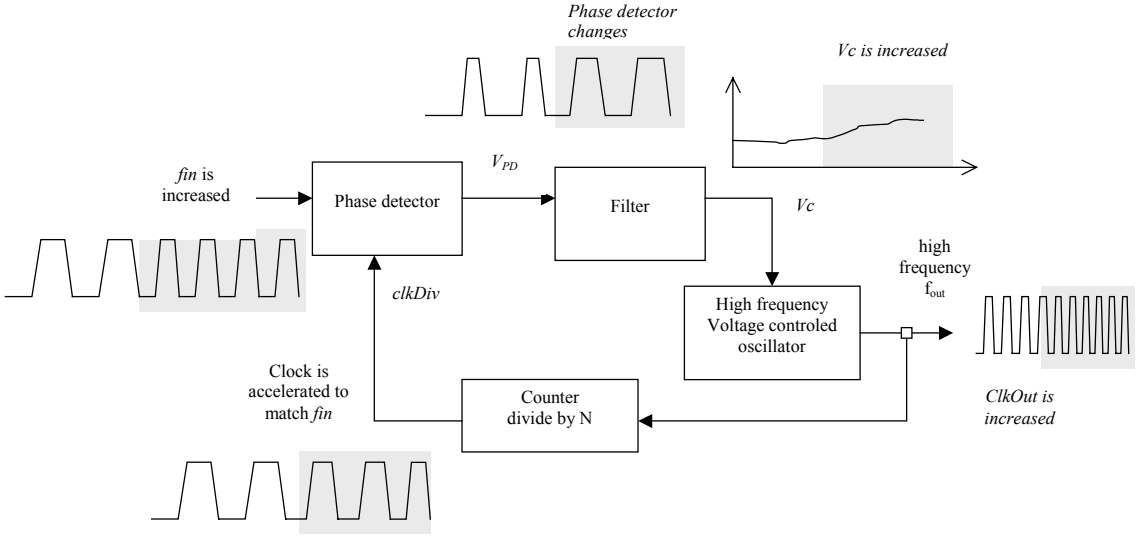
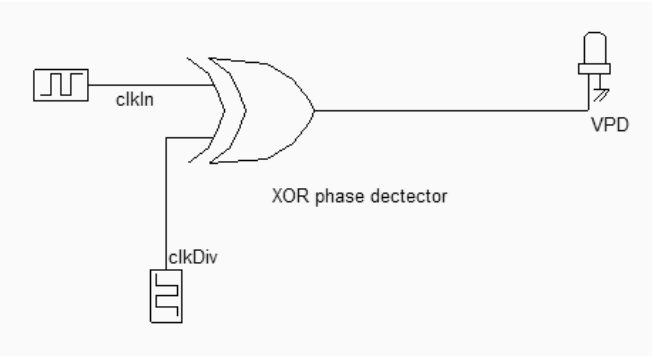


Figure 12-51. Principles of phase lock loops

PHASE DETECTOR

The most simple phase detector is the XOR gate. The XOR gate output produces a regular square oscillation V_{PD} when the input *clkIn* and the signal *divIn* have one quarter of period shift (or 90° or π/2). For other angles, the output is no more regular. In figure 12-52, two clocks with slightly different periods are used in Dsch2 to illustrate the phase detection.



ClkIn	DivIn	Xor
0	0	0
0	1	1
1	0	1
1	1	0

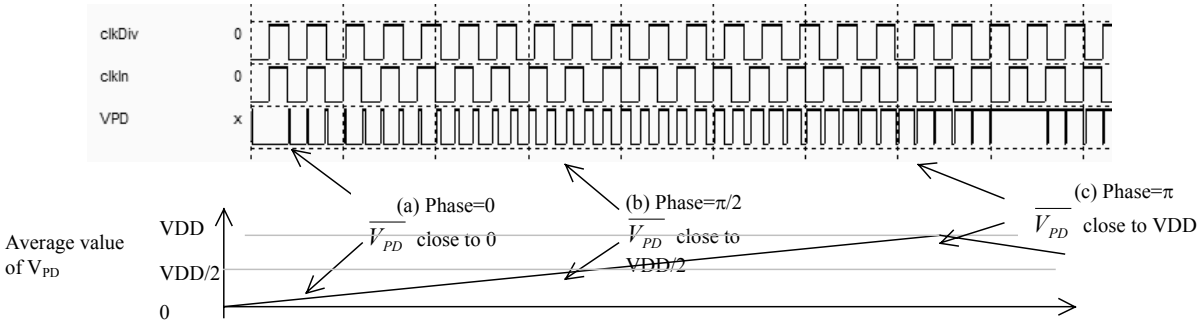


Figure 12-52. The XOR phase detector at work (PhaseDetectXor.SCH)

At initialization, (Figure 12-52) the average value of the XOR output $\overline{V_{PD}}$ is close to 0. When the phase between *clkDiv* and *clkIn* is around π/2, $\overline{V_{PD}}$ is VDD/2. Then it increases up to VDD. Consequently, $\overline{V_{PD}}$ and the phase difference are linked by expression 12-10. For example, when Δϕ=π/2, $\overline{V_{PD}}$ is VDD/2.

$$\overline{V_{PD}} = \frac{VDD.\Delta\phi}{\pi} \qquad \textit{(Equ. 12-10)}$$

The gain of the phase detector is the ratio between $\overline{V_{PD}}$ and Δϕ. The gain is often written as K_{PD}, with an expression derived from equation 12-10, which is valid for Δϕ between 0 and π, as drawn in figure 12-53.

$$K_{PD} = \frac{VDD}{\pi} \qquad \textit{(Equ. 12-11)}$$

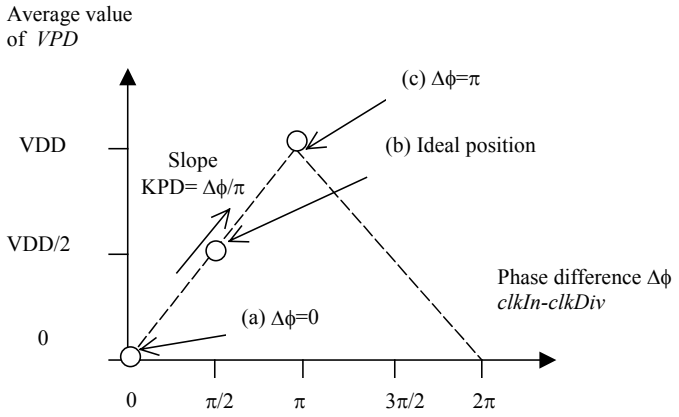


Figure 12-53. The XOR phase detector at work (PhaseDetectXor.SCH)

When the phase difference is larger than π, the slope sign is negative until 2π. When locked, the phase difference should be close to π/2.

Filter

The filter is used to transform the instantaneous phase difference V_{PD} into an analog voltage V_c which is equivalent to the average voltage $\overline{V_{PD}}$. The rapid variations of the phase detector output are converted into a slow varying signal V_c which will later control the voltage controlled oscillator. Without filtering, the VCO control would have too rapid changes which would lead to instability. The filter may simply be a large capacitor C, charged and discharged through the R_{on} resistance of the switch. The $R_{on}.C$ delay creates a low-pass filter. Figure 12-54 shows a XOR gate with the output charged with a large poly/poly2 capacitor and a serial resistance to create the desired analog voltage control V_c.

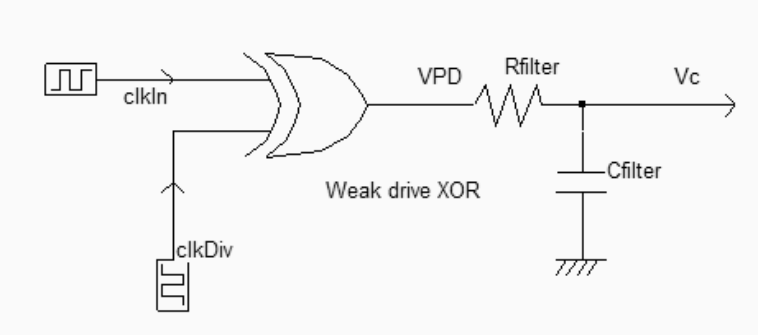


Figure 12-54. Large load capacitance and weak XOR output stage to act as a filter (phaseDetectAndFilter.SCH)

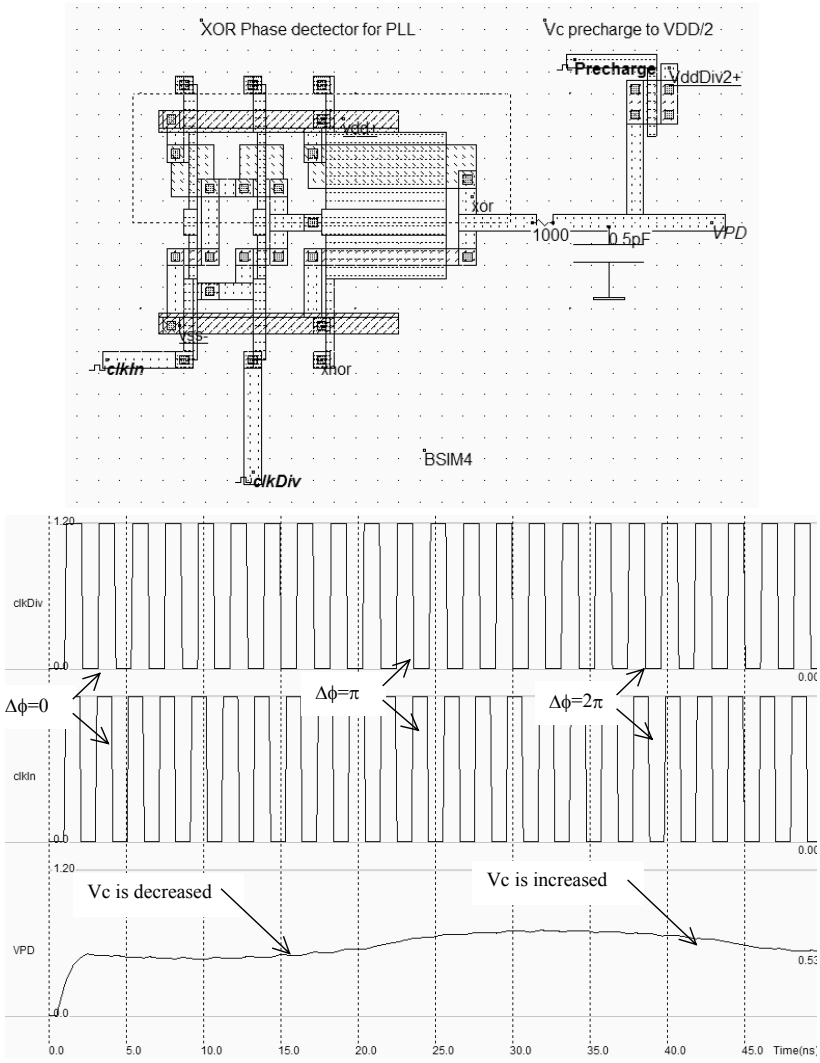


Fig. 12-55. Response of the phase detector to slightly different input clocks (phaseDetect.MSK)

In the figure above, the filtered version of the XOR gate output *VPD* is shown. It can be seen that *VPD* is around VDD/2 when the phase difference is $\pi/2$ or $-\pi/2$. The duty cycle of the phase detector output should be as close as possible to 50%, so that *Vc* is very close to VDD/2 when the inputs are in phase. If this is not the case, the PLL would have problems locking or would not produce a stable output clock. The XOR gate layout has been modified so that the output voltage *Vc* is very close to VDD/2 when one input in fixed to ground and the other input is a regular clock.

Voltage controlled oscillator for PLL

Important characteristics of the PLL can be listed:

- The oscillating frequency should be restricted to the required bandwidth. For example, in European mobile phone applications, the VCO frequency should be varying between f_{low}=1700 and f_{high}=1800MHz (Figure 12-56).

- Due to process variations, the VCO frequency range should be extended to f_{min}, f_{max}, typically 10% higher and lower than the request range (figure 12-56).
- When the control voltage *Vc* is equal to VDD/2, the VCO clock should be centered in the middle of the desired frequency range.
- The duty cycle of the VCO clock output should be as close as possible to 50% [Baker]. If this is not the case, the PLL would have problems locking or would not produce a stable output clock.

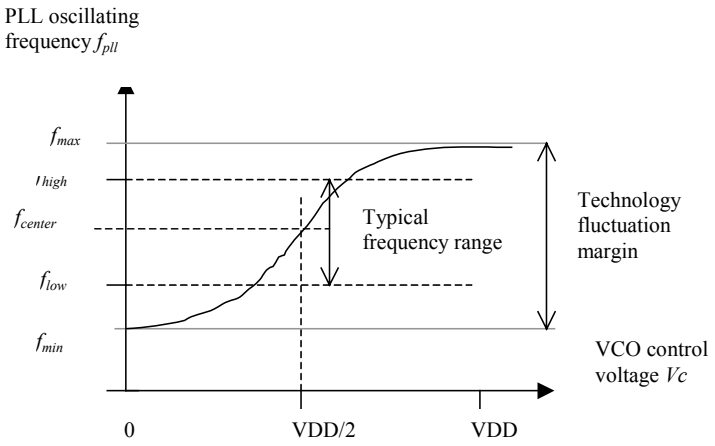


Figure 12-56: Requirements for the VCO used in the PLL

The current starved oscillator can be used as a VCO for the phase lock loop, with a modification of its voltage control circuit so that the center frequency is 2450MHz at Vc=VDD/2, and the frequency range does not exceed 2800MHz and does not drop lower than 1800MHz. The modification consists in providing a permanent current path through *Rvdd2* to VDD/2 (Figure 12-57), which helps keeping *Vc* around VDD/2. When *VPD* is VDD, *Vc* is increased and the VCO frequency is close to f_{max}. When *VPD* is 0, *Vc* is lowered and the VCO frequency is close to f_{min}.

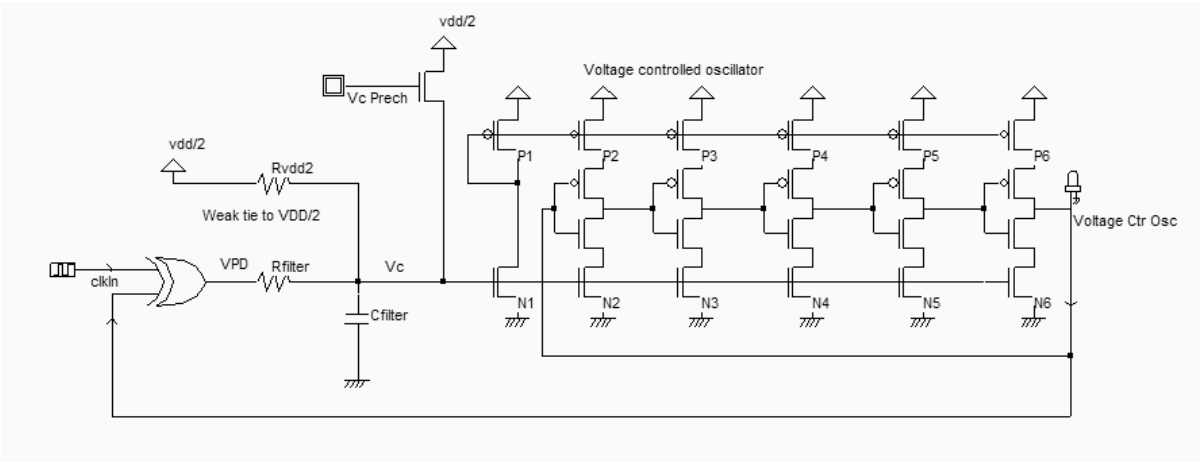


Figure 12-57: Connecting the current-starved VCO to the phase detector (Pll.SCH)

A second important sub-circuit added in the PLL is the precharge to VDD/2. The nMOS device controlled by *Vc_Prech* helps the big capacitor *Cfilter* to reach VDD/2 during the first nanoseconds. This precharge circuit speeds up the locking of the PLL.

Complete Phase Lock Loop

The implementation of the PLL shown in figure 12-58 is a direct copy of the schematic diagram of figure 12-57. Notice that the resistor *Rfilter* (1000Ohm) and *Rvdd2* (5000 Ohm) have been implemented using virtual elements and not physical resistance. The same can be said for the capacitor *Cfilter* (0.3pF). However, these resistance and capacitance are easy to integrate on-chip.

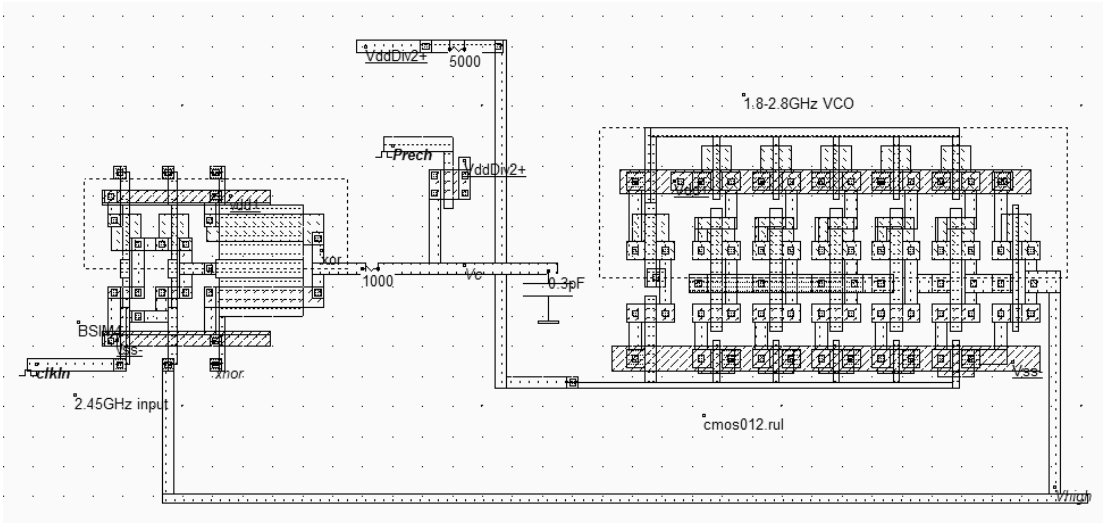


Figure 12-58: Connecting the current-starved VCO to the phase detector (VCOPll.SCH)

The input frequency is fixed to 2.44GHz. During the initialization phase (Simulation of figure 12-59), the precharge is active, which pushes rapidly the voltage of *Vc* around VDD/2. The VCO oscillation is started and the phase detector starts operating erratically. The output *Xnor* is an interesting indication of what happens inside the phase detector. We see that the phase difference is very important during the first 10 nanoseconds. Then, the VCO output starts to converge to the reference clock. In terms of voltage control, *Vc* tends to oscillate and then converge to a stable state where the PLL is locked and stable. The output is equal to the input, and the phase difference is equal to one fourth of the period ($\pi/2$) according to the phase detector principles.

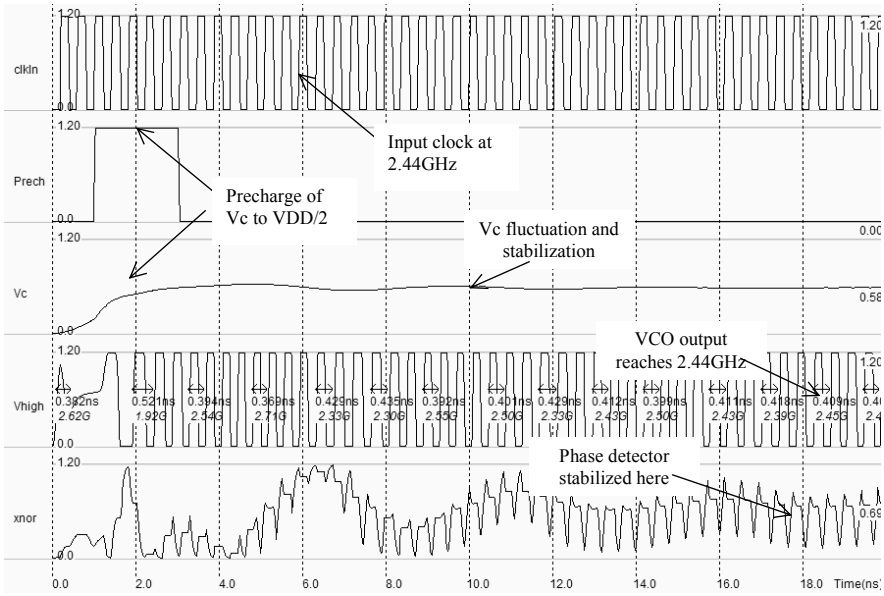


Figure 12-58: Simulation of the PLL showing the locking time (VCOPll.SCH)

Frequency demodulation

The PLL may be used to transform a frequency into a voltage. When clocks with a small frequency difference are applied serially to the input of the PLL thanks to a multiplexor, the *Vc* voltage changes accordingly. A fast clock leads to a high Vc voltage, a slow clock to a low *Vc* voltage.

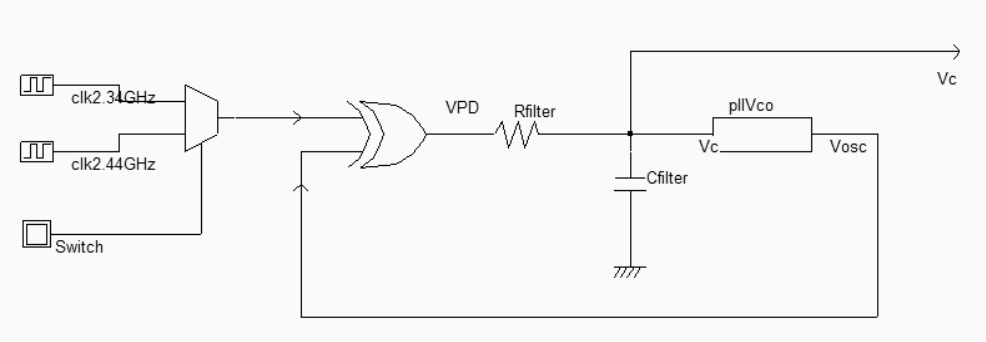


Figure 12-59: Using the PLL for frequency demodulation (PllFm.SCH)

Multiplexing clocks is done by a CMOS multiplexor, with a switching from one clock to the next every each 25ns. The simulation shows that *Vc* is decreased when the input frequency is decreased. Over a certain range of input frequencies, the circuit is able to convert a frequency into a voltage in a linear way, which is the based of frequency demodulation.

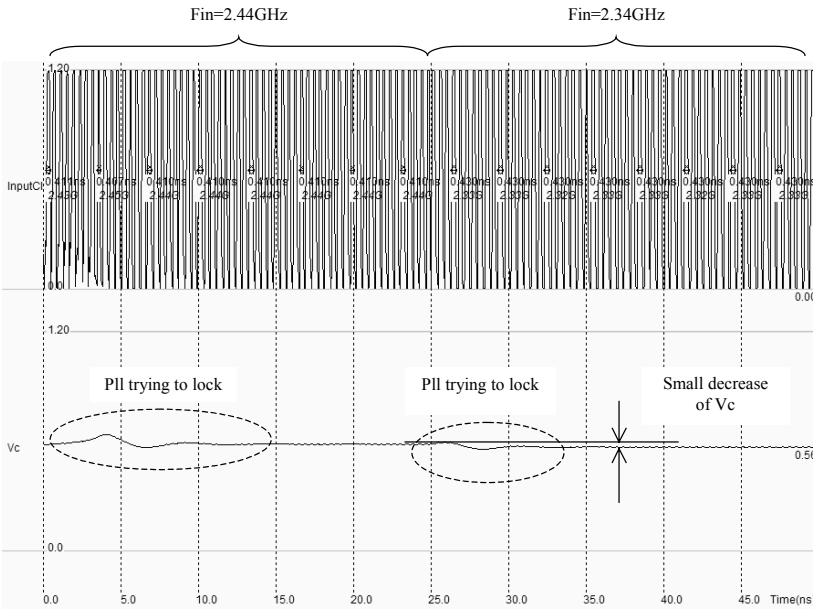


Figure 12-60:Frequency demodulation using the PLL(PllFm.MSK)

Frequency synthesis

One very important application of PLL in micro-processors and controllers consists in generating a fast on-chip clock from a slow external clock, usually fixed by a quartz. The fast clock signal is synthesized by the VCO and its stability is controlled by the PLL. The new feature is a clock divider circuit on the path of the feedback loop, as shown in figure 12-61. The fast clock is divided by N which can be programmed by the user. For example, a 100MHz external clock may be used to create a 500,600,700 or 800MHz internal clock. In that case, N is 5,6,7 or 8. The VCO should cover the range 500-800MHz with sufficient margin due to process variations.

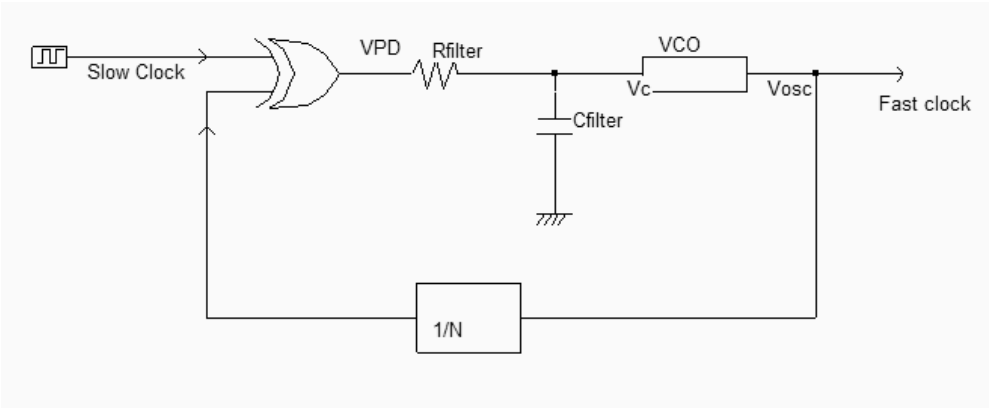


Figure 12-61:Frequency synthesis to generate a fast clock (PllDigital.SCH)

A schematic diagram for the frequency divider by N is given in figure 12-62. The number N is fixed on the keyboard and the circuit performs the division of the input clock *Clock1* by N, with a result appearing on *ClkOut*. In the logic simulation, once the *Reset* is inactive, the number N is fixed on the keyboard.

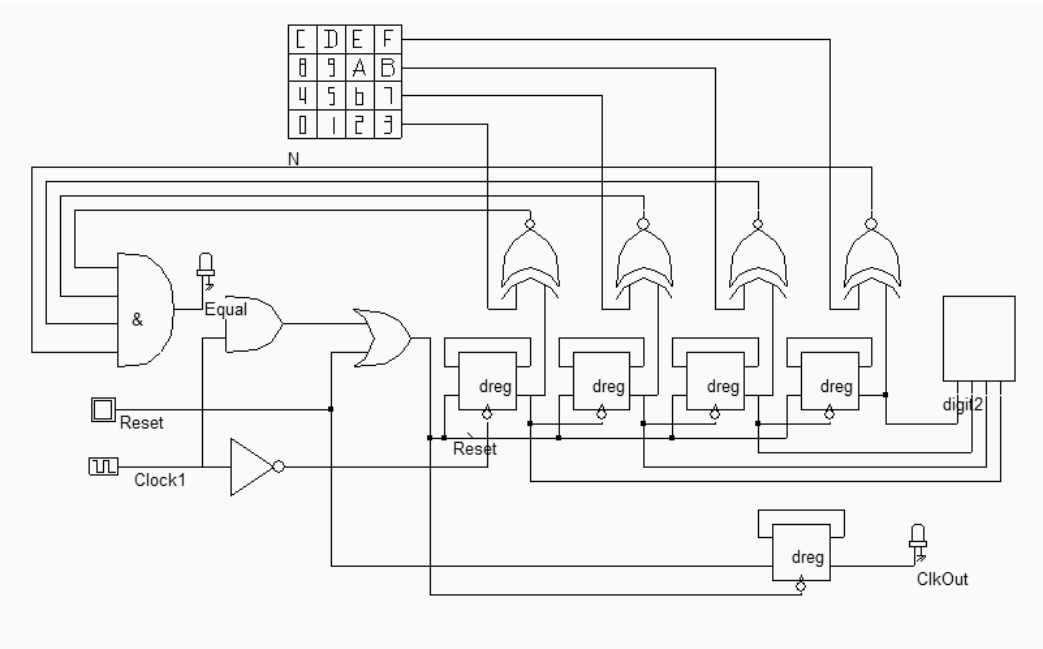


Figure 12-62 Programmable clock divider for the Digital Phase lock loop (PllDivn.SCH)

When the asynchronous counter attains the desired value N, an *Equal* pulse appears in the loop thanks to the XNOR comparators and the AND gate, which provokes an asynchronous *Reset* and restarts the counter.

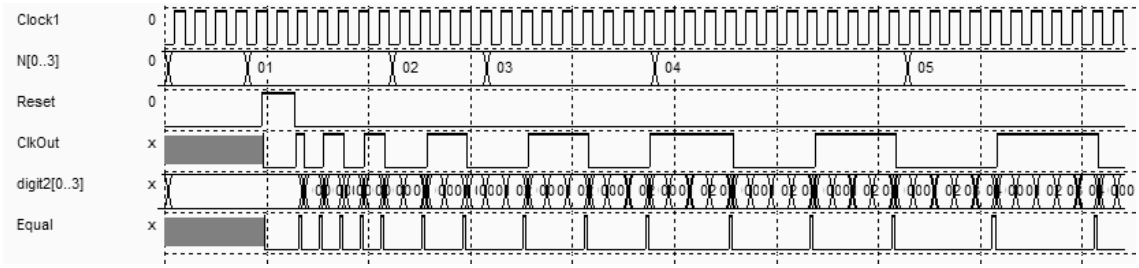


Figure 12-63 Simulation of the clock divider for various values of N (PllDivn.SCH)

An implementation of the frequency synthesizer into layout is proposed for N fixed to 8. The reference clock is 100MHz, the VCO target clock is 800MHz. A three stage clock divider is implemented on the layout to divide the VCO clock by 8 before entering the phase comparator. The VCO transistor sizing has been rearranged to produce a 800MHz oscillation around VDD/2, which eases the locking. Furthermore, the filter capacitance has been increased to 2pF to avoid instability in the VCO.

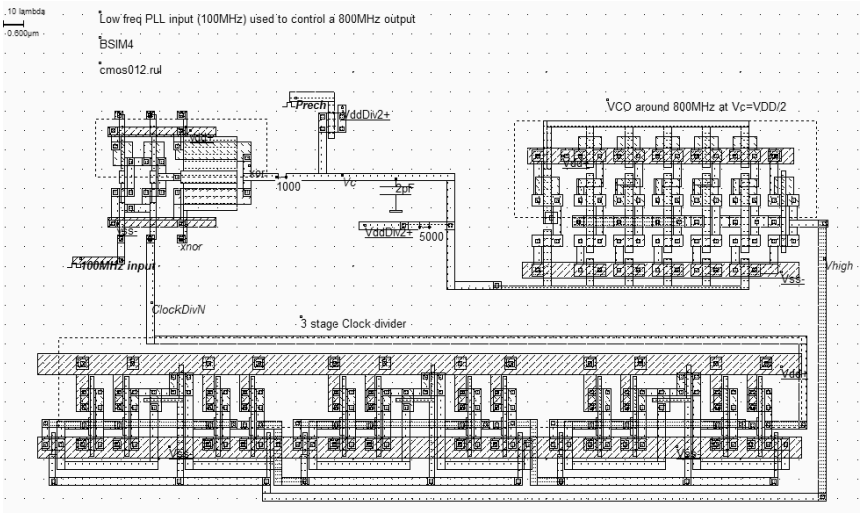


Figure 12-64: A 100MHz external reference clock used to control a 800MHz on-chip clock (PllDigital.MSK))

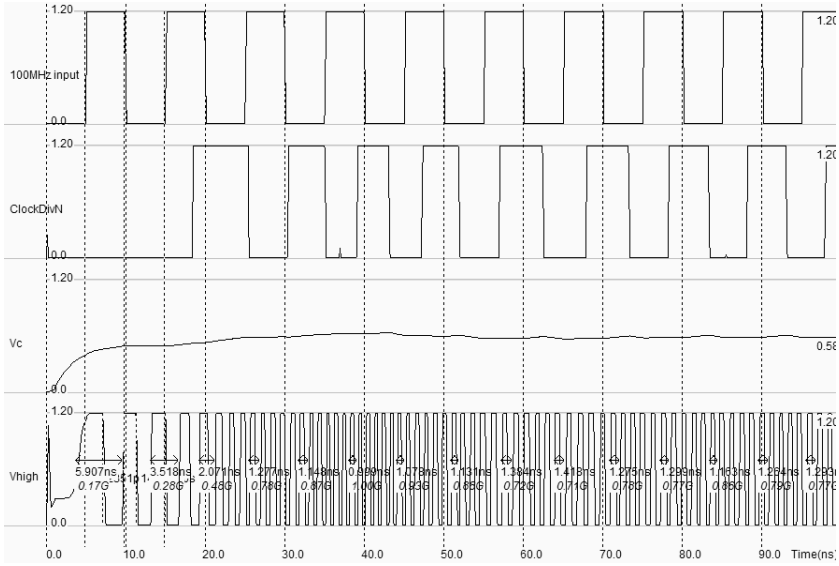


Figure 12-65: Simulation of the 800MHz PLL controlled by a 100MHz external clock (PllDigital.MSK))

In the simulation of figure 12-65, the first 20ns correspond to the initialization phase. The VCO is warmed up and the clock divider starts to produce the signal *ClockDivN*, which is equal to *Vhigh* divided by 8. Around 80ns are required to lock the VCO to the desired frequency (100x8=800MHz). What we observe in the output signal is a phenomenon called jitter: the output frequency is not stable as *Vc* fluctuates around 0.6V. The VCO output exhibits a spread of frequency around 800MHz.

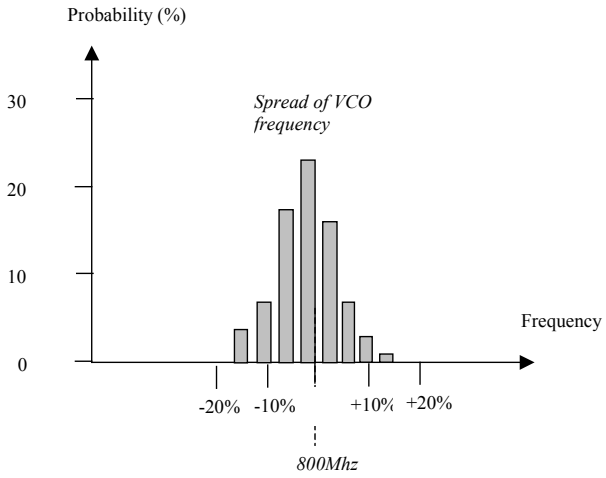


Figure 12-66: The VCO frequency is jittering around 800MHz (PllDigital.MSK))

The requirements in terms of jitter are very severe in most PLL designs. For example, the PLL used in mobile phones should produce a very stable frequency around 800MHz with less than 100KHz jittering. In some cases however, a voluntary jitter is added to the PLL, which creates a small fluctuation of the synthesized clock. This technique is found in some clock synthesis circuits in micro-controllers, to transform the perfect synchronous clocking into a slightly asynchronous clocking, which lowers the peaks of parasitic interferences.

Several techniques exist to lower the jitter, that are described in [Baker]:

- Lowering the gain of the VCO. The effect of *Vc* is less important than the VCO frequency. The drawback is the reduction in frequencies lock range.
- Increasing *Rfilter* and *Cfilter*. The effect of *VPD* change is less important on the VCO control. The drawback is a larger locking time, and a larger silicon area required to implement the capacitance. A very high value for the on-chip resistance is not recommended as it generates a parasitic noise proportional to the resistance.
- Reducing the gain of the phase detector. The sizing of the XOR gate may be changed to produce less current. However, the MOS parasitic noise is increased, the design is more sensitive to supply and substrate noise, which tends to cancel the benefits of a lower phase gain.

6. Frequency Converter

Principles

In many situations for radio frequency emitters and receivers, there is a need for shifting an input waveform into a lower or higher frequency waveform. From an emission point of view, most of the signal processing is done within the range 10-100MHz. However, the emission bandwidth may be significantly higher (900MHz, 1.8GHz for mobile, 2.4, 5GHz for wireless local area network).

A direct generation of the desired signal at such a high frequency would consume too much power. A low power frequency translator circuit is preferred. In the case of figure 12-67, the frequency converter shifts the original signal (Say 100MHz) to the desired emission frequency 900MHz.

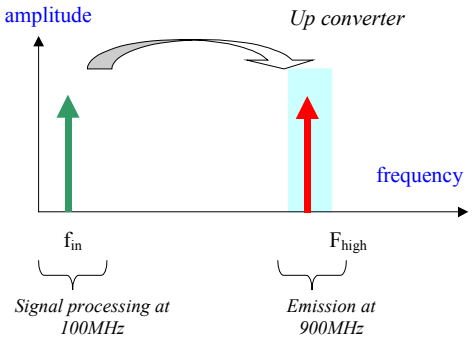


Figure 12-67: the principles for frequency conversion

The operation which translates a high frequency signal into a low frequency signal is called down conversion. In frequency domain, it consists in shifting a high frequency information contained in frequency f_{in} to a lower frequency f_{low}, as illustrated in figure 12-68. The information contained in the original signal fin (Which may include an amplitude, frequency or phase variation) is preserved in the resulting signal *fout*.

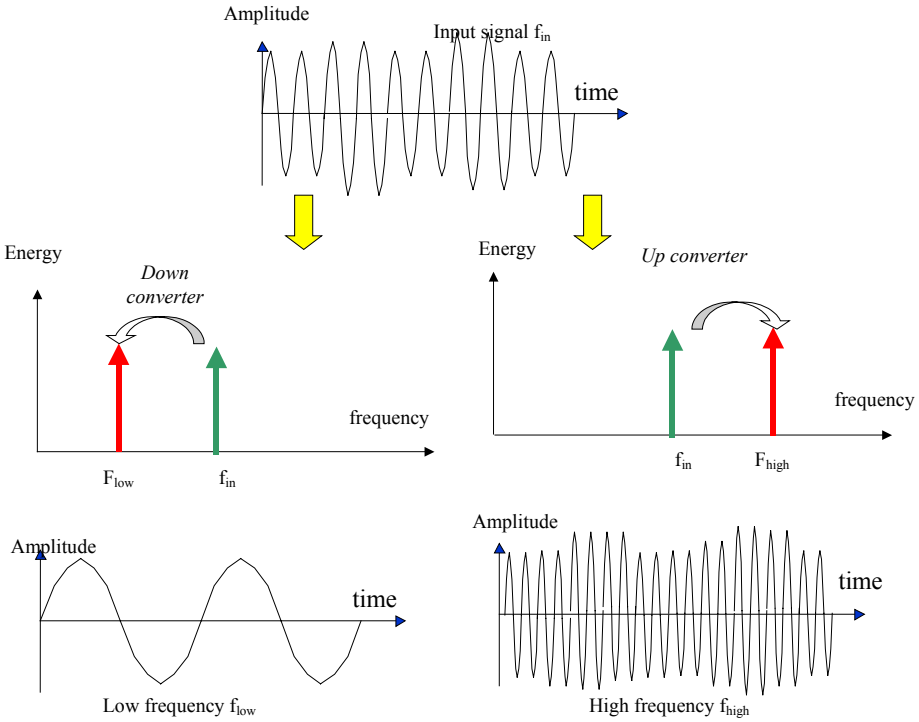


Figure 12-68: the principles for frequency conversion

Adding sinusoidal waves

Adding sinusoidal waves is very easy. A simple circuit containing 3 resistor produces the addition of two sinusoidal waves, as shown in figure 12-12. The formulation is easily demonstrated using the superposition theorem.

$$Vout = \frac{1}{3}\left[\cos\omega_1 t + \cos\omega_2 t\right] \quad \text{(Equ. 12-12)}$$

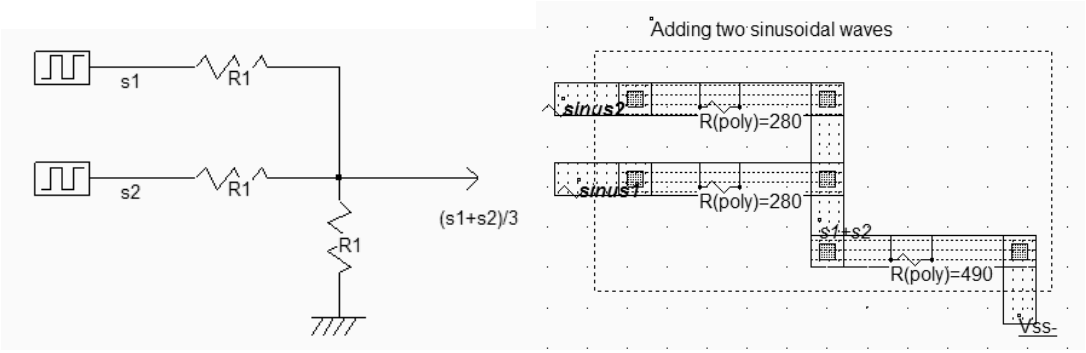


Figure 12-69: Adding sinusoidal waves is easy, a set of 3 resistors is sufficient to build the sum (AddSinus.MSK)

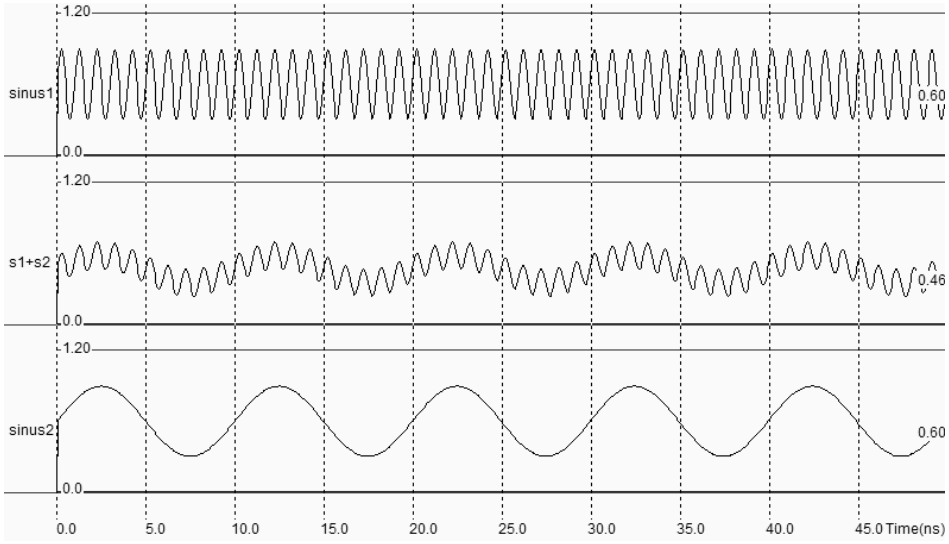


Figure 12-70: The simulation of the sinusoidal wave adder (AddSinus.MSK)

The Fourier transform of the signal *s1+s2* reveals two harmonics (Figure 12-71), one at the frequency of signal 1, the other at the frequency of signal 2, as the formulation 12-12 suggested. Clearly, no frequency shift may be obtained using sinusoidal addition.

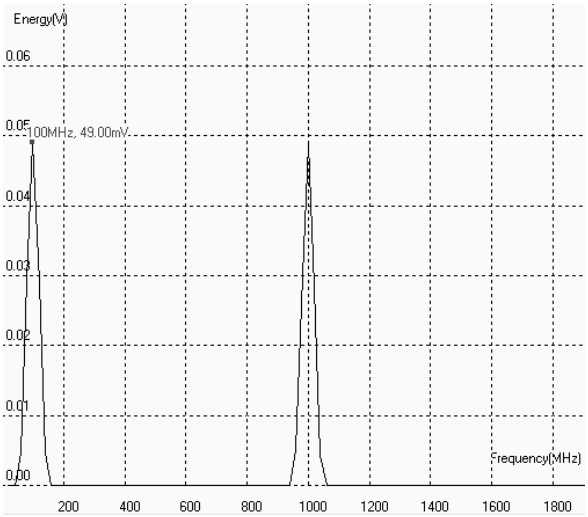


Figure 12-71: The Fourier transform of s1+s2 reveals two harmonics, one at 100MHz the other at 1GHz (AddSinus.MSK)

Multiplying sinusoidal waves

At the core of up/down frequency conversion is the multiplication of two sinusoidal waves in the time domain [Lee]. The result of that multiplication is the generation of two new frequencies: one at the sum of frequency, one for the difference.

$$\sin(\omega_1 t).\sin(\omega_2 t) = \frac{1}{2}\left[\sin(\omega_1 - \omega_2)t - \sin(\omega_1 + \omega_2)t\right] \qquad \text{(Equ. 12-13)}$$

where

ω1=2π.f1

ω2=2π.f2

f1 = frequency of signal 1 (Hz)

f2 = frequency of signal 2 (Hz)

If we consider a low frequency f_{in}, and a high frequency f_{Osc} and only consider absolute values, the multiplication of these two sinusoidal signals creates two new sinusoidal contributions: one at $f_{Osc} - f_{in}$, one at $f_{Osc} + f_{in}$ (Figure 12-72). Using an LC resonant circuit, we only keep the desired frequency contribution. In the case of figure 12-72, the L and C values are tuned to highlight the $f_{Osc} + f_{in}$ contribution which fits with the emission bandwidth. The LC resonator also serves as a filter of undesired harmonics, such as $f_{Osc} - f_{in}$ and f_{Osc}.

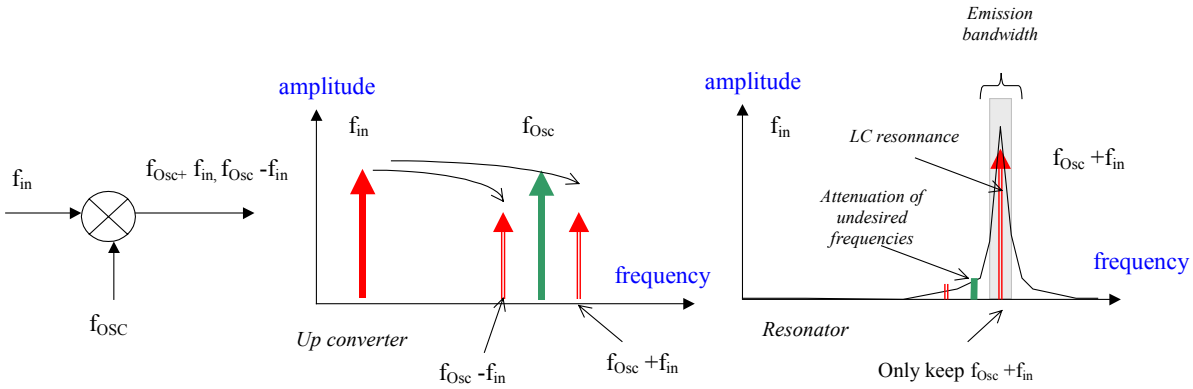


Figure 12-72: The multiplication of two frequencies creates new frequency components

Using a MOS for Sinus Multiplication

The process for multiplying signals with CMOS devices is far from being simple. The nMOS and pMOS are non-linear devices. The best example is the long channel nMOS which gives approximately a square law dependence between *Vgs-Vt* and *Ids*, as illustrated in figure 12-73. A linear device would give a linear dependence between *Ids* and *Vgs*, which is almost the case for short-channel devices. See chapter 3 for more details about device modeling.

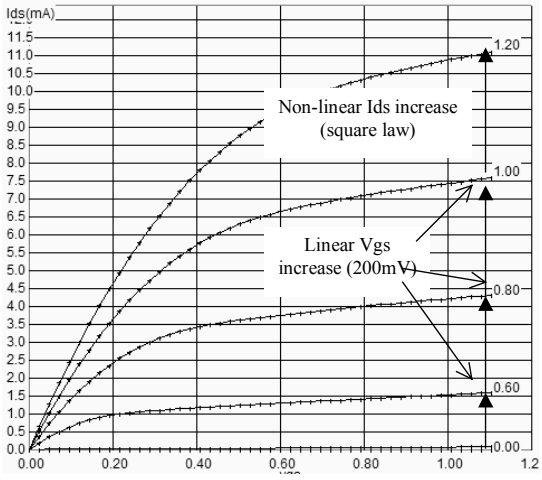


Figure 12-73: The long-channel MOS characteristics exhibit a square dependence of Ids vs. Vgs (MixerMos.MSK)

The idea is as follows (Figure 12-74): the two sinusoidal inputs f_{in} and f_{Osc} are added on the gate *Vgs*. The current *Ids* is a non linear function of *Vgs*. The static characteristics of the device (W=50µm, L=0.5µm) show a "quadratic" dependence: each *Vgs* step induces a square increase of *Ids*. This can be simply written as:

$$I_{DS} \approx k.(V_{GS} - Vt)^2 \quad \text{(Equ. 12-14)}$$

where

k depends on the design and technology

Vt is the threshold voltage (Around 0.35V)

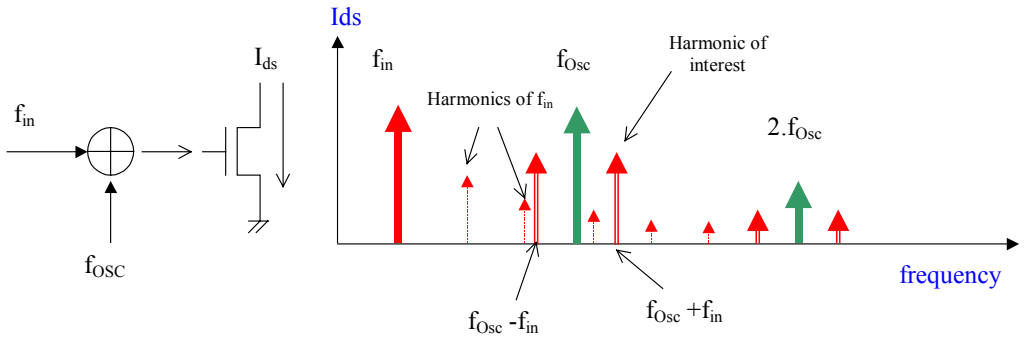


Figure 12-74: The Ids current exhibits several harmonics, including the desired high frequency fOsc+fin (MixerMos.MSK)

If Vgs is a sum of sinusoidal waveforms, as we did in the previous section, the current may be written as:

$$I_{DS} \approx k.\left[V_{bias} + v_{in}.\sin(\omega_{in}t) + v_{osc}\sin(\omega_{osc}t) - Vt\right]^2 \quad \text{(Equ. 12-15)}$$

$$I_{DS} \approx I_{DS0} + k_1.\left[v_{in}.v_{osc}(\sin\omega_{osc}t.\sin\omega_{in}t)\right] \quad \text{(Equ. 12-16)}$$

$$I_{DS} \approx I_{DS0} + \frac{k_1}{2}.\left[v_{in}.v_{osc}sin(\omega_{osc}+\omega_{in})t - sin(\omega_{osc}-\omega_{in})t\right] \quad \text{(Equ. 12-17)}$$

The most important result beyond this approximation is that the input signal and the oscillator signal are indeed multiplied and create the desired harmonics. In other words, passing a sum of sinusoidal waveforms into a non-linear device create several harmonics, from which f_{in}+f_{Osc} and f_{in}-f_{Osc} are the most important. The desired harmonic is underlined in equation 12-17 by rearranging the product of sinus into a sum of sinus. The term *Ids0* also contains the original input signal, the oscillator signal and all their respective harmonics too, whichs lead to a quite complex output. A band-pass filter is mandatory to eliminate undesired harmonics and amplify the desired signal. The circuit is called a single-balanced mixer.

Layout Implementation

The n-channel MOS implemented in the mixer layout must have a large length to eliminate short channel effects and exhibit a square law dependence between *Vgs* and *Ids*. This is the case of MOS devices with a length larger than 0.5µm. A resistance load is mandatory to perform amplification. The resistor is matched to the *Ron* resistance of the nMOS device. The input is the sum of two sinusoidal components, through a resistor bridge (Figure 12-75).

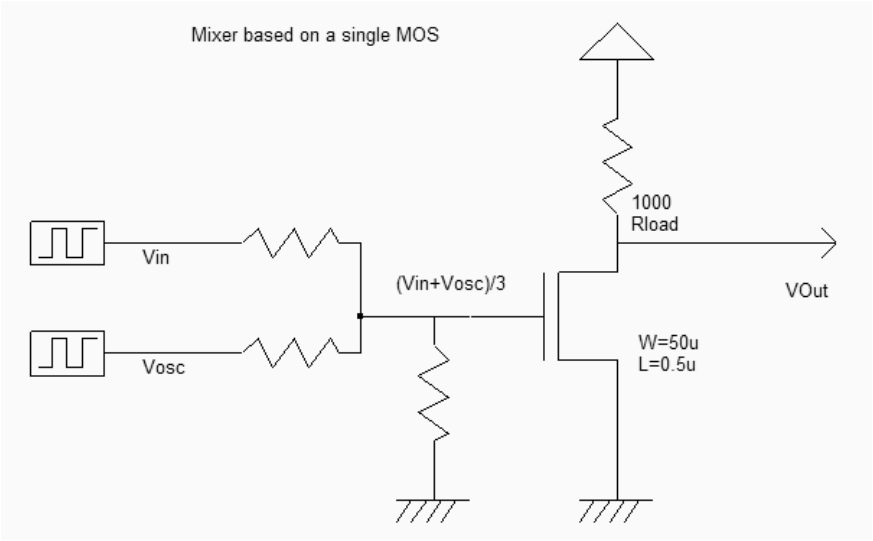


Figure 12-75: Building a single-balanced mixer with an n-channel MOS device (MixerMos.SCH)

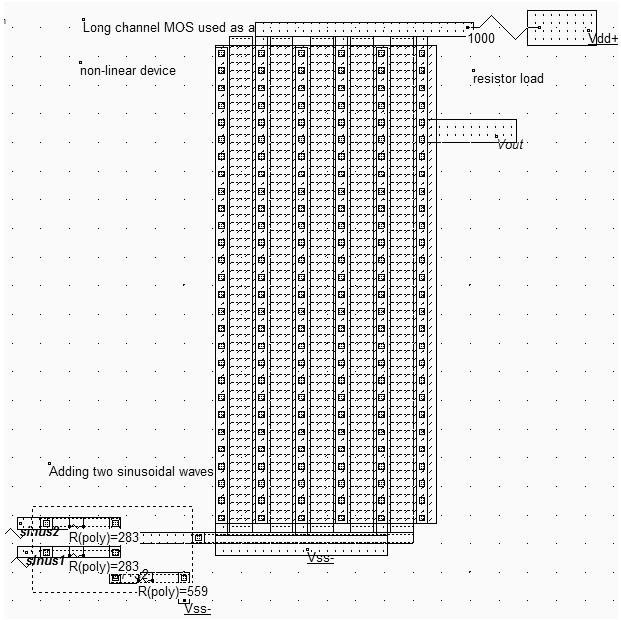


Figure 12-76: Design of a mixer using a large width, large length nMOS device, with a sum of sinusoidal waves at the input (MixerMos.MSK)

Notice the unusual aspect of the MOS device in the layout shown in figure 12-76. Five gates are connected in parallel, which is equivalent to one single MOS with the sum of channel widths, but at the same time, the length is enlarged to obtain a sufficient quadratic dependence between voltage and currents which is the main origin of harmonics . According to the theory, the time-domain simulation of the mixer reveals that the signal *Vout* has a very complex aspect (Figure 12-77).

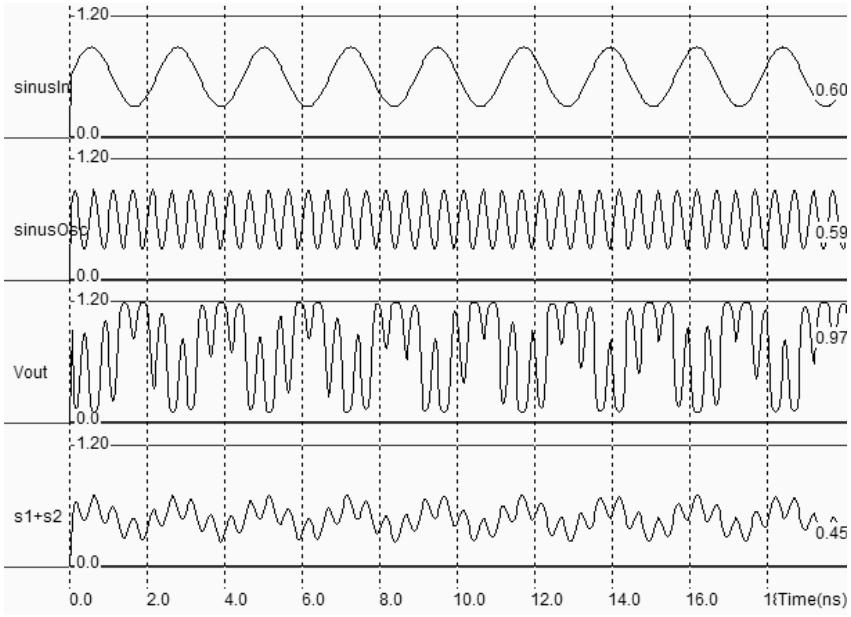


Figure 12-77: Simulation of the mixer with a 450Mhz and 2Ghz added inputs (MixerMos.MSK)

The Fourier Transform is obtained by a click on "FFT" in the simulation window (Figure 12-78). The 450MHz input signal, the 2GHz oscillator signal, as well as the harmonics and products are present in the spectrum. The only desired harmonic is the 2.45GHz contribution, corresponding to $f_{in}+f_{osc}$.

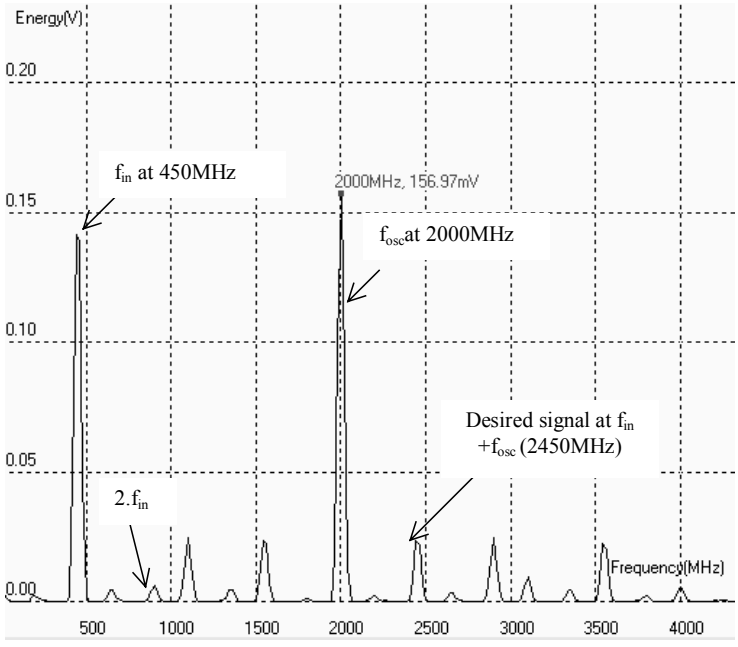


Figure 12-78: The output voltage includes fin, fosc and their corresponding harmonics. The desired signal is at fosc+fin (MixerMos.MSK)

Mixer with LC resonator

The mixer shown in figure 12-79 has two important features: the serial resistor is replaced by an inductor L_{HF} of 3nH, and a capacitor C_{HF}=1.2pF is added to the output. The LC resonator formed by the inductor L_{HF} and the capacitor C_{HF} matches the target frequency 2.45GHz (Use the resonant frequency evaluator in the **Analysis** menu to confirm). The serial resistor *RL* accounts for the finite quality of the inductor, and corresponds to the long metal wire resistance of the physical inductor. Removing this serial resistor would create overestimated oscillations, possibly numerical instability, and the results could not be exploited.

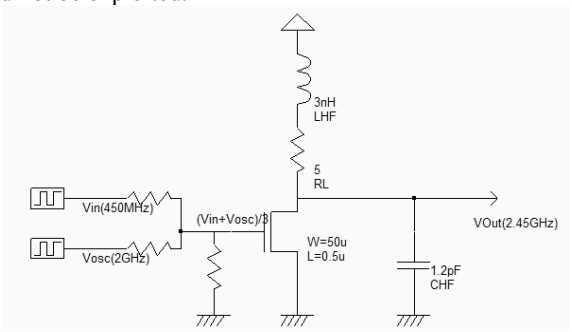


Figure 12-79: The schematic diagram of a mixer with a LC resonator tuned to 2.45GHz

The mixer implementation has not been completed in the layout of figure 12-80. For simplicity's sake we used virtual L and C rather than a physical inductor. The 3nH inductor is placed in series with a parasitic resistance which accounts for the physical serial resistance of the on-chip inductor, and limits the LC resonance effect. The capacitor 1.2pF is also virtual, and is placed near *Vout*.

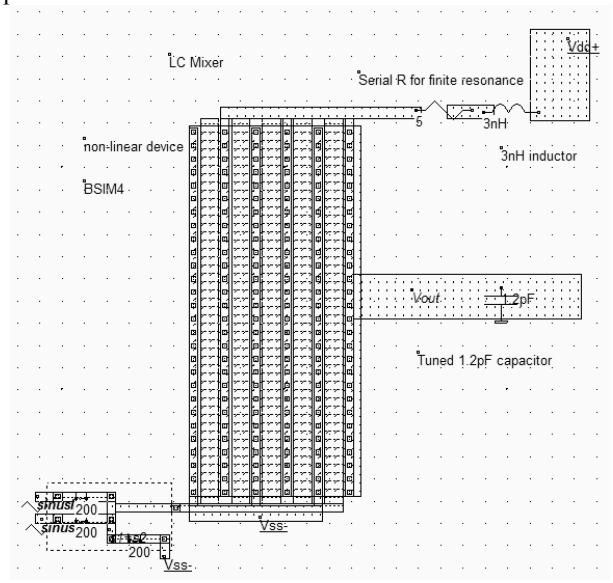


Figure 12-80: The mixer with a tuned LC resonator targeted to 2.45GHz (MixerLC.MSK)

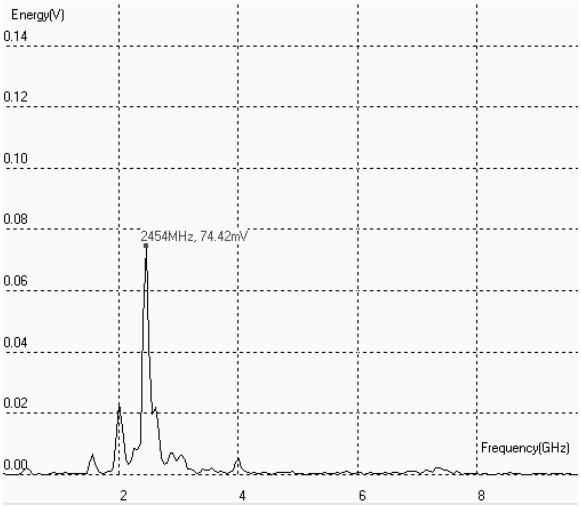


Figure 12-81: The Fourier transform of Vout shows a main contribution at the desired frequency and residues of other harmonics (MixerLC.MSK)

The Fourier transform of the time-domain simulation is proposed in figure 12-81, and corresponds to the output node *Vout*. The desired signal at 2.45GHz appears much more clearly than in figure 12-78, because of the pass-band passive resonator centered around that frequency. Unfortunately, the selectivity of the LC circuit is not high enough to erase the oscillator frequency at 2GHz. Residues of other harmonics also appear in the Fourier transform: 1.6GHz, 4GHz.

An increase of the input frequency *fin* is translated into a corresponding increase of the output frequency. For example, a slow increase in *fin* shifts the main peak to the right in a proportional way. Also, an increase of the amplitude of *fin* induces a corresponding increase of the 2.45GHz harmonic. This property is illustrated in figure 12-82 by adding a regular increase of the sinusoidal input (Parameter **Increase f**).

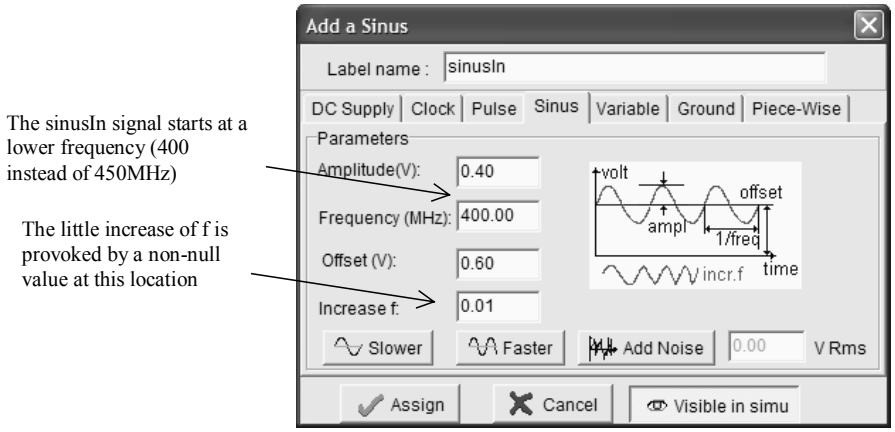


Figure 12-82: The input SinusIn starts from 400MHz and slowly rises to 500MHz (MixerLC.MSK)

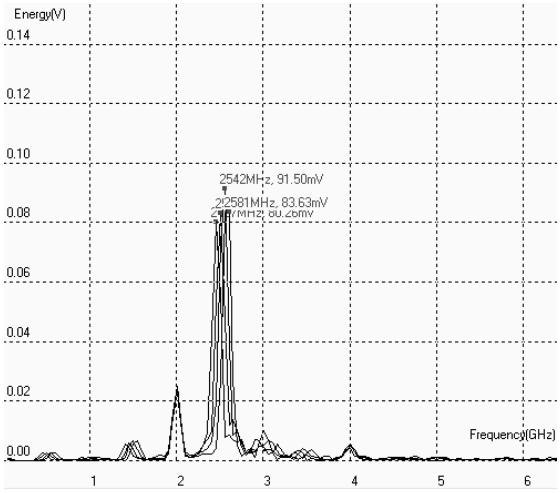


Figure 12-83: A little increase of the input frequency is translated into an increase of the main harmonic (MixerLC.MSK)

The evolution of the FFT of *Vout* shows a shift in the peak resonance, due to the fact that the input sinusoidal wave has also shifted toward high frequencies. This illustrates an important property of mixers that are conservative in terms of amplitude and frequency variations, except that the output frequency is situated at a fixed distance of the the input frequency.

Double-balanced Mixer

The main drawback of the mixer output provided by the LC mixer is the important amount of parasitic signals added to the desired signal. The undesired signals 2.55GHz (*fosc-fin*), 2GHz (*fosc*), 2.9GHz (*fosc+2.fin*), 4GHz (*2.fosc*), appear in the spectrum and should be eliminated. A very brilliant idea would consist in creating two signals where all harmonics would be in opposite phase except the desired harmonics which would be in phase. Adding these two signals would create a miraculous signal with *fosc+fin* and *fosc-fin*.

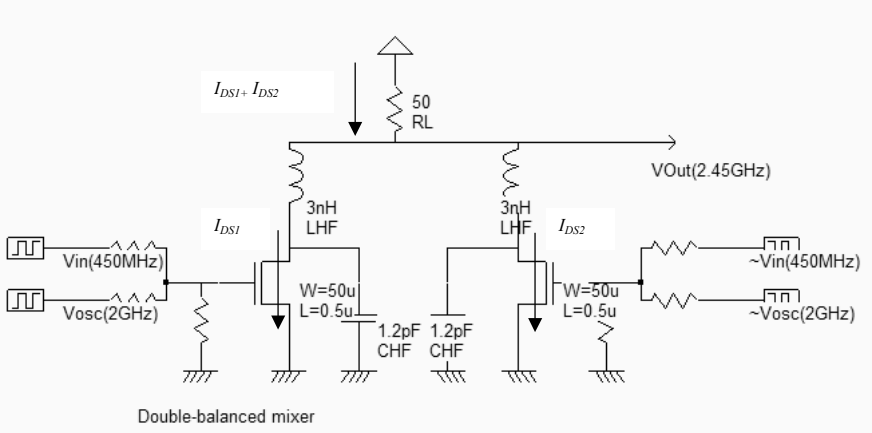


Figure 12-84: Implementation of the double-balanced mixer (MixerDoubleLC.SCH)

A circuit that realizes this function is proposed in figure 12-84. The signals *vin* and *Vosc* are combined as seen previously, in the left branch of the mixer, on the gate of the n-MOS device. The current that flows through the nMOS device situated on the left is *Ids1,* which can be approximated by equation 12-18. In the right branch of the mixer, the signals ~*vin* and ~*vosc*, representing the same signals as *vin* and *vosc* but with an opposite phase, are combined on the gate of the second n-MOS device. The current that flows on the right nMOS device is *Ids2* which can be approximated by equation 12-19.

$$I_{DS1} \approx k.\left[V_{bias} + v_{in}.sin(\omega_{in}t) + v_{osc}sin(\omega_{osc}t) - Vt\right]^2 \quad \text{(Equ. 12-18)}$$

$$I_{DS2} \approx k.\left[V_{bias} - v_{in}.sin(\omega_{in}t) - v_{osc}sin(\omega_{osc}t) - Vt\right]^2 \quad \text{(Equ. 12-19)}$$

Developing equations 12-18 and 12-19, the sum can be arranged as:

$$I_{DS1} + I_{DS2} \approx k[I_{DS0} + 2v_{in}.sin(\omega_{osc} + \omega_{in})t + 2v_{in}.sin(\omega_{osc} - \omega_{in})t] \quad \text{(Equ. 12-20)}$$

The remarkable point that can be seen in equation 12-20 is that the sum of currents I_{ds1}+I_{ds2} that flows in the 50ohm load resistor *RL* mainly includes a constant value I_{ds0} and the mixer products at frequencies f_{osc}+f_{in} and f_{osc}-f_{in}, which was exactly the goal of the mixer.

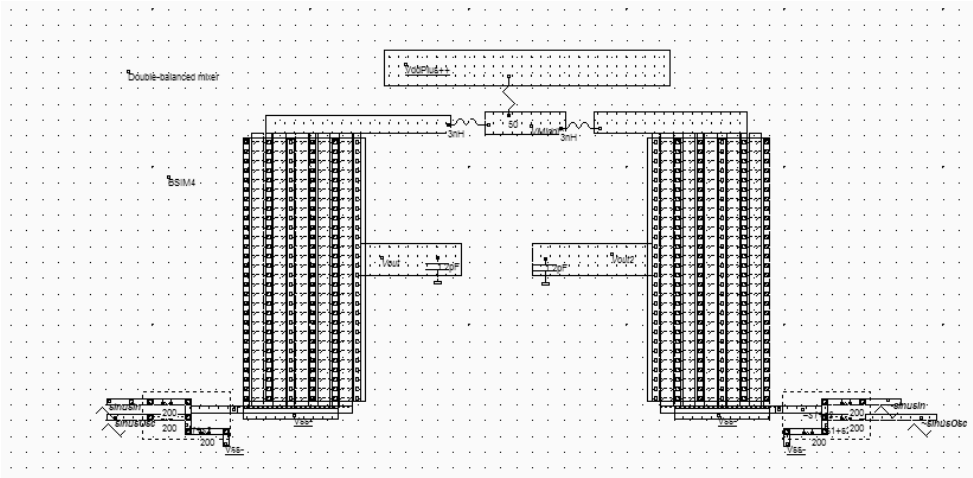


Figure 12-85: Layout of the double-balanced mixer (MixerDoubleLC.MSK)

The layout implementation (Figure 12-85) makes an extensive use of virtual R,L,C elements. This technique is recommended for the tuning of the circuit, but one should remember that the final goal is a complete layout implementation. The simulation performed in figure 12-86 confirms the theoretical assumption: the Fourier transform clearly includes the two main contributions near 1500MHz and 2500Mhz, without f_{osc} in between. Removing the undesired harmonics is quite easy, in order to keep the desired 2500MHz contribution.

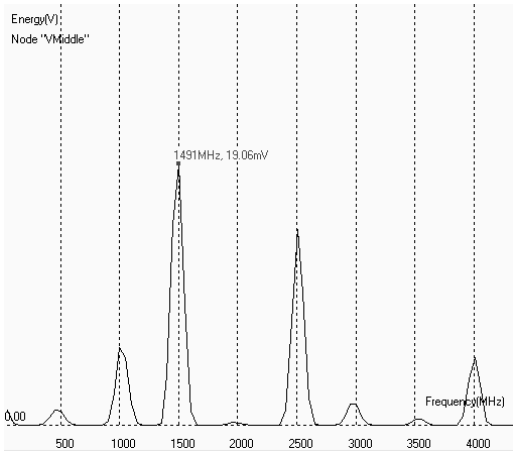


Figure 12-86: Fourier transform of the double-balanced mixer output (MixerDoubleLC.MSK)

Gilbert Mixer

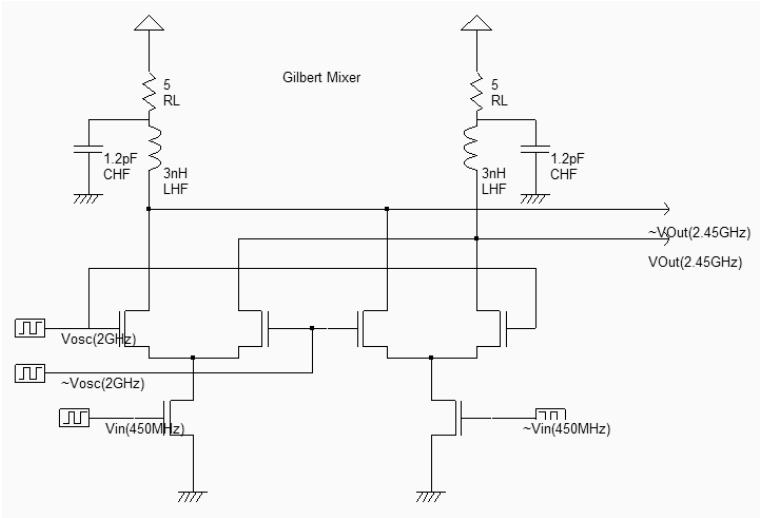


Figure 12-87: The Gilbert mixer (MixerGilbert.SCH)

The double-balanced mixer is not implemented using a resistor based voltage adder, as suggested in the schematic diagram shown previously (Figure 12-84). Most mixers use the Gilbert cell [Gilbert] which consists of only six transistors, and performs a high quality multiplication of the sinusoidal waves [Lee]. The schematic diagram shown in figure 12-87 uses the tuned inductor as loads, so that *Vout* and *~Vout* oscillate around the supply VDD.

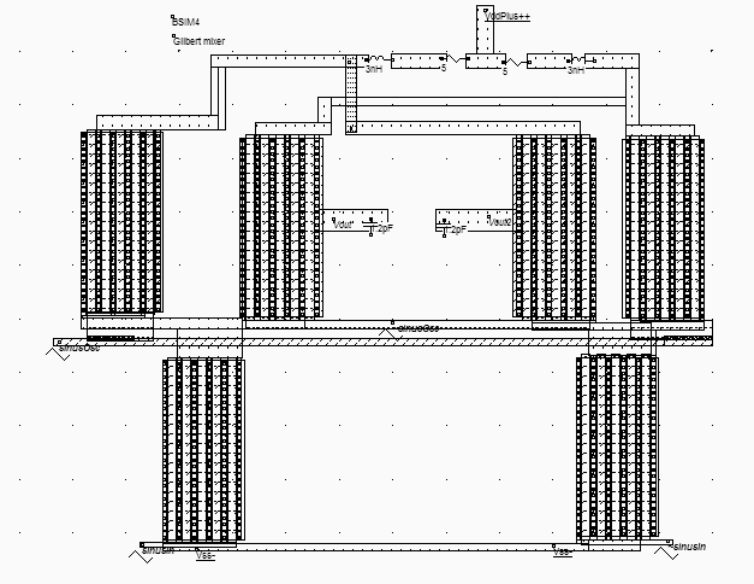


Figure 12-88: The Gilbert mixer implementation with virtual R,L and C (MixerGilbert.MSK)

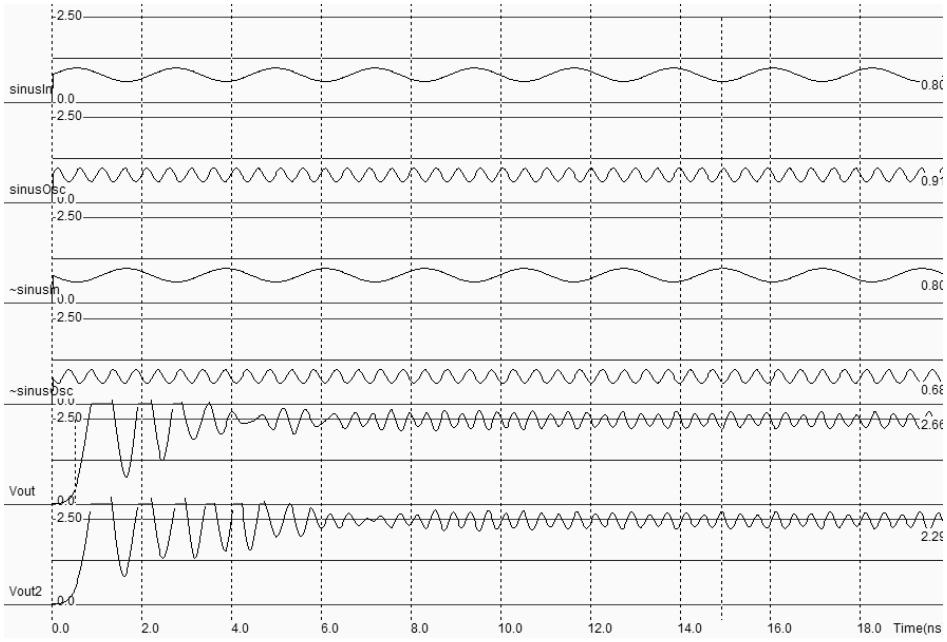


Figure 12-89: Time-domain simulation of the Gilbert mixer (MixerGilbert.MSK)

The implementation shown in figure 12-88 makes again an extensive use of virtual R,L and C elements. The 3nH inductor is in series with a parasitic 5 ohm resistance, on both branches. The time domain simulation reveals a transient period from 0.0 to 8ns during which the inductor and capacitor warm-up. This initialization period is not of key interest. The most interesting part starts from 8ns, when the output *Vout* and *Vout2* are stabilized and oscillate in opposite phase around 2.5V.

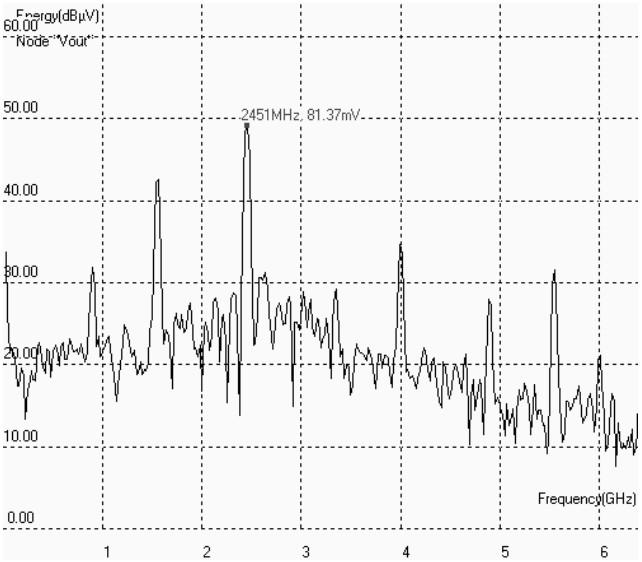


Figure 12-90: Fourier transform of the Gilbert mixer output (MixerGilbert.MSK)

The Fourier transforms of nodes *Vout* and *Vout2* are almost identical. We present the Fourier transform in logarithm scale to reveal the small harmonic contributions. As expected, the 2GHz f_{osc} signal and 450MHz f_{in} signals have disappeared, thanks to the cancellation of contributions. The two major contributors are $f_{osc}+f_{in}$ and $f_{osc}-f_{in}$.

Notice that the simulation time has an influence on the Fourier Transform result: a short simulation (5ns) would lead to a poor precision in our frequency range of interest, but a high precision on very high frequencies (Above 10GHz). In our case, it is preferable to perform the time domain simulation over a large time (50ns) which will give a high precision at low frequencies (From DC to 5GHz), but to limit the Fourier spectrum to around 10GHz. As the target frequency is around 2.5GHz, a 50ns simulation gives the best results.

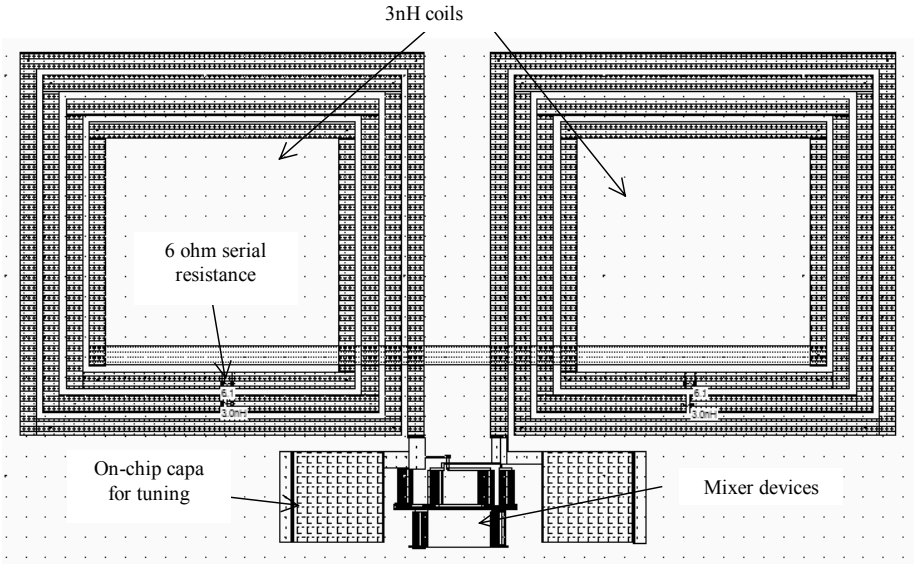


Figure 12-91: The complete implementation of a Gilbert mixer circuit (MixerGilbert2.MSK)

In figure 12-91, a complete implementation of the Gilbert mixer has been realized, so that virtual R,L and C components are replaced by physical elements. The coils have a target 3nH inductance, and their associated parasitic resistance is approaching 6 ohm when the combination of metal6,metal5 and metal4 are used. The tuning capacitor is added to the parasitic coil capacitor to perform the best resonance at the desired 2.5GHz frequency. The design relies on good models for the inductor and capacitor, which is not the case in the Microwind software which uses first order approximations of parasitic resistance, capacitance and coil inductance. In a real case implementation, we may expect significant differences between measurements and simulations. Having accurate predictions of such circuits is quite challenging.

7. Sub-sampling Frequency Converter

Let us recall that the frequency down conversion consists in shifting the input signal with a frequency *fin* down to a lower frequency f_{out}, without altering its amplitude or frequency modulation. One interesting solution consists in using a transmission gate with a very accurate tuning of the gate clock.

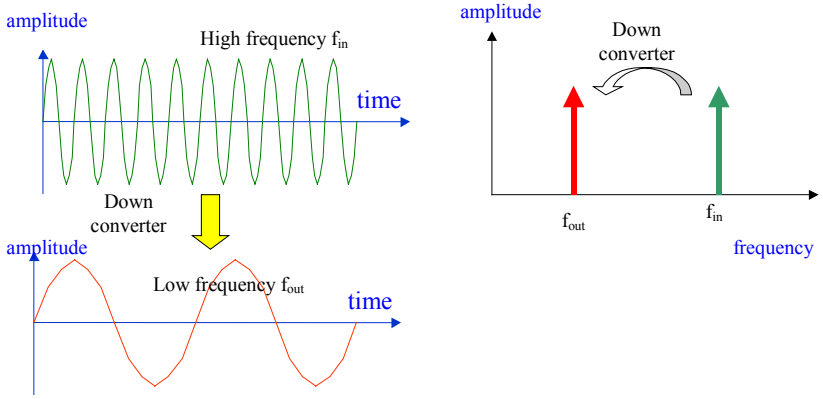


Fig. 12-92: Principles for down conversion

As an illustration, we use a 1.900 GHz sinusoidal wave (*DataIn*), and a 1.818 GHz sampling signal (*Enable*). The expected output frequency is therefore 1.900-1.818=0.082 GHz, that is 82MHz. The layout of the sample circuit is a simple transmission gate with an RC filter (Figure 12-93).

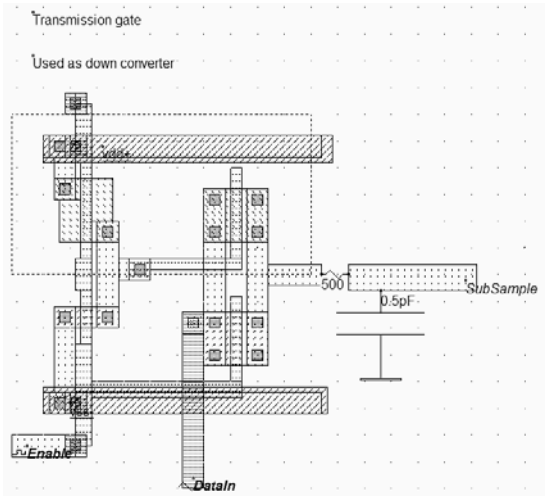


Fig. 12-93. Layout of the transmission gate and RC filter used for down conversion (DownConverter.MSK)

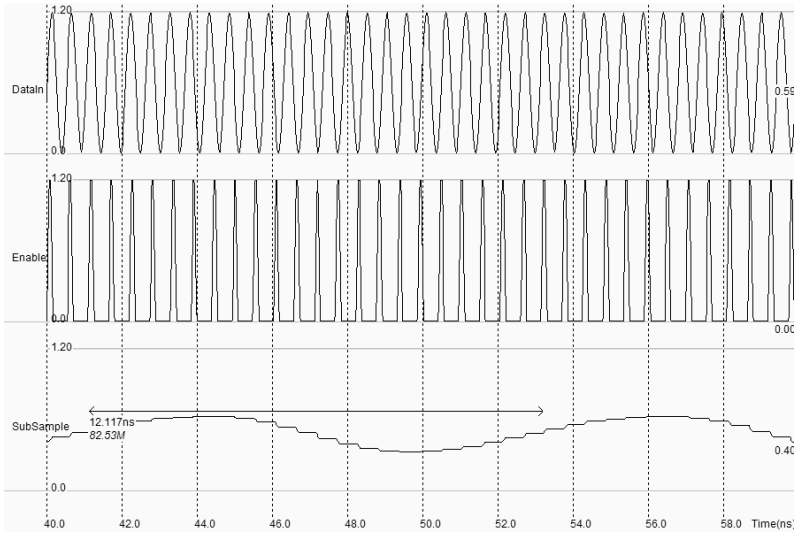


Fig. 12-94. Down conversion of the 1.9GHz input sinusoidal wave to a low frequency near 82MHz

The sampling signal *Enable* operates at a rate slightly slower than the input frequency, which leads to a signal at low frequency at the output of the transmission gate (Figure 12-94). With a simple RC filtering, the output signal becomes a sinusoidal wave with a frequency equal to the difference between f_{DataIn} and the gate frequency f_{Enable}. When simulating over a 20ns time interval (Figure 12-94), and asking for the evaluation of the frequency of the output *subSample*, we find 82MHz as expected.

8. Conclusion

In this chapter, we have described in the first part the role of on-chip inductor for resonant circuits. Then, we have detailed the power amplifiers and the associated notions of power efficiency and amplifier class. Thirdly, we have presented some circuits used to generate oscillations, based on ring oscillation and passive LC networks. Next, we

have described the main parts of the phase lock loop and illustrated three applications in the GHz range. The frequency conversion was presented through the addition of sinusoidal waveforms in non-linear devices. We also presented the Gilbert mixer and looked at the frequency conversion performances in frequency domain thanks to the Fourier Transform. Finally, the sub-sampling principles were applied to frequency down conversion through a simple example.

References

[Macnamara] Macnamara T. "Handbook of Antennas for EMC", Artech House Publishers, ISBN 0-89006-549-7

[Weste] Neil H. E. Weste, Kamran Eschraghian "Principles of CMOS VLSI Design", Addison-Wesley, 1993, ISBN 0-201-53376-6

[Niknejad] Niknejad Ali M., Meyer, robert G. "Design, simulation and applications of Inductors and Transfromers for Si RF Ics", Kluwer, 2000, Isbn 0-7923-7986-1

[Lee] T.H.Lee "The Design of Radio-frequency Integrated Circuits", Cambridge University Press, 1998, ISBN 0-521-63061-4

[Wheeler] H. A. Wheeler "Simple Inductance Formulas for Radio Coils", Proceedings of the IRE, Oct. 1928, pp 1398-1400

[Thompson] M. Thompson "Inductance Calculation Techniques – Part II: Approximations and Handbook Methods", Power Control & Intelligent Motion, Dec 1999

[Hella] Mona M. Hella, Mohammed Ismail "RF CMOS power Amplifiers, theory, Design and Implementation", Kluwer academic publishers, 2002, ISBN 0-7923-7628-5

[Bendhia] Sonia Bendhia "xxx" Delay cell reference

Exercises

Exercise 12-1

Design a 10mW power amplifier operating near 1.9GHz (UMTS frequency range). Add a second power MOS device to be able to tune the output power from 10mW to 30mW, using logic controls.

Exercise 12-2

Optimize the power amplifier for a maximum power efficiency delivered to a 30Ω load, as the radiating resistance is often closer to that value than the standard 50Ω.

Exercise 12-3

Design a LC oscillator targeted to 5.4GHz, corresponding to the frequency used in wirelesss area network protocols such as IEEE 802.11a.

Exercise 12-4

Redesign the high-performance VCO to oscillate around 5.4GHz, with a span of 0.5GHz (Corresponds to IEEE 802.11a).

Exercise 12-5

The main problem of the XOR phase detector is that the "ideal" position corresponds to a phase difference of $\pi/2$. In high performance PLL applications, an other type of phase detector is used, as shown below. Implement the phase detector and extract the effect of the phase difference between *clkDiv* and *clkIn* to the voltage *Vc*.

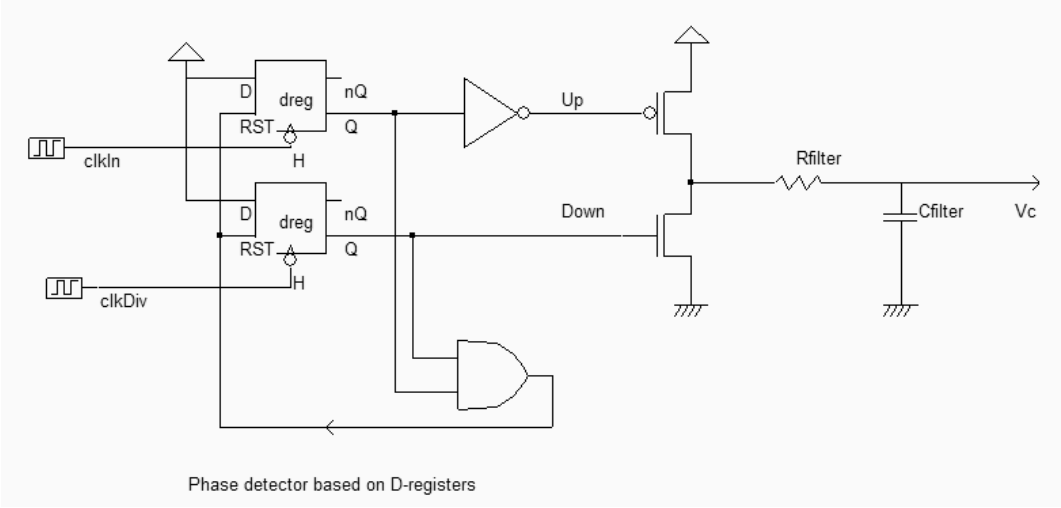


Figure 12-95. The D-Latch phase detector at work (PhaseDetectD.SCH)

Answer: See phaseDetectD.MSK