11 Analog Cells

This chapter deals with analog basic cells, from the simple resistor and capacitor to the operational amplifier.

1. Resistor

An area-efficient resistor available in CMOS process consists of a strip of polysilicon [Hasting]. The resistance between *s1* and *s2* is usually counted in a very convenient unit called "ohm per square", noted Ω/□. The default value polysilicon resistance per square is 10Ω, which is quite small, but rises to 200Ω if the salicide material is removed (Figure 11-1).

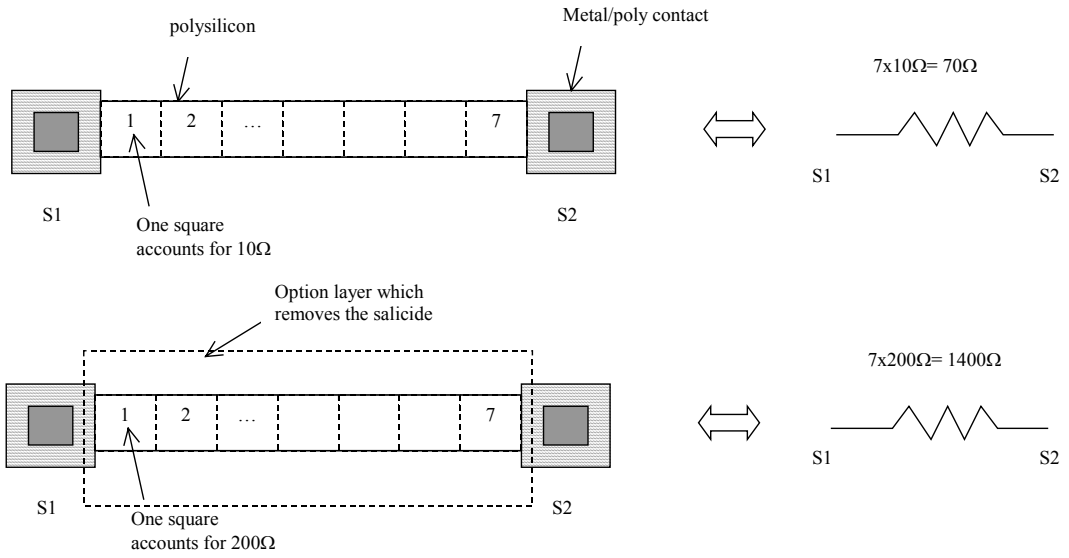


Figure 11-1 : The polysilicon resistance with unsalicide option

In the cross-section shown in figure 11-2, the salicide <Gloss> material deposited on the upper interface between polysilicon and the oxide creates a metal path for current that reduced the resistance dramatically. Notice the shallow trench isolation and surrounding oxide that isolate the resistor from the substrate and other conductors, enabling very high voltage biasing (up to 100V). However, the oxide is a poor thermal conductor which limits the power dissipation of the polysilicon resistor.

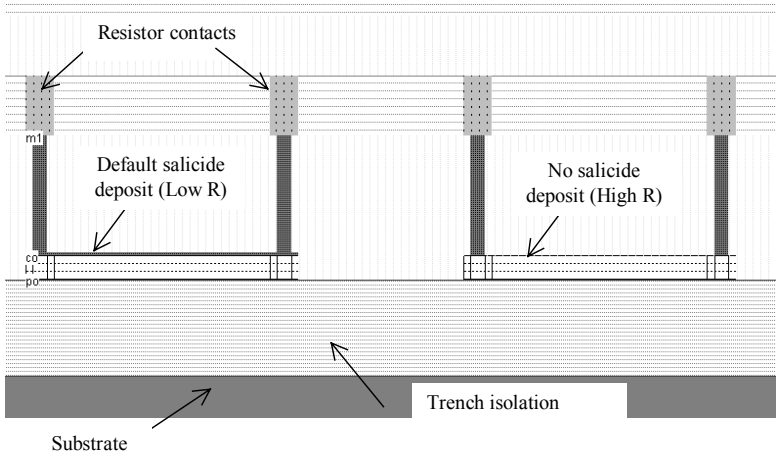


Figure 11-2 : Removing the salicide material to increase the sheet resistance (ResPoly.MSK)

The salicide is part of the default process, and is present at the surface of all polysilicon areas. However, it can be removed thanks to an option layer programmed by a double click in the option layer box, and a tick at "Remove Salicide". In the example shown in figure 11-3, the default resistance is 76Ω, and the unsalicide resistance rises to 760Ω.

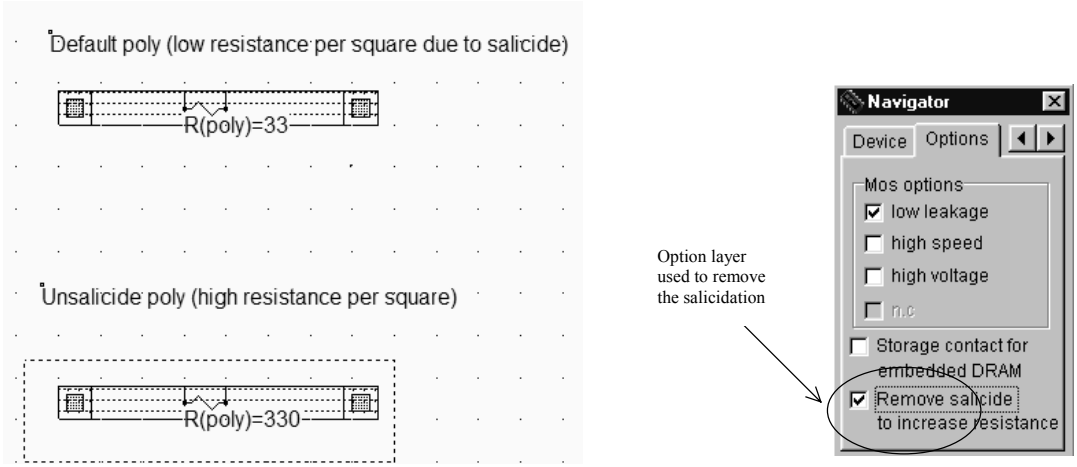


Figure 11-3 : Removing the salicide material thanks to an option layer

Other resistors consist of N+ or P+ diffusions. An interesting feature of diffusion resistor is the ability to combine a significant resistance value and a diode effect. As illustrated in figure 11-4, when V1 goes below 0V, the P-substrate/N+ diode is turned on and a path is created to the ground. Remember that the P-substrate is usually considered as a common ground reference. The diffusion resistor is used in input/output protection devices which are described in chapter 13.

The command **Help → Design Rules** gives access to the square resistance and unsalicide square resistance of all materials, as reported in figure 11-4.

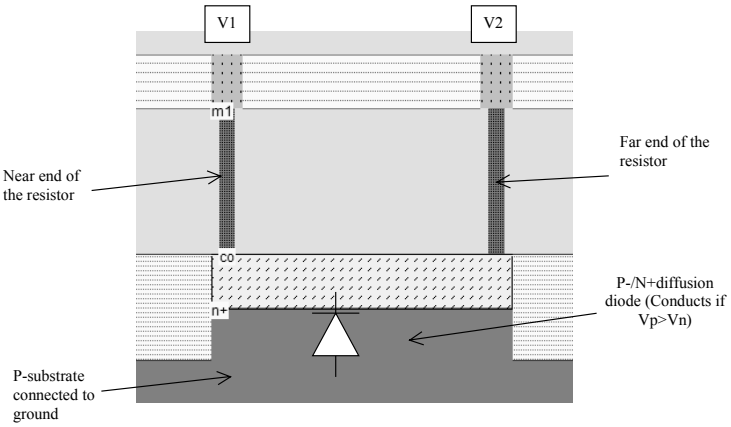
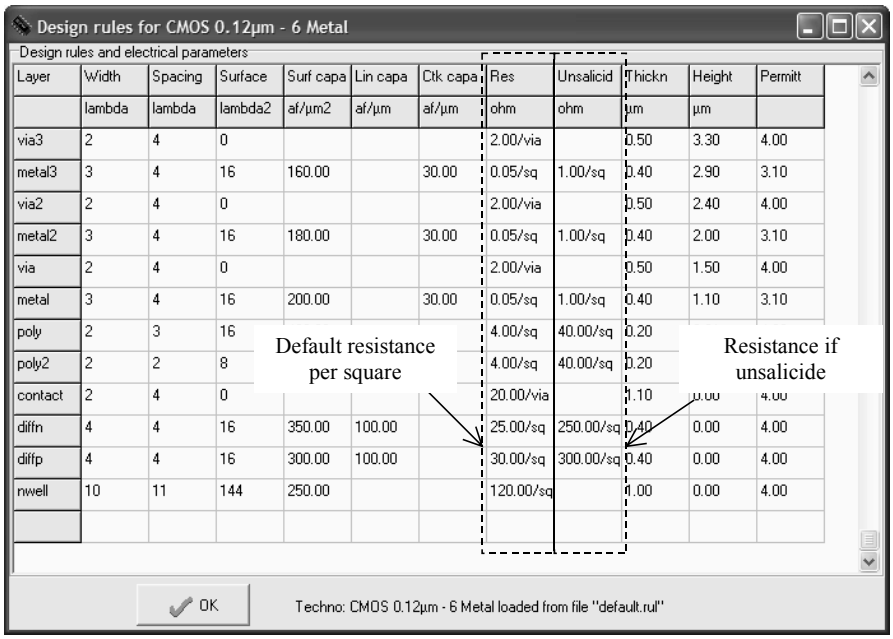


Figure 11-4 : The diffusion resistor combines a resistance effect and a diode (ResDiff.MSK)



Layer	Width	Spacing	Surface	Surf capa	Lin capa	Ctk capa	Res	Unsalicid	Thickn	Height	Permitt
	lambda	lambda	lambda2	af/µm2	af/µm	af/µm	ohm	ohm	µm	µm	
via3	2	4	0				2.00/via		0.50	3.30	4.00
metal3	3	4	16	160.00		30.00	0.05/sq	1.00/sq	0.40	2.90	3.10
via2	2	4	0				2.00/via		0.50	2.40	4.00
metal2	3	4	16	180.00		30.00	0.05/sq	1.00/sq	0.40	2.00	3.10
via	2	4	0				2.00/via		0.50	1.50	4.00
metal	3	4	16	200.00		30.00	0.05/sq	1.00/sq	0.40	1.10	3.10
poly	2	3	16				4.00/sq	40.00/sq	0.20		
poly2	2	2	8				4.00/sq	40.00/sq	0.20		
contact	2	4	0				20.00/via		1.10	0.00	4.00
diffn	4	4	16	350.00	100.00		25.00/sq	250.00/sq	0.40	0.00	4.00
diffp	4	4	16	300.00	100.00		30.00/sq	300.00/sq	0.40	0.00	4.00
nwell	10	11	144	250.00			120.00/sq		1.00	0.00	4.00

Figure 11-5 : Resistance parameters in CMOS 0.12µm

Process Variations

The process variations have a strong impact on the physical value of the resistor. Most processes specify square resistance within +/-25% [Hastings]. This means that the value of the resistor is linked to a statistical distribution, usually between a min-max range, and not an exact value. In reality, the spread of resistance is usually less than 10% within a single integrated circuit. However, two different integrated circuits may produce a significantly different resistance distribution. In figure 11-6, the average resistance *R1* measured on a test chip n°1 is 5% higher than the target resistance R_{typ}, and the average resistance *R2* on a test chip n°2 is 10% lower than the typical value R_{typ}. In his process specifications, the integrated circuit manufacturer only warranties that the measured resistance will not be larger than +/-25% the typical value R_{typ}.

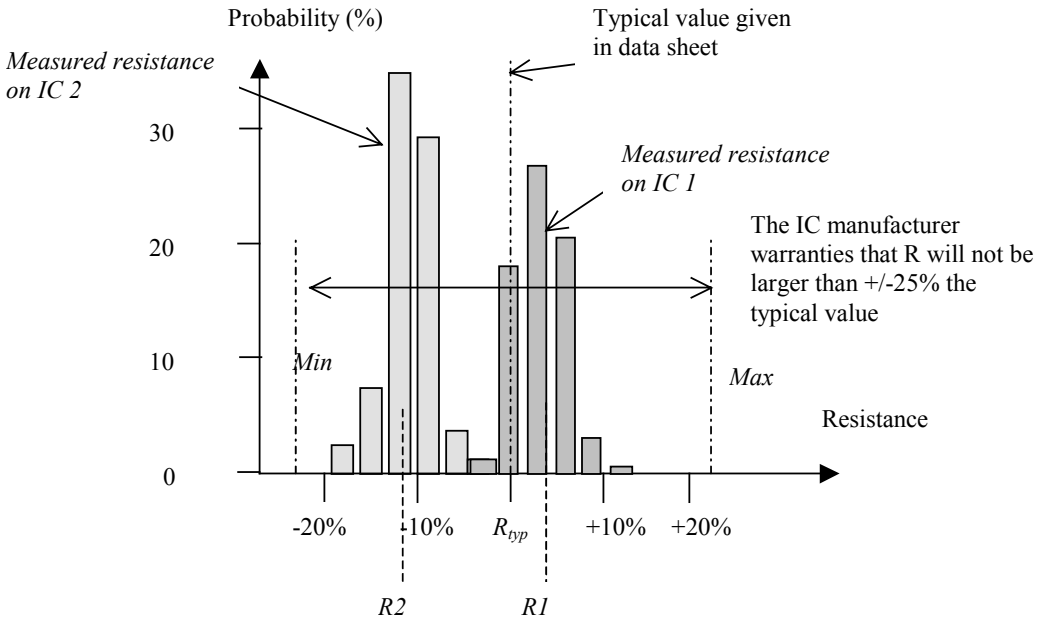


Figure 11-6: The spread in resistance value and the typ/min/max specifications

The resistor value varies because of lithography and process variations. In the case of the poly resistance, the width, height and doping may vary (Figure 11-7 left). Polysilicon resistors are rarely designed with the minimum 2 lambda width, but rather 4 or 6 lambda, so that the impact of the width variations is smaller. But the equivalent resistance is smaller, meaning less silicon efficiency. As illustrated in figure 11-7, a variation ΔW of 0.2λ on both edges results in a 20% variation of the resistance on a 2λ width resistor, but only a 10% variation for a larger resistor designed with a width of 4λ.

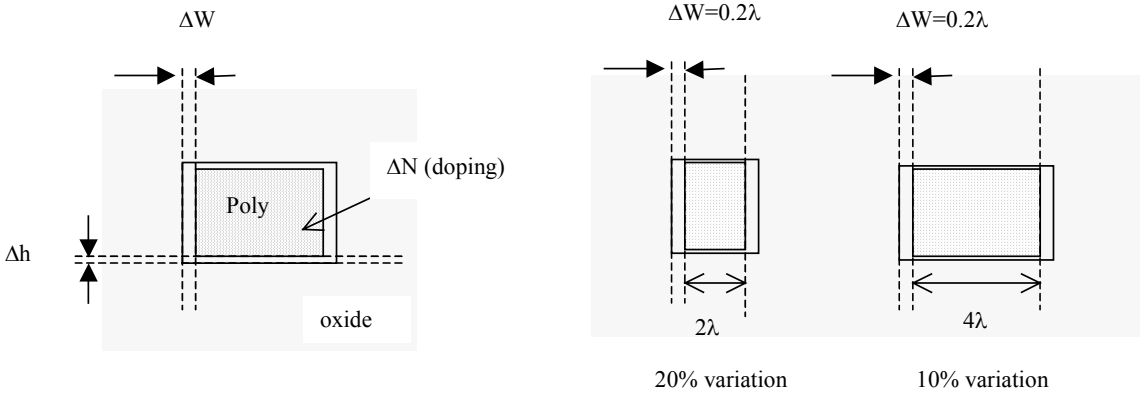


Figure 11-7 : Resistance variations with the process

Resistor design

There exist efficient techniques to reduce the resistance variation within the same chip. In figure 11-8, the resistor design on the left upper part is not regular, uses various polysilicon widths, and sometimes uses too narrow conductors.

Although the design rules are not violated, the process variations will enlarge the spread of resistance values. To minimize the effects of process variations, resistors should:

- Always be laid out with an identical width
- Use at least twice the minimum design rules
- Use the same orientation
- Use dummy resistance. Theses boxes of poly have no active role. Their role is to have a regular width variation on the active part.

Dog-bone resistors (Figure 11-8) may not pack as densely as serpentine resistors as two metal layers are used and induce supplementary design rules [Baker][Hastings] but are said to be less sensitive to process variations.

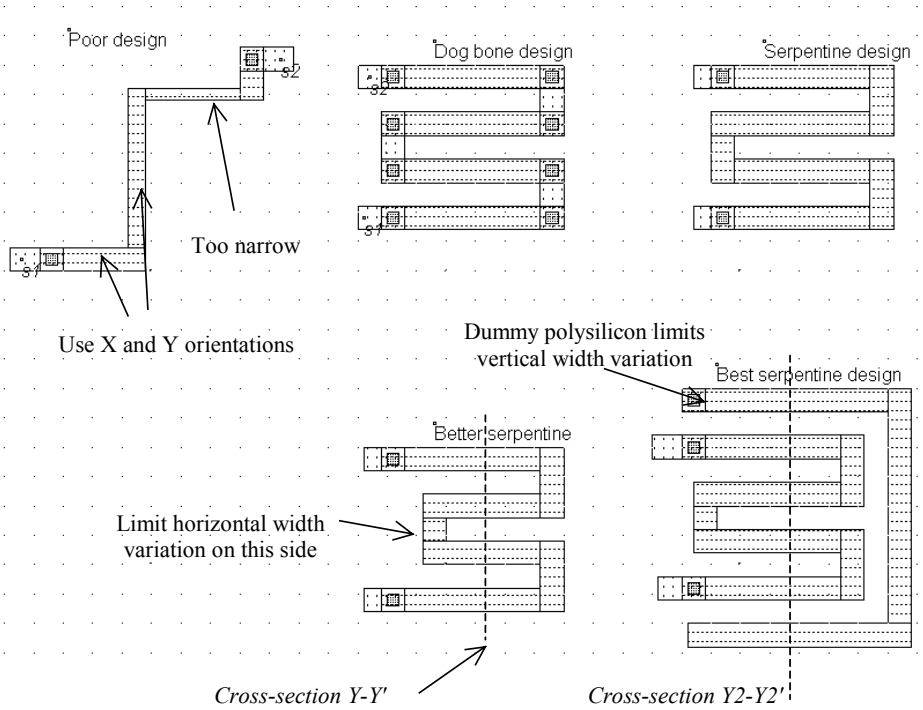


Figure 11-8 : Resistance design (ResPoly.MSK)

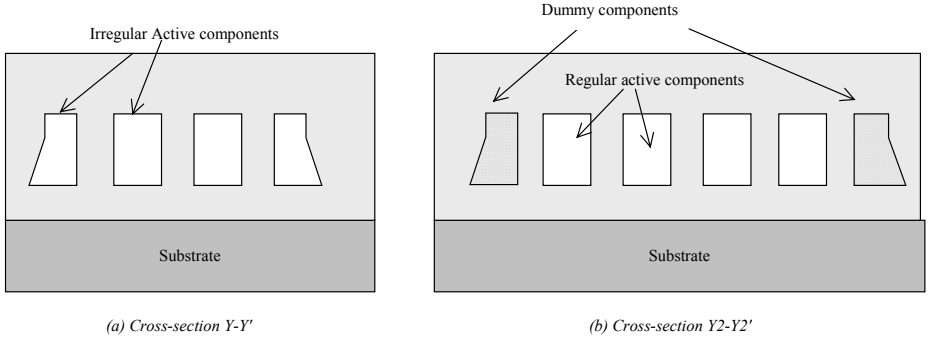


Figure 11-9: 2D aspect of the circuit without and with dummy components

The use of dummy devices is an efficient technique to avoid irregularities in resistor elements. In the case of a polysilicon serpentine without dummy devices, the cross-section Y-Y' in figure 11-9 exhibits important irregularities between bones. This results in an important process dependence and resistance variation. Now, if dummy components are inserted at the bottom and top of the design (Cross-section Y2-Y2'), the irregularities impact the dummy bones, but not the active parts of the resistor, which is much less impacted by the process variations. Typically, the resistance variation between two identical designs within the same chip is around 5% without dummy devices, and less than 1% with dummy devices.

2. Capacitor

Capacitors are used in analog design to build filters, compensation, decoupling, etc.. Ideally, the value of the capacitor should not depend on the bias conditions, so that the filtering effect would be situated at constant frequencies. We describe in this paragraph the diode capacitor, the MOS capacitor, the poly-poly2 and inter-metal capacitor. Some of these capacitors exist between an active node and a fixed voltage.

Diode Capacitor

Diodes in reverse mode exhibit a capacitor behavior. However, the capacitance value is strongly dependent on the bias conditions [Hastings]. A simple N+ diffusion on a P-substrate is a NP diode, which may be considered as a capacitor as long as the N+ region is polarized at a voltage higher than the P-substrate voltage which is usually the case as the substrate is grounded (0V). In 0.12µm, the capacitance is around 300aF/µm2 (1 atto-Farad is equal to 10^{-18} Farad).

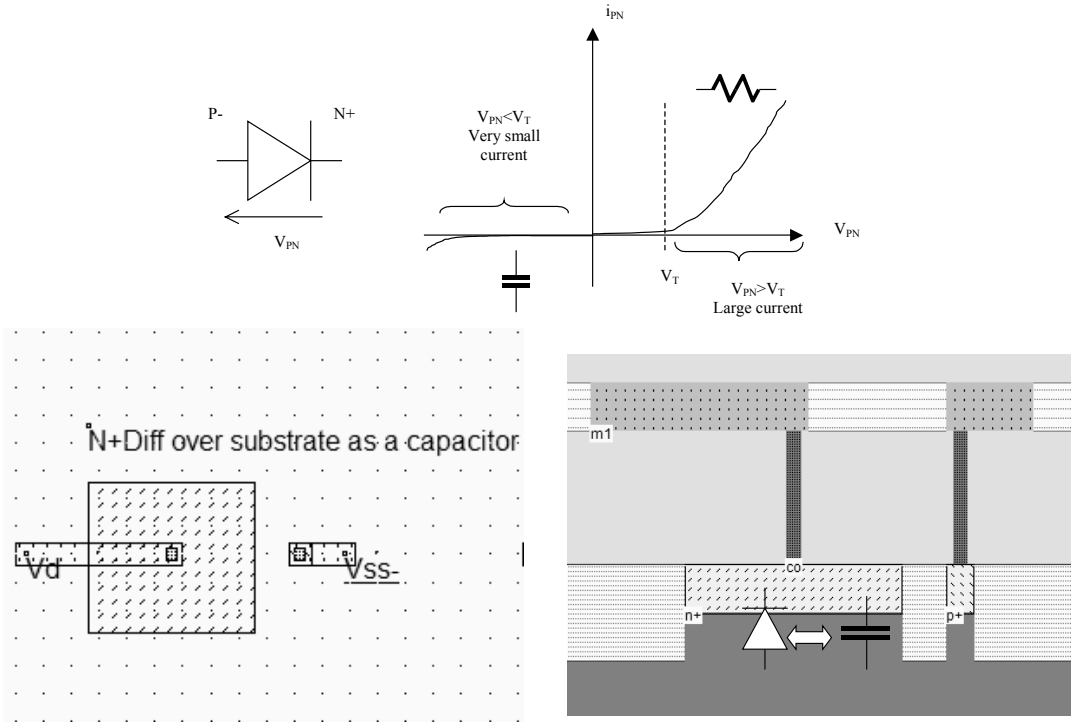


Figure 11-10: The diffusion over substrate as a non-linear capacitor (Capa.MSK)

Let us recall briefly the diode operation. A strong current flows from the P to the N region when the voltage difference is significantly higher that the threshold voltage V_T. For example, the P-/N+ diode is in such conditions when V_P is significantly higher that $V_N + V_T$, where V_T is approximately 0.3V in 0.12µm. The current is limited by the serial resistance of the diode, which is the order of 100 ohm to 1000ohm, depending on the surface of the diode (Figure 11-10). A very small current flows between the P and the N region as long as $V_P < V_N + V_T$. In such conditions, the diode may be considered as a capacitance. The order of the parasitic current is between the nano-ampere and the pico-ampere (10^{-9} to 10^{-12} A). As the substrate is grounded, V_N is always higher than V_P meaning that the N+/P- combination is equivalent to a capacitor.

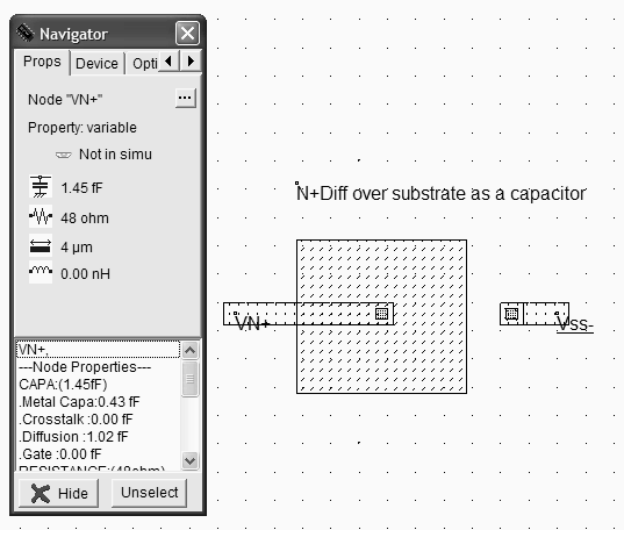


Figure 11-11: Extraction of the diffusion capacitance (Capa.MSK)

The capacitance may be extracted by a double click in the N+ diffusion area, or by the icon **View Electrical Node**. The N+diffusion has an equivalent parasitic capacitance of around 1fF, as extracted in figure 11-11. Notice that the value of this capacitance is an average value, computed for V_N equal to VDD/2. This capacitor suffers two main drawbacks: first, the capacitance is small as compared to the silicon area. Secondly, the capacitance depends significantly on the value of V_N, with a non-linear law.

The typical variation of the capacitance with the diffusion voltage V_N is given in figure 11-12. The capacitance per µm2 provided in the electrical rules is a rude approximation of the capacitance variation. A large voltage difference between V_N and the substrate result in a thick zone with empty charges, which corresponds to a thick insulator, and consequently to a small capacitance. When V_N is lowered, the zone with empty charges is reduced, and the capacitance increases. If V_N goes lower than the substrate voltage, the diode starts to conduct.

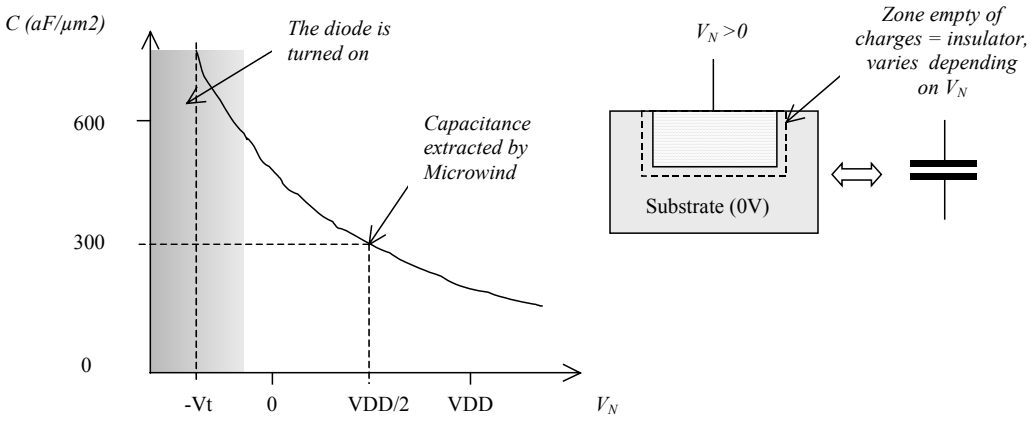


Figure 11-12: The diffusion capacitance varies with the polarization voltage

Mos Capacitor

The MOS transistor is often the simplest choice to build a capacitor. In 0.12µm, the gate oxide has an equivalent thickness of 2nm (20 angstrom, also written 20Å), which leads to a capacitance evaluated by formulation 11-1. There is also a thicker oxide used for high voltage MOS devices, called dual-oxide (5nm or 50Å in CMOS 0.12µm), for which equation 11-2 is applicable. The parameter in the design rules used to configure the gate oxide capacitor is `CPOOxide`.

$$C_{thinox} = \frac{\varepsilon_0 \varepsilon_r}{e} = \frac{8{,}85e^{-12} x3.9}{2.0x10^{-9}} = 17e^{-3} F/m^2 = 17e^{-15} F/\mu m^2 = 17fF/\mu m^2 \qquad \text{(Eq. 11-1)}$$

where

e= gate oxide thickness (m)

ε_0=vacuum permittivity (F/m)

ε_r=relative permittivity (no unit)

$$C_{dualox} = \frac{\varepsilon_0 \varepsilon_r}{e2} = \frac{8{,}85e^{-12} x3.9}{5.0x10^{-9}} = 6{,}8\, fF/\mu m^2 \qquad \text{(Eq. 11-2)}$$

where

e_2= dual-oxide thickness (m)

The design of a gate capacitor using a large MOS device is shown in figure 11-13, with a capacitance of around 300fF. In analog design, the gate capacitor is often surrounded by a guard ring. It is usually very difficult to integrate capacitors of more than a few hundred pico-farads. If nano-farad capacitors are required, these components are too large to be integrated on-chip, and must be placed off-chip.

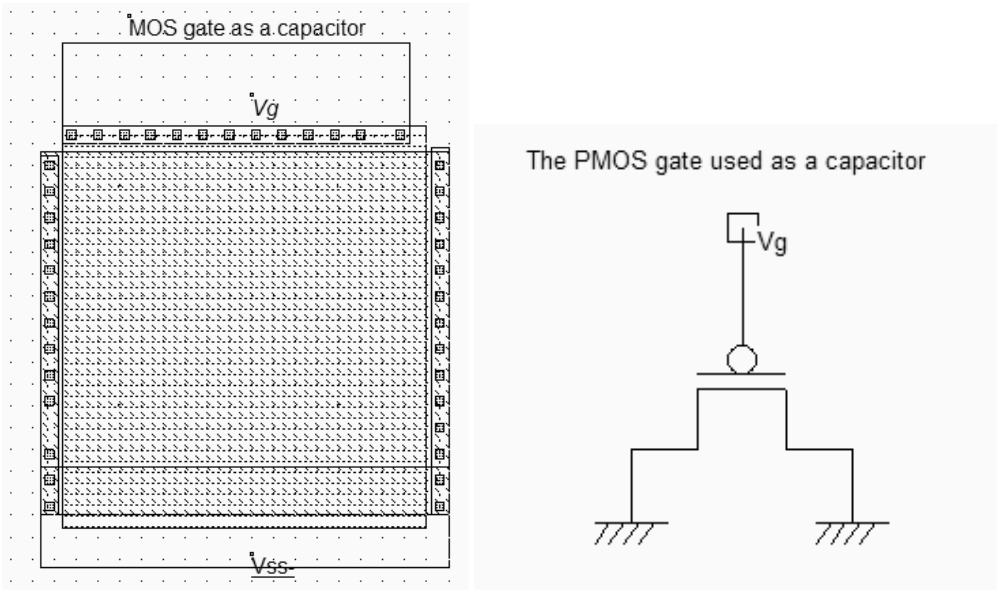


Figure 11-13: Generating an efficient capacitor based on a MOS device with a very large length and width (CapaPoly.MSK)

Using the ultra-thin gate increases the capacitance, however the risk of oxide damage due to overstress is significantly increased. The dielectric strength of the SiO2 oxide is the critical field above which the electric field damages the dielectric material. The dielectric strength E_{crit} ranges from 4 to 10MV/cm, depending on the fabrication technique [Hasting]. The critical voltage V_{crit} above which the oxide is damaged is approximated by equation 11-3. Be careful with the unusual units: the oxide thickness is directly expressed in nanometers and the dielectric strength in MV/cm.

$$V_{crit} = 0,1.e.E_{crit} \qquad \text{(Eq. 11-3)}$$

where

e= equivalent thickness (nm)

E_{crit}= dielectric strength (MV/cm)

A SiO_2 gate dielectric of 2nm leads to a critical voltage ranging between 0.8V (Dry oxide growth) and 2V (High quality gate oxide deposit). Long term reliability requires the supply voltage to keep below half of this critical voltage. This is why VDD is around 1V, and a voltage stress significantly above VDD may lead to the gate oxide destruction. The gate oxide used in high voltage MOS devices is fitted with the user requirements: to handle 3.3V, a reliable value for the gate oxide is 7nm. To handle 5V, the minimum gate oxide rises to 10nm.

Poly-Poly2 Capacitor

Most deep-submicron CMOS processes incorporate a second polysilicon layer (poly2) to build floating gate devices for EEPROM. An oxide thickness around 20nm is placed between the poly and poly2 materials, which induces a plate capacitor around 1,7fF/µm^2 (equation 11-3).

In Microwind, the command **Edit → Generate → Capacitor** gives access to a specific menu for generating capacitor (Figure 11-14). The parameter in the design rules used to configure the poly-poly2 capacitor is `CP2PO`.

$$C_{PolyPoly2} = \frac{\varepsilon_0 \varepsilon_r}{e_{pp}} = \frac{8{,}85e^{-12} x3.9}{20x10^{-9}} = 1700aF/\mu m^2 \qquad \text{(Eq. 11-1)}$$

where

e_{pp}= distance between poly1 and poly2 (m)

ε_0=vacuum permittivity (F/m)

ε_r=relative permittivity (no unit)

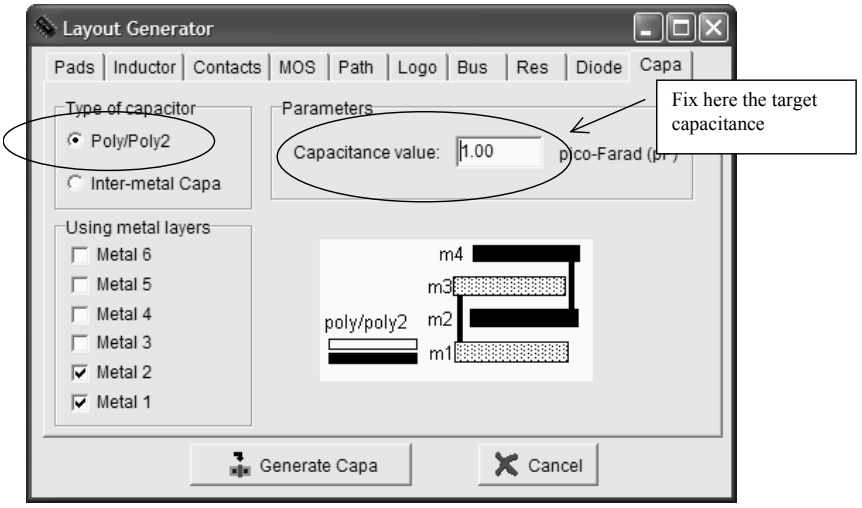


Figure 11-14: The generator menu handles the design of poly/poly2 capacitor and inter-metal capacitors

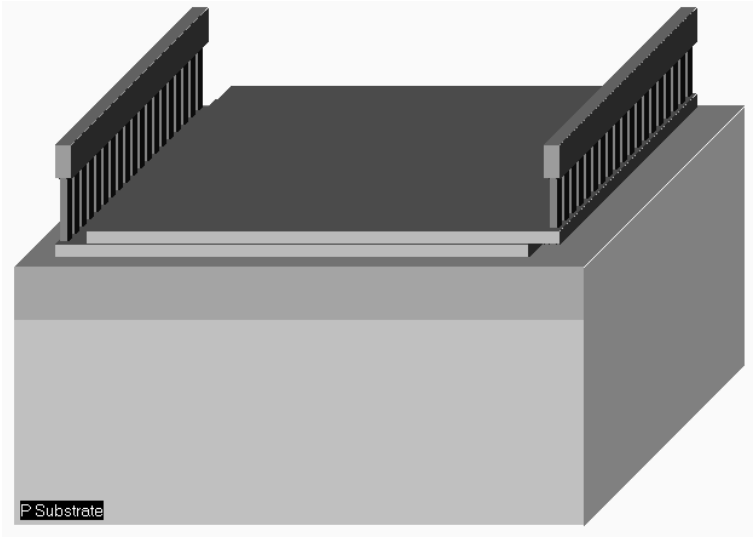


Figure 11-14: The 3D aspect of the poly-poly2 capacitor (CapaPolyPoly2.MSK)

The poly/poly2 capacitor simply consists of a sheet of polysilicon and a sheet of poly2, separated by a specific dielectric oxide which is 20nm in the case of the default CMOS 0.12µm process. The contacts are placed on both sides of the capacitor, between poly and metal on the left, between poly2 and metal on the right (Figure 11-14). The gate oxide is not used here because of its low breakdown voltage. A dual-oxide (5nm) would also suffer from voltage overstress that may occur in many analog designs, such as power amplifiers in radio-frequency (See chapter 12). Moreover, a thick oxide suffers from less process variations, which ensures a better control of the final capacitance.

High precision Poly-Poly2 Capacitor

As process variations mainly affect the peripheral aspect of the layers, square geometry performs better than rectangular geometry. The optimum dimensions lie between 10x10µm and 50x50µm [Hastings]. If larger sizes are used, gradient effects affect the quality of the oxide which is no more uniform in the whole dielectric surface. Consequently, the capacitor should be split into 50x50µm units. Also, no device or diffusion region should be designed next to the capacitor. It is highly recommended to shield the capacitor area by using a guard ring of contacts which limit the substrate noise that may couple to the lower capacitor plate.

Also, the high impedance node should be connected to the upper plate of the metal, which is more isolated from the substrate and lateral noise. Finally, dummy capacitors can also be placed on the layout, for high precision matching. An example of high precision capacitor using 4 units of 4pF each is shown in figure 11-15. Dummy capacitors do not have the same size as capacitor units for a reason of silicon area saving. However, the spacing between the dummy capacitor and the active capacitor is preserved. The dummy devices serve as electrostatic shielding.

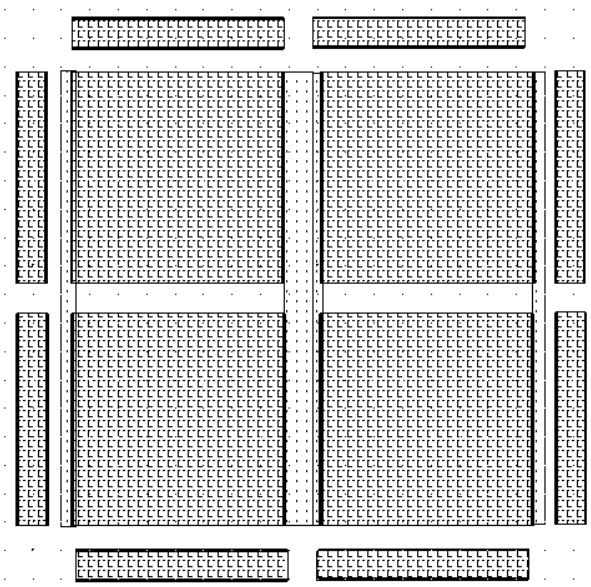


Figure 11-15: The layout of a 16pF poly-poly2 capacitor (CapaPoly15pF.MSK) using four units and dummy capacitor

Inter-Metal Capacitor

The multiplication of metal layers create lateral and vertical capacitance effects of rising importance. Although the inter-metal oxide is 10 to 50 times thicker than the ultra-thin gate oxide, the spared silicon area in upper metal layers may be used for small size capacitance, which might be attractive for compensation or local decoupling.

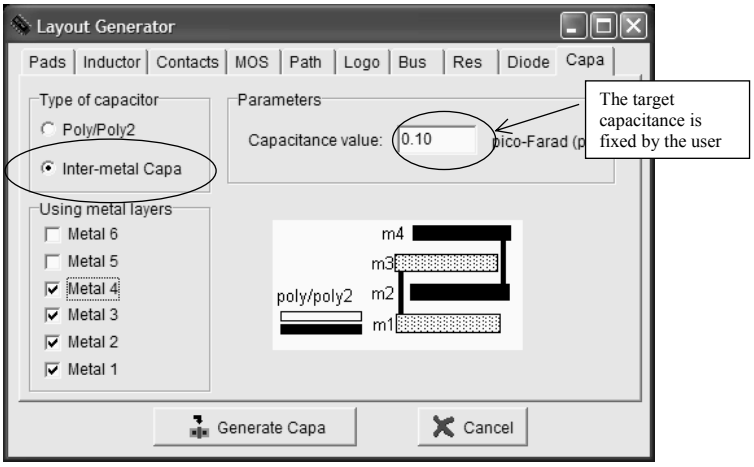


Figure 11-16: Menu for generating an inter-metal capacitor

The menu for generating the inter-metal capacitor is the same as for the poly/poly2 capacitor, except that the type of capacitor is changed (Figure 11-16). Depending on the desired capacitor value, Microwind computes the size of the square structure, made of metal plates, that reaches the capacitance value. In figure 11-16, a sandwich of metal1, metal2, metal3 and metal 4 is selected, for a target value of 100fF. The comparative aspect of the poly/poly2 capacitor and inter-metal capacitor is given in figure 11-17 for an identical capacitance value of 100fF. We confirm the poor efficiency of inter-metal capacitor due to the thick oxide, in comparison with the area-effective poly/poly2 structure.

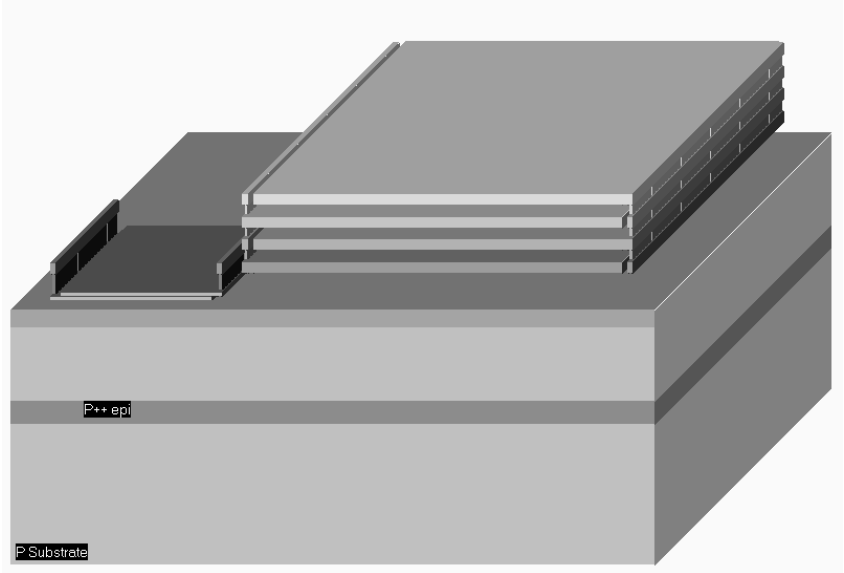


Figure 11-17: Generating an inter-metal capacitor (CapaPolyMetalComp.MSK)

Capacitor Cell

Notice that a capacitor cell also exist in most logic cell libraries. This cell is inserted regularly in the design to add voluntary capacitance between the power rails VDD and VSS. This capacitor acts as a noise decoupling and reduces the external parasitic noise provoked by logic gate switching. The main drawback of this gate oxide capacitor is its low breakdown voltage, and the non-negligible possibility of gate-oxide defect which may result in a permanent conductive path between the supply rails. An implementation of the capacitor cell in a silicon area identical to the basic inverter is proposed in figure 11-19 left. Using a larger cell area, the gate area can be enlarged, which raises the equivalent decoupling capacitance very rapidly.

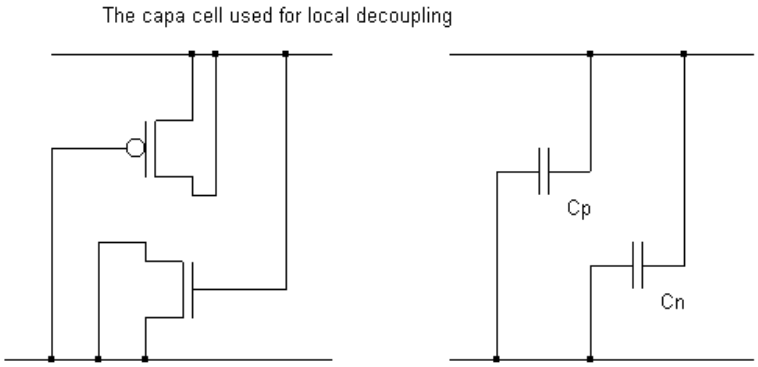


Figure 11-18: Principles and equivalent diagram of the capacitor cell, inserted in the logic circuit core for improved noise decoupling (CapaCell.MSK)

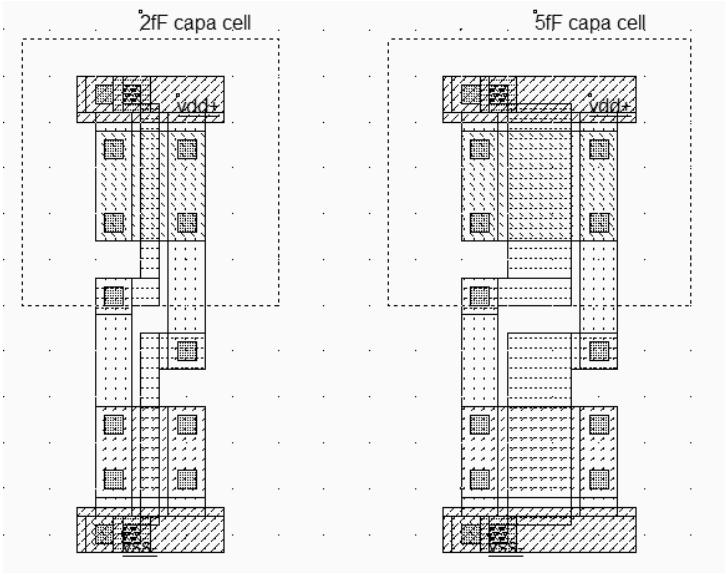


Figure 11-19: Two implementations of the capacitor cell (2fF, 5fF) (CapaCell.MSK)

3. The MOS device for analog design

The MOS has been used in previous chapters mainly as a switch. The most important parameters are the maximum available current *Ion* current and the parasitic leakage current *Ioff*. The Ion current corresponds to a maximum *Vgs* and maximum *Vds* (Upper right point in figure 11-20). In the case of analog design, the MOS do not operate only in cut-off or saturation regime. It also operates in the so-called quadratic zone, that appears in the static characteristics shown in figure 11-20. In that case, *Vds* is rarely very large, as well as *Vgs*. The MOS device operates in an intermediate regime which is attractive for most analog applications.

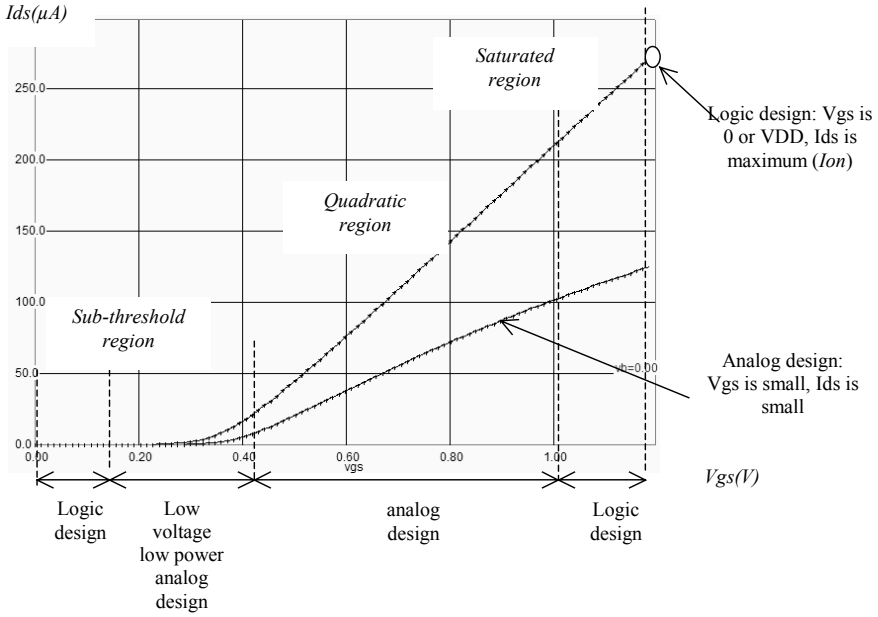


Figure 11-20: In analog design, the MOS device also operates in quadratic zone

Using Bsim4

The MOS model "level 3" is reasonably accurate in the case of logic circuits. When dealing with analog circuits, significant mismatch are observed between MOS level 3 and the advanced model BSIM4. This is because the equations of the model in level 3 do not account for many second order parameters, that have a very important impact when running in small voltages and currents. We recommend the use of the model BSIM4 in all analog cells described in this chapter. Select BSIM4 in the menu of the command **Simulate → Using Model → BSIM4**. An alternative consists in selecting the model BSIM4 in the list proposed in the simulation parameters (**Simulate → Simulation parameters**).

You may automatically select BSIM4 by adding a text in the layout that starts with "`BSIM4`". In the layout example shown in figure 11-21, we added a text "`BSIM4`", which forces the simulator to use the BSIM4 model instead of the default MOS level 3. This text appears for example at the left lower part of the layout of the transmission gate, described in figure 11-22.

Analog switch

The analog switch is able to transfer or interrupt an analog signal. It can be constructed using the pass gate described in chapter 2 which used one n-channel MOS and one p-channel MOS in parallel. The transmission gate lets an analog signal flow if *en=1* and *~en*=0. In that case both the n-channel and p-channel devices are on.

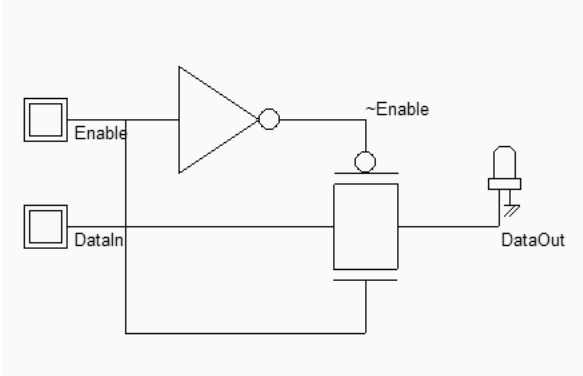


Figure 11-22: Schematic diagram of the analog switch (TGATE.Sch)

The layout of the analog switch is shown in figure 11-23. The inverter is situated on the left, the transmission gate on the right. A sinusoidal wave with a frequency of 2GHz is assigned to *DataIn*. The sinusoidal property may be found in the palette of Microwind2, near the clock and pulse properties. With a zero on *Enable* (And a 1 on *~Enable*), the switch is off, and no signal is transferred (Figure 11-24). When *Enable* is asserted, the sinusoidal wave appears nearly identical to the output.

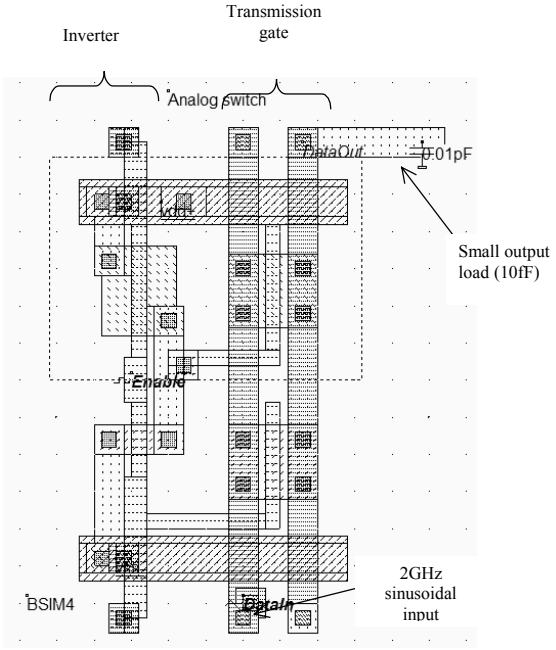


Figure 11-23. Simulation of the analog switch (AnalogSwitch.MSK)

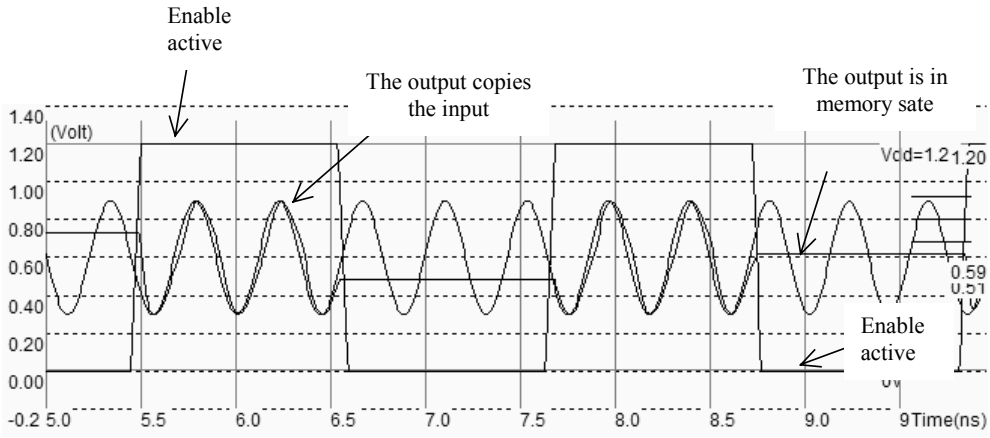


Figure 11-24. Simulation of the transmission gate (AnalogSwitch.MSK)

As the output is loaded with a 10fF virtual capacitance, the output is slightly distorted. This is due to the non linear resistance variation of the transmission gate with the input voltage. Consequently, the transmission gate reacts faster for a low voltage or a high voltage, and slower for an intermediate voltage where n-channel and p-channel devices have less current capabilities, even if both conduct at the same time.

4. Diode-connected MOS

The schematic diagram of the diode-connected MOS is proposed in figure 11-25. This circuit features a high resistance within a small silicon area. The key idea is to build a permanent connection between the drain and the gate. Most of the time, the source is connected to ground in the case of n-channel MOS, and to VDD in the case of p-channel MOS.

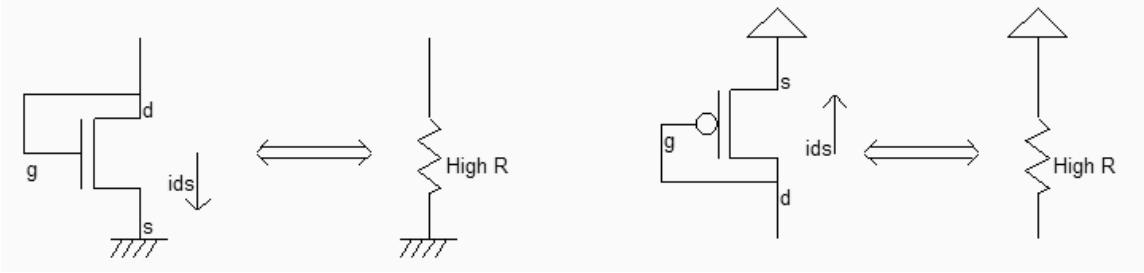


Figure 11-25 : Schematic diagram of the MOS connected as a diode (MosRes.SCH)

To create the diode-connected MOS, the easiest way is to use the MOS generator. Enter a large length and a small width, for example W=0.24µm and L=2.4µm. This sizing corresponds to a long channel, featuring a very high equivalent resistance.

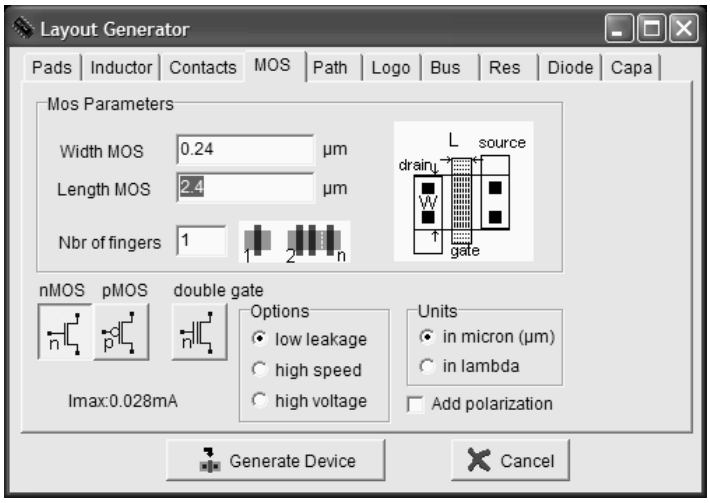


Figure 11-26 : Using the MOS generator to create a n-channel MOS with a large length and small width.

Add a poly/metal contact and connect the gate to one diffusion. Add a clock on that node. Add a VSS property to the other diffusion. The layout result is shown in figure 11-27.

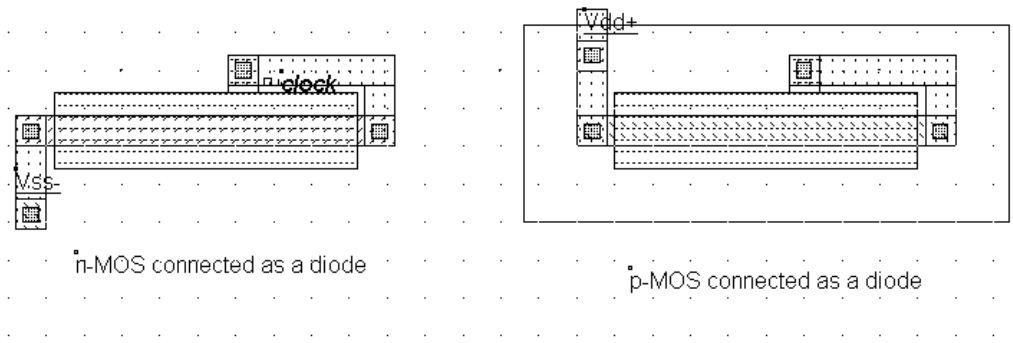


Figure 11-27 : Schematic diagram of the MOS connected as a diode (ResMos.MSK)

Now, click **Simulation on Layout.** In a small window, the MOS characteristics are drawn, with the functional point drawn as a color dot (Figure 11-28). It can be seen that the *I/V* characteristics correspond to a diode. The resistance is the invert value of the slope in the *Id/Vd* characteristics. For Vds larger than 0.6V, the resistance is almost constant. As the current *Ids* increases of 10µA in 0.4V, the resistance can be estimated around 40KΩ. A more precise evaluation is performed by Microwind if you draw the slope manually. At the bottom of the screen, the equivalent resistance appears, together with the voltage and current.

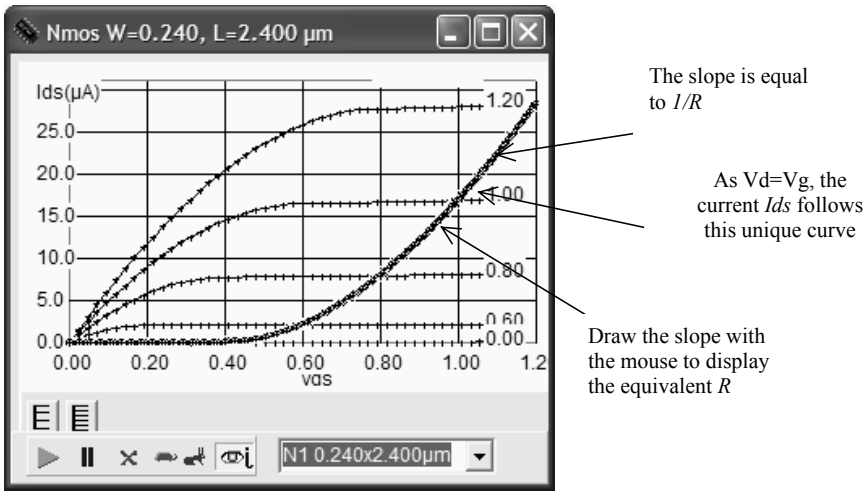


Figure 11-28 : Using the Simulation on Layout to follow the characteristics of the diode-connected MOS (ResMos.MSK)

In summary, the MOS connected as a diode is a capacitance for $Vgs<Vt$, a high resistance when Vgs is higher than the threshold voltage Vt. The resistance obtained using such a circuit can easily reach 100KΩ in a very small silicon area. The same resistance can be drawn in poly but would require a much larger area. The resistance per square of an unsalicide polysilicon serpentine is approximately 40 ohm. In figure 11-29, a polysilicon resistance of 30KΩ is drawn close to the MOS device with a 30KΩ resistance. The advantage of using a MOS resistance rather than a polysilicon resistance is obvious in terms of silicon area.

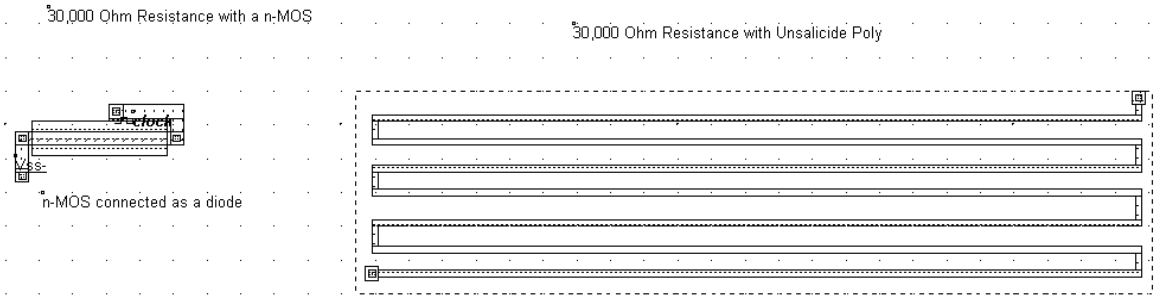


Figure 11-29: A MOS device resistance compared to the same resistance in Poly(ResMos.MSK)

5. Voltage Reference

The voltage reference is usually derived from a voltage divider made from resistance. The output voltage *Vref* is defined by equation 11-4.

$$V_{ref} = \frac{R_N}{R_N + R_P} V_{DD} \qquad \text{(Eq. 11-4)}$$

with

V_{DD}=power supply voltage (1.2V in 0.12µm)

R_N=equivalent resistance of the n-channel MOS (ohm)

R_P=equivalent resistance of the p-channel MOS (ohm)

The value of the resistance must be high enough to keep the short -circuit current low, to avoid wasted power consumption. A key idea is to use MOS devices rather than polysilicon or diffusion resistance to keep the silicon area very small. Notice that two n-MOS or two p-MOS properly connected feature the same function. P-MOS devices offer higher resistance due to lower mobility, compared to n-channel MOS. Four voltage reference designs are shown in figure 11-30. The most common design uses one p-channel MOS and one n-channel MOS connected as diodes.

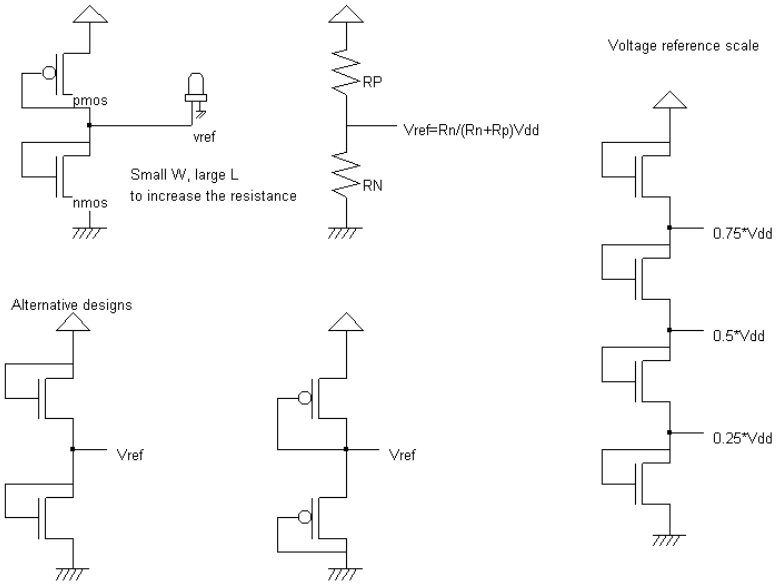


Figure 11-30 : Voltage reference using PMOS and NMOS devices as large resistance

The alternative solutions consist in using two n-channel MOS devices only (Left lower part of the figure), or their opposite built from p-channel devices only. Not only one reference voltage may be created, but also three, as shown in the right part of the figure, which use four n-channel MOS devices connected as diodes.

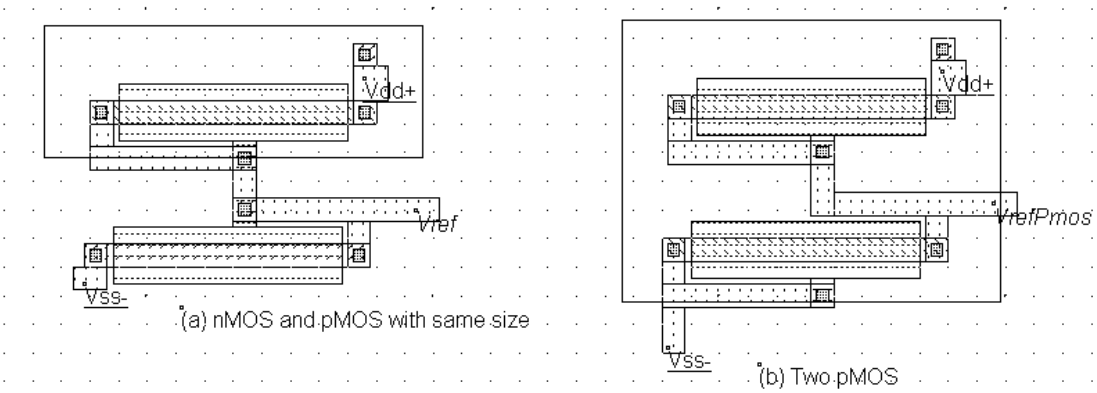


Figure 11-31 : Voltage reference circuits (a) with one nMOS and one pMOS (b) with two pMOS (Vref.MSK)

In the layout of figure 11-31, the pMOS and nMOS have the same size. Due to lower pMOS mobility, the resulting *Vref* is a little lower than VDD/2. Using BSIM4 instead of model 3, we see that the voltage reference obtained with two identical pMOS devices is not VDD/2 either, as shown in the simulation of figure 11-32. This is due to the non-symmetrical polarization of the pMOS regarding the substrate voltage *Vbs* which has a significant impact on the current (Figure 11-33). Consequently, a good VDD/2 voltage reference requires a precise adjustment of MOS sizing, a good confidence in the accuracy of the model, and several iterations of design/simulation until the target reference voltage is reached.

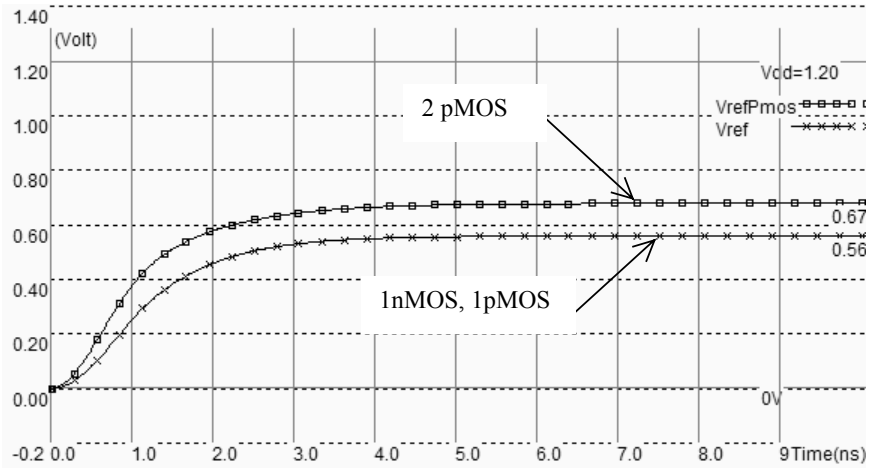


Figure 11-32 : Simulation of the two voltage reference circuits (Vref.MSK) using BSIM4 model

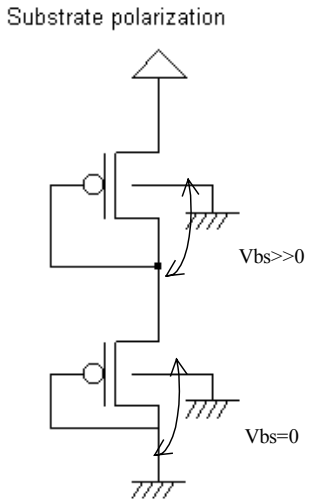


Figure 11-33 : The polarization of the two pMOS is not identical due to the substrate effect (Vref.SCH)

The value of the voltage reference *Vref* versus the size of the n-channel and p-channel MOS is quite difficult to calculate as the resistance of the channel is highly non-linear. In [Baker], the formulation is deduced from the equations of model 1:

$$V_{ref} = \frac{V_{DD} - V_{tp} + \sqrt{\frac{\beta_N}{\beta_P}} V_{tn}}{\sqrt{\frac{\beta_N}{\beta_P}} + 1} \qquad \text{(Equ. 11-5)}$$

with

$$\beta_N = \mu_N \frac{W_N}{L_N} \text{ and } \beta_P = \mu_P \frac{W_P}{L_P}$$

where

μ_N=mobility of electrons (600 cm^2/V.s)

μ_P=mobility of holes (250 cm^2/V.s)

Wn= nMOS width (µm)

Ln=nMOS length (µm)

Wp=pMOS width (µm)

Lp = pMOS length (µm)

Multiple voltage reference

Not more than three MOS devices can be connected in series to produce intermediate voltage references. The limiting factor is the threshold voltage. When trying to simulate a series of more than 3 MOS connected as diodes, the operating regime keeps in sub-threshold mode, which is attractive for very low power consumption, but introduces important setup delays and creates very weak voltage references. When more than 3 reference voltages are needed, the network is built using resistance, as shown in figure 11-34. The static power consumption is 100µW, which is due to the DC current flowing through the resistors between VDD and VSS. Larger resistance would decrease this static power, down to the specified user requirement.

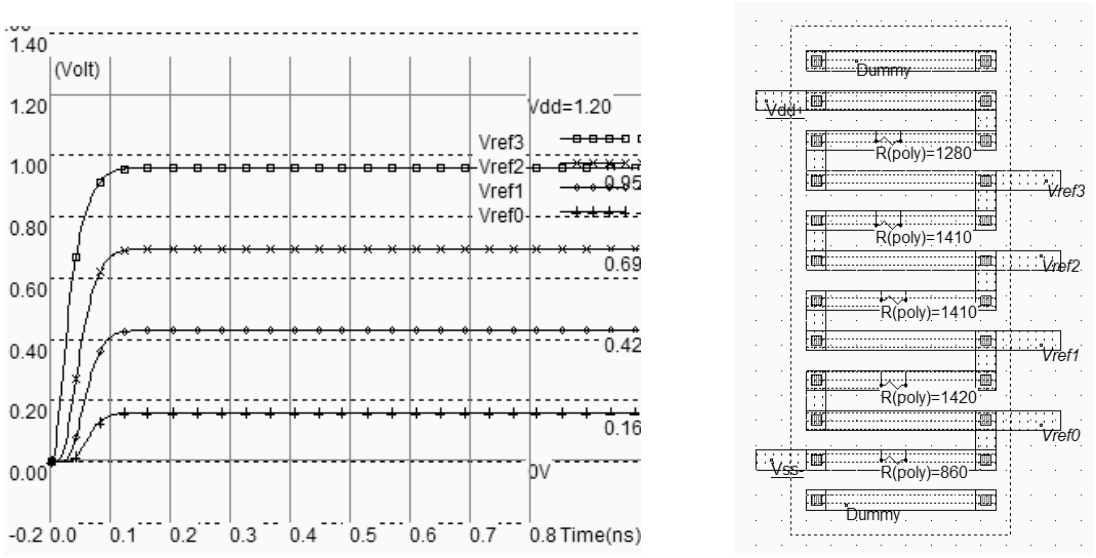


Figure 11-34 : Resistor scale (VrefMul.MSK)

Shielding

The voltage reference *Vref* created by our circuits is very weak, in the sense that the current which flows in the MOS branch is small. In other words, the *Vref* signal is highly resistive, we say also "high impedance". This means that a parasitic signal that couples with the *Vref* connection may induce some noise, for example by proximity effect and capacitance coupling *Cx*, as shown in figure 11-35.

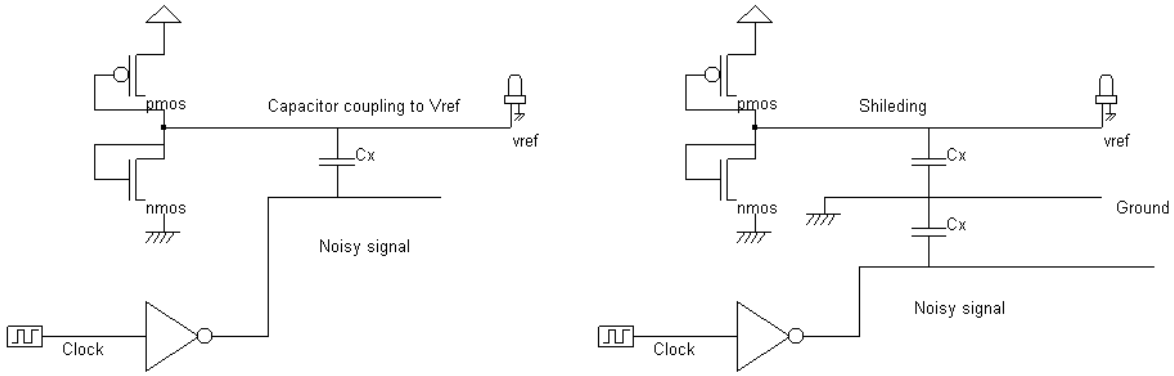


Figure 11-35 : Without shielding, the Vref voltage may be altered by noisy signals routed close to its interconnect (VrefNoise.SCH)

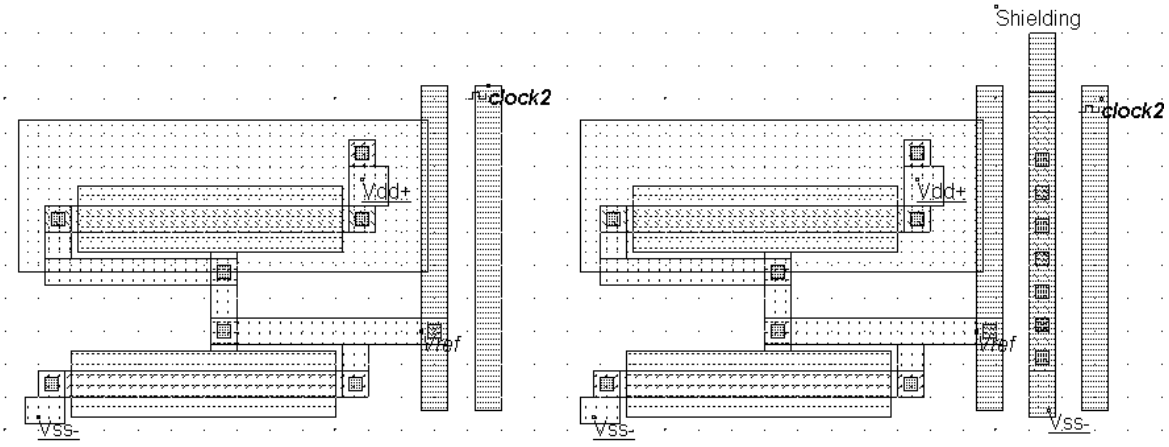


Figure 11-36 : Unshielded voltage reference (left) and shielded voltage reference (right) (VrefNoise.MSK)

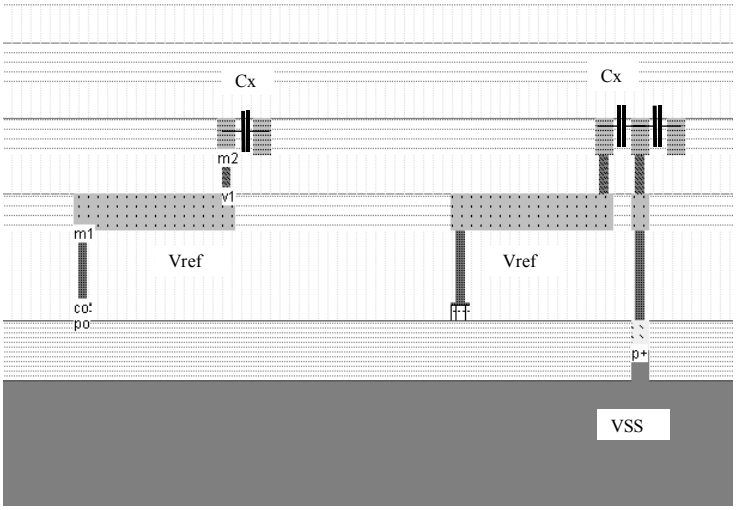


Figure 11-37 : 2D cross-section of the unshielded (Left) and shielded voltage reference (VrefNoise.MSK)

Adding a metal shielding acts as a noise barrier and protects *Vref* from the clock coupling (Figure 11-36). The 2D cross-section shows the two structures: on the left side, the output signal *Vref* has a parasitic coupling capacitance *Cx* connected to the noise signal. When the noisy signal switches, the voltage reference is altered. On the right structure, a barrier made of a p-type diffusion, metal and metal2 create an electrostatic screen. The coupling still exists, but *Cx* is now connected to a cold signal, meaning that the ground capacitance is increased, and the noise is eliminated.

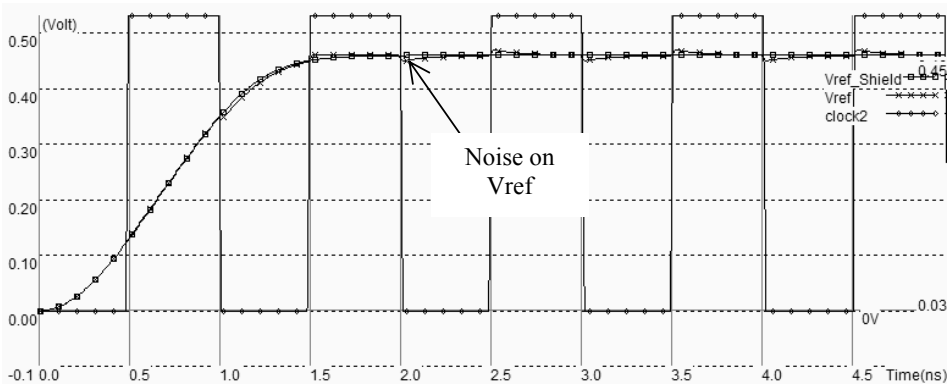


Figure 11-38 : Simulation of the unshielded and shielded Vref showing a small crosstalk noise (VrefNoise.MSK)

The effect of the shielding is demonstrated in the simulation shown in figure 11-38. In Microwind, the crosstalk effect due to lateral coupling is extracted but not simulated by default. The crosstalk simulation is activated by the command **Simulate → With crosstalk**. Although the coupling capacitor still exists, the shielding is connected to ground and prevents the clock from interfering with the *Vref_shield* signal which remains flat.

Influence of Temperature

You may change the temperature (**Simulate → Simulate Options**) and see how the voltage reference is altered by temperature. The circuit based on one nMOS and one pMOS, already presented in figure 11-30, is not much influenced by temperature. The temperature coefficient (TC), to a first order, is almost equal to zero. A similar result is obtained using model 3 or BSIM4. This means that a stable on-chip voltage reference around VDD/2 is quite simple to achieve.

The design of a reference voltage VDD/3 lead to unbalanced resistivity, which has a direct impact on the temperature coefficient. This time, the voltage is no more a reference voltage as it only coincides with VDD/3 at room temperature of 25°C. At high temperature, the voltage reference is much too low. The simulation results are summarized in figure 11-39. The parametric analysis has been used to compute the voltage *Vref* iteratively at the end of a 5ns simulation, with increased temperature from -40 to 120°C.

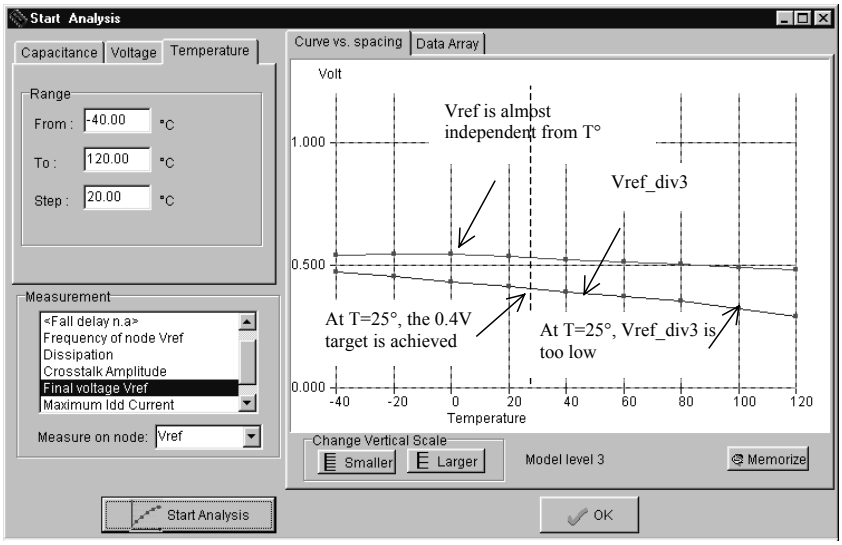


Figure 11-39 : Simulation of the influence of temperature on the reference voltage (Vref.MSK)

6. Current Mirror

The current mirror is one of the most useful basic blocs in analog design. It is primarily used to copy currents. When a current flows through a MOS device *N1*, an almost identical current flows through the device *N2*, as soon as *N1* and *N2* are connected as current mirrors. In its most simple configuration, the current mirror consists of two MOS devices connected as shown in figure 11-40. A current *I1* flowing through the device *Master* is copied onto the MOS device *Slave*. If the size of *Master* and *Slave* are identical, in most operating conditions, the currents *I2* and *I1* are identical. The remarkable phenomenon is that the current is almost independent from the load, represented in figure 11-40 by a resistor R_{load}.

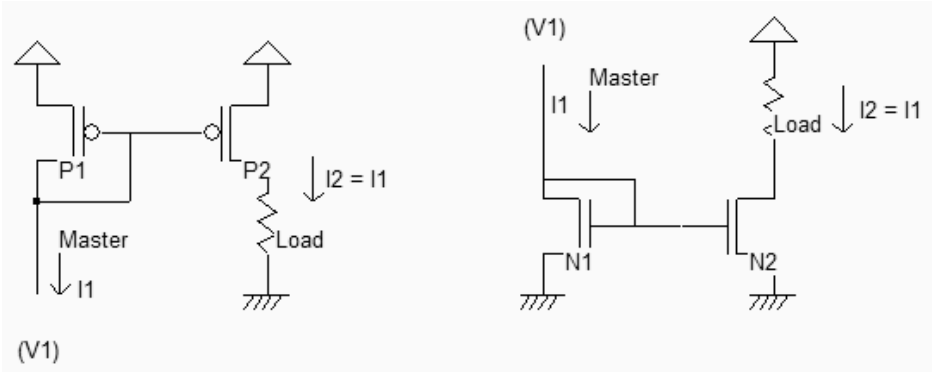


Figure 11-40: Current mirror principles in nMOS and pMOS version (CurrentMirror.SCH)

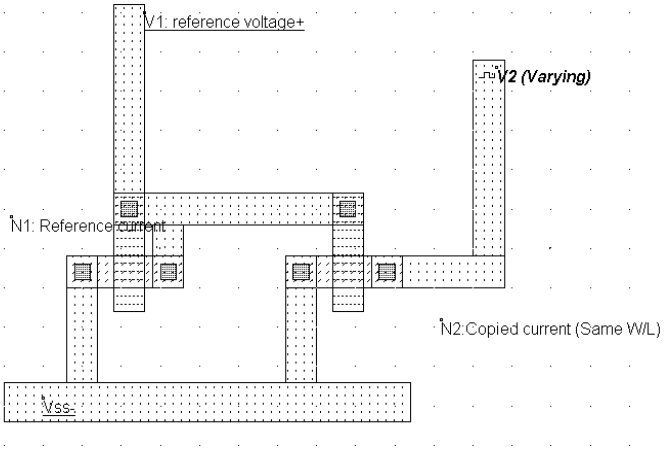


Figure 11-41: Layout of an n-channel current mirror with identical size (CurrentMirror.MSK)

The illustration of the current mirror behavior is proposed in the case of two identical N-channel MOS (Figure 11-41). The current of the master *N1* is fixed by *V1*, which is around 0.6V in this case. We use the simulation on layout to observe the current flowing in *N1* and *N2*.

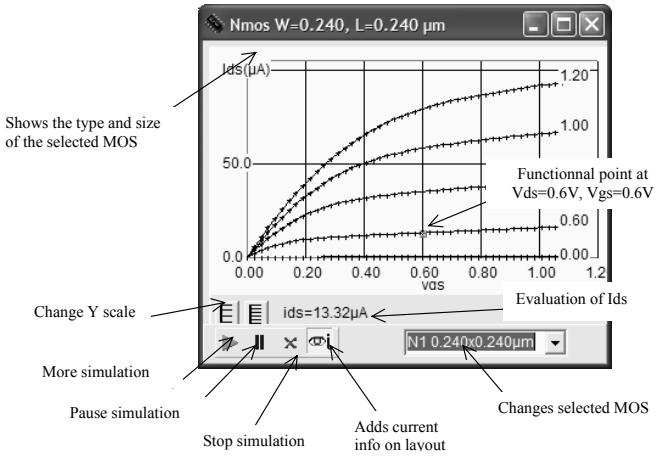


Figure 11-42: The nMOS N1 has a fixed current around 12µA flowing between drain and source (CurrentMirror.MSK)

Concerning *N1*, the gate and drain voltage is fixed to 0.6V, which corresponds to a constant current of around 13µA, as shown in figure 11-42. The voltage *V2* (Figure 11-43) varies thanks to a clock. We observe that the current *I2* is almost equal to 13µA, independently of *V2*, except when *V2* is lower than 0.2V. More precisely, the variation of *I2* is between 12 and 16µA when *V2* varies from 0.2 to 1.2V.

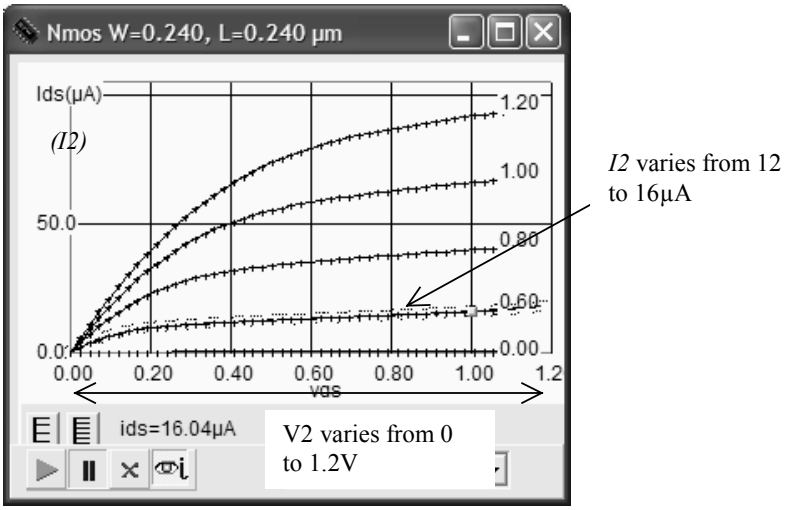


Figure 11-43: Illustration of the nMOS current mirror principles (CurrentMirror.MSK)

Improving the Current Mirror

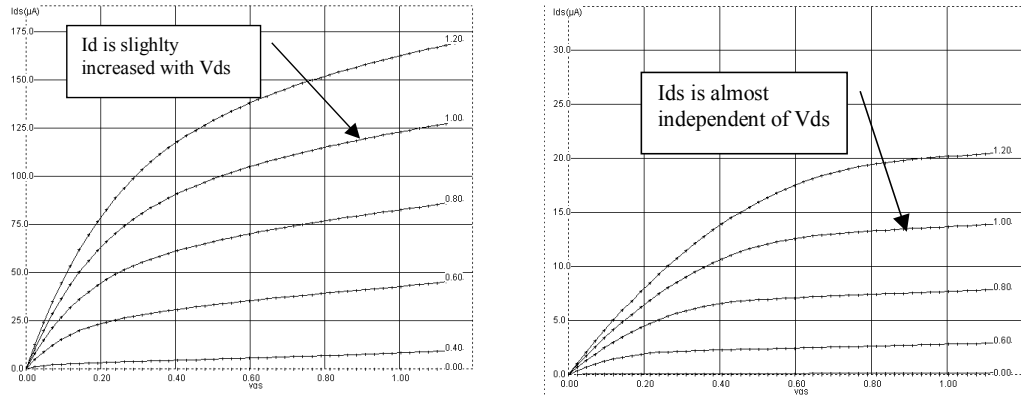


Figure 11-44: Long channel MOS are preferred for high performance current mirrors

As the basic principle of the current copy is the assumption that *Id* is independent of *Vds*, the long channel MOS (Fig 11-44 right) is a better candidate than the short channel MOS (Fig 11-44 left). Although the short channel MOS works faster, the long channel MOS is preferred for its higher precision when copying currents.

Mos Matching

A set of design techniques can improve the current mirror behavior, which are described hereafter.

- All MOS devices should have the same orientation. During fabrication, the chemical process has proven to be slightly different depending on the orientation, resulting in variations of effective channel length. This mismatch alters the current duplication if one nMOS are implemented horizontally, the other vertically.
- Long channel MOS devices are preferred. In such devices, the channel length modulation is small, and consequently *Ids* is almost independent of *Vds*.

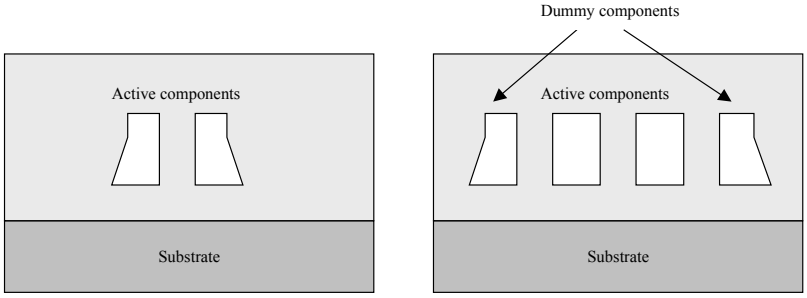


Figure 11-45: 2D aspect of the circuit without and with dummy components

- Dummy gates should be added on both sides of the current mirror. Although some silicon area is lost, due to the addition of inactive components, the patterning of active gates leads to very regular structures, ensuring a high quality matching (See figure 11-45).
- MOS devices should be in parallel. If possible, portions of the two MOS devices should be interleaved to reduce the impact of an always-possible gradient of resistance, or capacitance with the location within the substrate.

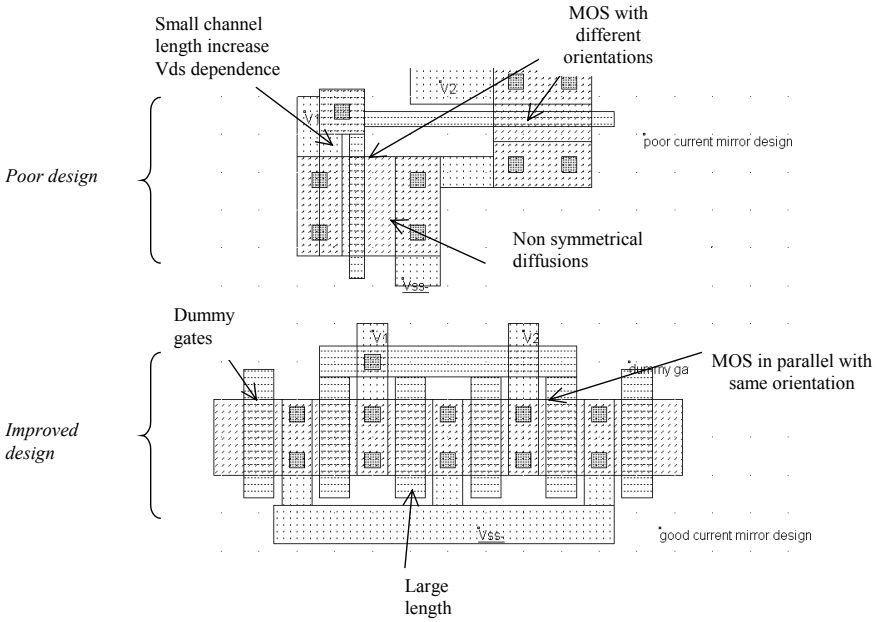


Figure 11-46: Design of high performance current mirrors (MirrorMatch.MSK)

A synthesis of these recommendations is proposed in the two designs of figure 11-46. The current mirror situated at the top of the figure cumulates design weaknesses: short channel length, non-symmetrical drain and source design, and different orientations for the devices. The design at the bottom realizes the same current copying function, and complies with the most important rules for a good current copying: dummy components, same orientation, symmetrical design, and MOS devices with large length.

Current Multiplier

If the ratio W/L of the *Slave* (Transistor *P2*) is 10 times the ratio of the *Master*, the current *I2* on the right branch is 10 times the current *I1* on the left branch. This is illustrated by the schematic diagram in the left of figure 11-47. In the case of the PMOS current mirror, the ratio W/L of the *Slave* (*P2*) is 5 times the ratio of the *Master,* the current *I2* is 5 times the current *I1*.

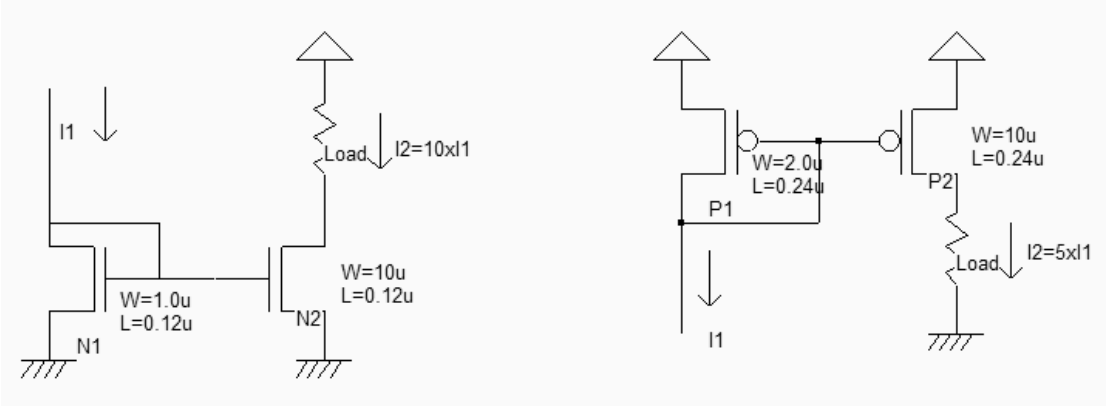


Figure 11-47: Multiplying currents by changing the size of the MOS (MirrorMatch.MSK)

7. The MOS transconductance

In its most simple form, the MOS can be represented as a current generator controlled by the voltage, or Voltage-Controlled Current Source (VCCS). The schematic diagram of the VCCS is given in figure 11-6. We add to V_{GS} a small sinusoidal input v_{gs} which provokes a small variation of current i_{ds} to the static current I_{DS}. For small variations of v_{gs}, the link between the variation of current i_{ds} and the variation of voltage v_{gs} can be approximated by (equ. 11-6).

$$i_{ds} = g_m v_{gs} \qquad \text{(Equ. 11-6)}$$

The transconductance *gm* has the dimension of the ratio of current to voltage, that is the invert of the resistance, and its definition is given in equation 11-7.

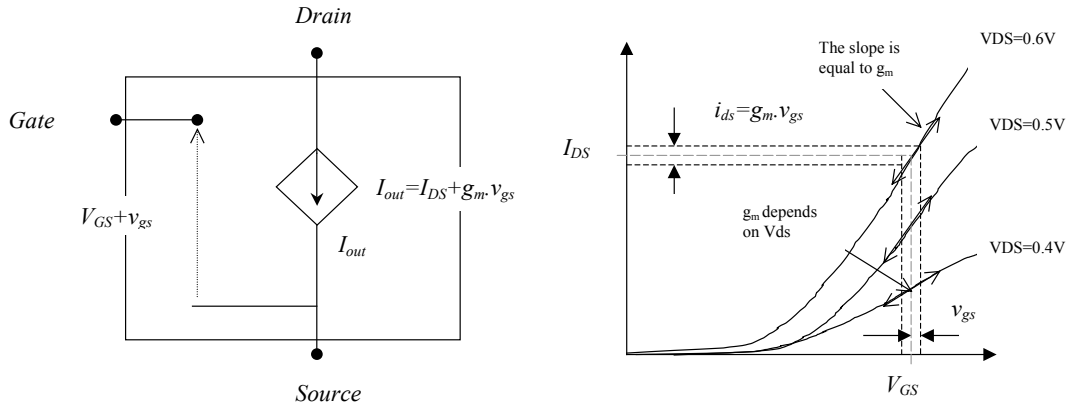


Figure 11-47 : The MOS transconductance gm

$$g_m \equiv \frac{\partial I_{DS}}{\partial V_{GS}} \qquad \text{(equ. 11-7)}$$

The derivation of the transconductance *gm* from the MOS equations in level 1 leads to a quite simple expression reported in equations 11-8 (Linear region) and 11-9 (saturation region).

Linear region $$g_m = \frac{\partial(\beta((V_{gs}-vt).V_{ds} - \frac{(V_{ds})^2}{2})}{\partial V_{GS}} = \beta(V_{ds}) \qquad \text{(Equ. 11-8)}$$

Saturation region $$g_m = \frac{\partial(\beta(V_{gs}-vt)^2)}{\partial V_{GS}} = \frac{\beta(V_{gs}-vt)}{2} \qquad \text{(Equ. 11-9)}$$

with

$$\beta = UO\frac{\varepsilon_0\varepsilon_r}{TOX}.\frac{W}{L}$$

where

Vgs=voltage between gate and source (V)

Vt= threshold voltage (V)

W=transistor width (µm)

L=transistor length (µm)

U0=electron mobility (m/V^{-2})

TOX=gate oxide (m)

For deep submicron technology, more accurate expressions of the transconductance gm are proposed such as those proposed in [Janssens]. The most important point to remember is the dependence (Linear in a first approximation) of *gm* with the width and *Vds*.

8. Single Stage Amplifier

The goal of the amplifier is to multiply by a significant factor the amplitude of a sinusoidal voltage input *Vin*, and deliver the amplified sinusoidal output *Vout* on a load. Such a circuit may be found at the input stage and the output stage of all telecommunication devices such as mobile phones. The input stage amplifier increases the amplitude of the captured signal from around 0.1-1mV to 10-100mV for further processing, while the output stage amplifier delivers a high voltage on the antenna to emit a significant power (Figure 11-48).

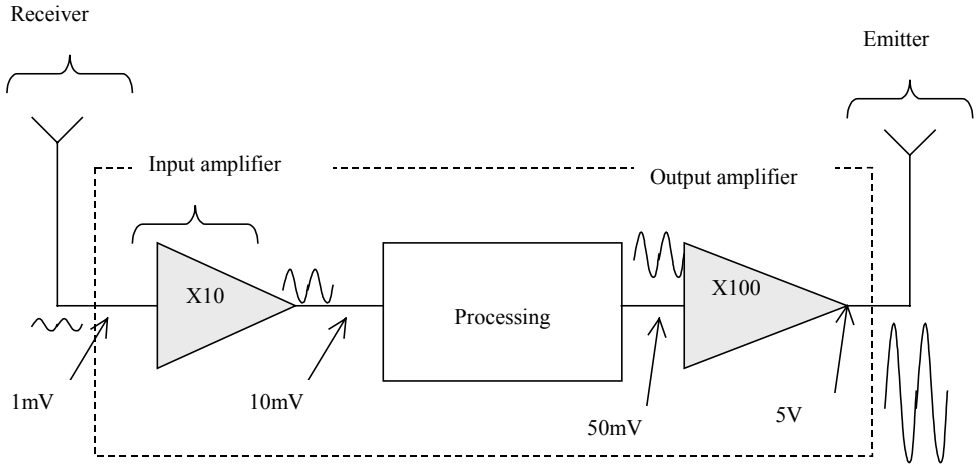


Figure 11-48: Example of amplifier circuits used in mobile devices

The single stage amplifier may consist of a MOS device (we choose here an n-channel MOS) and a load. The load can be a resistance or an inductance. In the circuit, we use a resistance made with a p-channel MOS device with gate and drain connected (Figure 11-49). The pMOS which replaces the passive load is called an active resistance.

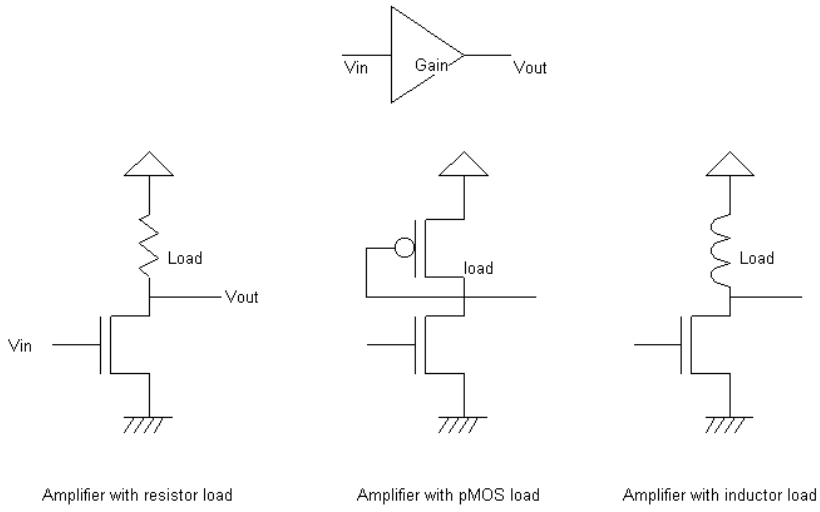


Figure 11-49: Single stage amplifier design with MOS devices (AmpliSingle.SCH)

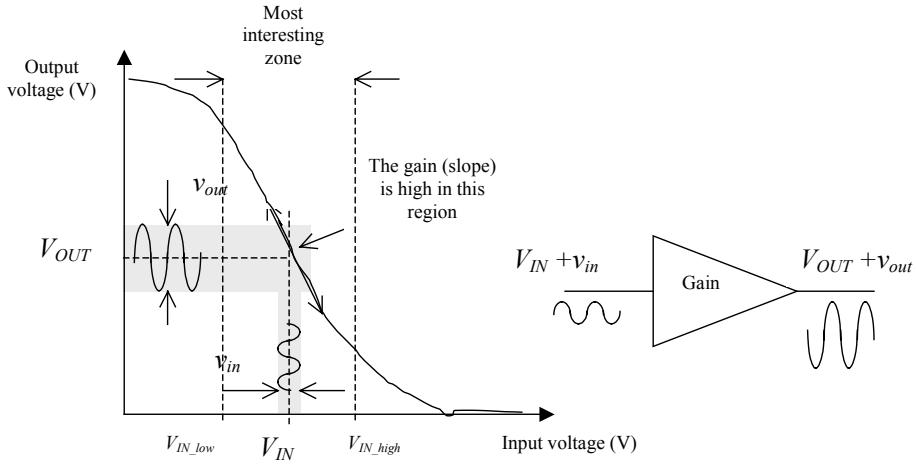


Figure 11-50: The amplifier has a high gain at a certain input range, where a small input signal vin is amplified to a large signal vout.

The single stage amplifier characteristics between *Vin* and *Vout* have a general shape shown in figure 11-50. The most interesting zone corresponds to the input voltage range where the transfer function has a linear shape, that is between *VIN_low* and *VIN_high*. Outside this voltage range, the behavior of the circuit does not correspond anymore to an amplifier. If we add a small sinusoidal input v_{in} to V_{IN}, a small variation of current i_{ds} is added to the static current I_{DS}, which induces a variation v_{out} of the output voltage V_{OUT}. The link between the variation of current i_{ds} and the variation of voltage v_{in} can be approximated by equation 11-10.

$$i_{ds} = g_m v_{gs} \qquad \text{(Equ. 11-10)}$$

Consequently, the gain of the amplifier for small signals can be expressed by equation 11-11.

$$Gain = \frac{v_{in}}{v_{out}} = \frac{-i_{ds}\dfrac{1}{g_{mp}}}{i_{ds}\dfrac{1}{g_{mn}}} = -\frac{g_{mn}}{g_{mp}} \qquad \text{(Equ. 11-11)}$$

In other words, the gain of the amplifier is high if g_{mp} is low, which is equivalent to a high pMOS pass resistance. The sign minus in equation 11-11 illustrates the fact that an increase of *vin* corresponds to a decrease of *vout*. The diode-connected p-channel MOS creates a high resistance when the channel width is minimum and the channel length is very large. Such a design means a high amplifier gain. In figure 11-51, an nMOS device with large width and minimum length is connected to a high resistance pMOS load. A 50mV sinusoidal input (*vin*) is superimposed to the static offset 0.6V (V_{IN}). What is expected is a 500mV sinusoidal wave (*vout*) with a certain DC offset (V_{OUT}).

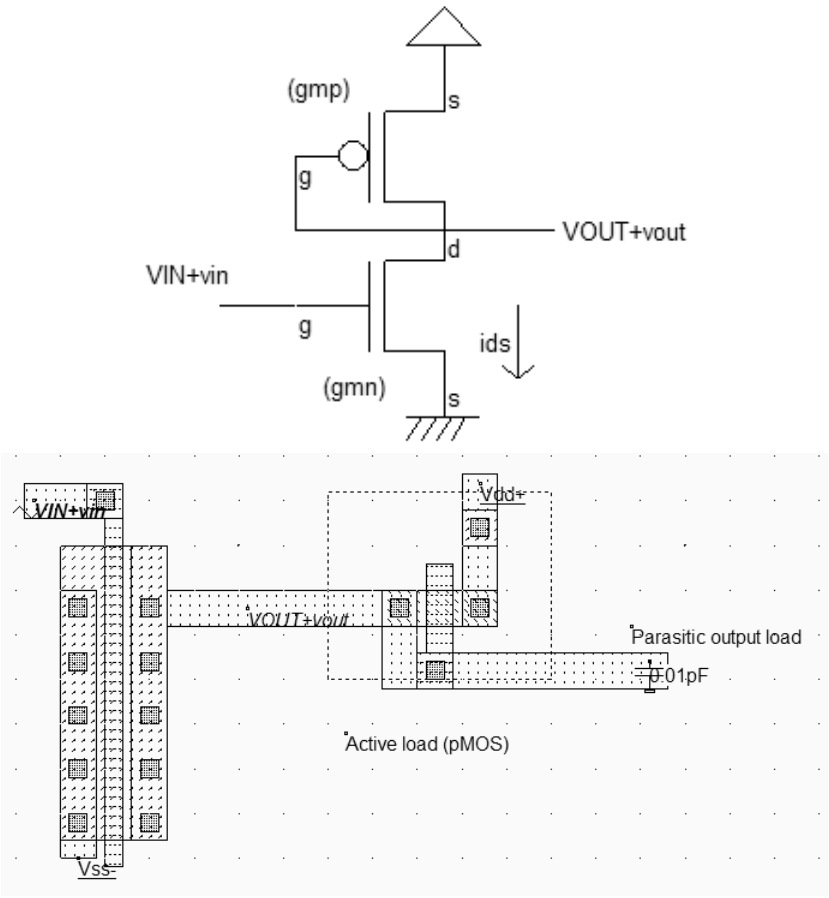


Figure 11-51: Single stage amplifier layout with a pMOS as a load resistor (AmpliSingle.MSK)

The time-domain simulation of the amplifier with a 1GHz sinusoidal input exhibits very poor performances. The gain is almost 0 and the output is very low, close to ground. This is because the offset V_{IN} has been fixed to a default value of VDD/2 (0.6V) which does not correspond to the region where the circuit provides a high gain. We are probably higher than $V_{IN\_high.}$

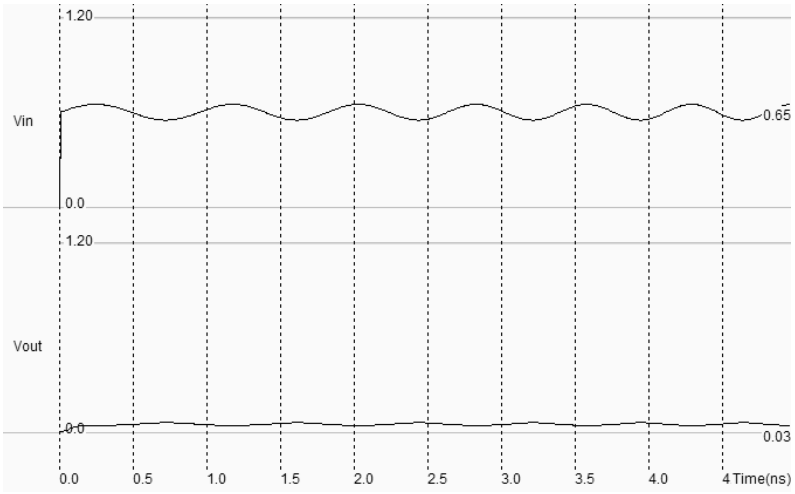


Figure 11-52: Simulation of the amplifier response to a 50mV input with a 0.6V offset (AmpliSingle.MSK)

What we need now is to find the characteristics *Vout/Vin* in order to tune the offset voltage V_{IN}. In the simulation window, click **Voltage vs voltage**" and **More**, to compute the static response of the amplifier (Figure 11-53). The range of voltage input that exhibits a correct gain appears clearly. For V_{DS} higher than 0.25V and lower than 0.4V, the output gain is around 3. Therefore, an optimum offset value is 0.35V. Change the parameter **Offset** of the input sinusoidal wave to place the input voltage in the correct polarization.

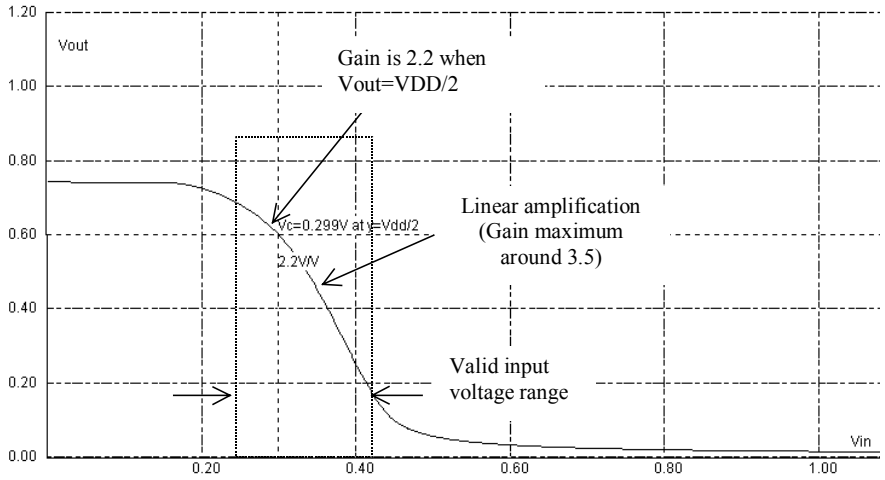


Figure 11-53: Single stage amplifier static response showing the valid input voltage range.

We change the sinusoidal input offset and start again the simulation. A gain of 3.5 is observed when the offset V_{IN} is 0.35V. In figure 11-54, the input amplitude is 100mV peak to peak, the output amplitude is 350mV peak-to-peak. These pieces of information appear in the information bar of the main window.

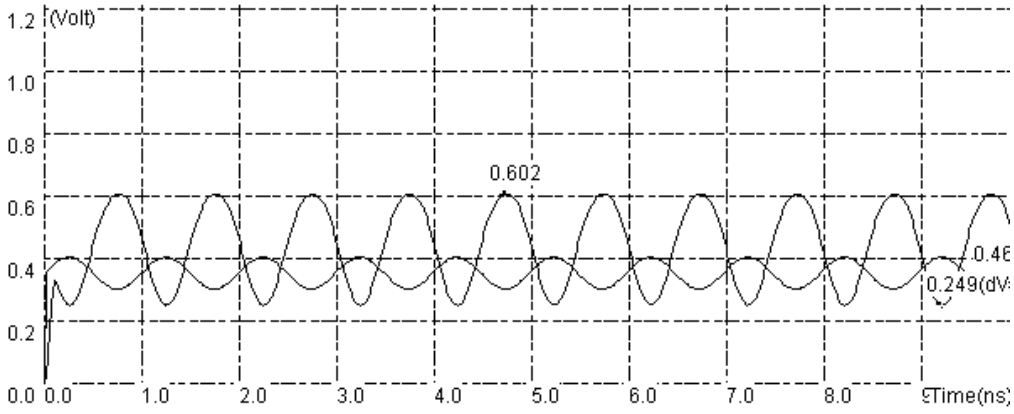


Figure 11-54: Single Stage amplifier with correct polarization V_{IN}=0.35V

To increase the gain, the ratio between the active load resistance and the n-channel MOS resistance should be increased. In the layout proposed in figure 11-55, three amplifiers are implemented: one with a pMOS load (layout with output *sinus1*), the second with high resistance pMOS (Layout with output *sinus2*), and the third with a very high resistor symbol (20Kohm).

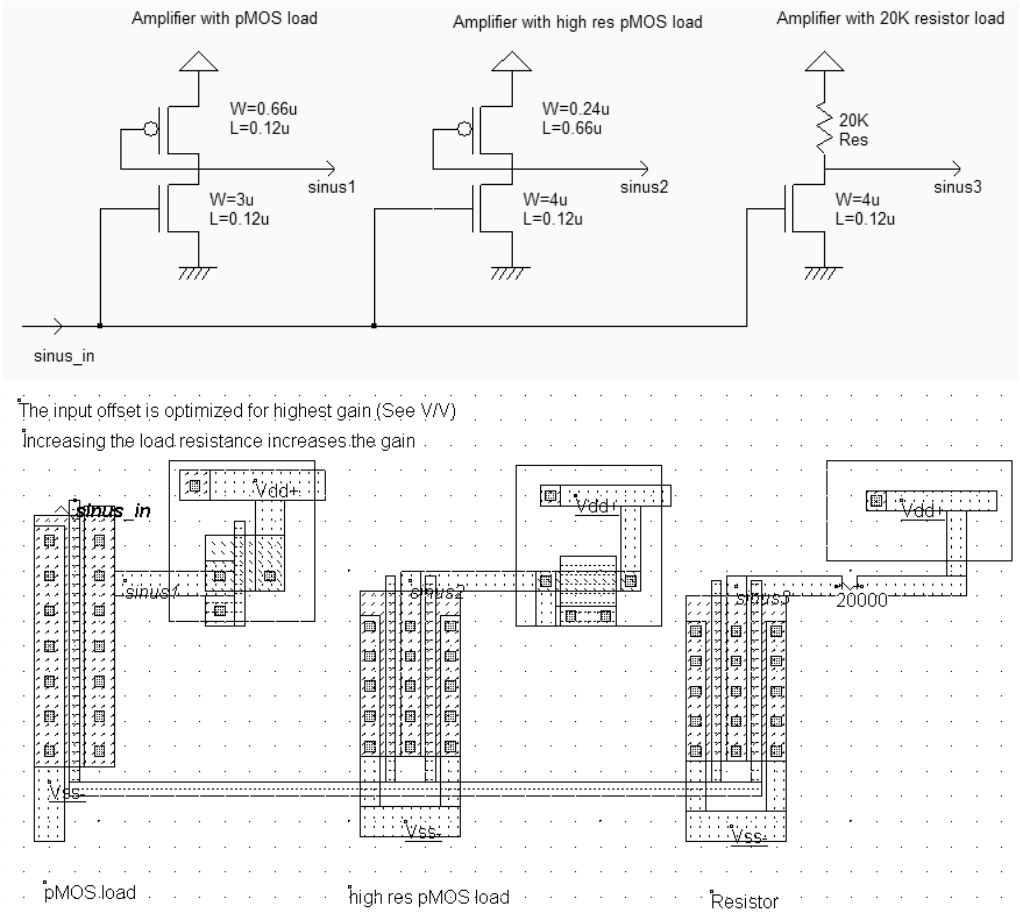


Figure 11-55: Single Stage amplifier with correct polarization V_{IN}=0.35V (AmpliSingle2.MSK)

The gain for *sinus2* is increased to 4.5, as observed in the static simulation (Figure 11-56), with sharper characteristics, but the input voltage range that features amplification is significantly reduced. A further increase of the pMOS resistance does not increase the gain. The gain saturates to around 8. If we replace the pMOS device by a resistor symbol, we also observe that the gain is limited to around 9.0.

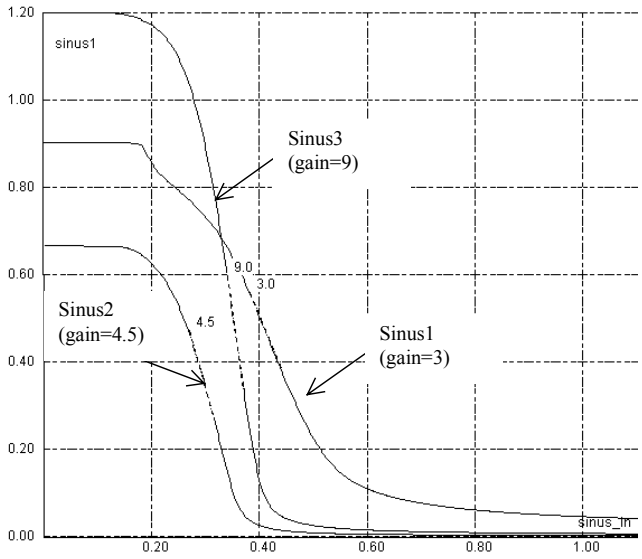


Figure 11-56: The active load sizing acts on the gain, but reduces the input voltage range for amplification (AmpliSingle2.MSK)

Transit and Cutt-Off frequency

The transit frequency f_t is a parameter well representative of the "speed" of the MOS device. It corresponds to the frequency at which the current *ids* starts being lower than the current flowing through the gate *igs*. The *igs* current is due to the charge and discharge of the capacitor *Cgs*. The *ids* current is the main amplifier current that flows between the drain and the source. Thus, f_t is the frequency for which the current gain of the MOS device is unity. Based on the equations of level 1, an analytical approximation of f_t is reported below [Baker].

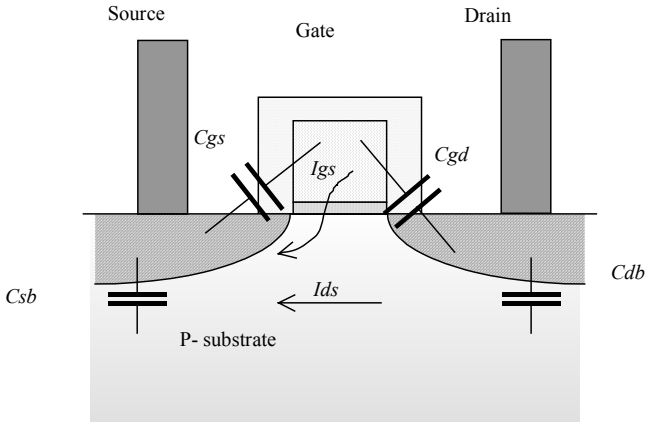


Figure 11-57: Cross-scetion of the MOS device showing the main parasitic capacitors

$$f_t = \frac{\varepsilon_0 \varepsilon r \cdot \mu_n W}{2\pi \cdot TOX.LC_{gs}}(V_{gs} - V_t) \qquad \text{(Equ. 11-12)}$$

with $C_{gs} \approx \frac{2}{3}(WLC_{ox})$

with

μn =electron mobility ($m.V^{-2}$)

W = channel width (μm)

L = channel length (μm)

Cgs = gate to source capacitance (F)

Vgs= gate to source voltage (V)

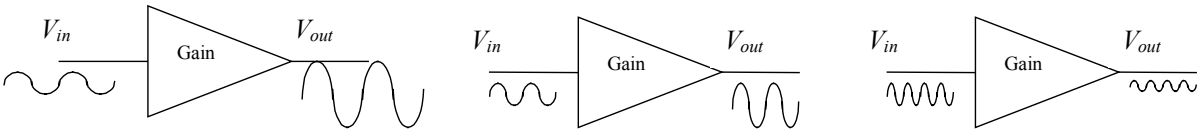
Vt= threshold voltage (V)

Replacing the value of *Cgs* in the expression of *ft*, the transit frequency becomes independent of the channel width (Equation 11-13). For an n-channel MOS device in 0.12μm, the measured value of f_t is around 50GHz, for *Vgs* around *Vdd/2*. The transit frequency f_t is an important metric of technology performances for very high frequency circuit design.

$$f_t = \frac{\varepsilon_0 \varepsilon r \cdot \mu_n}{\frac{4}{3}\pi^2 \cdot \mathrm{TOX.L}^2 . C_{ox}} (V_{gs} - V_t) \qquad \text{(Equ. 11-13)}$$

A similar parameter, the cut-off frequency, is the frequency at which the gain starts decreasing. We consider *G0* as the gain for low frequency input signals. The cut-off frequency is usually defined as the frequency when the gain is decreased by 1.4, according to equation 11-14.

$$f_{cut-off} = f(Gain = \frac{G0}{\sqrt{2}}) \qquad \text{(Equ 11-14)}$$



Low frequency: high gain G0 *Cut-off: gain divided by 1.4* *Higher than cut-off: gain tends to 0*

Figure 11-57: The cut-off frequency corresponds to the input frequency where the gain starts to decrease

Microwind does not perform frequency analysis. However, we can create a sinusoidal wave with an increasing frequency, thanks to the parameter **Increase f** of the sinus property assigned to *Vin* which is fixed in figure 11-58 to 0.2. At each period, the frequency is increased by 20%.

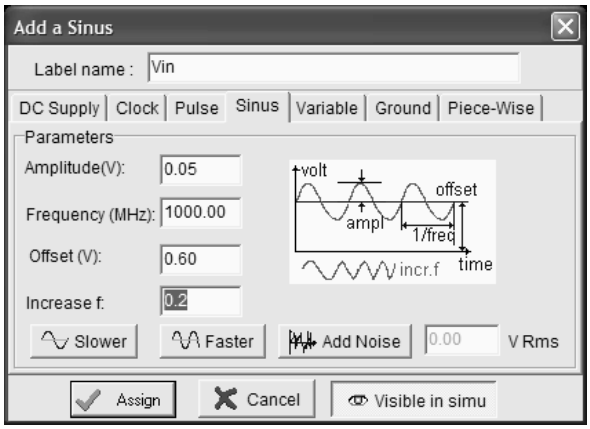


Figure 11-58: Time-domain simulation with a sinusoidal wave with frequency sweep (AmpliSingle.MSK)

The best simulation mode is **Frequency vs. time**. The upper screen displays the input frequency while the lower screen shows the amplitude of the input and output signals (Figure 11-59). There is no precise tool to locate the cut-off frequency. However, we observe a significant decrease of the gain from 2 GHz onwards, when the output is loaded with a 10fF parasitic capacitance. The parasitic capacitance of the output node has a direct impact on the cut-off frequency.

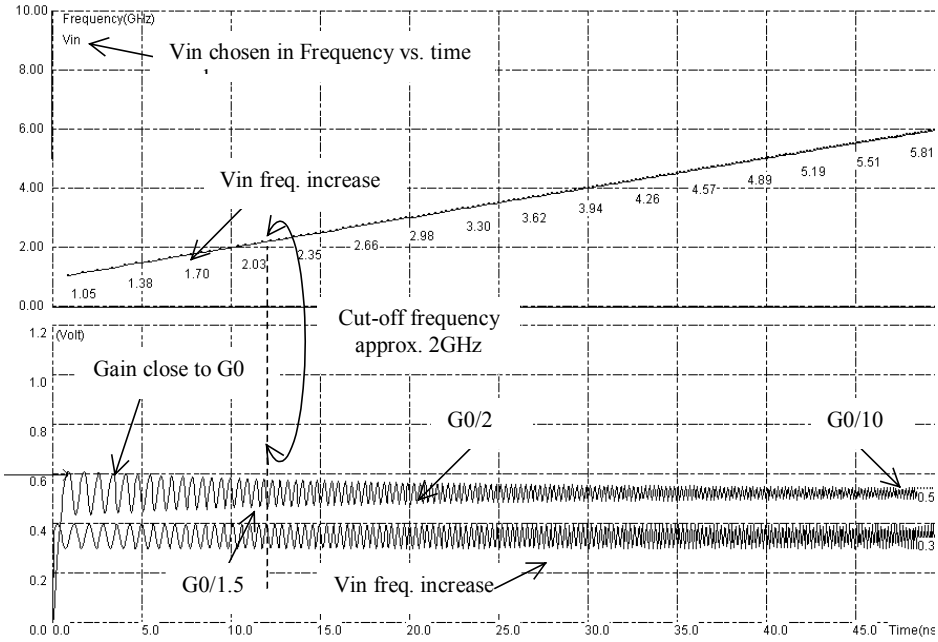


Figure 11-59: Extracting the cut-off frequency from sweep sinusoidal input response (AmpliSingle.MSK)

The Inverter as an Amplifier?

Could the logic CMOS inverter act as an amplifier? Theoretically yes, as the static characteristics of the CMOS inverter are very much like the static response of the basic amplifier described earlier. Using the mode **Voltage vs. Voltage**, we find a gain of 10 for the basic inverter.

To operate in the amplifier zone, we should inject a signal around VDD/2, otherwise there is no chance of taking advantage of the high amplification. The commutation point varies according to the ratio between the nMOS and pMOS size, as illustrated in figure 11-60 where the static characteristics of three inverters are compared. The BSIM4 model is mandatory for reliable simulations.

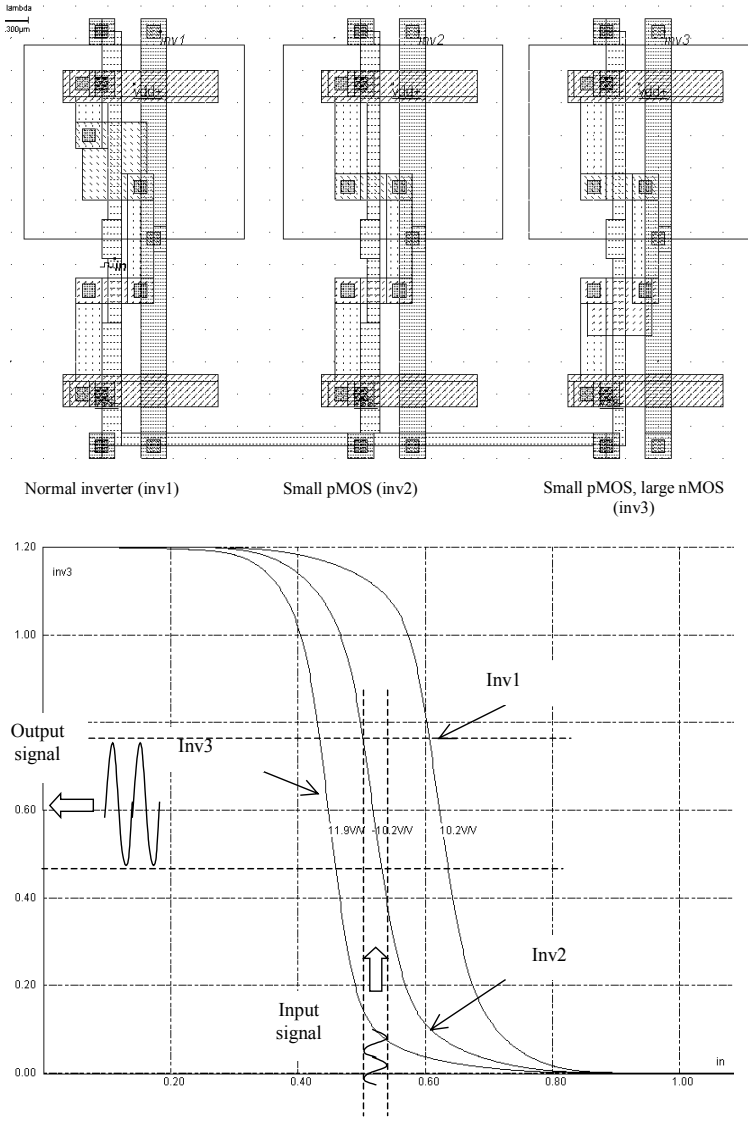


Figure 11-60: Static characteristics of the CMOS inverter in 0.12µm (invAmpli.MSK)

In 0.35µm CMOS technology, the static characteristics of the three inverters exhibit a much higher gain (Figure 11-61). Use the command **File →Select Foundry** and choose **cmos035.RUL** to switch to the 0.35µm technology. Again the BSIM4 model is forced thanks to the label 'BSIM4' in the layout, for accurate results. The measured gain is around 15. As the process parameters are not well controlled, the commutation point of the inverter may fluctuate over a significant range, depending on the location of the die on the wafer, or even on the die itself. As a consequence, placing the input voltage in the exact region of amplification is difficult and requires a specific control circuitry.

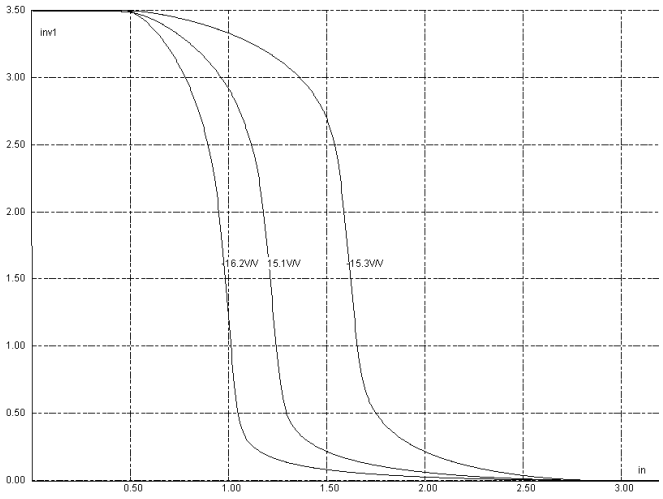


Figure 11-61: CMOS inverter characteristics in 0.35µm exhibit higher gain (invAmpli.MSK)

High gain amplifiers are preferably built from two medium gain stages of amplifiers, rather than one very high gain stage (Figure 11-62). The constraints for the input voltage range are easier to handle in the case of two stage amplifiers. Also, voltages higher than the logic voltage supply are used to increase the voltage range of the circuit. In 0.12µm technology, the majority of analog amplifiers is based on dual-oxide MOS devices, operating at 2.5V.

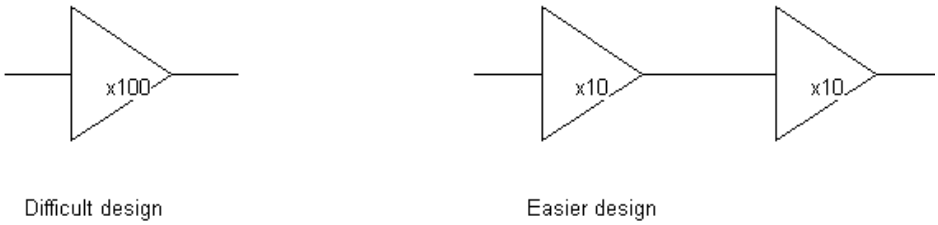


Figure 11-62: High gain is usually achieved by two stages of amplifiers

9. Simple Differential Amplifier

The goal of the differential amplifier is to compare two analog signals, and to amplify their difference. The differential amplifier formulation is reported below (Equation 11-13). Usually, the gain *K* is high, ranging from 10 to 1000. The consequence is that the differential amplifier output saturates very rapidly, because of the supply voltage limits.

$$Vout = K(Vp - Vm) \qquad \text{(Equ. 11-13)}$$

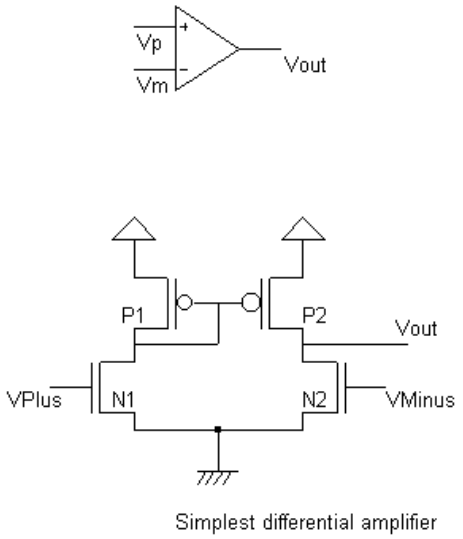
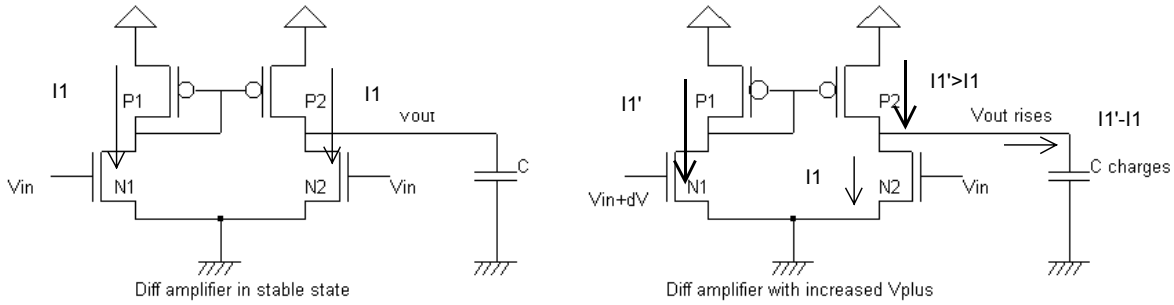


Figure 11-63: Symbol and schematic diagram of the differential amplifier

The usual symbol for the differential amplifier is given at the top of figure 11-63, with its most simple MOS implementation. The differential amplifier principles are illustrated in figure 11-64. We suppose that both *Vp* and *Vm* have an identical value *Vin*. Consequently, the two branches have an identical current *I1* so that no current flows to charge or discharge the output capacitor, which is connected to the output *Vout* (Left figure). Now, if the gate voltage of the *N1* device is increased to *Vin+dV*, the current through the left branch is increased to *I1'*, greater than *I1*. The current mirror copies this *I1'* current on the right branch, so that *I1'* also flows through P2. As the *N2* gate voltage remains at *Vin*, the over-current *I1'-I1* is evacuated to the output stage and charges the capacitor. The output voltage *Vout* rises.



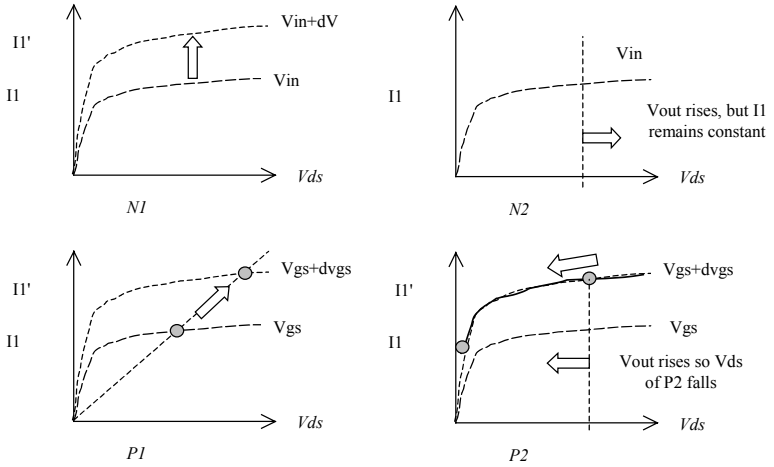


Figure 11-64: The differential amplifier at work (AmpliDiff.SCH)

The process will end when *Vout* is high enough so that *P2* is no more a good current mirror, which means that *I1'* is finally decreased to *I1*. The key idea is that a small variation *dV* of the input voltage is transformed into a huge variation of the output voltage *Vout*, which is the definition of a high gain amplifier.

A Poor Design

A direct translation of the differential amplifier into layout is performed as illustrated in figure 11-65. The differential pair is built from short channel nMOS devices. Their size is kept identical, and drawn with the same orientation, to minimize the offset generated by the transistor mismatch. In the simulation, it can be seen that a 50mV voltage difference between *Vp* and *Vm* is amplified by the circuit. However, the output is very far from saturation. The gain of the circuit is very small. The main reasons are the use of very short channel MOS devices for which the current mirror performances are quite poor, and the high voltage difference between the drain and source of the differential pair which forces the devices to operate at a low performance regime, with several saturation effects.

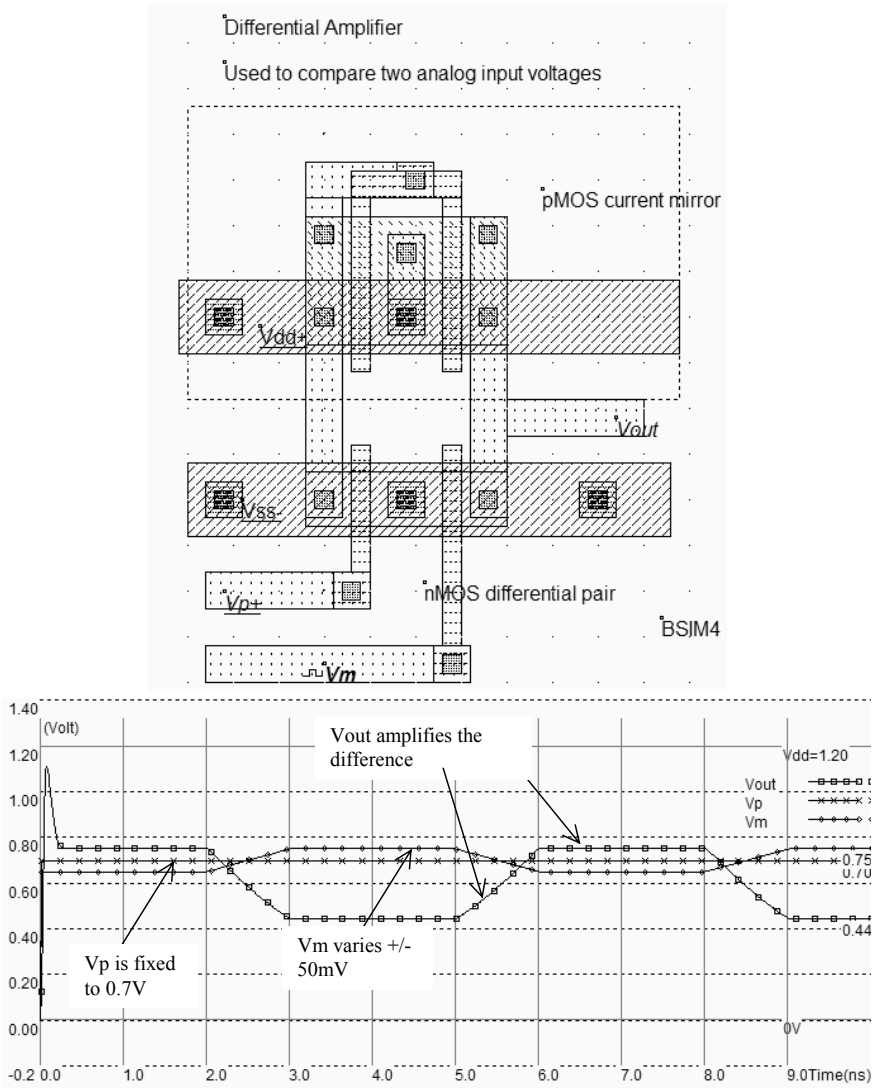


Figure 11-65: Layout and transient simulation of the differential amplifier (AmpliDiff.MSK)

The mismatch between Level 3 and BSIM4 models is quite important in this particular circuit. This is why it is highly recommended to use BSIM4 to simulate properly the performances of analog circuits. Remember that a convenient way of forcing Microwind to use BSIM4 instead of the default Model 3 is to add a text in the layout starting with "BSIM4".

Measure the Gain

The gain of the differential amplifier is the *K* factor appearing in the equation 11-13. This equation is only valid for small differences between *Vp* and *Vm*, otherwise *Vout* saturates near VSS or near VDD.

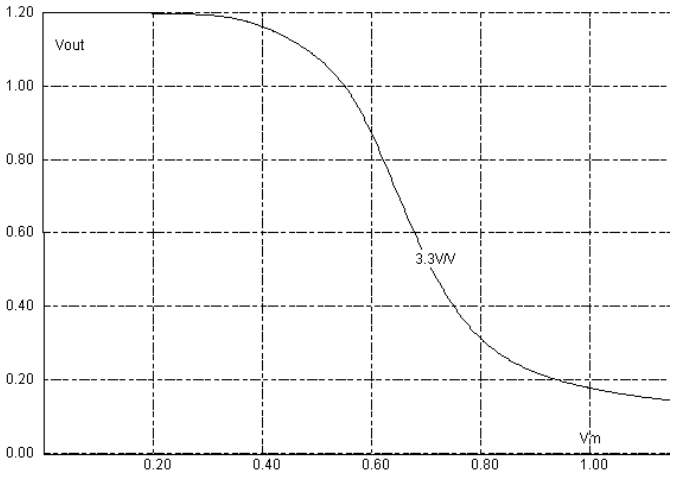


Figure 11-66: Computing the gain of the differential amplifier (AmpliDiff.MSK)

The gain can be computed by Microwind in the Voltage vs. Voltage simulation mode, by selecting the item **Slope** appearing in the menu **Evaluate**. Once the static characteristics of the differential amplifier are obtained, the gain is extracted at the crossing of VDD/2. The gain is very low : 3.3V/V (Figure 11-66).

Improving the Amplifier

The first action consists in the use of long channel MOS device which suffers less channel modulation effects. This is proposed in the layout shown in figure 11-67. The second action consists in inserting an nMOS device between the differential pair and the ground. The gate voltage *Vbias* controls the amount of current that can flow on the two branches. This pass transistor permits the differential pair to operate at lower *Vds*, which means better analog performances and less saturation effects.

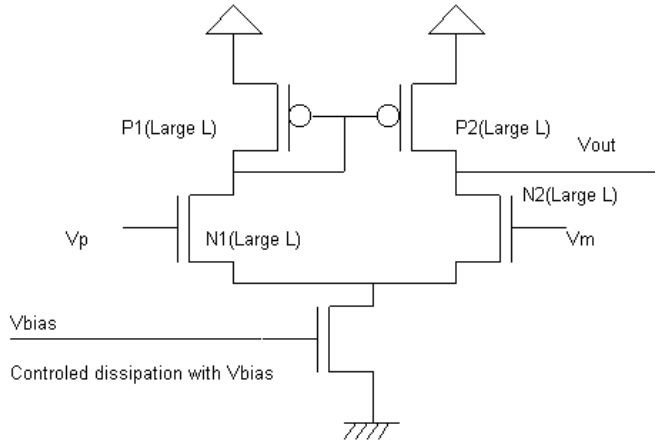


Figure 11-67: An improved differential amplifier (AmpliDiff.SCH)

Find the input Range

The best way to measure the input range is to connect the differential amplifier as a follower, that is *Vout* connected to *Vm*, as shown in figure 11-68. The *Vm* property is simply removed, and a contact poly/metal is added at the appropriate place to build the bridge between *Vout* and *Vm*. The new differential amplifier layout is shown in figure 11-68. A slow ramp is applied on the input Vin and the result is observed on the output. We use again the « Voltage vs. Voltage » to draw the static characteristics of the follower. The BSIM4 model is forced for simulation by a label "BSIM4" on the layout.

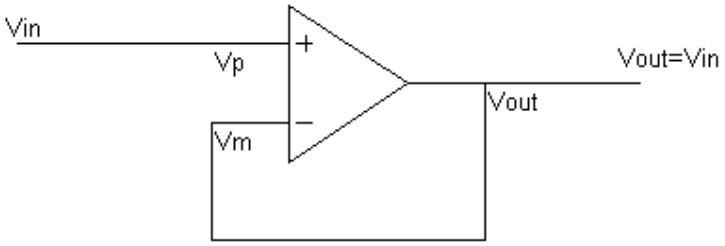


Figure 11-68: The connection between Vout and Vm creates a follower (AmpliDiff2.MSK)

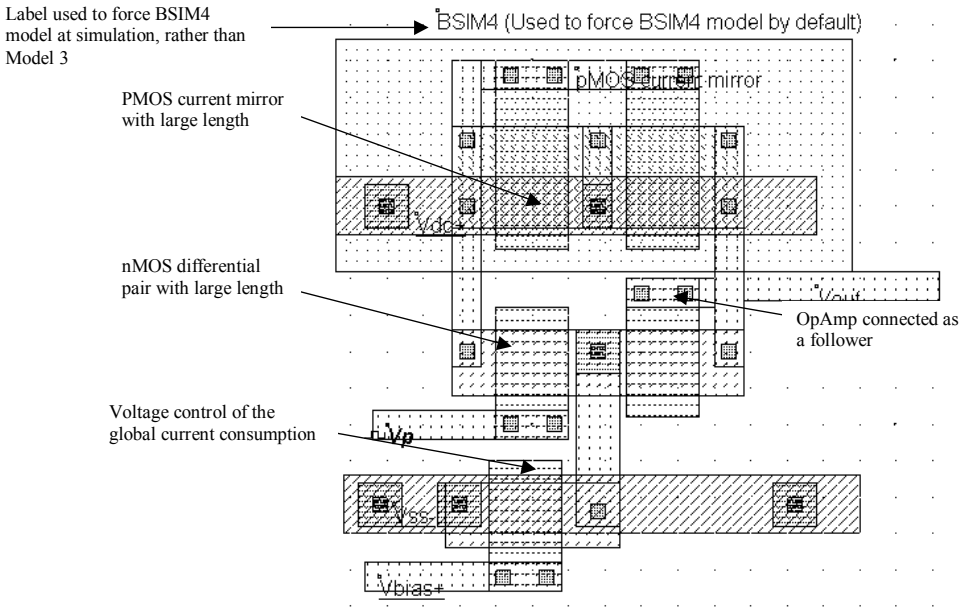


Figure 11-69: The layout corresponding to the improved differential amplifier (AmpliDiffLargeLength.SCH)

One convenient way of simulating the follower response is to assign *Vp* a clock with a very slow rise and fall time. As can be seen from the resulting simulation reported in figure 11-70, a low *Vbias* features a larger voltage range, specifically at high voltage values. The follower works properly starting 0.4V, independently of the *Vbias* value.

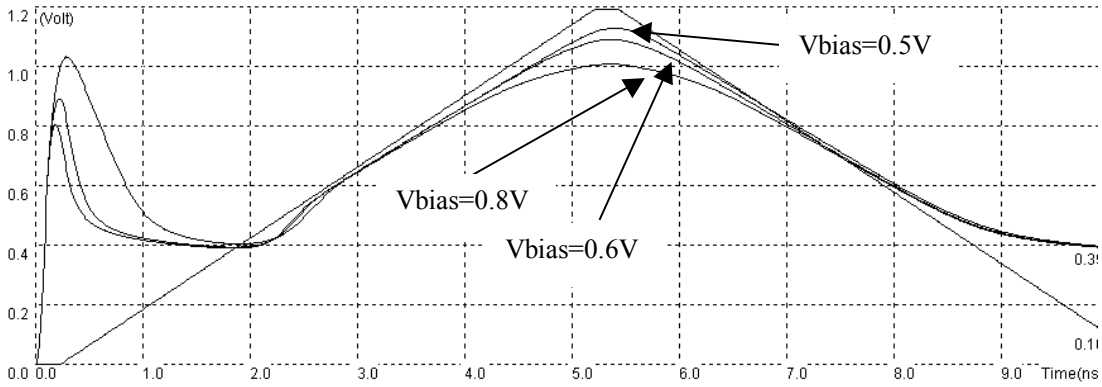


Figure 11-70: Effect of Vbias on the differential amplifier performance (AmpliDiffVbias.MSK)

A high *Vbias* leads to a slightly faster response, but reduces the input range and consumes more power as the associated nMOS transistor drives an important current. The voltage *Vbias* is often fixed to a value a little higher than the threshold voltage *Vtn*. This corresponds to a good compromise between switching speed and input range.

The differential amplifier may be constructed using nMOS devices for the current mirror and pMOS devices for the differential pair. This circuit, proposed in figure 11-71, features a symmetrical behavior, that is a good follower performance for low voltages and an intrinsic limitation near VDD-0.4V.

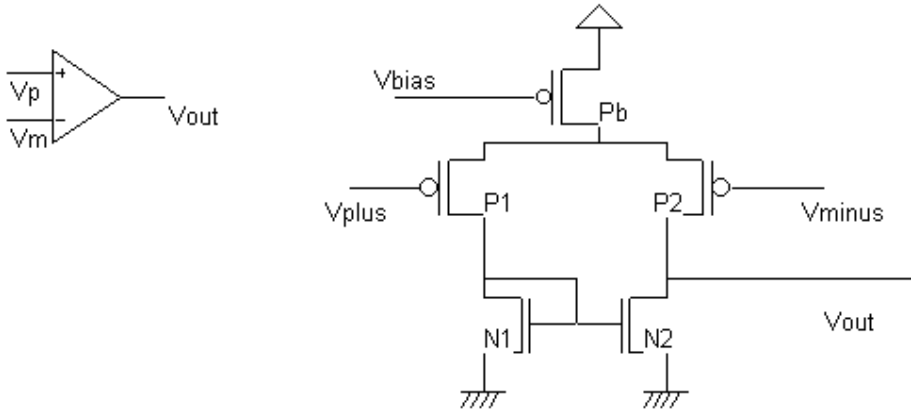


Figure 11-71: A differential amplifier based on a pMOS differential pair and an nMOS current mirror

Double Differential Amplifier

The double differential amplifier is built using the two previous differential amplifiers connected to a common output. This circuit is valid because the output stage works alternatively: one for the high voltages, one for the low voltages. The result, shown in figure 11-72, is quite correct: the follower copies the input with a reduced error, from 0.1V to 1.1V, that is 100mV close to the supply voltage. This amplifier is close to a rail-to-rail operational amplifier that may be found in most CMOS analog cell libraries.

Still the layout is incomplete: neither dummy devices nor proper isolation circuits have been placed. The devices could also be arranged in a more compact way, to decrease the silicon area. Finally, to further decrease the channel length modulation effect, MOS devices with larger length could be used. The speed performances could be kept identical with an increased width, at the price of a larger silicon area.

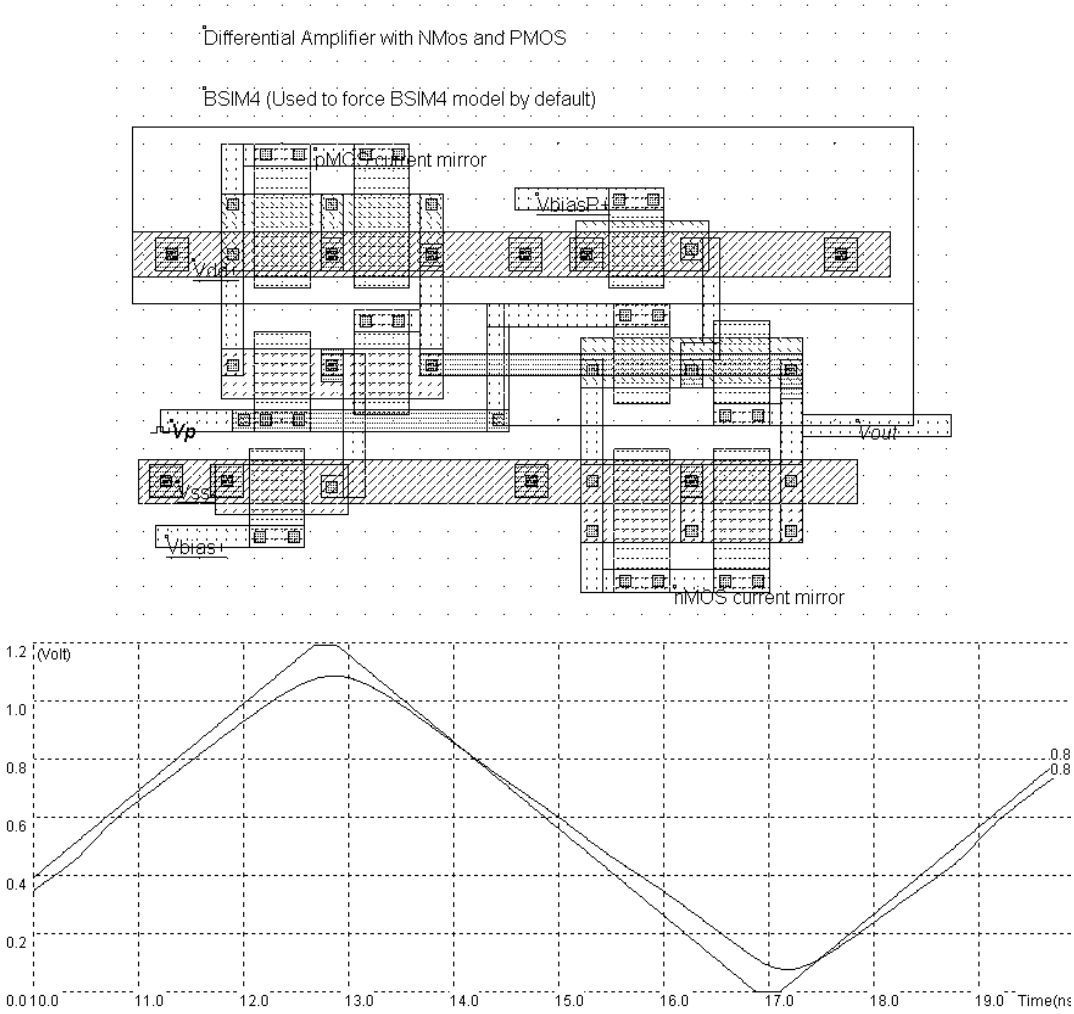


Figure 11-73: Two differential amplifiers with symmetrical structure to enhance performances (AmpliDiffNP.MSK)

Push-Pull Amplifier

The push-pull amplifier is built using a voltage comparator and a power output stage. Its schematic diagram is reported in figure 11-74, with some details about the important voltage nodes. The difference between *Vp* and *Vm* is amplified and produces a result, codified *Vout*. Transistors *Nb* and *Pb* are connected as diodes in series to create an appropriate voltage reference V_{bias}, fixed between the nMOS threshold voltage *Vtn* and half of VDD. The differential pair consists of transistors *N1* and *N2*. This time, two stages of current mirrors are used: *P1, P2* and *P3, PO*.

Node	Description	Typical value
V+	Positive analog input	Close to VDD/2
V-	Negative analog input	Close to VDD/2
Vbias	Bias voltage	A little higher than VTN
Vout	Analog output	0..VDD

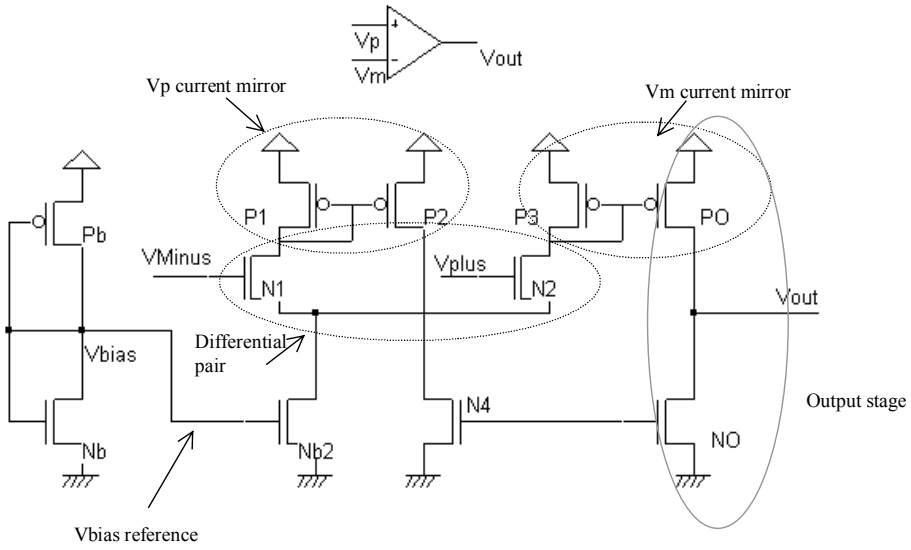
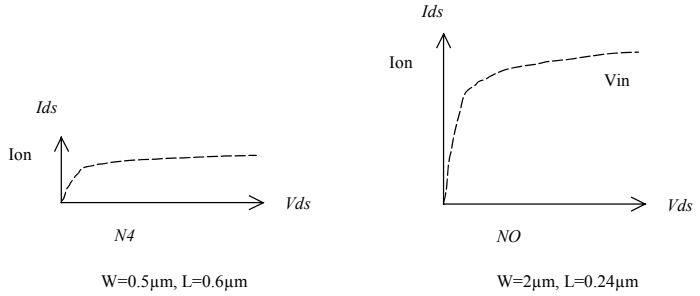


Figure 11-74: Push-pull operational amplifier (AmpliPushPull.SCH)

The output stage consists of transistors PO and NO. These transistors are designed with large widths in order to lower the output resistance. Such a design is justified when a high current drive is required: high output capacitor, antenna dipole for radio-frequency emission, or more generally a low impedance output. The ability to design the output stage according to the charge is a key advantage of this structure compared to the simple differential pair presented earlier.

The implementation shown in figure 11-75 uses NO and PO output stage devices with a current drive around five times larger than the other devices. In practice, the ratio may rise up to 10-20.



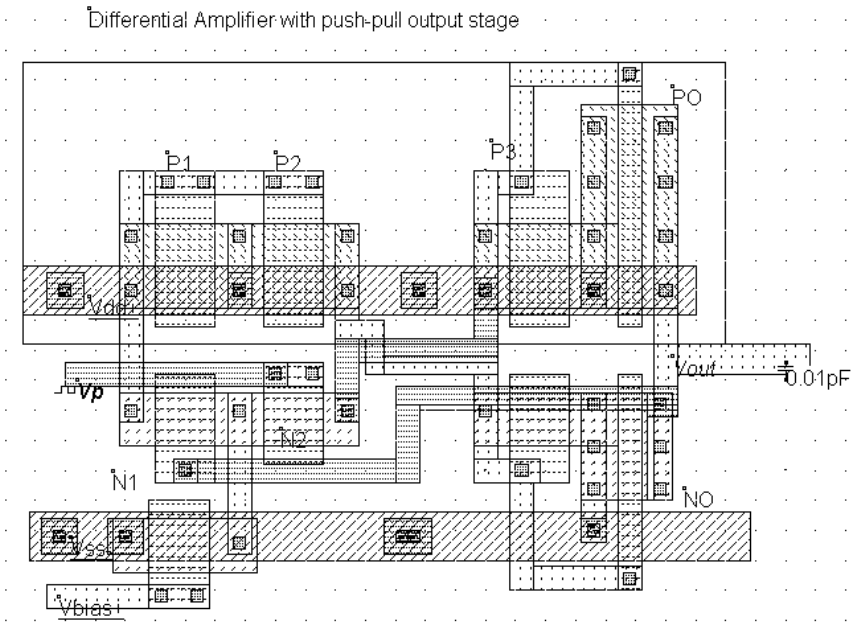


Figure 11-75: Push-pull operational amplifier (AmpliDiffPushPull.MSK)

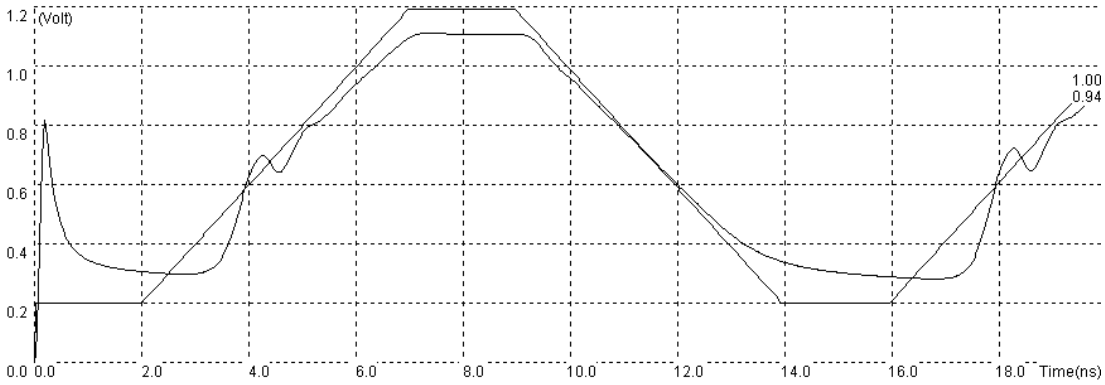


Figure 11-76: Simulation of the push-pull operational amplifier (AmpliDiffPushPull.MSK)

The transient simulation (Figure 11-76) shows an interesting phenomenon called ringing. The oscillation appearing at time 4.0ns is typical for a feedback circuit with a large loop delay and a very powerful output stage. Although an extra 10fF have been added to load the output artificially, its voltage is strongly driven by the powerful devices PO and NO. The oscillation is not dangerous in itself. However, it signifies that the output stage is too strong compared to its charge. If you use the **Voltage vs. Voltage** simulation mode to get the transfer characteristics Vout/V+, you may see the consequence of the oscillation effect : the simulator hardly converges to a stable result. Increasing the precision does not improves the design significantly (Figure 11-77).

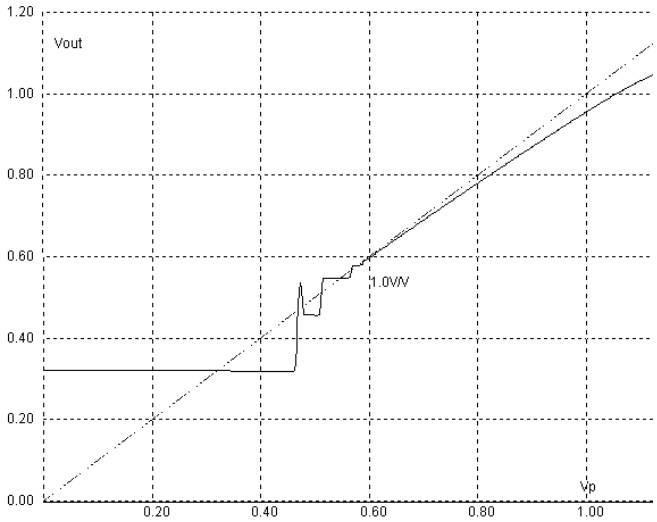


Figure 11-77: The oscillation of the push-pull operational amplifier is also observed when trying to obtain the transfer characteristics of the circuit (AmpliDiffPushPull.MSK)

10. Wide Range Amplifier

An other popular operational amplifier design is shown in figure 11-78. The amplifier is built using a classical voltage comparator and a power output stage similar to the push-pull circuit. However, the pMOS device *PO* has a constant gate voltage, thus acting as a current generator, while the nMOS device *NO* is controlled as seen before.

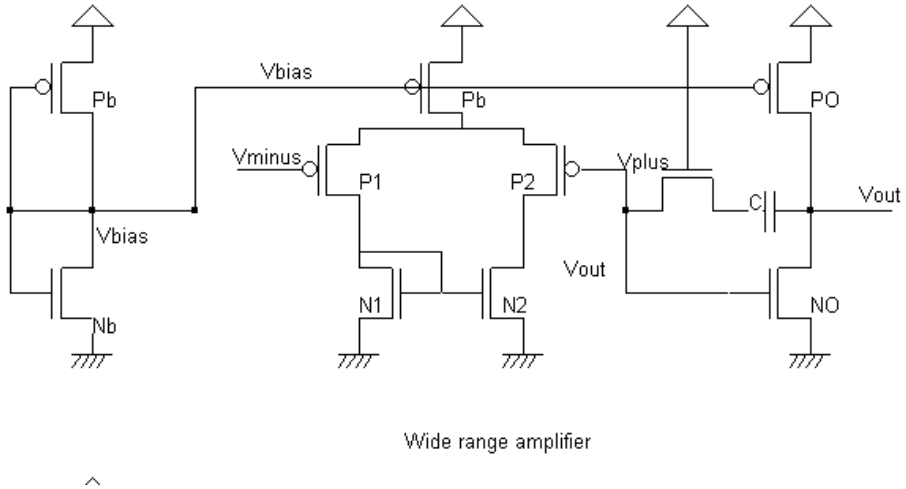


Figure 11-78. Schematic diagram of the wide range amplifier

The circuit shown in figure 11-79 has been implemented in a 0.35µm CMOS process. The corresponding layout is reported in figure 11-80. Not all design rules for a high quality analog design have been observed at that time:

- The orientation of the upper pMOS is not identical. This may impact the quality of the mirror (Design warning 1)
- The differential pairs use channels with minimum length. This increases strongly the second order effects, the offset and non-linearities (Design warning 2)

- No dummy device has been used to improve the quality of the differential pair response (Design warning 3)
- The arrangement is far from being optimal. A lot of silicon area remains unused (Design warning 4)

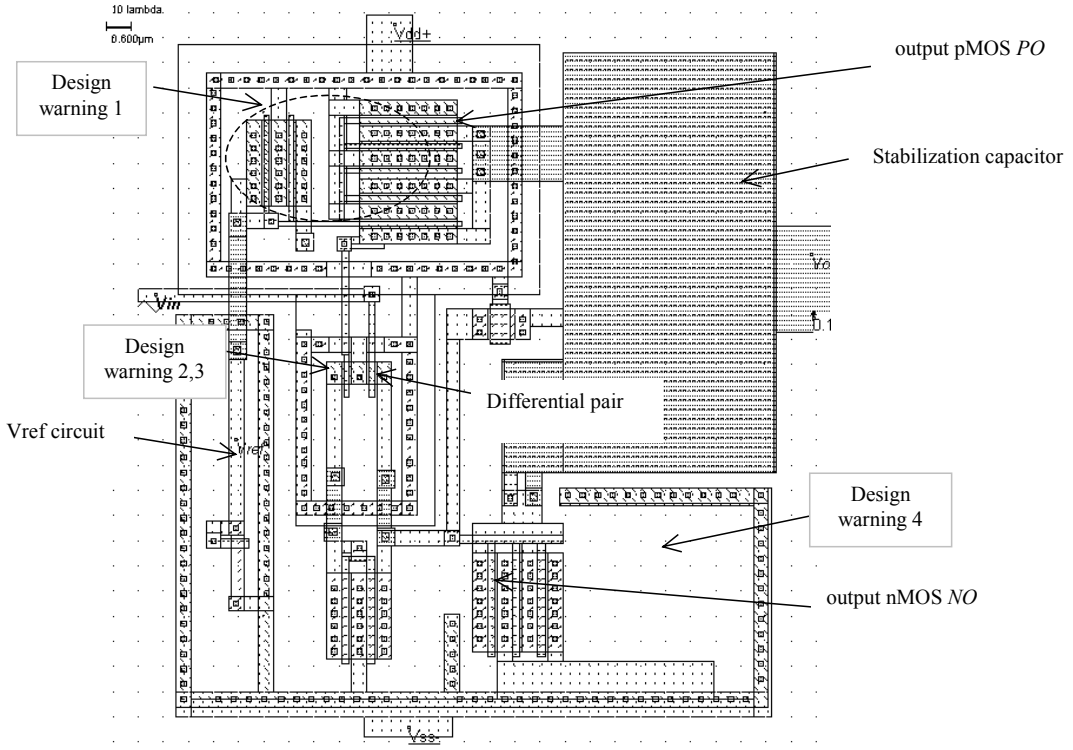


Figure 11-79. Implementation of the wide range amplifier using a 0.35µm CMOS technology (AmpliWide.MSK)

To minimize the parasitic offset, the critical MOS devices (N1,N2, P1 and P2) should be divided into sub-elements N1a,N1b, etc.. and placed in a centroid geometry as illustrated in figure 11-80. Dummy elements are also added around the amplifier. The effects of process non-uniformity are efficiently compensated and parasitic electrical effects are consequently reduced [Haraszti] .

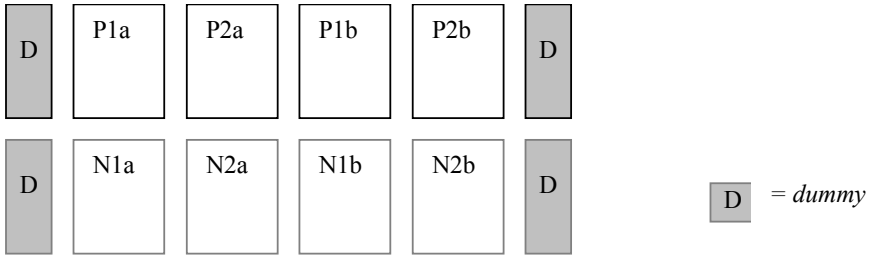


Figure 11-80: Design efforts to limit the impact of process variations on the sense amplifier

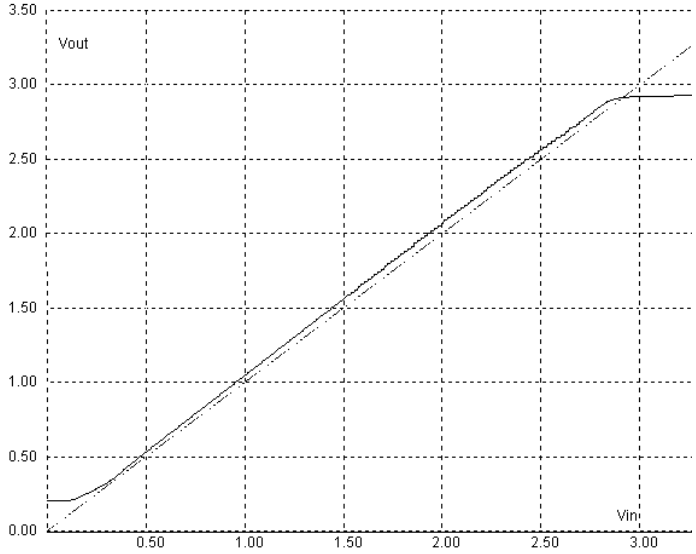
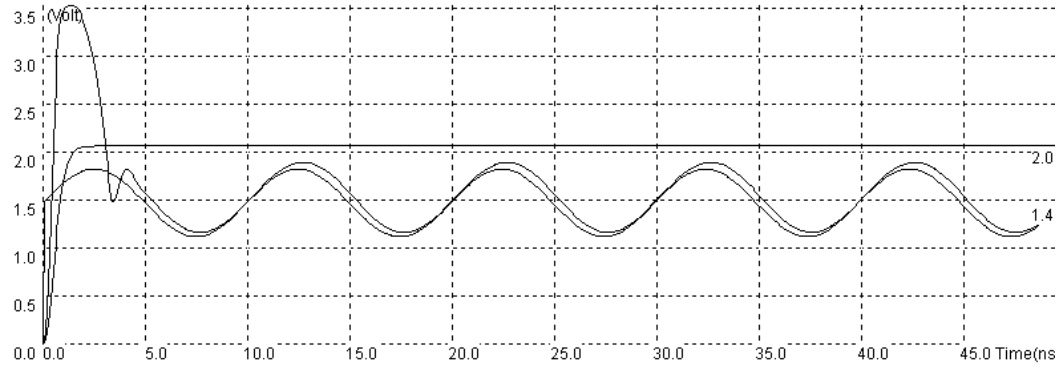
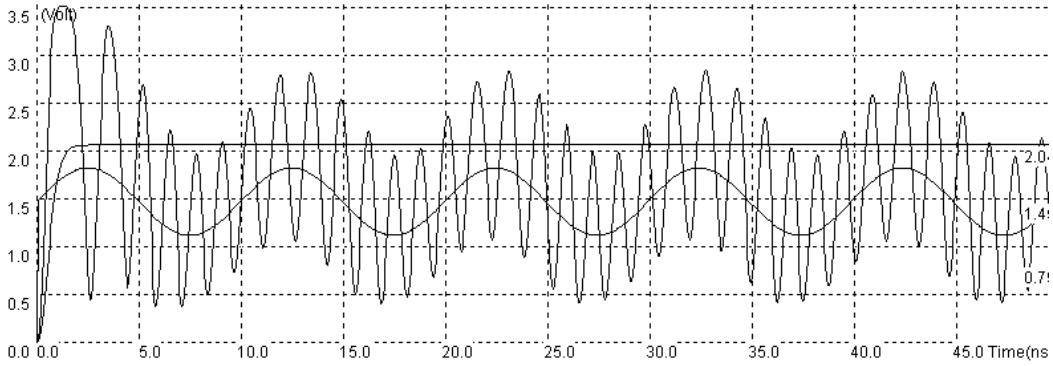


Figure 11-79. Simulation of the wide range amplifier in 0.35µm CMOS technology (AmpliWide.MSK)

The simulation of the wide range amplifier is reported in figure 11-79. It matches very nicely with real case measurements made on a CMOS test chip fabricated in 0.35µm, which included the circuit without any modification, except of course the addition of supply rails and input/output pads.



(*a) With feedback capacitor*



(*b) Without feedback capacitor*

Figure 11-80: The stabilization circuit is required to ensure a correct follower response and avoid instability (AmpliWide.MSK)

It is important to point out that the compensation capacitor has a very important role. When the stabilization circuit is active, we notice almost no ringing effect except at the early stages when the circuit is turned on (Figure 11-80-a). In contrast, if we delete one connection in the stabilization circuit, an enormous ringing effect is superimposed to the output voltage (Figure 11-80-b).

11. On-chip Voltage Regulator

In deep sub-micron technology, the use of very thin gate oxide implies a low supply voltage. This supply decrease is mainly due to the increased risk of damaging the oxide that separates the gate from the drain and source regions, when high voltage differences are present. In contrast, the input/output interface of the integrated circuit must meet standard requirements in terms of voltage, basically 5V or 3.3 V supply. This means that a specific circuit must be designed to generate a low voltage source internally from an external high voltage supply.

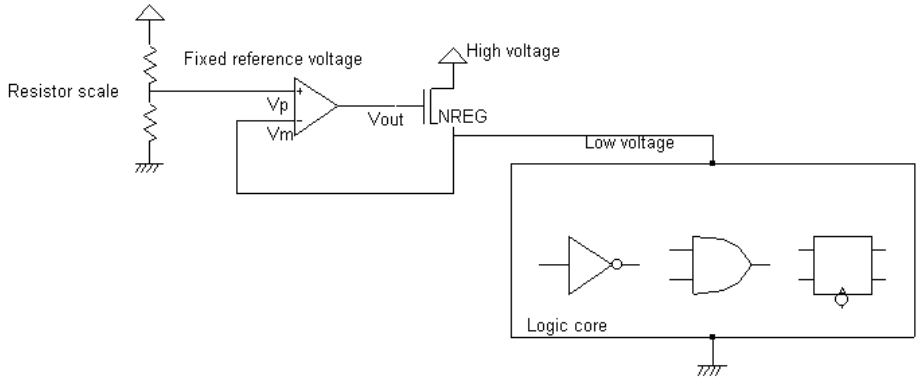


Figure 11-81: Principles of an on-chip voltage regulator based on an operational amplifier

A circuit that realizes the voltage shift is proposed in figure 11-81. The basic idea consists in using an operational amplifier to control the gate of an n-channel MOS device. When the logic core switches, the core voltage connected to *Vm* is lowered. Consequently the operational amplifier tends to increase *Vout,* which reduces the *NREG* device resistance, and increases the voltage until the reference voltage is attained. The negative feedback creates a stable feedback loop to recover from the voltage drops during the switching of circuits.

From a design point of view, the NREG device must be designed very large, even when the supplied logic circuit is small (Figure 11-82). If the equivalent width of the NREG is too small, the gate voltage saturates and the feedback is inefficient. In the case of figure 11-82, the initial design using a width of 100 lambda did not work properly. Using a 200 lambda MOS device, the regulation is effective.

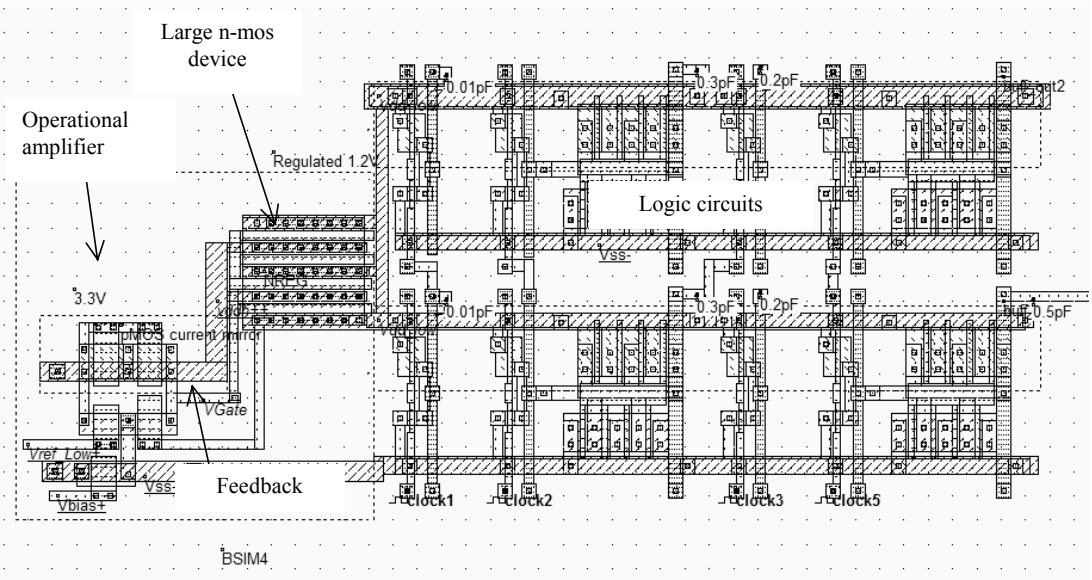


Figure 11-82 : Implementing a small on-chip voltage regulator(Vreg.MSK)

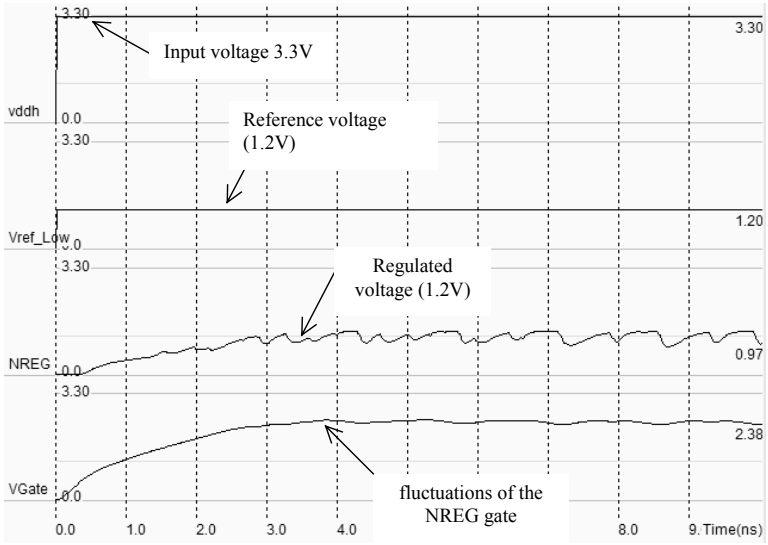


Figure 11-83 : The on-chip voltage regulator at work during multiple transitions of the logic core (Vreg.MSK)

In the example shown in figure 11-83, the voltage *Vref_Low* is fixed to approximately 1.2V. The high voltage supply is 3.3V, which requires high voltage MOS devices for the amplifier and the regulator device *NREG*. When a strong current flows due to concurrent switching in the core, the regulator reacts quite rapidly. In the case of very large logic core, the size of the pass transistor is increased to very impressive values : the combined width may be larger than a millimeter. Such a giant MOS device is obtained by placing MOS gates in parallel. A design example is shown in figure 11-84, which has a width of 1mm, with an *Ion* current around 600mA.

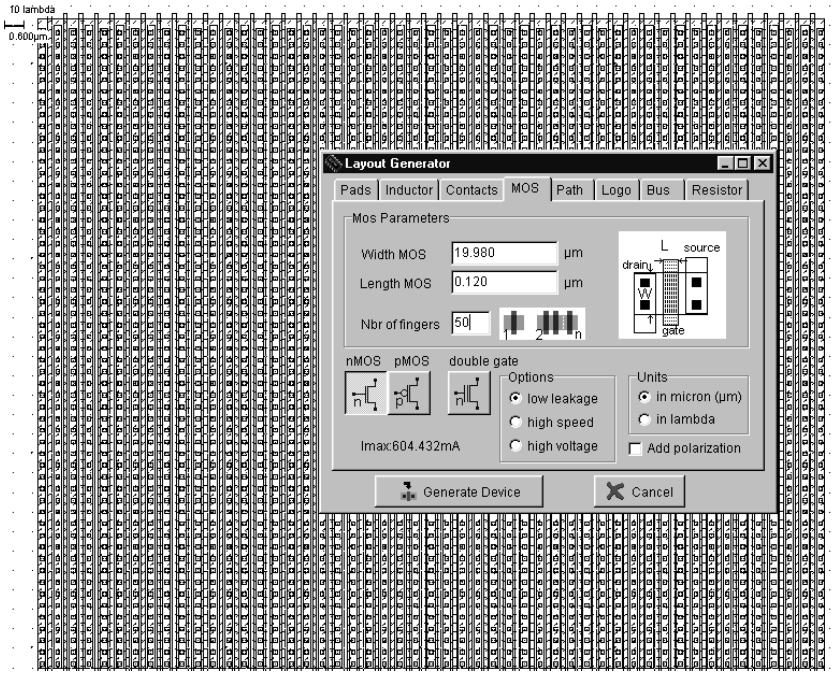


Figure 11-84 : Giant MOS built from MOS devices in parallel, to regulate very high density core circuits (VregBigMos.MSK)

12. Noise

The random motion of electrons in conductors create an unwanted signal called noise. The two major sources of noise in CMOS circuits are the resistors and MOS devices. The thermal noise is a very important parasitic effect in resistor. The parasitic voltage due to thermal noise is shown in figure 11-85. Without thermal noise in resistors, the voltage should be constant. Taking into account the thermal noise, a small random fluctuation is observed.

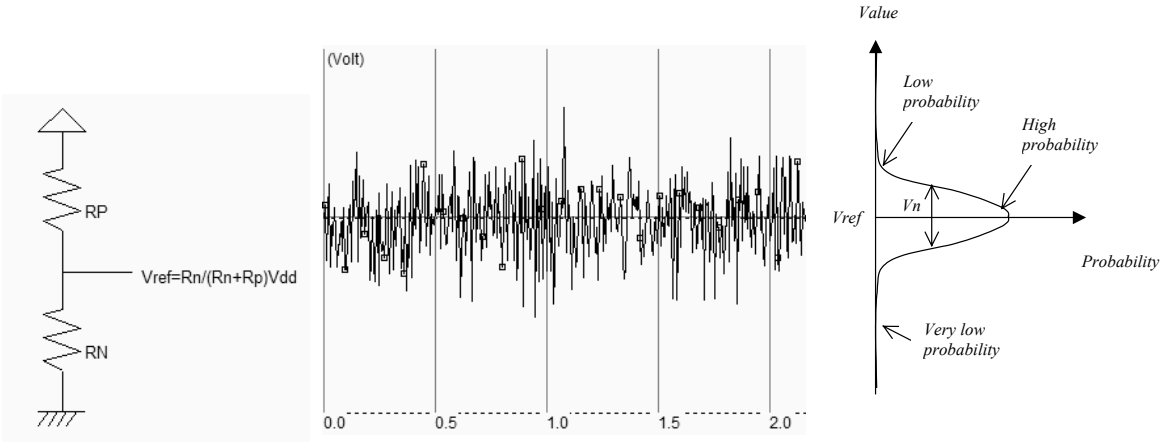


Figure 11-85 : Thermal noise created by large resistances

The voltage oscillates around the desired voltage with a Gaussian distribution. The amplitude of the noise is linearly proportional to temperature and to the value of the resistor. The noise is almost independent of the nature of the resistor material and the frequency.

The signal is not periodic due to its random nature. However, its properties are well predictable when we consider a long time and average parameters. It can be seen in a spectrum analyzer that the energy is homogenously spread over the whole range of measurable frequencies (Typically 1KHz, 10GHz). The thermal noise is considered as a "white noise" by analogy to light where all colors added together create a white color. As the thermal noise is Gaussian distributed, it is called a "Gaussian white noise". Its spectral power density (SPD <gloss>) can be approximated by the following formulation.

$$SPD \approx 4kTR \qquad \text{(Equ. 11-14)}$$

where

k=Boldzmann constant = 1.38 10^{-23} J/K

T=temperature (°K)

R=resistance value (Ohm)

An example of measured noise power density is given in figure 11-86. The thermal noise appears as predicted by the formulation 11-14, at a level approaching 10^{-17} V^2/Hz. A new noise source is also found at low frequencies. The noise is called *1/f* noise as it is proportional to *1/f*. We also observe other important noise around 100MHz, which corresponds to the FM radio emission. Any discrete device with dimensions larger than some millimeter acts as an antenna than captures a small portion of radio-frequancy signals. The same effect is observed in mobile phone bans (900MHz, 1800MHz).

The MOS device has significant serial access resistance on the drain, source, gate and channels. Consequently, the MOS device is also an important source of noise. There is no noise model in Microwind MOS devices. But the noise analysis may be performed in SPICE simulations, as the noise sources and parameters are extensively described [WinSpice].

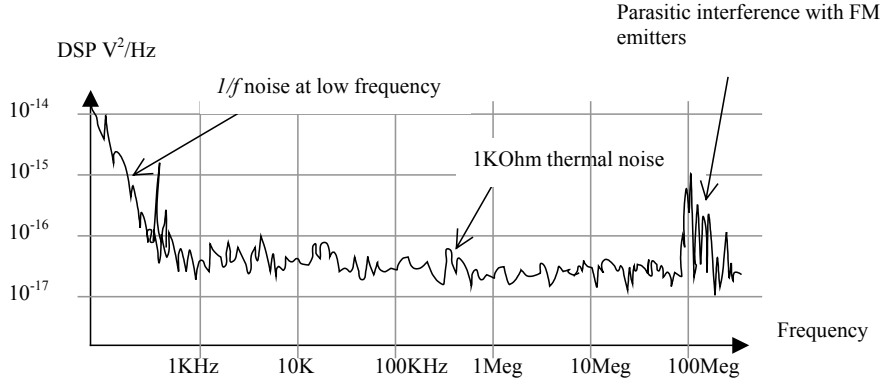


Figure 11-86 : Measured thermal noise on a 10K resistor

Low noise design [Ref book low noise] refers to specific techniques which try to limit the noise effect and its possible consequences on analog signal quality. The most efficient techniques consists in replacing resistors by inductors, by minimizing the values of resistors when such components are absolutely required, and by using MOS devices with large channel length, which have better noise performances than short channel devices.

13. Conclusion

Several aspects of analog design have been described in this chapter. First we detailed the implementation of resistor and capacitor elements. Secondly, we focused on several analog properties of the MOS device, as an analog switch and a high value resistance. We created voltage references, and analyzed the impact of the device size, temperature and shielding. In a third part, the current mirror was presented and simulated. Some guidelines for device matching were illustrated. The transient and frequency characteristics of the single stage amplifier were also studied, and several designs for the differential amplifier were reviewed, including a rail-to-rail amplifier. The gain and input range were characterized for each design. An example of fabricated wide-range amplifier was proposed. Finally, we detailed an on-chip voltage regulator, with a focus on very large MOS devices.

Exercises

Exercise 11.1

Considering the switch N1 off and switch N2 on, what is the value of the inverter output and input? When N1 is turned on and N2 is turned off, what is the value of the output if the input rises from Vin to Vin+dV? We assume an inverter slope with a maximum gain G of -5.

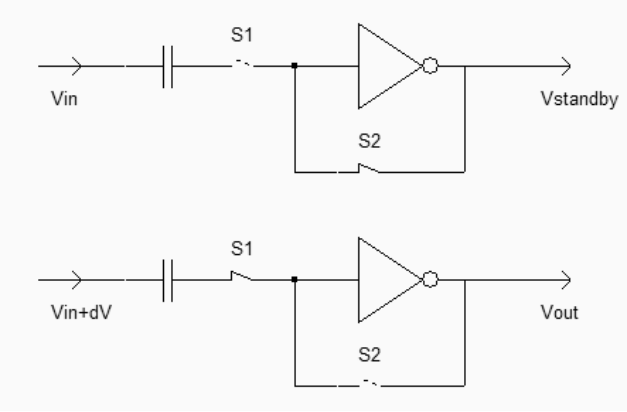


Figure 11-86 : Exercises 11-1

Exercise 11.2

The cascode current mirror [Gregorian p59] has several advantages over the simple current mirror. The output impedance is higher, and the current mirroring capabilities are better in terms of accuracy. The schematic diagram of the cascode current mirror is given in figure 11-87. The disadvantage of the structure is the minimum level of the output voltage which is reduced as compared to the regular current mirror. Design a nMOS or pMOS cascode mirror and compare it to the standard structure.

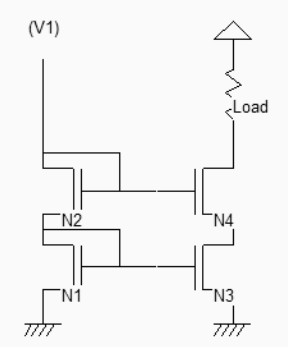


Figure 11-87 : The cascode current mirror

Exercise 11.3

Let us consider the amplifier of figure 11-88 [Gregorian p108].

- What is the typical value for Vo? What is the impact of a change in the voltage Vo?
- If the width of P2 W_{P2} is $10xW_{P1}$, and P3 is $50xW_{P1}$, what is the value of the current flowing through P2 and P3, compared to I1 crossing P1?
- Where are the V- and V+ inputs located?
- What is the role of P4 and P5?
- What is the equivalent function for N1 and N2?
- Locate the two stage output driver.
- Design the operational amplifier and extract the gain.

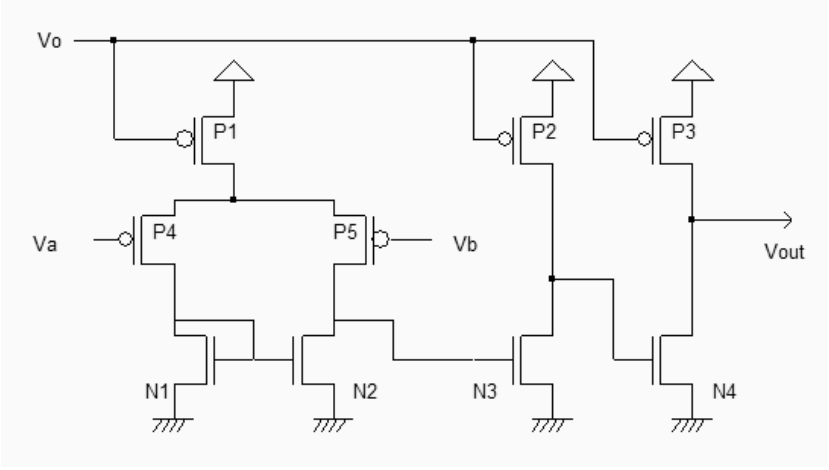


Figure 11-88 : An operational amplifier

[Gregorian p108] has several advantages over the simple current mirror. The output

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[Hastings] Alan Hastings "The art of Analog Layout", Prentice Hall, 2001, ISBN 0-13-087061-7

[Gregorian] tbd

[WinSpice] tbd