

CMOS-COMPATIBLE SURFACE-MICROMACHINED TEST STRUCTURE FOR DETERMINATION OF THERMAL CONDUCTIVITY OF THIN FILM MATERIALS BASED ON SEEBECK EFFECT

Z. Wang^{1,2}, P. Fiorini³, and C. Van Hoof^{3,2}

¹Holst Center/IMEC, Eindhoven, THE NETHERLANDS

²Catholic University of Leuven, Leuven, BELGIUM

³IMEC vzw, Heverlee, BELGIUM

ABSTRACT

This paper reports the design, modeling, fabrication and measurement of a CMOS-compatible surface-micromachined test structure for the determination of the thermal conductivity of thin films based on the Seebeck effect. The Seebeck effect-based temperature sensing is more advantageous for thin film materials with a relatively large Seebeck coefficient, such as lightly doped poly-Si and poly-SiGe. In this paper, the conceptual design is first analyzed and then verified with finite element modeling. The test structure is fabricated with poly-Si_{70%}Ge_{30%}. Its functionality is demonstrated from experimental results. The sources of the measurement error are discussed and the solutions to minimize the measurement error are proposed.

INTRODUCTION

The thermal conductivity of thin film materials, such as polycrystalline silicon (poly-Si) and polycrystalline silicon germanium (poly-SiGe), is an essential material property for both modern very large scale integration (VLSI) circuits and microelectromechanical system (MEMS) devices. The thermal conductivity of thin film sample can be largely different from that of bulk sample [1]. Moreover, the thermal conductivity is strongly dependent on the exact processing condition, because the heat transport is to a large extent determined by various process-related factors, such as the stoichiometry, the crystalline structure and the grain size. These facts highlight the need to precisely measure the thermal conductivity on thin film basis.

To measure the thermal conductivity, the temperature difference, induced by a certain heat flow, across the sample material needs to be measured. Most of the traditional micromachined test structures take advantage of the fact that the electrical resistance of some metals and semiconductors, such as aluminum and poly-Si, changes with temperature [2-5]. The percentage of resistance change per unit temperature difference is denoted as temperature coefficient of resistance (TCR). However, the TCR-based measurement can be complicated by the variable temperature profile in the sample material and by the temperature-dependent parasitic resistance. Moreover, KOH bulk etching is used in the fabrication process of most of the traditional test structures, which prevents or complicates their monolithic integration.

Besides the TCR-based principle, the Seebeck effect [6] can be employed for temperature sensing as well. Because the Seebeck voltage is determined only by the net temperature difference, it is independent from the particular temperature profile. This feature gives an edge to the Seebeck effect-based temperature measurement in terms of accuracy.

This paper introduces a new surface-micromachined test structure based on the Seebeck effect. Its use is especially advantageous for materials with a relatively large Seebeck coefficient α , such as lightly doped poly-Si and poly-SiGe. For these materials, the test structure can be made relatively simple by merging together the heater, the temperature sensor and the sample material. For materials having a relatively low α , such as heavily doped poly-Si and poly-SiGe, the test structure can be employed as well (for details please refer to the DESIGN section). The CMOS-compatible fabrication process of this test structure makes it possible to monolithically integrate it with VLSI circuits or MEMS devices.

DESIGN

The test structure is schematically shown in Figure 1. It essentially consists of two suspended thermocouples, which are connected by a heater, anchored on Si₃N₄-covered Si substrate. As illustrated in Figure 1, the n-type thermocouple legs, devised in meandering shape, are longer and narrower than the p-type thermocouple legs. Metal pads are made at the thermocouple junctions ("A" and "B") for electrical interconnect and on top of the anchors for proper measurement ("C", "D", "E" and "F").

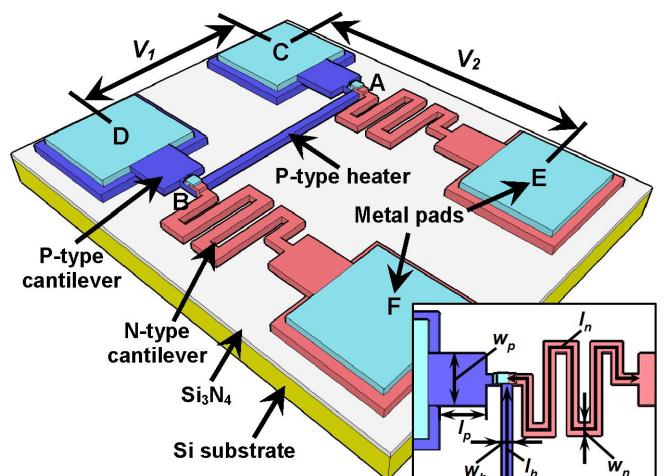


Figure 1: Schematic design of the Seebeck effect-based test structure (not drawn to scale); inset defines the geometries.

To measure the thermal conductivity λ_p of p-type material, an AC square voltage V_1 is first applied between "C" and "D". Due to Joule heating, a heat Q is generated mainly between "A" and "B", because the portion between "A" and "B" is much narrower and longer than the two cantilevers. The value of Q can be roughly calculated from the applied AC voltage V_1 and the measured electrical resistance R between "C" and "D".

The heat flows into the Si substrate, causing a temperature difference ΔT between points “A” or “B” and the Si substrate. This ΔT can be determined by measuring the established Seebeck voltage V_2 either between “C” and “E” or between “D” and “F”, provided that the Seebeck coefficients α_p and α_n for p-type and n-type materials are known. V_2 as a DC voltage can be measured accurately despite the partial superimposition of the AC voltage V_1 onto it. On the other hand, due to the large difference in thermal resistances of p-type and n-type cantilevers, most of the generated heat Q flows through p-type cantilevers into the Si substrate. Thus the thermal resistance R_{th} of p-type cantilevers is expressed as

$$R_{th} = \frac{\Delta T}{Q} = \frac{V_2 R}{V_1^2 (\alpha_p + \alpha_n)} \quad (1).$$

R_{th} is composed of two components: the one-dimensional thermal resistance R_{th_1D} and the spreading thermal resistance R_{th_s} . R_{th_1D} is expressed as

$$R_{th_1D} = \frac{l_p}{\lambda_p w_p t} \quad (2)$$

where l_p , w_p and t denote the length, the width and the thickness of p-type cantilevers, respectively, as shown in the inset of Figure 1. The R_{th_s} arises from the different cross-sectional areas of the heater and the cantilevers. Our case can be simplified as a heat source of isoflux strip attached to an isotropic rectangular flux channel [7]. R_{th_s} is expressed then as

$$R_{th_s} = \frac{1}{\lambda_p \pi^3 \left(\frac{w_h}{w_p} \right)^2} \sum_{n=1}^{\infty} \frac{\sin^2(n\pi \frac{w_h}{w_p})}{n^3} \quad (3)$$

where w_h denotes the width of the p-type heater. From Equation (2) and (3), it can be observed that R_{th} is inversely proportional to λ_p through a constant c , which is determined only by the geometries of the test structure. Thus, R_{th} is rewritten as

$$R_{th} = R_{th_1D} + R_{th_s} = \frac{c}{\lambda_p} \quad (4),$$

$$c = \frac{l_p}{w_p t} + \frac{1}{\pi^3 \left(\frac{w_h}{w_p} \right)^2} \sum_{n=1}^{\infty} \frac{\sin^2(n\pi \frac{w_h}{w_p})}{n^3} \quad (5).$$

Hence, λ_p is obtained as

$$\lambda_p = \frac{c V_1^2 (\alpha_p + \alpha_n)}{V_2 R} \quad (6).$$

The thermal conductivity of n-type material can be measured in the same way on a test structure wherein the p-type and n-type materials are switched over as opposed to the scheme shown in Figure 1. For sample materials having a relatively low α , such as heavily doped poly-Si and poly-SiGe, this test structure can be built in such a way that the short cantilevers and the heater are made with sample material while the long meandering cantilevers are made with another material having a large α . In this case, the heating is implemented in the sample material while the temperature sensing is implemented mainly through the material having a large α .

The rest of this paper is focused on the detailed analysis of a test structure made of poly-Si_{70%}Ge_{30%} deposited by Low Temperature Chemical Vapor Deposition (LPCVD) due to our interest in its thermoelectric properties [8].

MODELING

Finite element modeling (FEM) is implemented to verify the analytical modeling with the software MSC.Marc [9]. The finite element model is shown in Figure 2. Thanks to the structural symmetry, it is enough to model only half of the test structure. An electrical-thermal coupled analysis is performed to simulate the function of the test structure. A current is injected into the middle cross section (“A” in Figure 2) of the p-type heater. At the bottom surface (“B” in Figure 2) of the anchor, the electrical potential is grounded and the temperature is fixed.

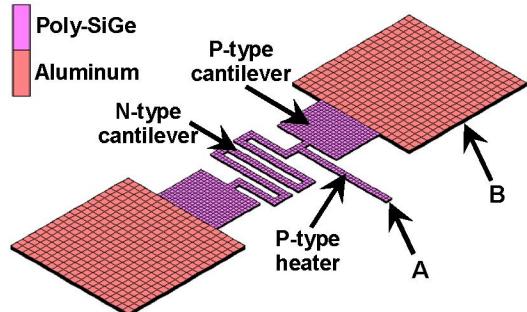


Figure 2: Finite element model for the designed test structure built with MSC.Marc.

The simulated temperature distribution within the p-type cantilever due to Joule heating with the mentioned boundary conditions is shown in Figure 3.

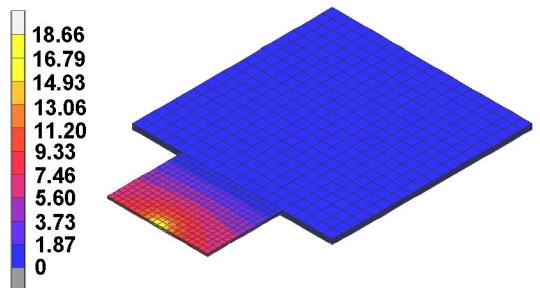


Figure 3: Simulated temperature distribution within the p-type cantilever due to Joule heating. The spreading of heat flow is clearly observed.

Based on FEM result, the thermal resistance R_{th} of the p-type cantilever can be calculated. It is 4.39×10^5 K/W with the assumption that the generated heat completely flows through the p-type cantilever. Calculated with the same set of parameters analytically with Equation (4) and (5), the thermal resistance R_{th} of the p-type cantilever is 4.58×10^5 K/W, which is 4.3% larger than the value obtained from FEM. If the heat loss through the n-type cantilever is considered, the gap between the two values narrows down further to 3.6%. This consistency confirms the correctness of the analytical expressions for the thermal resistance of the cantilever and hence of the value of the thermal conductivity derived from it.

FABRICATION

The designed test structure is fabricated by using surface micromachining technology, as schematically depicted in Figure 4. A layer of 1.2- μm -thick sacrificial SiO_2 is first deposited with Plasma Enhanced Chemical Vapor Deposition (PECVD) and patterned with BHF on Si_3N_4 -covered Si substrate (Figure 4(a)). Then a layer of 1.0- μm -thick p-type poly- $\text{Si}_{70\%}\text{Ge}_{30\%}$ is deposited with LPCVD and patterned by Reactive Ion Etching (RIE) (Figure 4(b)). So is the n-type poly- $\text{Si}_{70\%}\text{Ge}_{30\%}$ layer (Figure 4(c)). To electrically interconnect the p-type and n-type poly- $\text{Si}_{70\%}\text{Ge}_{30\%}$, a layer of 1.0- μm -thick aluminum is sputtered and then patterned with wet etch (Figure 4(d)). Finally, the sacrificial SiO_2 is released in diluted BHF and then dried in critical point dryer (Figure 4(e)).

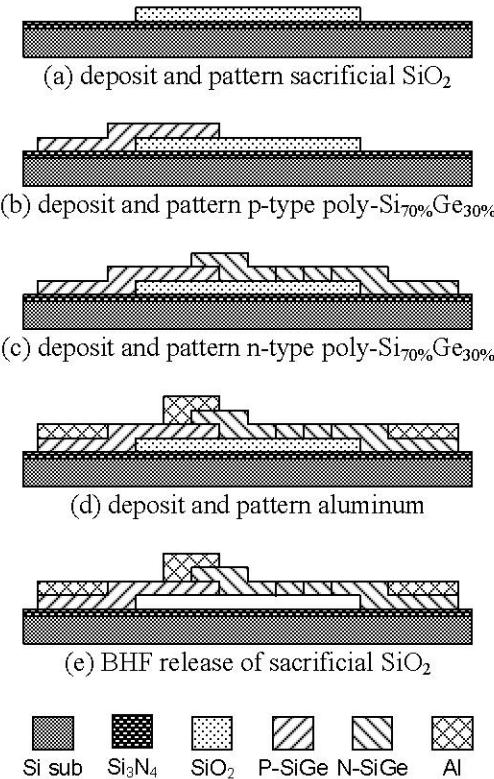


Figure 4: Schematic process flow for the designed test structure (not drawn to scale).

Because no exotic process steps are involved in this process flow, it is completely CMOS-compatible. The fabricated test structures are shown in Figure 5. Each test structure occupies a footprint area of around $200 \mu\text{m} \times 300 \mu\text{m}$. The width of the p-type heater and the n-type

cantilever is variable from $4 \mu\text{m}$ to $10 \mu\text{m}$. From Figure 5(b), it can be clearly observed that the release is complete and moreover, no stiction occurs.

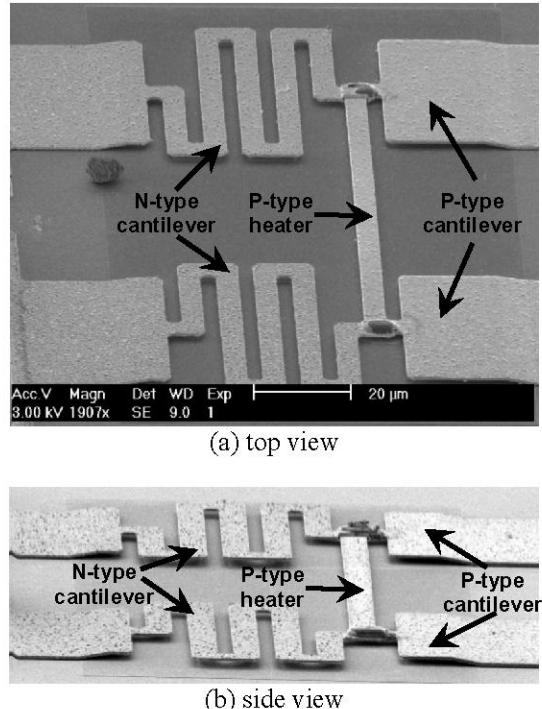


Figure 5: SEM micrographs of the fabricated test structure: (a) top view; (b) side view.

MEASUREMENT

The application of the designed test structure requires *a priori* knowledge of the Seebeck coefficients for the p-type and n-type poly- $\text{Si}_{70\%}\text{Ge}_{30\%}$. This issue is addressed by measuring macroscopic poly- $\text{Si}_{70\%}\text{Ge}_{30\%}$ samples on a custom designed set-up. As shown in Figure 6, the Seebeck coefficients measured at variable temperature differences are about $40 \mu\text{V/K}$ and $190 \mu\text{V/K}$, respectively.

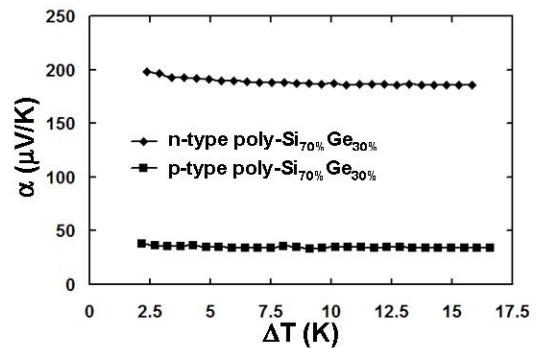


Figure 6: Measured Seebeck coefficients for p-type and n-type poly- $\text{Si}_{70\%}\text{Ge}_{30\%}$ at variable temperature differences.

The thermal measurement is performed in a manual vacuum prober system PMV150 from SüssMicrotec to minimize the thermal loss through air convection and conduction. The experimental vacuum is below 10^{-4} mBar. A function generator is used to apply the AC square voltage V_1 and meanwhile, a Keithley digital multimeter is used to measure the generated Seebeck voltage V_2 . In the experiment, V_1 is increased stepwise from 50 mV to 400 mV. The measured V_2 on a fabricated

