

An Adaptive Beamforming Algorithm based on FPGA synthesis for MIMO Antennas

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Abstract—The Multiple Input and Multiple Output (MIMO) system, combined with adaptive beamforming antenna array technology, is prospective to play a significant role in the 5G wireless system. The objective of the beamforming technique is to steer the beam in the necessary direction and to reduce interference in the other direction using an adaptive filter. This paper aims to incorporate the antenna array system into the hardware. Therefore, the adaptive beamforming algorithm is designed, developed and synthesised using Verilog (VHDL) with the Electronic System Level (ESL) SystemVue software and ModelSim tool. In this paper, with the help of ESL SystemVue software, the intended signal and interfering signals are generated for the Millimeter (mm)-wave frequency, with 8 uniform linear array antennas. These signals are fed to the hardware architecture of the beamforming algorithm. From the result, it is detected that the proposed adaptive beamforming algorithm has better performance when related to the other algorithms.

Index Terms—Adaptive Beamforming, Uniform linear array antenna, Millimeter wave, SystemVue software, Verilog.

I. INTRODUCTION

In 5G networks, the intelligent system plays a vital role to encounter the demands and requirements. Various intelligent techniques are applied to different layers in the networks. Hence, in the forthcoming mobile network, the intelligent antenna is mandatory to improve the system's spectral efficiency. Therefore, intelligent system has drawn abundant attention in the application of signal processing [1] [2]. MIMO system consists of an array of antenna elements with a signal-processing algorithm. This algorithm can identify and suppress the signal in the unwanted direction by the beamforming techniques [3]. Beamforming has wider applications in various technologies such as wireless communications, cognitive communication, acoustics, radar and sonar [4], [5], [6]. The objective of the beamforming technique is to modify the magnitude and phase of each antenna element such that the main lobe is steered in the desired direction and nullifies the side lobes in the interfered direction. The 5G signal uses the beamforming technique to overwhelm the difficulties faced by this signal that includes interference and range restrictions. The beamforming technique is classified into switched and adaptive beamforming. In the switched beamforming technique, the beams are fixed or predetermined therefore, the beams are switched from one to another during the connections based on

the signal strength [7]. The adaptive beamforming approach is based upon the weights which are calculated as an iterative approach so that the maximum radiated power is in the desired direction and suppresses the power in the unwanted direction. This approach is broken into blind and non-blind algorithms. Several standard non-blind algorithms such as LMS, RLS, and NLMS are proposed to improve the signal strength in the intended direction [8].

A. Previous Work on adaptive beamformer

In [9], an efficient hardware realization based on division-free and variable regularized LMS architecture is proposed for generalized side lobe cancel. The author in [10], implemented a multi-stage LMS hardware architecture to achieve better performance when compared to the standard LMS architecture. In the same way, the author in [11], [12] incorporates a two-stage beamformer algorithm by combining the RLS and LMS algorithms in hardware devices for better performance. The drawback in both the multi-stage hardware architecture and the requirement of the computational cost is huge. In [13], a hybrid adaptive beamformer algorithm is presented which consists of a normalized least mean square and normalized constant modulus algorithm to reduce the gain of the side lobe.

B. Motivation

In wireless communication applications, the antenna plays an eminent role as it transmits and receives signals at both ends of the communication system. Therefore, unremitting research is required for antenna design to reduce the interference in wireless communication devices such as mobile or cellular communication, multimedia communication, etc., The essential component for antenna design is the beamformer, which depends on the beamforming algorithm. Implementing beamforming algorithms in hardware devices such as digital signal processors (DSP), field programmed gate arrays (FPGA) or ASIC, but mostly preferred hardware device is FPGA because it has the ability to reconfigurable and simple. From the survey, it was noticed that implementing the beamformer algorithm in hardware devices like Field Programmable gate array (FPGA) has a lot of limitations and is complicated to compute. The key

objective is to reduce hardware computational complexity and offer improved performance.

C. Contribution and Organization

The contribution of this paper is as follows

- The intended and interfering signal is generated in the Keysight's Electronic System Level (ESL) SystemVue software for MIMO antennas.
- The adaptive beamforming model is incorporated in the hardware design.
- The proposed a multistage LMS algorithm with parallel inputs is synthesize and the results were obtained in Xilinx FPGA.

The remaining paper is systematized as Section II - Outlines the signal model and the conventional non-blind Least Mean Square LMS algorithm. Section III - Discuss the proposed hardware architecture for the adaptive beamformer algorithm in FPGA Section IV - Emphasises simulation and synthesis results Section V - Affords the conclusion and imminent work

II. SIGNAL MODEL

This section describes the mathematical description of the intended, interference signal and the conventional LMS algorithm. Consider an M number of antenna elements of Uniform Linear Array (ULA) with identical space of $\lambda/2$ between each antenna element. At discrete intermission of time t , the input vector $X(t)$ is expressed as,

$$X(t) = [x_1(t)x_2(t) \dots x_M(t)]^T \quad (1)$$

$$X(t) = Ad(t) + I(t) + n(t) \quad (2)$$

From the above equation $d(t)$ and $I(t)$ denotes the intended and interfering signal. The intended signal's beam steering vector is then described as A . The beam steering vector A in [14] is expressed as

$$A = [1 + e^{j\omega}, e^{j2\omega}, \dots, e^{j(M-1)\omega}]^T \quad (3)$$

$$\omega = \frac{2\pi D}{\lambda} \sin(\theta) \quad (4)$$

Therefore, the signal wavelength is denoted by λ , D represents distance among the serial antenna elements and the beam-former signal is expressed as

$$y(t) = W^H(t)X(t) \quad (5)$$

Here, $W(t)$ describes the weight vector. In this paper, the key optimization is to measure and minimize the Minimum Mean Square Error (MMSE). Therefore, the error signal is given by,

$$e(t) = d(t) - y(t) \quad (6)$$

Here $y(t)$ is the beamformer signal as expressed in eq. (5) The objective function is to obtain an optimal weight vector of \check{W}

$$\check{W} = E[|e(t)|^2] \quad (7)$$

A. Non-Blind Adaptive Algorithm – Least Mean Square (LMS) Algorithm

Utilizing the steepest descent optimization technique, the least mean square (LMS) algorithm reduces the mean square error (MSE) as follows [15], [16]:

$$e(t) = d(t) - y(t) \quad (8)$$

$$W(t+1) = W(t) + \mu X(t)e^*(t) \quad (9)$$

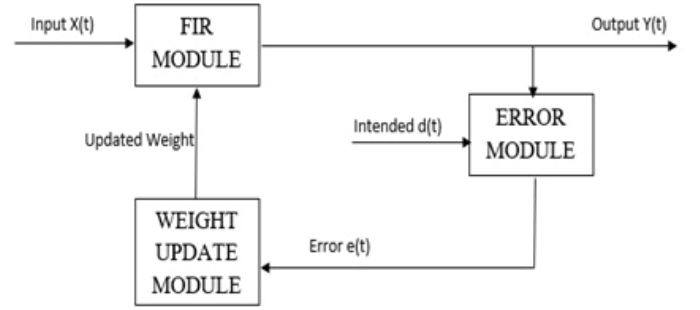


Fig. 1. Block diagram of Adaptive Beamformer

The output $y(t)$ is given by

$$y(t) = W^H(t)X(t) \quad (10)$$

The Fig. 1 describes the simple LMS mechanism, which consists of 3 modules. For output calculation, the 2 major modules are weight updation and error computation modules. The mechanism used for weight updating is multiplication, in other words, LMS algorithm is simply a MAC operation. Therefore, implementing this algorithm in hardware is a single-cycle computation.

III. HARDWARE ARCHITECTURE

In digital signal processing, implementing the adaptive filter architecture involves more area for the operations of digital multiplications. Thus, the computational complexity is large. Therefore, this paper proposed low computational complexity architecture for adaptive beamformer using 2 stage algorithm.

The proposed 2-stage non-blind adaptive beamformer using LMS is enlightened in Fig. 2. The input for both the stage of LMS is the intended and the input signal. In each stage of LMS, the input signal is multiplied by the complex weight to produce a beamformer signal. The error signal from each stage is obtained by subtracting the beamformer signal of each stage from the intended signal. The output error signal is derived as a composite of the individual stage in the parallel operation of 2 LMS stages. The error signal from the first stage is combined with that of the error signal from the second stage LMS, which is multiplied by the j . where j is the imaginary number of values $\sqrt{-1}$. The signal to both the stage LMS are the same. The intended signal and the input signal is denoted by $d(t)$ and $X(t)$ respectively.

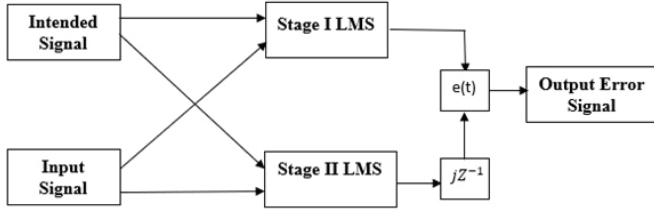


Fig. 2. Proposed 2-stage adaptive beamformer

Stage:1 LMS

$$y_1(t) = W_1^H(t)X(t) \quad (11)$$

$$e_1(t) = d(t) - y_1(t) \quad (12)$$

$$W_1(t+1) = W_1(t) + \mu X(t)e_1^*(t) \quad (13)$$

Stage:2 LMS

$$y_2(t) = W_2^H(t)X(t) \quad (14)$$

$$e_2(t) = d(t) - y_2(t) \quad (15)$$

$$e(t) = e_1(t) - je_2(t-1) \quad (16)$$

$$W_2(t+1) = W_2(t) + \mu X(t)e_2^*(t) \quad (17)$$

where,

$y_1(t)$ - represents the beamformer signal

$e_1(t)$ - denotes error signal

$W_1(t)$ - denotes complex weight vector for stage I LMS

$y_2(t)$ - represents the beamformer signal

$e_2(t)$ - denotes error signal

$W_2(t)$ - denotes complex weight vector for stage II LMS

IV. SIMULATION AND SYNTHESIS RESULTS

The simulation setting and inputs for the hardware implementation of the adaptive filter were created using the ESL SystemVue software and synthesised in ModelSim software using Verilog HDL. The training data (input signal) and the intended signal for the adaptive filter architecture are generated using Keysight's Electronic System level SystemVue software. The uniform linear array antenna of 8 antenna elements. The intended and interfering signals are modulated with a 16 QAM with transmitting power of 37 dBm.

The simulation is executed in System Vue software and obtained the intended and interfere signal. Using this signal, a Verilog code is developed and synthesised in ModelSim software and parameters such as area, power and delay are calculated using Xilinx ISE software. Assume that the intended and interfere signal are at 30° and 45° respectively.

With the help of Electronic System Level SystemVue software, the beam radiation pattern simulation output is presented, in Fig. 3 to illustrate the beam directivity. The beam directivity represents that the beam radiated at the intended user i.e., 30° while nulling the other interfering signals.

The above Table 2 shows the comparison of resource utilization for various algorithms. From table: 2 it is observed

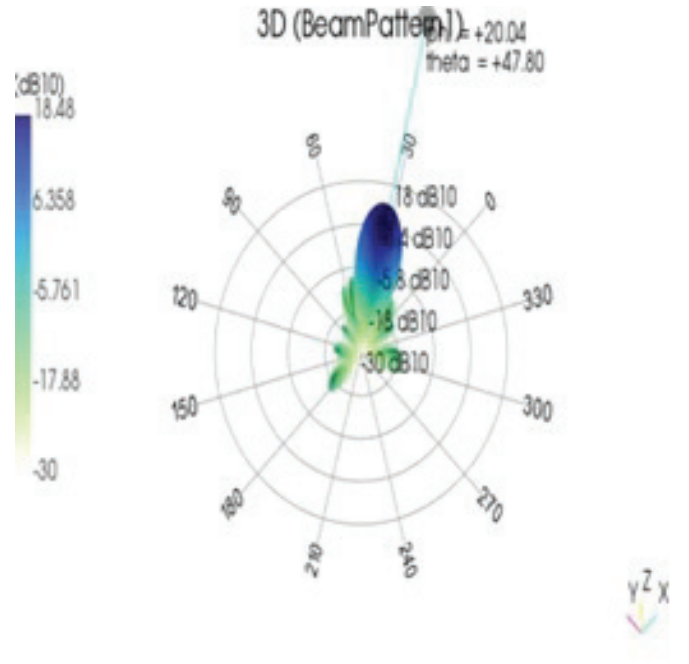


Fig. 3. 3D Beam pattern of Adaptive Beamformer

TABLE I
SIMULATION PARAMETERS IN SYSTEMVUE SOFTWARE

Parameters	Values
Array Elements	8
Antenna Spacing	$\lambda/2$
Digital data type	16 QAM
Frequency	28 GHz
Desired Angle	30°
Interfere Angle	45°

that the RLMS and LLMS algorithm requires $M+1$ and 1 complex division respectively whereas the proposed algorithm requires zero complex division. Therefore, the computation complexity is less in the proposed algorithm.

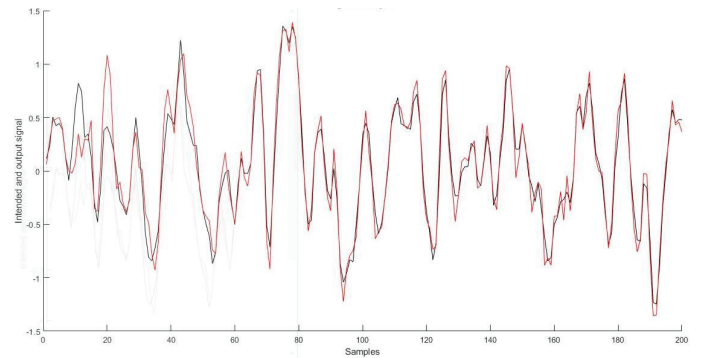


Fig. 4. Intended and Output Signal for 200 samples

Fig. 4 and Fig. 5 represents the comparison of the intended and output signal for 200 and 500 samples. The blue and red colour represents the intended and output signal respec-

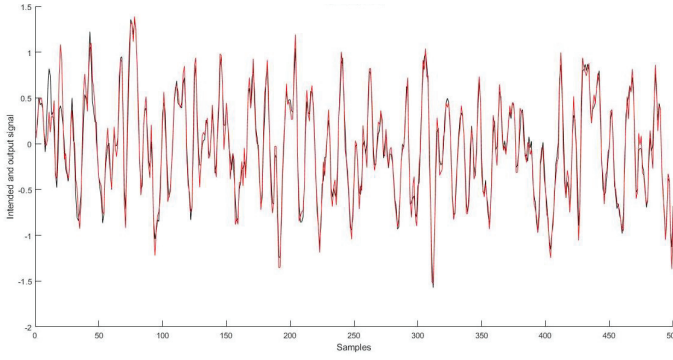


Fig. 5. Intended and Output Signal for 500 samples

TABLE II
RESOURCE UTILIZATION

Algorithm	Complex multiply	Complex add	Complex divide
RLMS [11]	$3M^2 + 11M + 2$	$2M^2 + 9M + 6$	$M + 1$
LLMS [12]	$6M + 2$	$5M + 4$	1
Proposed	$4M + 2$	$4M + 4$	0

tively. Table 3 shows the synthesis results of the proposed beamformer architecture. The 8 - bit beamformer architecture was developed into Verilog HDL by considering the input and the intended signal generated from the ESL System Vue software. Using Xilinx ISE software, the Verilog HDL is synthesised to evaluate the area, power and delay for the proposed architecture in FPGA. The overall 8 - bit beamformer architecture achieves a delay of 1.602 ns, the number of slices LUTs as 135 and power of 3.300W with the help of Xilinx ISE software.

V. CONCLUSION

In smart antenna systems, adaptive beamforming is become an inevitable feature for the future wireless communication system as it reduces spectral congestion both at the signal reception as well as at the transmission side. When adaptive algorithms are used on dedicated, limited resource devices, like as Field Programmable Gate Arrays (FPGA), the rise of internet-connected devices has drained spectrum resources and put difficult limits on it. These limitations may be seen in the system's requirements to achieve fast convergence and excellent precision while preserving a low complexity design. Therefore, the proposed adaptive algorithm for beamforming is well suited for a hardware implementation. Because of its low-complexity and $O(N)$ structure, where N signifies the number

TABLE III
SYNTHESIS RESULT

Parameters	Proposed adaptive beamformer
Number of Slice Registers	326
Number of Slice LUTs	135
Number of Occupied Slices	101
Number of IOBs	26
Delay (ns)	1.602
Power (W)	3.300

of antenna elements. Synthesis outcome illustrate that the proposed adaptive beamformer architecture achieves a delay of 1.602ns, the Number of Slice LUTs as 135, and a power of 3.300W. At last, the future work is to increase the antenna element.

VI. ACKNOWLEDGEMENT

The All India Council for Technical Education (AICTE), New Delhi, India, is funding this research project under RPS-NDF (grant no. 8-3/RIFD/RPS-NDF/Policy-1/2018-2019).

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