UCSB ECE 274 – Winter 2025

Assignment 2: Verilog Design and Simulation of Leaky Integrate-and-Fire Neurons

Total Points: 100

Due at 5pm, Friday, Feb 14 (no late submission)

1. Background

In this assignment, you will build a model of LIF (Leaky Integrated-and-Fire) using Verilog. The discretized model with a zero-th order synaptic model that you will implement in Verilog is as follows:

$$V_i[t_k] = V_i[t_{k-1}] + K_{syn} \sum_{j=1}^{M} w_{ji} \cdot S_j[t_{k-1}] - V_{Leak} \quad (1),$$

where V_i is the membrane potential of neuron *i*, *M* is the number of pre-synaptic neurons connected to neuron *i*, K_{syn} is the synaptic weight parameter, w_{ji} is the synaptic weight between neurons *j* and *i* (neuron j is the pre-synaptic neuron connected to neuron *i*), S_j is the indicator function that indicates whether neuron j fired (S_j will be 1 if neuron j fired and otherwise 0), and V_{Leak} is the leaky parameter.

In this assignment, suppose that the network consists of one post-synaptic neuron and three pre-synaptic neurons with the following setting:

$V_i[t_0] = V_{rest}$(*resting membrane potential*) = 6, V_{Leak} = 1, w_{1i} = 1, w_{2i} = 2, w_{3i} = 3, K_{syn} = 1, V_θ(*threshold voltage*) = 14. All parameters are normalized and ready-to-use. Note that the lowest possible membrane potential is constrained to V_{rest} at all times. This means that input excitations or leakage shall not be applied in such a way to bring membrane potential to below V_{rest}.

Based on the pre-synaptic spikes generated by the three pre-synaptic neurons, you shall show the corresponding waveforms of $V_i[t]$ and the output firing spikes. Recall that when $V_i[t] \geq \theta$, you shall set $V_i[t]$ to V_{rest} and produce an output spike at the same time.

2. Problem and Credit Breakdown

For the following experiments, set your clock cycle to 10ns (i.e. $t_k - t_{k-1}$ = 10ns = one clock cycle). Each discretized time point occurs at every rising edge of the clock. You can use up to two 'always @' blocks in your Verilog design.

For each of the four following sets of pre-synaptic firing sequences, you shall generate the corresponding **waveforms** of:

1) $'V_i[t]'$

2) Output spike trains of neuron *i* (output waveform of post-synaptic neuron *i*)

and report the above in your report.

(1) Pre-synaptic firing sequences:

The 1st neuron : 1111100111110011111001111001111100

The 2nd neuron : 1111100111110011111001111001111100

The 3rd neuron : 1111100111110011111001111001111100

(2) Pre-synaptic firing sequences:

The 1st neuron : 1111100111110011111001111001111100

The 2nd neuron : 1111100111110011111001111001111100

The 3rd neuron : 0000011000001100000011000000110000011

(3) Pre-synaptic firing sequences:

The 1st neuron : 0000011000001100000011000000110000011

The 2nd neuron : 0000011000001100000011000000110000011

The 3rd neuron : 1111100111110011111001111001111100

(4) Pre-synaptic firing sequences:

The 1st neuron : 0000000000111110000000000111110000 0

The 2nd neuron : 0000011111000000000011111000000000

The 3rd neuron : 1111100000000000111110000000000011111

Note that in the above, the presynaptic (input) sequences are specified over 35 steps starting from time step 1 (the beginning of simulation) to time step 35. Since the forward Euler rule, i.e. (1), is used to emulate the behavior of the output neuron, you shall report output neuron membrane potential and firing activities from time step 2 to time step 36 and properly label the time in your submitted waveforms.

Hints: Below are some hints regarding how you may choose the bit resolutions for different parameters. You don't have to follow the specific numbers below exactly; you shall choose the right bit resolutions that are appropriate for the ranges of the parameters under consideration.

$V_i[t]$: 5 bits: For example, since $V_\theta = 14_{(10)} = 1110_{(2)}$, 4- or more bits would be used for $V_i[t]$.

Pre-synaptic firing sequence: 35 bits

What to submit:

A report including:

1) The waveform of '$V_i[t]$'
2) The waveform of output spike trains of neuron *i* (spike trains of post-synaptic neuron *i*)
3) A high-level description of your design

Verilog code and testbench

Credit Breakdown

- Quality of the report & Verilog code, test bench: 20 points
- Correctness of each simulation: 20 points each; 80 points total

Submission Note

To complete this assignment, prepare three files: 1. report in PDF, 2. Verilog file, 3. Testbench file, and then zip them into a single file for uploading to Canvas.