MEMORY DESIGN PRESENTATION

Group - 10
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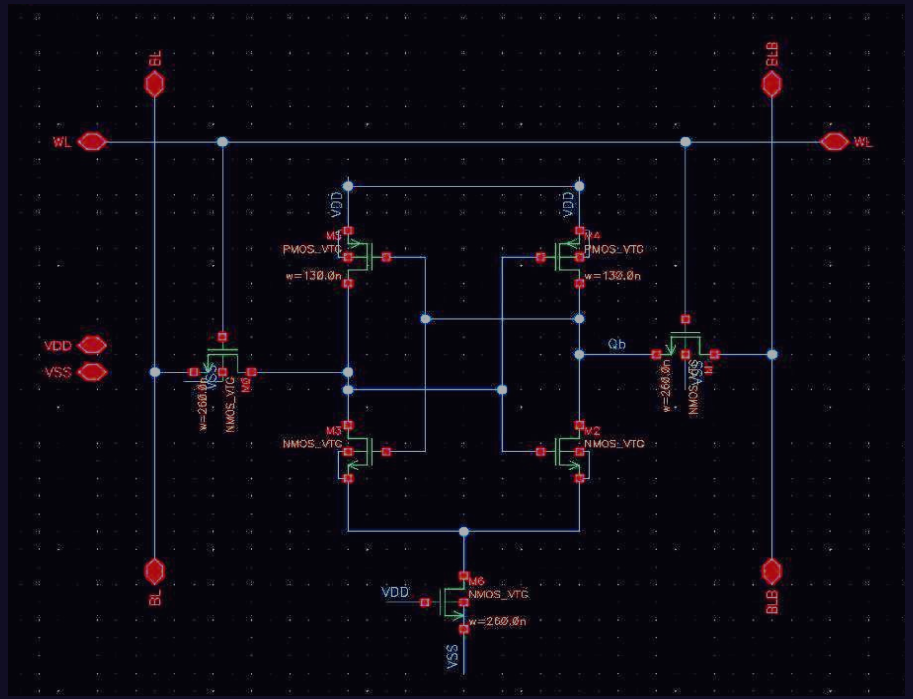
TABLE OF CONTENTS

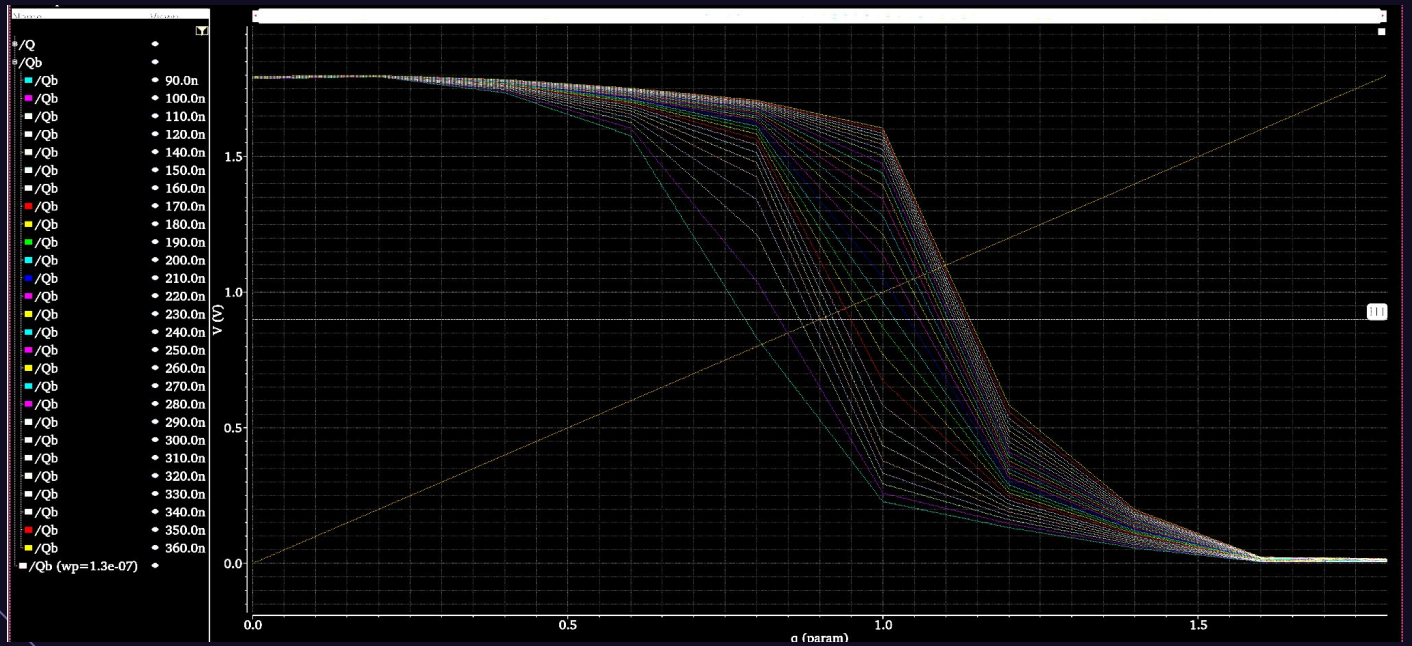
Gated V_{DD} 7T SRAM CELL

- Reduced leakage power losses
- Disable the supply voltage (VDD) when the SRAM cell is not in use thereby eliminating any leakage current



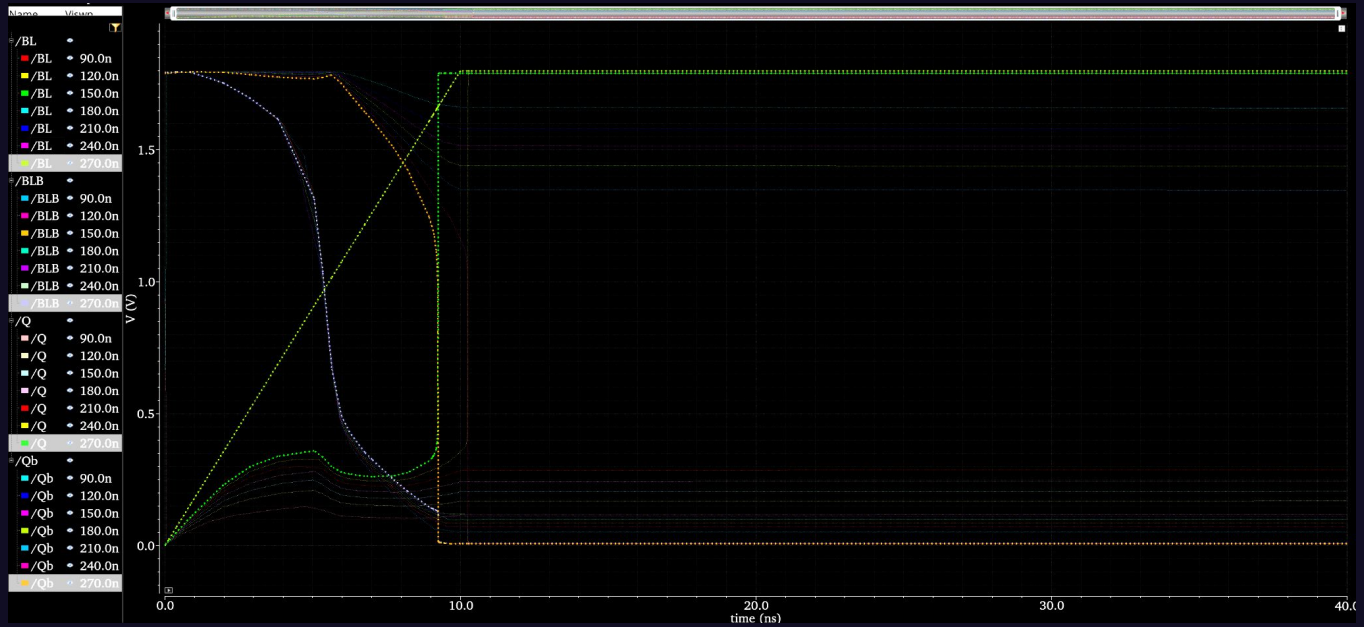
SRAM CELL

- DC Analysis for inverter characteristics for the SRAM Cell.
- Sweeped the parametric width of PMOS = from 90 nm to 360 nm and the Wp = 130nm



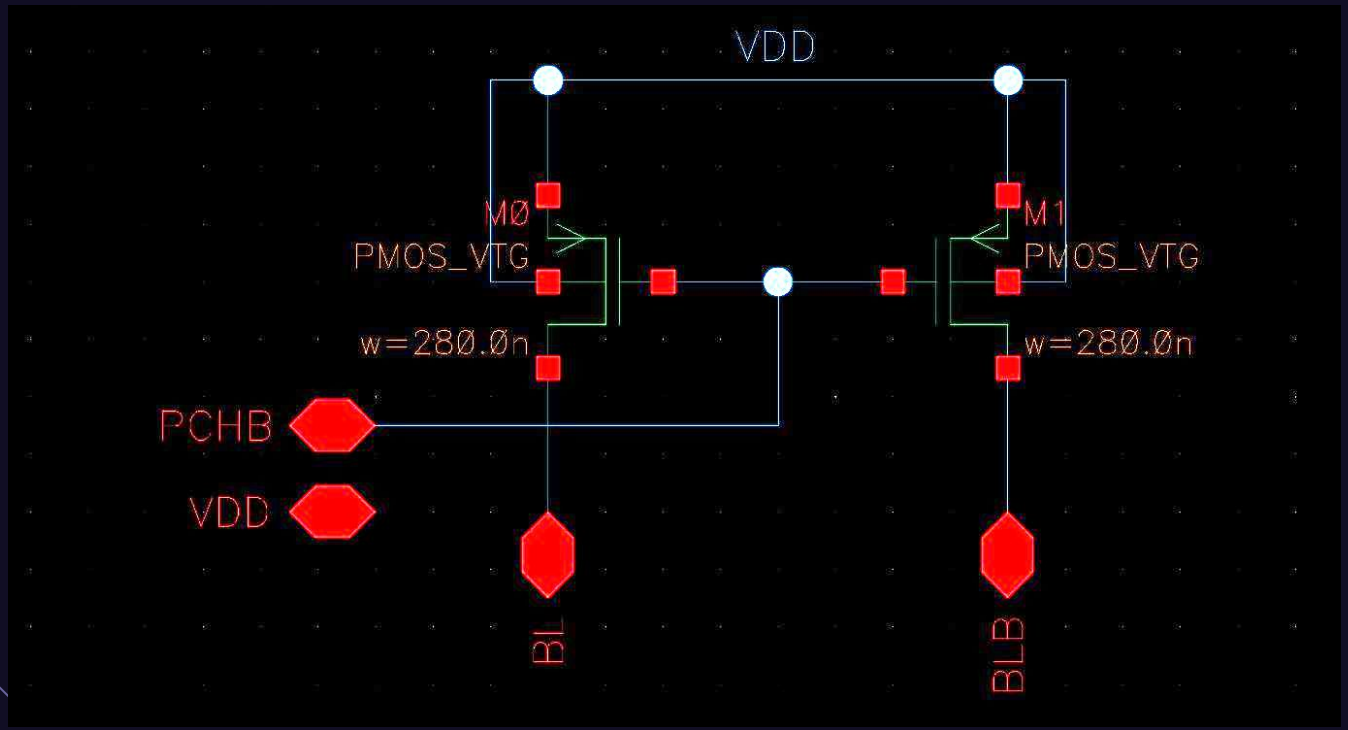
Access Transistor Transient Analysis

- Changed the width of the NMOS from 90 nm to 260 nm.
- Rise time and Fall time Analysis for transiting from BL to Q, while write operation.

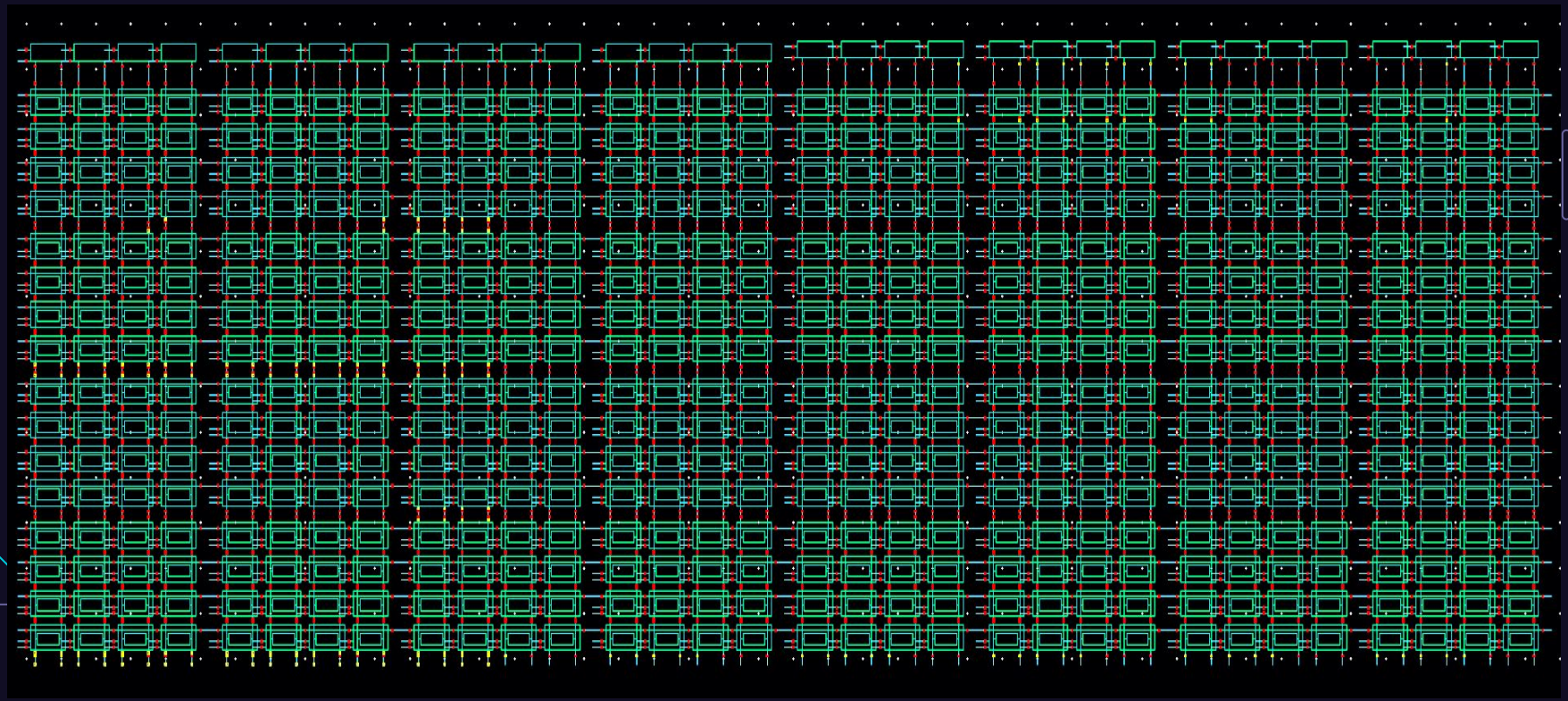


PRE - CHARGE CIRCUIT

- Changed width from 150 nm to 280 nm.

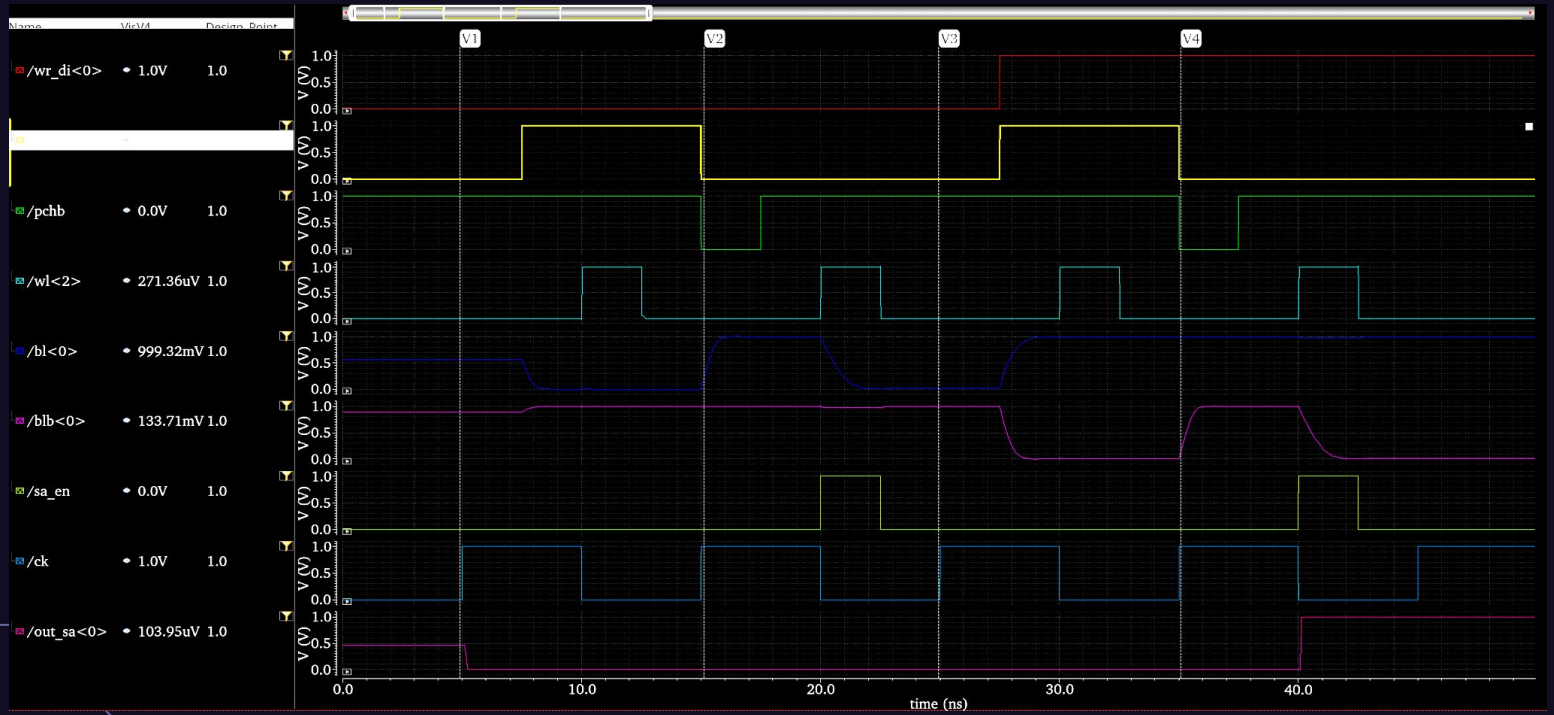


SRAM (32 x 16) ARRAY



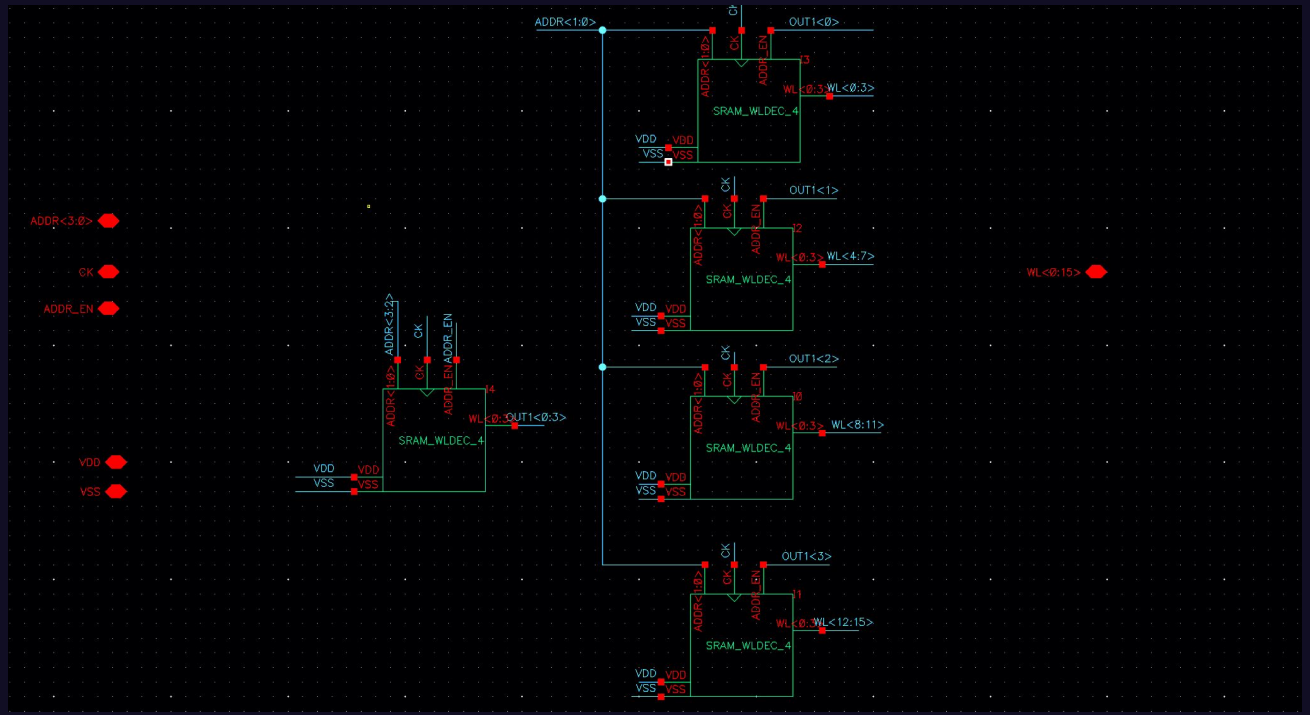
SRAM Timing Analysis

- Timing Analysis for single SRAM cell considering full memory unit



ROW DECODER

- Implemented 4 :16 decoder



THANK YOU!