The Journal of Supercomputing (2022) 78:2287–2306
https://doi.org/10.1007/s11227-021-03851-z

Design and analysis of SRAM cell using reversible logic gates towards smart computing

O. Mohana chandrika[1] · **M. Siva kumar**[1]

Accepted: 29 April 2021 / Published online: 28 June 2021

Abstract

With the enhancement of technology, the usage of electronics in various applications involving large memories for storing and processing data has increased. In this sort of application, SRAM is mainly used because of its high speed. Moreover, with the high usage of memory cells, power consumption has increased to a great extent. The current literature shows that the various parameters of SRAM, such as speed and power, need to be improved for memory cells used in object tracking applications. To improve these parameters, the architectures of SRAM must be combined with new techniques. In recent years, reversible circuits have gained extensive attention because of their low-power and low-speed characteristics. In this brief, a low-power high-speed reversible static RAM is proposed. The proposed SRAM has the combined features of data processing with low-power dissipation and high speed. The proposed architecture of SRAM yields better performance and is similar to traditional SRAM architecture in terms of delay. This paper also implements a 32×64 memory block for object tracking applications. This work is carried out with 45 nm CMOS technology. In the proposed design, transistors are made to operate in the weak inversion region through the use of the EKV model. The design proposed in this paper reduces garbage outputs by 60%, the quantum cost by 70%, and the quantum delay by 70% compared to the current architectures. The proposed design is simulated at different supply voltages to ensure that the power dissipation and delay of SRAM are proportional to the voltage supplied.

Keywords 45 nm CMOS technology · EKV model · Delay · Power consumption · Reversible logic · Weak inversion region

✉ O. Mohana chandrika
mohana.chandrika@gmail.com

[1] Department of ECE, Koneru Lakshmaiah Education Foundation, Vaddeswaram, Guntur, Andhra Pradesh, India

1 Introduction

In theory, object detection and tracking devices primarily use two architecture types, a sensor and a memory system logic mechanism via a standardized algorithm, and the processing speed of the monitoring device can be enhanced. Nevertheless, a subthreshold metal-oxide semiconductor (MOS) architecture or hardware is required to check the standby power and overall system efficiency. High-capacity random access (SRAM) static cache memory is important because tracking systems need large amounts of data space. Nonetheless, because of its high bit-line capacitance, SRAM is considered a power-hungry tool.

Object tracking is a key computer vision aspect. Object tracking has three main steps in place: object detection, frame-to-frame tracking, and object movement analysis. In the past, a considerable amount of work was carried out to improve object tracking accuracy and speed. The main focus of researchers in the literature has been to increase the accuracy of real-time object tracking in scenarios that incorporate additional hardware, particularly static SRAM (static random access memory) architectures [1, 2].

SRAM was used for signals and networks of communications systems due to its high precision and rapid speed. Object detection and tracking systems, however, consume a considerable amount of static energy. A great deal of memory is needed to save random moving object data to the detection and tracking system. To compare successive frames, the saved information is used to identify any movement changes. Nevertheless, the identification and monitoring of object movement in real time are considered a challenge [3, 4].

The read-static noise margin (RSNM) can be improved by the use of read-disconnected logic to further increase the accuracy of an SRAM cell. In subthreshold regions, RSNM is sensitive in the reading of a full-swing sensory amplifier (SA) [5, 6]. Researchers have therefore suggested improvements to SRAM architecture for writing in the subthreshold region, such as the use of an 8 T SRAM cell using a reverse shorter channel effect, which improves the writability at lower voltages [7–11]; an 8-T SRAM variability tolerance; and cache operation at low voltage [11]. Reducing the magnitude of leaks remains a challenge for wireless sensing and communication networks using memory devices.

SRAM is used in applications such as signal processing and communication systems due to its high accuracy and speed. Nevertheless, devices designed to detect and monitor objects consume a great deal of static energy. Devices for detection and tracking require large memories to store random moving object information and to compare the following frames with the stored information [10–16]; the literature focuses mainly on increasing object tracking accuracy in real-time situations by adding additional hardware, especially static RAM. Therefore, fast, accurate, less complicated memory object detection and tracking algorithms are proposed in this research. This target is accomplished with four steps: segmentation, thresholding, object identification, and a pixelation and tracking quadruple process [17–19].

In recent years, the VLSI architecture has become more popular due to its wide range of applications. Note that a heat in Joules of KT × ln 2 energy should be

dissipated. The temperature at which the device is working is expressed in the Boltzmann constant K and T in Kelvin. It is also proven that zero dissipation of power in logic circuits is only possible if there are reversible logic gates in a circuit. A gate that is reversible is a gate that loses no information. As nonadiabatic losses have been minimized, reversible circuits have gained interest for reducing thermal dissipation.

In recent years, designing low-power memory cells has become increasingly popular as memory usage increases. Static memory consists of circuits that maintain their position while using energy. Static random access memory (SRAM), because of its high speed, is common among memory cells. A simple bistable circuit is used by SRAM to maintain some data. A latch used to store the data is generated in two linked inverters in a conventional 6-T cell. If additional data are required to be processed in the same cell, the previous data must be removed, demonstrating the cell's irreversibility and resulting in the dissipation of heat. In modern memory, computations are permanent [20–22].

Morrison et al. [23] suggested a reversible system design for SRAM. Each redundant gate output is known as waste output. The key challenge is to reduce the waste output when designing the reversible circuit. An active SRAM cell with a minimized waste output, a minimized quantity delay and low quantum costs in comparison to the current model [23, 24] is presented in this paper. The proposed SRAM cell and the proposed decoder are built into a 32 to 64 SRAM array.

Therefore, this work proposes a fast, accurate, less memory-intensive object detection and tracking algorithm. The objective is accomplished in four phases: segmentation, thresholding, object identification, and a quad-tree process for reducing pixelation and monitoring.

The reversible SRAM proposed in this paper also overcomes the problem of SRAM cell stability during standby power, which increases the overall energy needed to detect and monitor objects. The rest of the paper is structured as follows.

In Sect. 2, the research methodology of the proposed architecture is discussed. In Sect. 3, various types of reversible gates are studied, and their performance characteristics are compared. In Sect. 4, reversible SRAM is proposed. The design of the 32 X 64 SRAM array is illustrated in Sect. 5. In Sect. 6, the results are analyzed, followed by conclusions in Sect. 7.

2 Methodology

Figure 1 presents the methodology involved in the design of the reversible SRAM architecture. The specifications of the proposed reversible SRAM architecture must first be defined on the basis of a literature survey. Second, the appropriate system technology should be selected on the basis of the specifications. The proposed circuit is subsequently simulated to meet the necessary requirements by means of a few techniques. In this work, a reversible logic technique is implemented for SRAM design. Later, the design is simulated in 45 nm CMOS technology to validate the results. In this work, the total design is implemented in 45 nm CMOS PTM technology. The SRAM is designed by using EKV model. Here, the transistor is made to

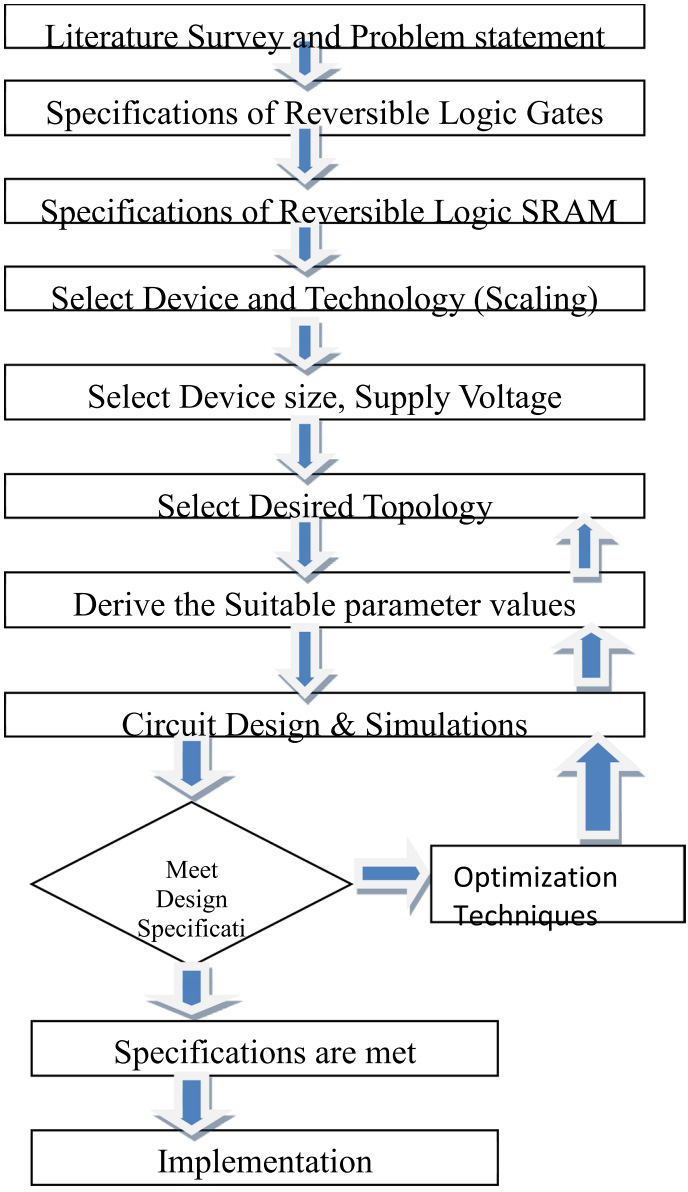

Fig. 1 Methodology involved in the design of the SRAM

operate in the weak inversion region. The definition of the inversion region comes from the design from a single, all-region MOSFET model named after the designers Enz, Krummenacher, and Vittoz, the "EKV Model," which is used to properly minimize the noise and power of the SRAM [25]. In the following equations, the EKV model for the MOS transistor is specified by

$$\mathrm{IC} = \frac{I_{\mathrm{D}}}{I_{\mathrm{S}}} \tag{1}$$

$$g_{\mathrm{m}} = \frac{I_D}{\eta \Phi_t} \frac{1 - \exp\left(-\sqrt{IC}\right)}{\sqrt{IC}} \tag{2}$$

$$I_{\mathrm{s}} = 2\mu C_{\mathrm{ox}} \frac{W}{L} \emptyset_t^2 \tag{3}$$

where I_{S} is the normalization current. I_{D} is the drain current. η is the slope factor and is between 1 and 1.3. Normally, this term is 1. C_{ox} is the oxide capacitance.

$$C_{\mathrm{ox}} = \frac{\in_0 \in_{\mathrm{si}}}{t_{\mathrm{ox}}}$$

$\in_0$ is the permittivity of free space, and $\in_{\mathrm{si}}$ is the relative permittivity of silicon. t_{ox} is the thickness of the oxide layer. ϕ_{t} is the thermal voltage at room temperature, and the value of this term is typically 25.6 mV. IC is the inversion coefficient.

If $\mathrm{IC} << 1$, then the transistor tends to operate or work in a weak inversion region, and if $\mathrm{IC} >> 1$, then the transistor tends to operate or work in a strong inversion region.

In this brief, it is presumed that the present drain ID is 500 nA. This supposition is based on observations made examining the NMOS transistor under voltage and current relationship dimensions $W = 180$ nm and $L = 90$ nm. The simulation is performed in 45 nm CMOS technology in this research. As the transistor is believed to function in the region of weak inversion, the drain current is assumed to be just below the threshold voltage. On this basis, a 500 nA drainage current is presumed.

The transistor dimensions based on the design of the EKV model are as shown in Table 1.

3 Reversible gates

Equal numbers of inputs and outputs are a basic requirement for reversible gates [26]. Thus, conventional Boolean logic gates such as logical OR, AND, NOR, NAND, XOR and XNOR are reversible, as they contain multiple inputs but only one output. However, fundamental reversible gates such as Feynman [27], Fredkin [27]

Table 1 Transistor dimensions for the proposed SRAM

Transistor type	Dimension ratio (W/L)
NMOS	2/1
PMOS	4/1

Fig. 2 Feynman gate

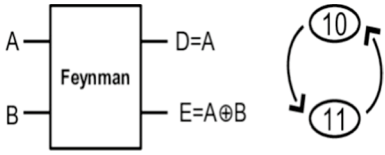

Table 2 Controlled NOT gate truth table

Inputs		Outputs	
A	B	D	E
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

and Toffoli [27] gates contain equal numbers of inputs and outputs. To satisfy the thermodynamic hypothesis, the circuit should be physically and sensibly reversible. These requirements are independent but similarly important regarding reversibility. Logical reversibility utilizes the standards for reversible rationale relating one of a kind yield to one of a kind information. Physical reversibility implies that the information can be exceptionally resolved from the yield, and crucially, the heat dispersal of a gate should not surpass (KT)(ln2) J per cycle. The contrast between consistent reversibility and physical reversibility is critical in light of the fact that heat dispersal can currently be surpassed by a legitimately reversible structure. This situation cannot be considered reversible. A Feynman gate with inputs (A, B) and outputs (D, E) is shown in Fig. 2. This Feynman gate can be written in equation form as

$$FEYMAN : ((A, B) \rightarrow (D, E)) \rightarrow ((0, 1, 2, 3) \rightarrow (0, 1, 3, 2,)) \tag{4}$$

Additionally, the Feynman gate can be set as a NOT (controlled NOT) gate. As the Feynman gate is set to a logic-0 input and B is set to logic-1, the Feynman gate is set to the NOT function as a gate (inverter) (Tables 2, 3 and 4). The gates of Fredkin (Fig. 3) and Toffoli (Fig. 4) are similar to those of the following:

$$FREDKIN : ((A, B, C) \rightarrow (D, E, F)) \rightarrow ((0, 1, 2, 3, 4, 5, 6) \rightarrow (0, 1, 2, 3, 4, 6, 5, 7)) \tag{5}$$

$$TOFFOLI : ((A, B, C) \rightarrow (D, E, F)) \rightarrow ((0, 1, 2, 3, 4, 5, 6) \rightarrow (0, 1, 2, 3, 4, 5, 7, 6)) \tag{6}$$

3.1 Comparison and simulation results

All reversible gates are simulated using Tanner EDA software with 130 nm technology here. Parameters such as the total power dissipation, delay, and slew speed for all reversible logic gates are also compared here. The simulation results from

Table 3 Controlled NOT gate truth table

Inputs			Outputs		
A	B	C	D	E	F
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

Table 4 Controlled SWAP gate truth table

Inputs			Outputs		
A	B	C	D	E	F
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

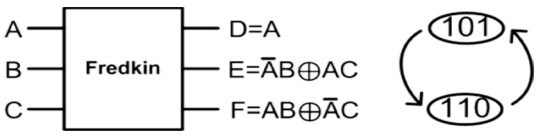

Fig. 3 Fredkin gate

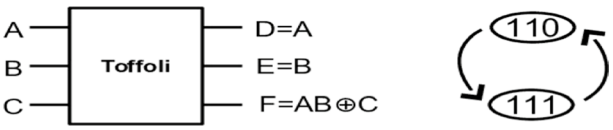

Fig. 4 Toffoli gate

Tanner EDA for the Feynman gate, Fredkin gate, Toffoli gate, DKG gate, Peres gate, and Sayem Gate are given in Fig. 5a, b, c, e and f, respectively.

Tables 5, 6 and 7 compare the parameters of all reversible logic gates w.r.t. various CMOS technologies. Furthermore, a comparative analysis of the various

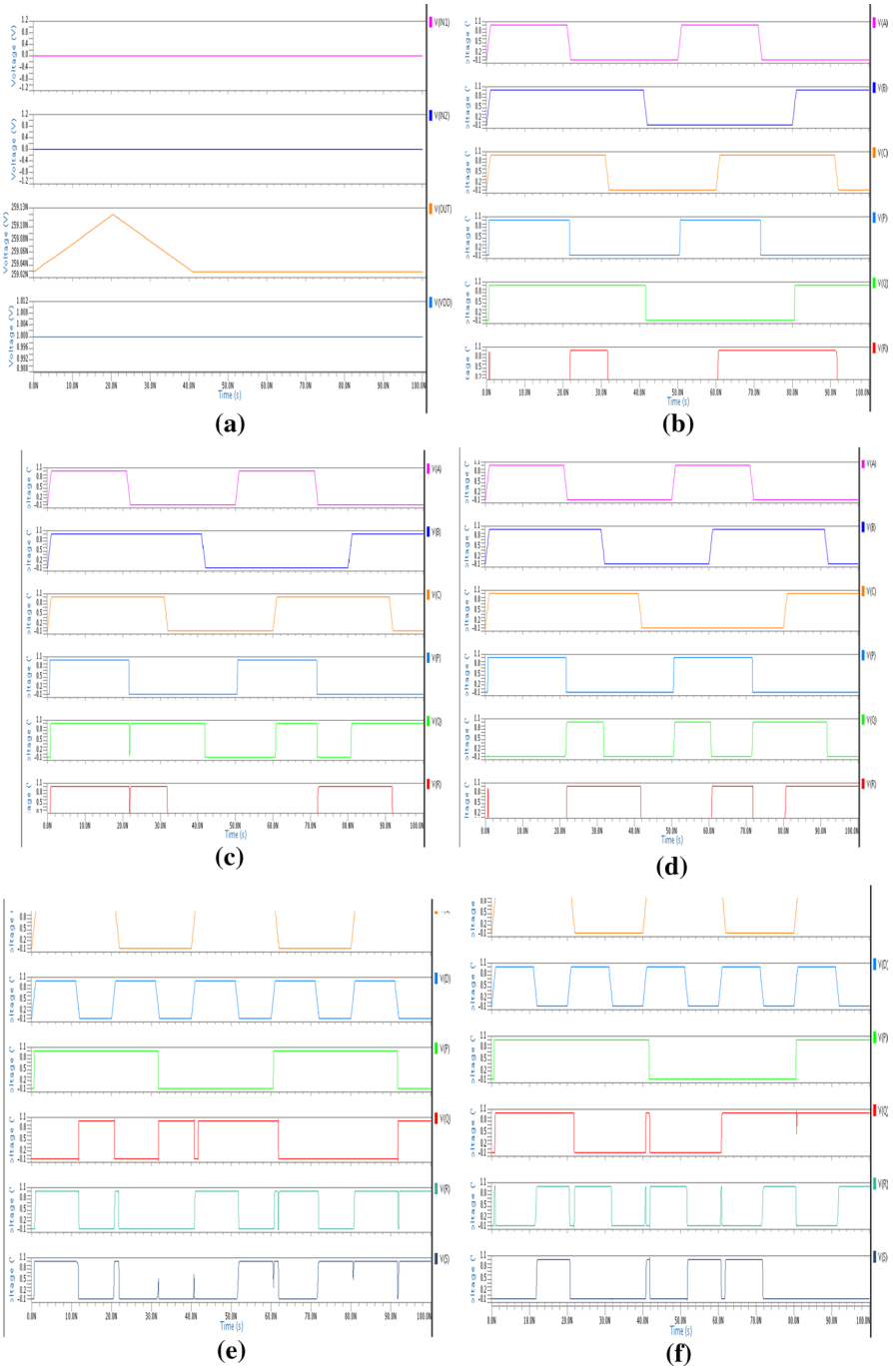

Fig. 5 Simulation waveforms for the **a** Feynman gate, **b** Toffoli gate, **c** Fredkin gate, **d** Peres gate, **e** DKG gate and **f** Sayem gate

Table 5 Comparison of various parameters in 130 nm technology

Parameter	FEYNMAN	FREDKIN	TOFFOLI	PERES	SAYEM	DKG
Total power dissipation (nW)	3.1	8.7	4.6	5.6	14.8	17.5
Delay (ns)	19.3	9.7	32.6	13.5	13.7	6.8
Slew rate (G)	10.8	10.7	7.5	9.7	9.1	10.5

Table 6 Comparison of various parameters in 180 nm technology

Parameter	FEYNMAN	FREDKIN	TOFFOLI	PERES	SAYEM	DKG
Total power Dissipation (nW)	5.6	11.2	7.1	8.1	17.3	20.2
Delay (ns)	21.8	12.5	35.1	16.2	16.7	9.4
Slew rate (G)	12.4	12.9	9.7	11.9	11.7	12.9

Table 7 Comparison of various parameters in 90 nm technology

Parameter	FEYNMAN	FREDKIN	TOFFOLI	PERES	SAYEM	DKG
Total power Dissipation (nW)	1.8	7.9	3.6	4.6	12.8	16.7
Delay (ns)	17.5	8.9	31.4	12.7	13.4	5.8
Slew rate (G)	8.2	8.9	5.9	7.9	7.7	8.9

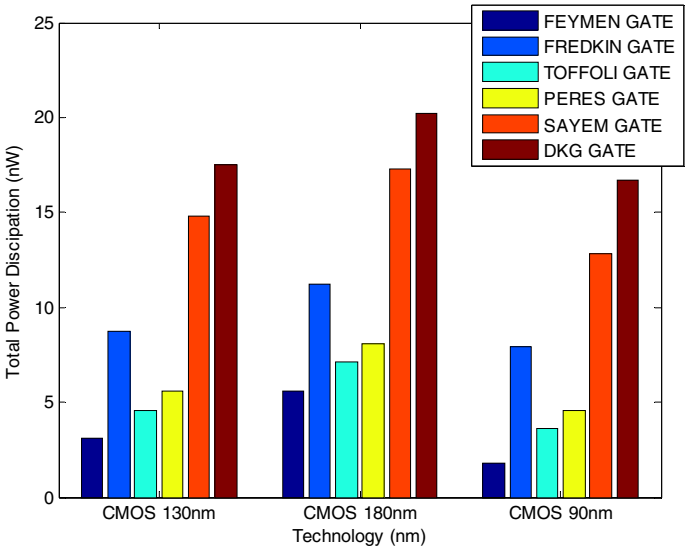

Fig. 6 Comparison of power dissipation w.r.t CMOS technologies of reversible gates

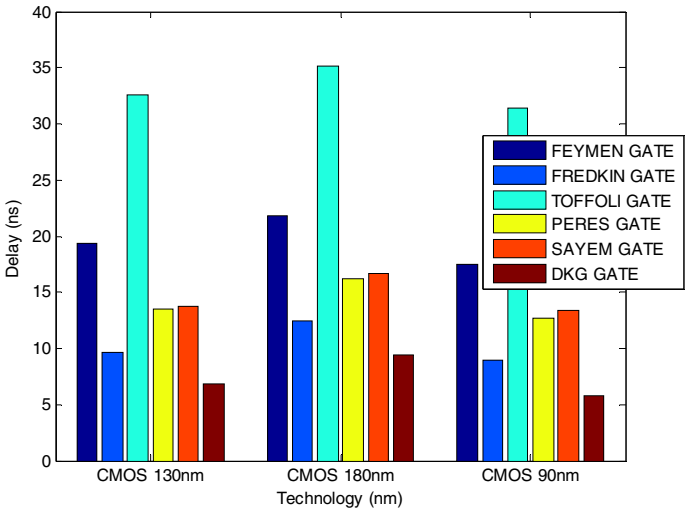

Fig. 7 Comparison of delay w.r.t CMOS technologies of reversible gates

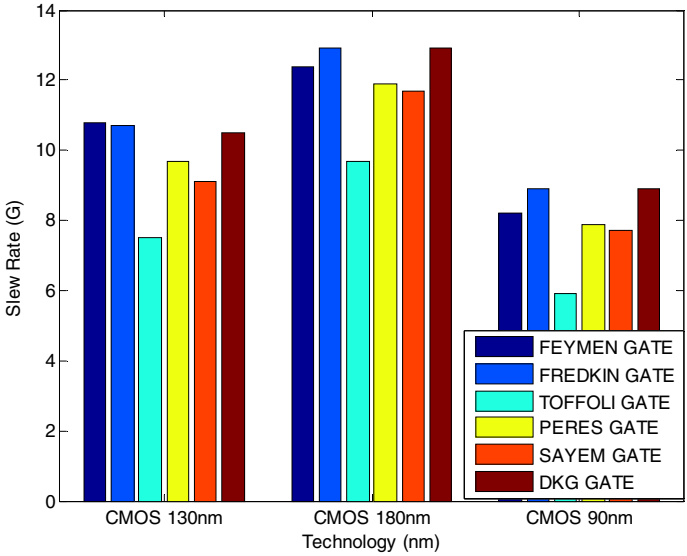

Fig. 8 Comparison of slew rate w.r.t CMOS technologies of reversible gates

parameters, such as total power dissipation, delay and slew rate, is shown in Figs. 6, 7 and 8, respectively.

From all the CMOS implementations of reversible gates, it is evident that the Feynman gate consumes less power than other gates but that it is somewhat slow. With a compromise on the delay, the Feynman gate is chosen for the implementation of SRAM.

4 Proposed SRAM

To track object data in pixels from the current and reference macroframes, an ultralow-power storage memory block is required. Each gray pixel contains 8-bit data. Processing a pixel involves an 8-bit memory array. Because of their fast writing and read access time, the memory array is fitted with SRAM cells. Nonetheless, some of the disadvantages of the SRAM-based memory architectural circuit include high-power leakage, a stability gap, a low noise margin, and vulnerability [28–32].

4.1 Conventional SRAM

Figure 9 displays a standard 6 T SRAM cell. The SRAM cell contains two cross-coupling NOT (inverters) gates that form a latch to store some information. The connection transistors (T1 and T2) link to bit lines in the SRAM cell (BL and BLbar). The SRAM cells function in one of the following modes: reading, writing, or carrying. If the word line (WL) = 0, then the SRAM maintains the stored data because the T1 and T2 reference transistors are in OFF [33] mode. The word line (WL) must be enabled to close the T1 and T2 access transistors so that the SRAM cell can read the data. Sense amplifiers are used for cell state setting or BL and BL bar state testing on bit lines. In conventional SRAM, to increase the functionality, the row cells are enabled by using WL output.

4.2 Cell architecture of the proposed SRAM

This section addresses the proposed cell structure of the SRAM with reversible gates. The completely reversible cell is shown in Fig. 10. For conventional SRAM, the latch and the control transistors are permanent; reversible elements are used to model latch and access transistors.

Here, the access transistor T1 denotes a Fredkin reversible gate, as shown in the figure. The 3X3 reversible Fredkin gate has three inputs, namely, the WL (word

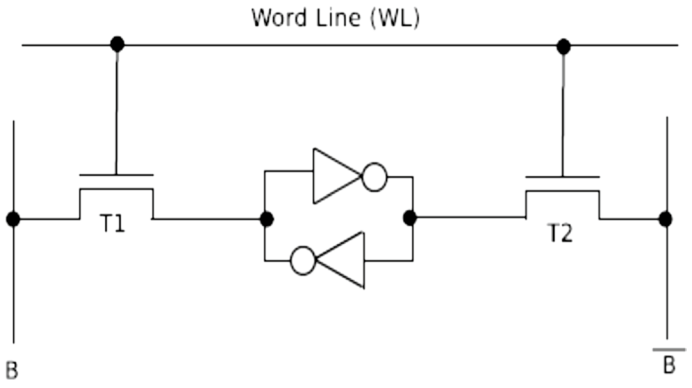

Fig. 9 Conventional SRAM

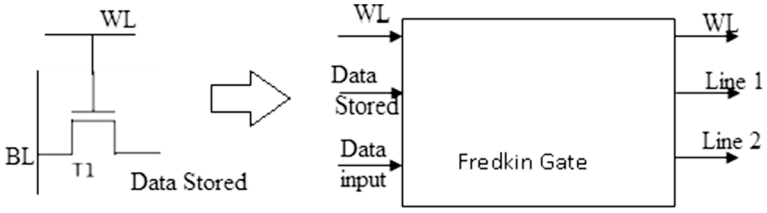

Fig. 10 Fredkin gate an access transistor

line), data storage input, and data input, and three outputs, namely, the WL, Line 1 and Line 2.

The proposed cell has two reversible Fredkin gates rather than two transistors, as in traditional 6 T SRAM. The latch in the traditional SRAM is modeled using a Feynman gate. Thus, 2 Fredkin reversible gates and one Feynman reversible gate are used for the implementation of SRAM. The SRAM operates in modes, i.e., write mode and read mode. A schematic of the reversible gate-based SRAM is shown in Fig. 11.

The first Fredkin gate has three inputs, WL, data stored and data input, and three outputs namely, WL, one left floating and the third related to the Feynman gate's first input. The second reversible gate is a Feynman gate with two inputs, where the first input is the last output of the Fredkin gate. The other input is always connected to logic '1' such that the first output of the Feynman gate comes internally from the buffer and the second output is the XOR output. The Feynman gate buffer output is related to the first Fredkin gate as feedback. The Feynman gate XOR output is connected as the third input to the second Fredkin gate. The other inputs are the RL (read line) and' 0' (logic). Dataout is the last output of the second Fredkin gate.

4.2.1 CMOS architectures of Fredkin and Feynman logic gates

Schematics of the Feynman and Fredkin gates implemented in CMOS technology are shown in Figs. 12 and 13, respectively. Figure 12 shows the CMOS realization of the Feynman gate. The initial output P is a buffer dependent on the input A, and the PMOS pass transistor gate is simply grounded to allow the input 'A' to pass into the output node 'P.' The second output has XOR functionality and consists of a total of 12 transistors for executing the XOR operation. Figure 13 illustrates the CMOS implementation of the Fredkin Gate. The Fredkin gate's very first output is the corresponding first input buffer. A PMOS transistor with a grounded gate

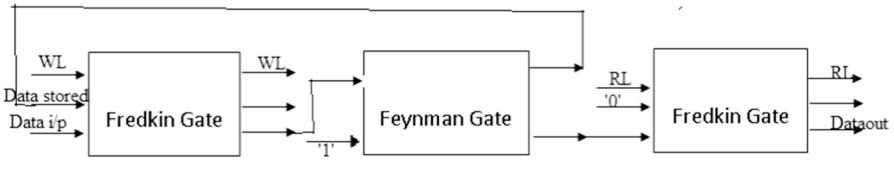

Fig. 11 Reversible architecture of the SRAM cell

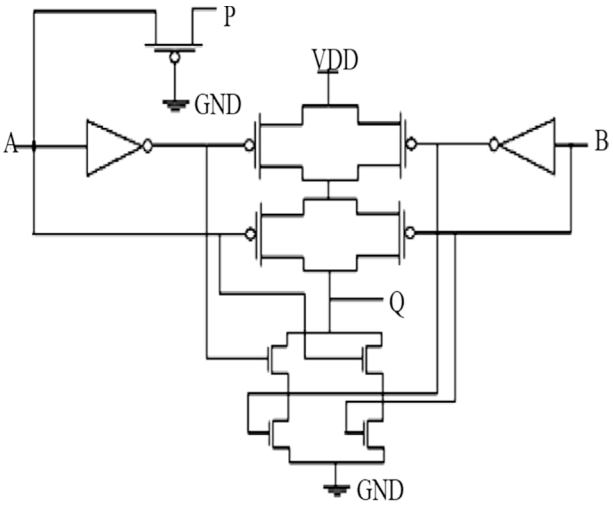

Fig. 12 CMOS implementation of the Feynman gate

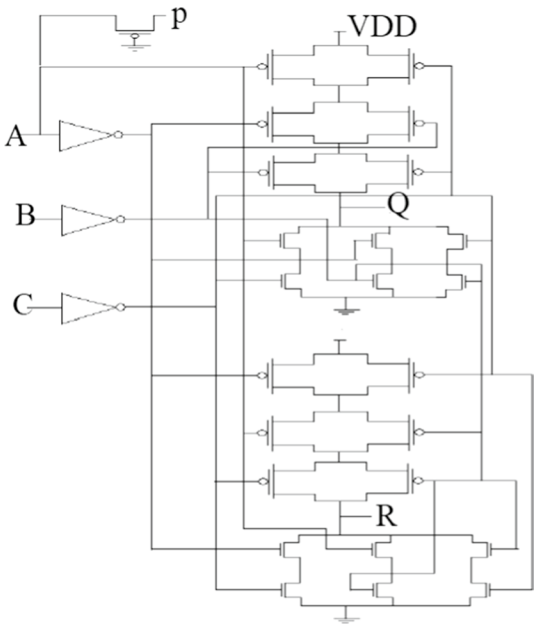

Fig. 13 CMOS implementation of the Fredkin gate

Table 8 SRAM operation w.r.t the read line and word line

Word line (WL)	Read line (RL)	Bit input	Data stored
1	0	1	1
1	0	0	0
0	1	x	Previously stored data is read
0	0	x	Data are held

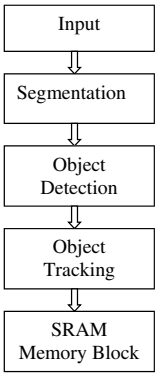

Fig. 14 The object tracking algorithm and its memory implementation with SRAM are proposed

is used. Pull-up and pull-down networks of PMOS and NMOS transistors, respectively, provide the second output $Q = A'B + AC$ and the third output $R = AB + A'C$.

4.2.2 Operation of SRAM

Table 8 displays the truth table of the proposed SRAM cell. When WL = '1' and RL = '0,' the output of the first Fredkin gate is the same as that of the data input, which is stored in the buffer of the Feynman Gate, thus achieving the write operation. Thus, at WL = '1,' SRAM can be said to be in write mode. When WL = '0' and RL = '1' are fed as the input to the second Fredkin gate, the inverse of the data is stored in the Feynman gate. This Fredkin gate gives the same input as the data output. Thus, at RL = '1,' SRAM can be said to be in read mode. When WL = '0' and RL = '0,' SRAM is said to be in hold mode. Previously stored data are held in the SRAM.

5 Design of the 32 X 64 SRAM array

An image is a series of pieces. An image is defined as a two-dimensional $f(x, y)$ function with X and Y as the coordinated image and an amplitude of $f(x, y)$ representing the pictorial force. Various measures are used to detect and track objects, as seen in the diagram showing blocks in Fig. 14 [33–38].

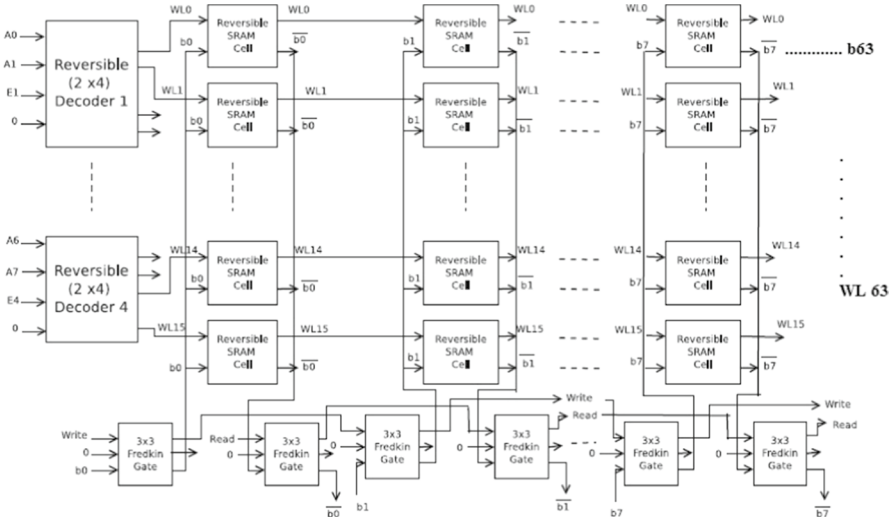

Fig. 15 Proposed architecture of the reversible SRAM cell array

Figure 15 demonstrates the structure of the 8 T SRAM macro. The macro has 32 and 64 columns. The proposed macro, which contains WWL and RWL, provides two rows of world-line writing and reading controls. To give SRAM an entry, the reversible gate decoder is shared with every SRAM macrocolumn. The decoder is also attached to each line, which essentially helps to reduce the power leakage. Here, by using the proposed reversible SRAM architecture, the SRAM array may be implemented for storing the pixel information of the object identified.

6 Results

Figure 16 demonstrates the implementation of the proposed SRAM architecture.

This work is performed using 45 nm CMOS technology in Tanner EDA. For the proposed SRAM, the following conditions are considered. $V_{dd} = 0.9$ V, 1 V, and 1.1 V, the clock frequency is 1 GHz, and the temperature is 27 °C. The proposed SRAM operates in three modes, i.e., in writing mode when WL = '1' and

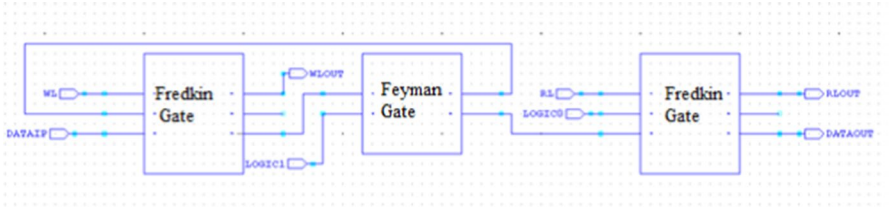

Fig. 16 CMOS implementation of reversible gate-based SRAM

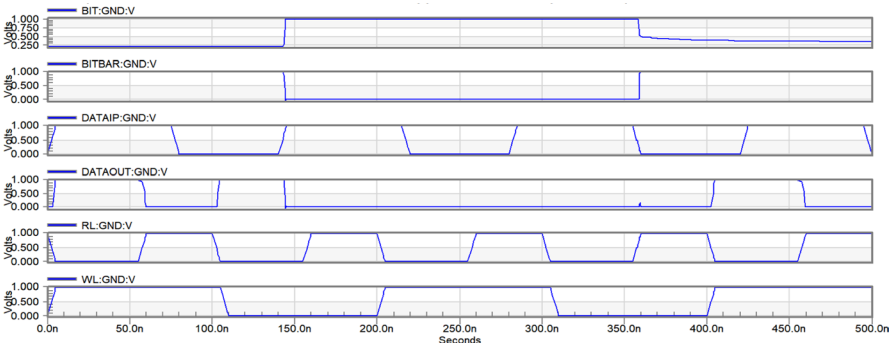

Fig. 17 Transient analysis of the proposed SRAM

RL = '0,' in read mode when WL = '0' and RL = '1', and in hold mode when WL = '0' and RL = '0.' The results of the proposed SRAM transient simulation are plotted in Fig. 17.

6.1 Write delay, read delay and power consumption

When RWL is enabled, the read time is calculated, BLB discharges, and the minimum sensing voltage is reached. The access time for writing '1' is determined when the WWL signal is activated and the *Q* data node reaches 90% of the VDD value. The write 0 access time is also defined because the time of activation of the WWL signal and the Q storage node is 10% of the VDD cost. The power calculated until the time of read access is known as the SRAM read access power. The power measured until the time of write access is defined as the SRAM write access. The average energy is considered here for better understanding. The results of the comparison of performance are shown in Table 9. Comparisons of the supply voltage w.r.t the power and read and write delays are depicted in Figs. 18, 19, and 20.

A comparison of the existing reversible SRAM properties with the proposed SRAM characteristics is shown in Table 10.

From the Table 11, it is evident that delay is shorter and the power dissipation is lower in the reversible SRAM architecture when compared with conventional SRAM. For high-density applications, SRAM with a reversible logic architecture can be used for the processing of applications.

Table 9 Comparison of the delay and power consumption w.r.t the supply voltage

Supply voltage (V)	Write delay (ns)	Read delay (ns)	Power consumption (μW)
1.1	73.13	123.2	2.00
1	72.73	122.79	1.619
0.9	71.78	121.99	1.31

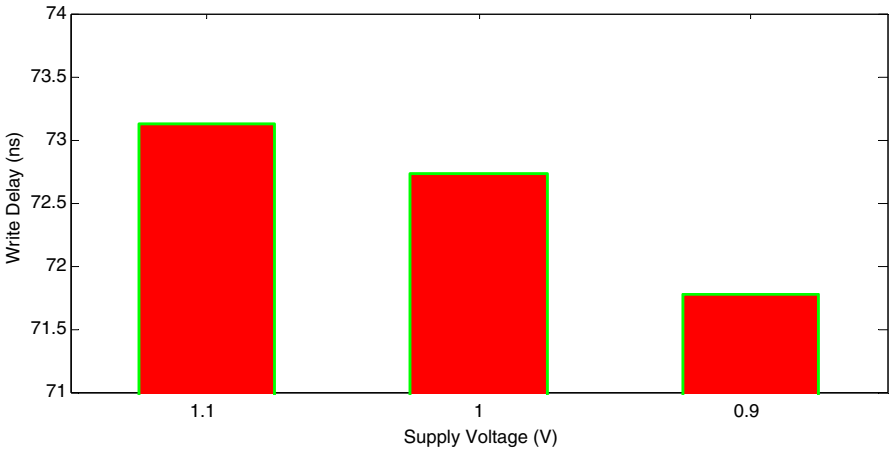

Fig. 18 Comparison of the supply voltage versus the write delay

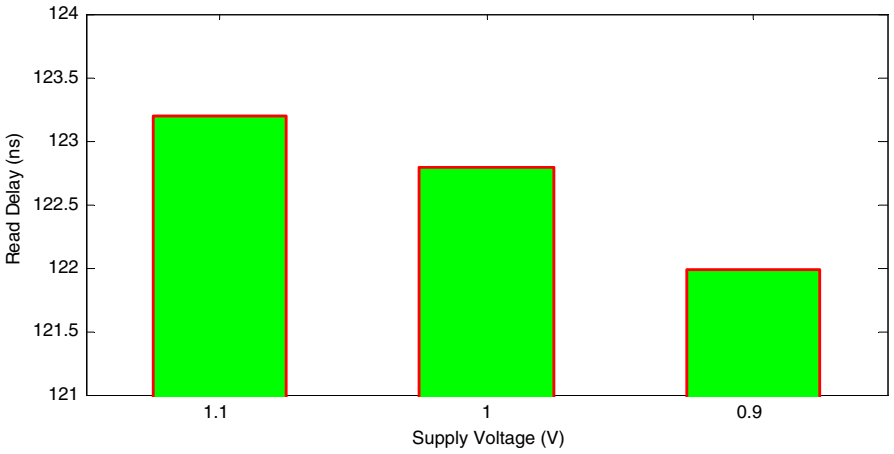

Fig. 19 Comparison of the supply voltage versus the read delay

7 Conclusion

The reversible SRAM presented shows lower power consumption and shorter delay than conventional 6 T, 8 T and 10 T SRAM in this brief. In addition, a high-speed, more efficient, less memory use object tracking processing of implementation is recommended. A new SRAM cell design is suggested for Fredkin and Feynman gates. The SRAM cell is built with Fredkin gates and a Feynman gate. This paper also implements a 32×64 memory block for applications in object tracking. The design proposed in this paper reduces waste by 60%, the quantum cost by 70%, and the delay by 70% compared with those other architectures. The

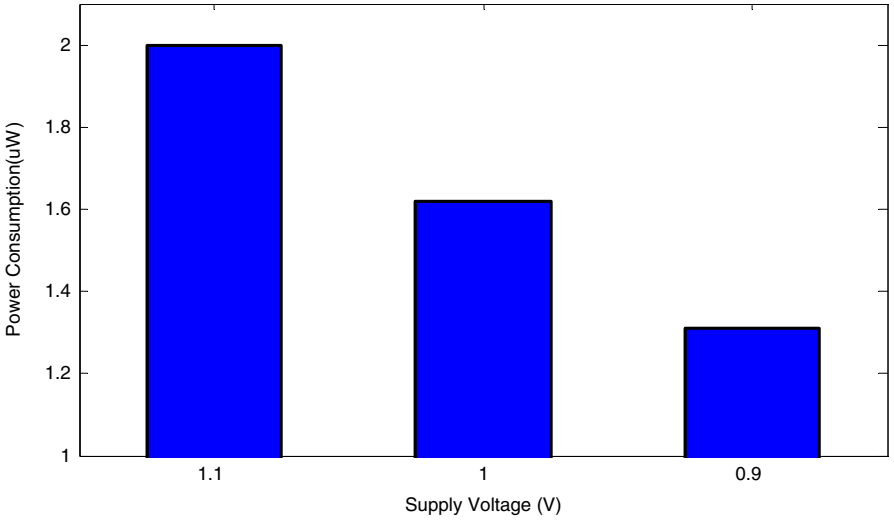

Fig. 20 Comparison of supply voltage versus power consumption

Table 10 Comparison of the reversible SRAM characteristics

SRAM	Garbage outputs	Quantum cost	Quantum delay
[26]	3	21	19Δ
Proposed	1	6	6Δ

Table 11 Comparison of the reversible SRAM characteristics with those of conventional SRAM at 45 nm

	Power dissipation (W)	Average delay (s)
Conventional 6 T SRAM	3.6e−006	3e−007
Conventional 8 T SRAM	*1.1e−005*	*3e−007*
Conventional 10 T SRAM	*3.2e−005*	*1.5e−007*
8 T SRAM with virtual ground	2.5e−005	7.8e−008
Single ended 6 T SRAM	2.3e−005	2e−007
Proposed SRAM	2e−005	1.23e−007

The data shown in italics are the comparitive results of proposed SRAM with respect to existing architectures

proposed SRAM design is simulated with different supply voltages and is shown to be proportional to the power and delay.

With the exponential growth in technology, innovative technical solutions and new architectures are being built to satisfy the need for technology scaling. In addition, with the continuous development of CMOS technology, researchers

concentrate on CMOS IC design strategies with a high degree of integration and low-power consumption. On the basis of modern technologies, there is room to develop construction techniques at both the circuit block level and the device level.

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