Visvesvaraya National Institute of Technology (VNIT), Nagpur

Digital Hardware Design (ECP313)

Project

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Write a VHDL Code for lift controller.

1.1 Problem statement: Write VHDL code for Lift Controller

In this project we assumed the floors to be 2.

1.2 Theory: The elevator is designed to take objects to higher altitudes. In this project 2 floors are taken for designing an elevator.
The lift stops at requested floor when it is less than current floor and lift travels down. Also, stops when requested floor greater than current floor and lift travels up.

The state diagram of the design is as shown in figure.

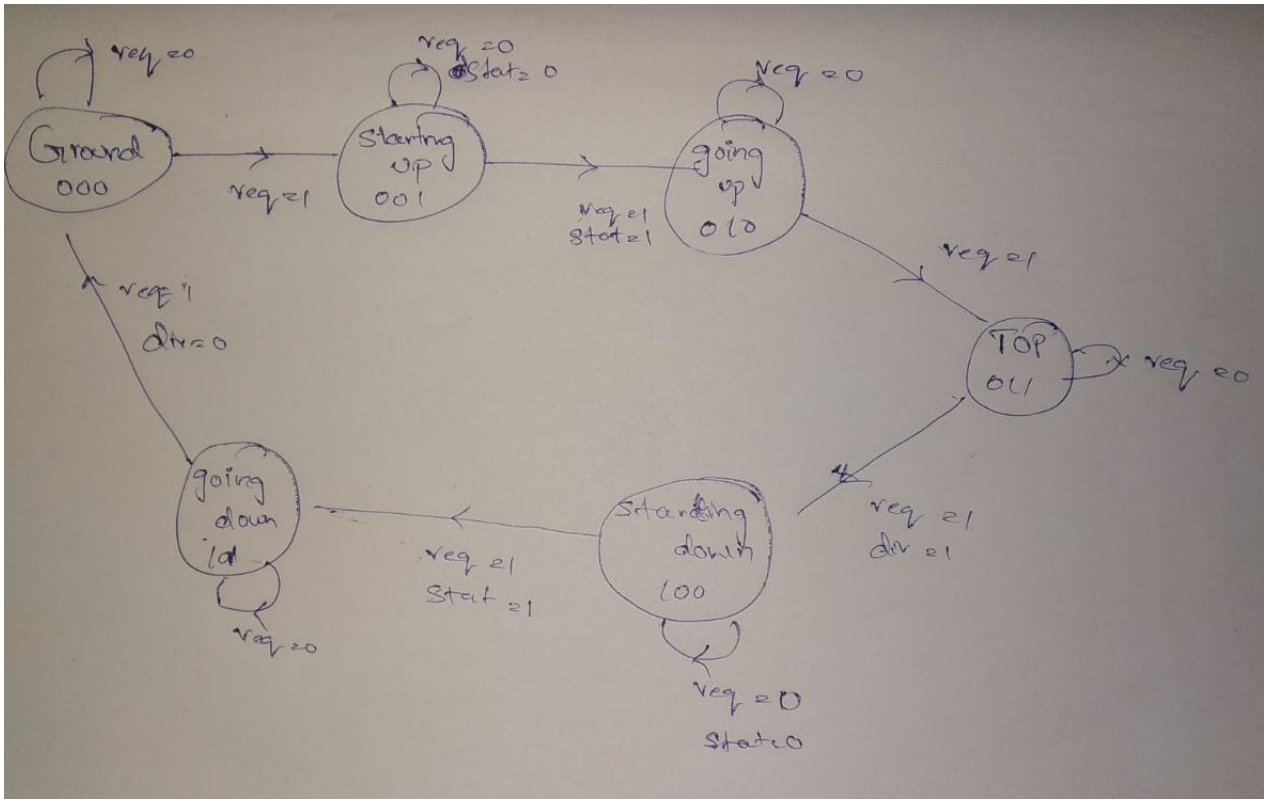


Figure 1: State diagram

And its State table is as follows

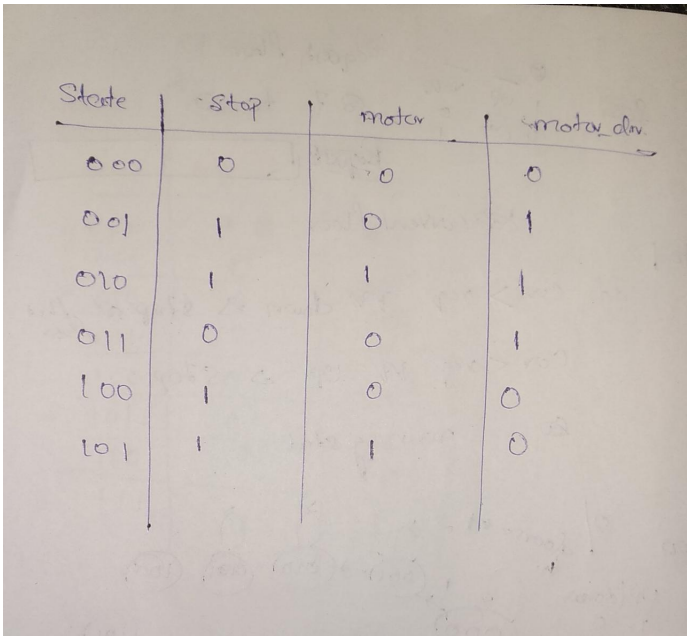


Figure 2: State Table

1.3 Codes:

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.std_logic_arith.all;
4  use ieee.std_logic_unsigned.all;
5
6  entity dhd_project is
7      port (request,stat,clk,dir0,dir1: in STD_LOGIC;
8          stop,motor,motor_dir: out STD_LOGIC);
9  end dhd_project;
10
11
12 architecture arch of dhd_project is
13 attribute enum_encoding: string;
14 type State_type is  (Ground, starting_up, going_up,  Top,  ...
       starting_down,
15                     going_down );
16 attribute enum_encoding of State_type: type is
17     "000 " &
18     "001 " &
19     "010 " &
20     "011 " &
21     "100 " &
22     "101" ;
23     signal State: State_type;
```

```
24      begin
25      LIFT : process (clk)
26      begin
27      if rising_edge(clk) then
28      case State is
29      when Ground =>
30          stop ≤ '0';
31          motor ≤ '0';
32      if request = '1' then
33          State ≤ starting_up;
34      elsif request = '0' then
35          State ≤ Ground;
36      end if;
37      when starting_up =>
38          stop ≤ '1';
39          motor_dir ≤ '1';
40
41      if stat = '1' then
42          State ≤ going_up;
43
44      elsif stat = '0' then
45          State ≤ starting_up;
46
47      end if;
48      when going_up =>
49          motor ≤ '1';
50      if dir1 = '1' then
51          State ≤ Top;
52
53      elsif dir1 = '0' then
54          State ≤ going_up;
55
56      end if;
57      when Top =>
58          stop ≤ '0';
59          motor ≤ '0';
60      if request = '1' then
61          State ≤ starting_down;
62
63      elsif request = '0' then
64          State ≤ Top;
65      end if;
66      when starting_down =>
67          stop ≤ '1';
68          motor_dir ≤ '0';
69      if stat = '1' then
70          State ≤ going_down;
71      elsif stat = '0' then
72          State ≤ starting_down;
```

```
73      end if;
74      when going_down =>
75          motor ≤ '1';
76
77      if dir1 = '1' then
78          State ≤ Ground;
79      elsif dir1 = '0' then
80          State ≤ going_down;
81      end if;
82      when others =>
83      null;
84      end case;
85      end if;
86
87      end process;
88  end arch;
```

Testbench:

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.std_logic_arith.all;
4   use ieee.std_logic_unsigned.all;
5
6   --empty entity
7   entity dhd_project_tb is
8   end dhd_project_tb;
9
10
11  architecture tb of dhd_project_tb is
12      component dhd_project
13      port(request,stat,clk,dir0,dir1: in STD_LOGIC;
14          stop,motor,motor_dir: out STD_LOGIC);
15      end component;
16
17      signal clk: std_logic:= '0';
18      signal request: std_logic:='0';
19      signal stat: std_logic:='0';
20      signal dir0: std_logic:='0';
21      signal dir1: std_logic:='0';
22
23      signal stop: std_logic;
24      signal motor: std_logic;
25      signal motor_dir: std_logic;
26
27      begin
28      clk ≤'0';
29      request ≤ '0';
```

```
30      stat ≤ '0';
31      dir0 ≤ '0';
32      dir1 ≤ '0';
33      wait for 100 ns;
34
35      clk ≤'1';
36      request ≤ '0';
37      stat ≤ '0';
38      dir0 ≤ '0';
39      dir1 ≤ '0';
40      wait for 100 ns;
41
42      clk ≤'1';
43      request ≤ '1';
44      stat ≤ '0';
45      dir0 ≤ '0';
46      dir1 ≤ '1';
47      wait for 100 ns;
48      wait;
49
50      end tb;
```

1.4 RTL Schematic: .RTL view

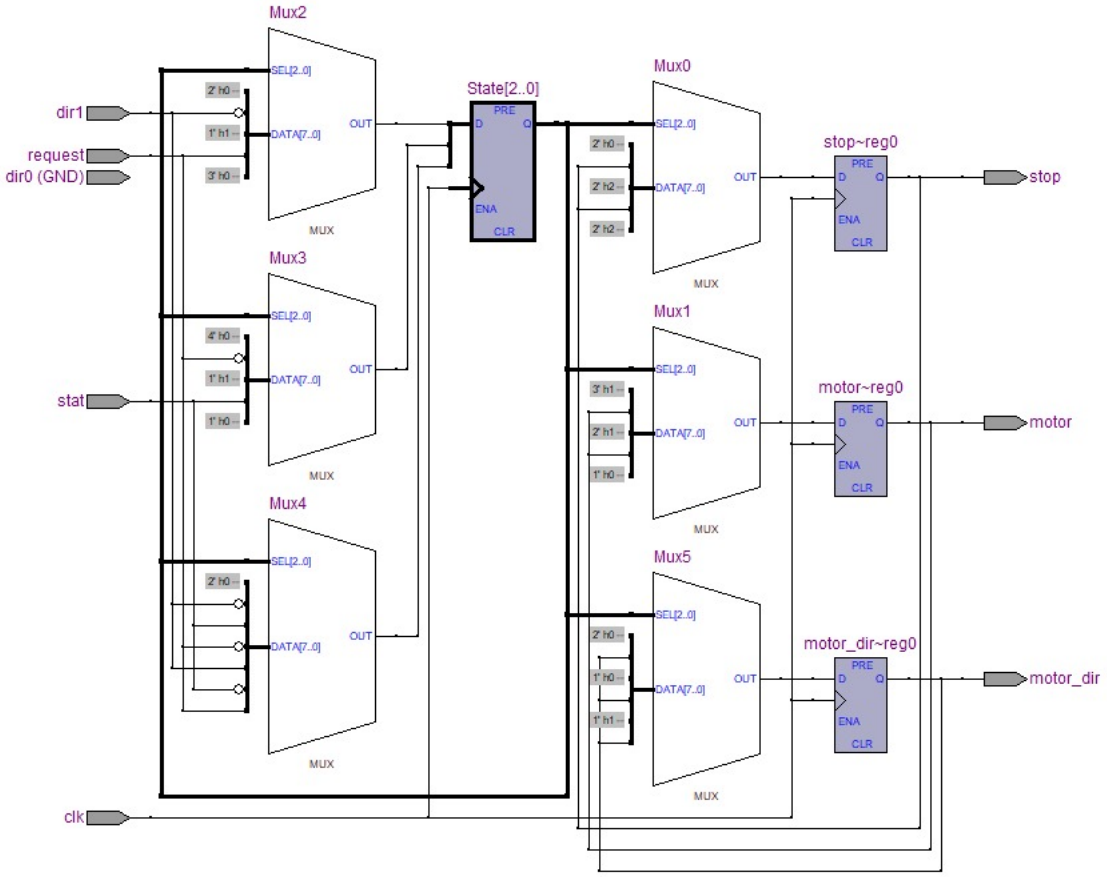


Figure 3: RTL Schematics

1.5 Simulation Waveform: .Simulation

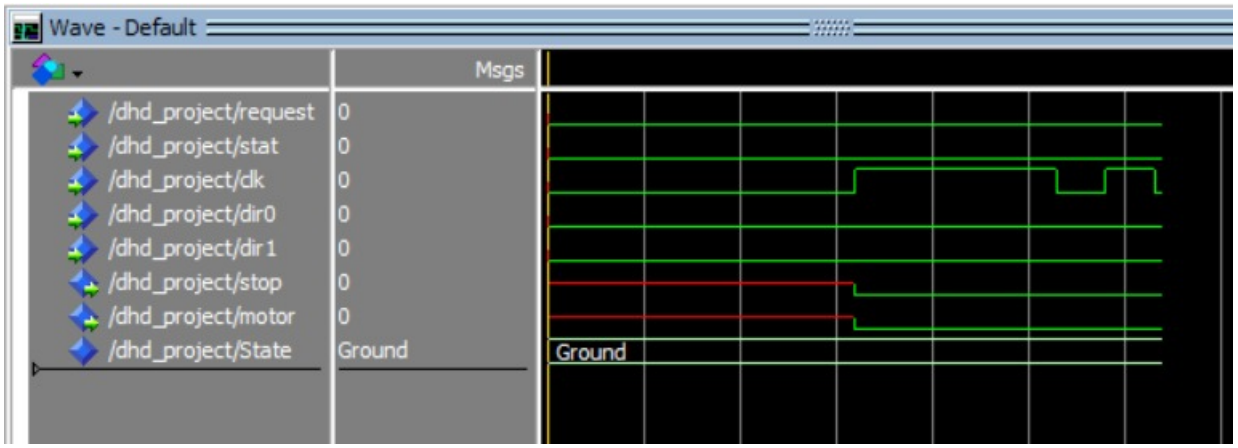
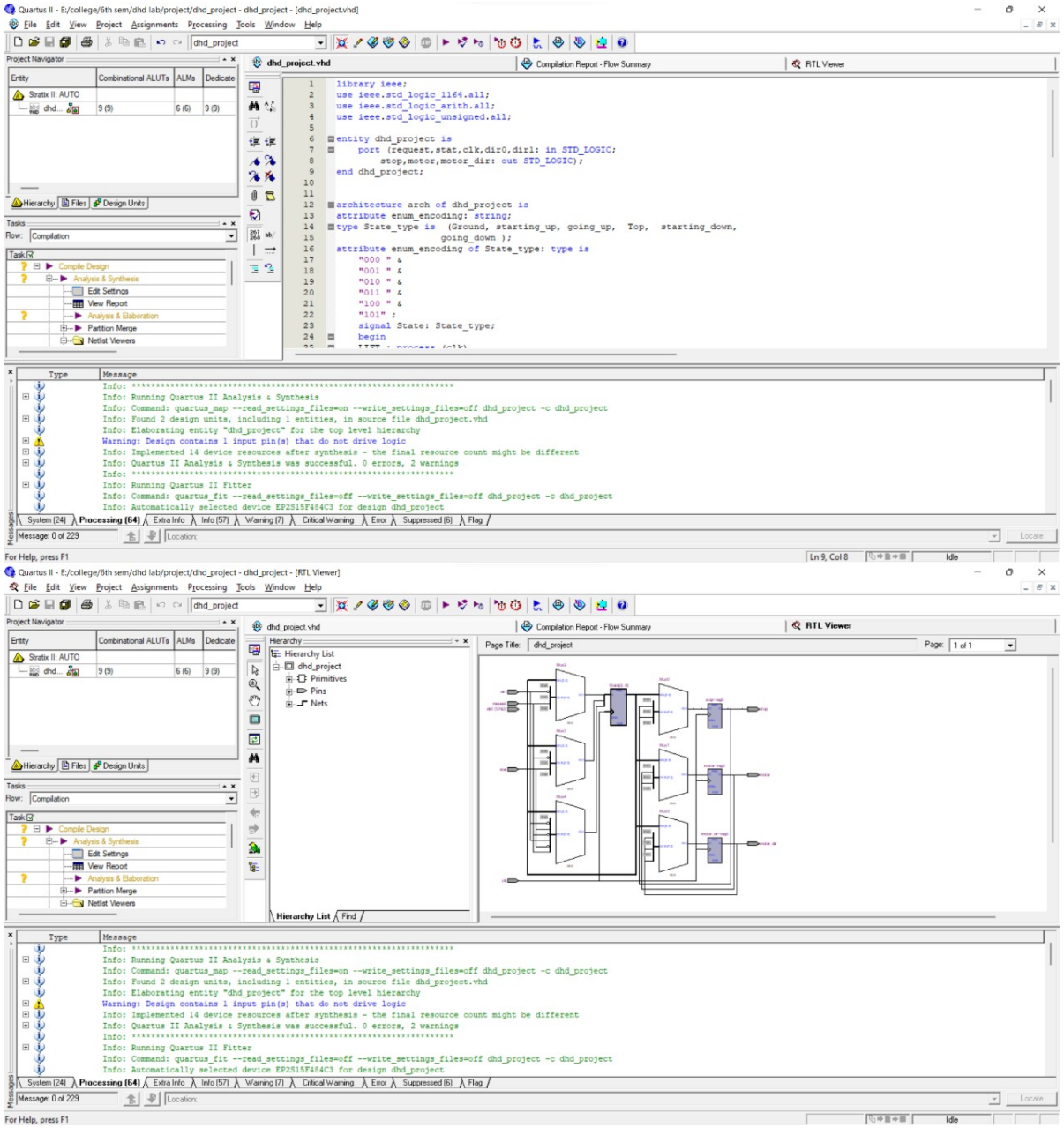


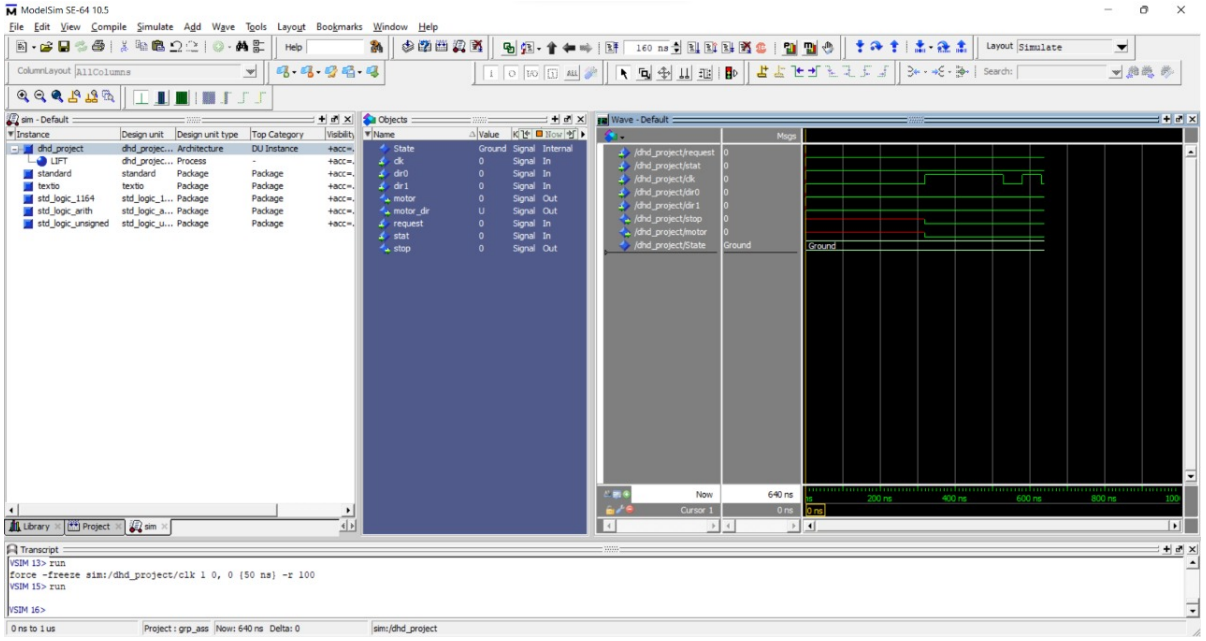
Figure 4: Waveform

1.6 Conclusions: The lift stops at requested floor when it is less than current floor and lift travels down. Also, stops when requested floor greater than current floor and lift travels up.

1.7 Screenshots: . .

1.7


Quartus II - E:/college/6th sem/dhd lab/project/dhd_project - dhd_project - [dhd_project.vhd]
File Edit View Project Assignments Processing Tools Window Help
dhd_project
Project Navigator
Entity
Combinational ALUTs
ALMs
Dedicate
Stratix II: AUTO
dhd...
9 (9)
6 (6)
9 (9)
Hierarchy
Files
Design Units
Tasks
Flow:
Compilation
Task
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
Netlist Viewers
dhd_project.vhd
Compilation Report - Flow Summary
RTL Viewer
1 library ieee;
2 use ieee.std_logic_1164.all;
3 use ieee.std_logic_arith.all;
4 use ieee.std_logic_unsigned.all;
5
6 entity dhd_project is
7 port (request,stat,clk,dir0,dir1: in STD_LOGIC;
8 stop,motor,motor_dir: out STD_LOGIC);
9 end dhd_project;
10
11
12 architecture arch of dhd_project is
13 attribute enum_encoding: string;
14 type State_type is (Ground, starting_up, going_up, Top, starting_down,
15 going_down);
16 attribute enum_encoding of State_type: type is
17 "000 " &
18 "001 " &
19 "010 " &
20 "011 " &
21 "100 " &
22 "101" ;
23 signal State: State_type;
24 begin
Type
Message
Info: Running Quartus II Analysis & Synthesis
Info: Command: quartus_map --read_settings_files=on --write_settings_files=off dhd_project -c dhd_project
Info: Found 2 design units, including 1 entities, in source file dhd_project.vhd
Info: Elaborating entity "dhd_project" for the top level hierarchy
Warning: Design contains 1 input pin(s) that do not drive logic
Info: Implemented 14 device resources after synthesis - the final resource count might be different
Info: Quartus II Analysis & Synthesis was successful. 0 errors, 2 warnings
Info: Running Quartus II Fitter
Info: Command: quartus_fit --read_settings_files=off --write_settings_files=off dhd_project -c dhd_project
Info: Automatically selected device EP2S15F484C3 for design dhd_project
System (24)
Processing (64)
Extra Info
Info (57)
Warning (7)
Critical Warning
Error
Suppressed (6)
Flag
Message: 0 of 229
Location:
Locate
For Help, press F1
Ln 9, Col 8
Idle
Quartus II - E:/college/6th sem/dhd lab/project/dhd_project - dhd_project - [RTL Viewer]
File Edit View Project Assignments Processing Tools Window Help
dhd_project
Hierarchy List
dhd_project
Primitives
Pins
Nets
Page Title:
dhd_project
Page:
1 of 1
Hierarchy List
Find


ModelSim SE-64 10.5
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance Design unit Design unit type Top Category Visibility
dhd_project dhd_projec... Architecture DU Instance +acc=.
LIFT dhd_projec... Process -
standard standard Package Package
textio textio Package Package
std_logic_1164 std_logic_1... Package Package
std_logic_arith std_logic_a... Package Package
std_logic_unsigned std_logic_u... Package Package
Objects
Name Value Signal
State Ground Signal Internal
clk 0 Signal In
dir0 0 Signal In
dir1 0 Signal In
motor 0 Signal Out
motor_dir U Signal Out
request 0 Signal In
stat 0 Signal In
stop 0 Signal Out
Wave - Default
/dhd_project/request
/dhd_project/stat
/dhd_project/clk
/dhd_project/dir0
/dhd_project/dir1
/dhd_project/stop
/dhd_project/motor
/dhd_project/State
Ground
Now 640 ns
Cursor 1 0 ns
200 ns 400 ns 600 ns 800 ns
Library Project sim
Transcript
VSIM 13> run
force -freeze sim:/dhd_project/clk 1 0, 0 {50 ns} -r 100
VSIM 15> run
VSIM 16>
0 ns to 1 us
Project : grp_ass
Now: 640 ns Delta: 0
sim:/dhd_project