

FACULTY OF SCIENCE AND TECHNOLOGY
Assignment (Laboratory) Coversheet

Student ID number	U3312590
Student Name	Jasmine Bajracharya
Unit name	Introduction to Computer Engineering
Unit number	10096
Name of lecturer/tutor	Dr. Julio Romero
Assignment topic	Latches and Counters
Due date	4 th November, 2025
Word Count	1124

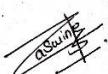
You must keep a photocopy or electronic copy of your assignment.

Student declaration

I certify that the attached assignment is my own work. Material drawn from other sources has been appropriately and fully acknowledged as to author/creator, source and other bibliographic details. Such referencing may need to meet unit-specific requirements as to format and style.

I give permission for my assignment to be copied, submitted and retained for the electronic checking of plagiarism.

Signature of student:



Date: 30th October 2025

(Students submitting work electronically can type their name in the space for signature above, but must produce a signed copy of this coversheet on request.)

Date of submission: 30th October 2025

*Note: All the files from micro cap simulation, hardware simulation videos from waveforms and the circuit and the hardware implementation images are provided in the respective folders.

1. Hardware Implementation First Sequential Circuit (25 marks)

Materials required:

- IC7400 - 2 input NAND gate
- IC7408 - 2 input AND gate
- IC7476 - Dual JK flip flop
- Multimeter
- Breadboard

Pin configuration:

For AND gate:

1. Pin 14- Voltage source
2. Pin 7- GND
3. Pin 1- DIO0
4. Pin 2- GND
5. Pin 3- Output to pin-1 of JK flip flop
6. Pin 4- DIO1
7. Pin 5- GND
8. Pin 6- Output to pin 4 of JK flip flop

For JK flip flop

1. Pin 3 and 8- GND
2. Pin 14- VCC
3. Pin 12- Clock
4. Pin 12- Output from JK flip flop
5. Pin 1 and Pin 4- input from AND gates

The Circuit was implemented as shown in the image below:

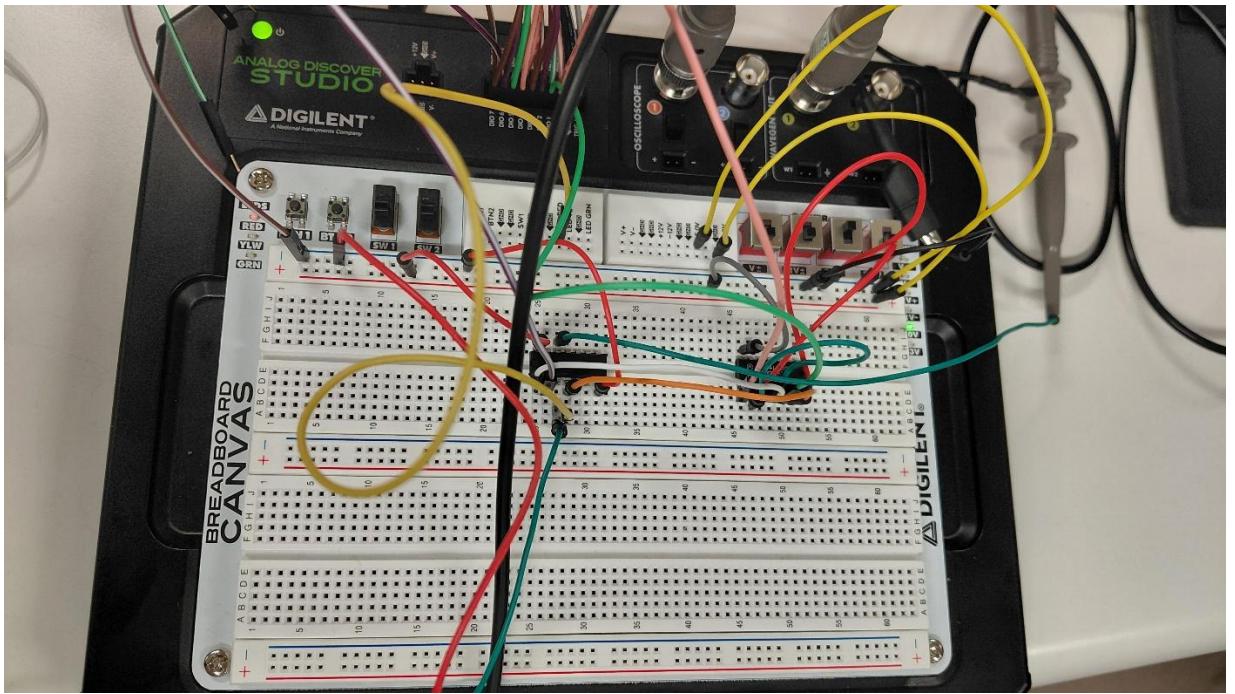


Figure: Hardware implementation of circuit 1

1.2 Generate and Complete table asked in point 3. Your measurements must be in volts.

The circuit was constructed and the voltage across the outputs were measured and obtained as follows:

All the outputs were obtained with respect to the clock which is edge-triggered

A	B	Q	Voltage
0	0	0	1.09
0	1	1	3.55
1	0	0	1.12
1	1	1	3.55

1.3 Apply signals shown in Figure 5. Include a screenshot of the time diagram under the different operating conditions.

The circuit was implemented under different operating conditions, and the following outputs were obtained:

UNIVERSITY OF CANBERRA
INTRODUCTION TO COMPUTER ENGINEERING (8223/10096)
TUTORIAL WEEK 7 Assignment Template

Under A=0 and B=0

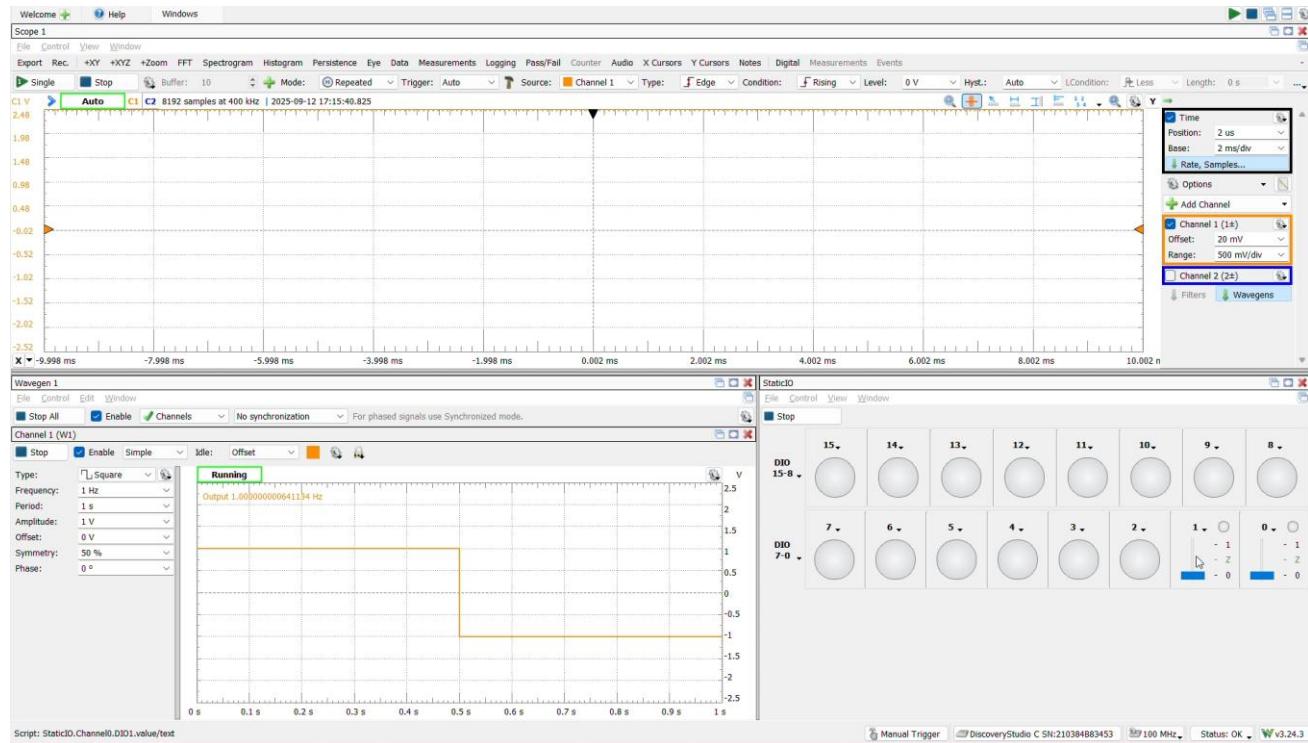
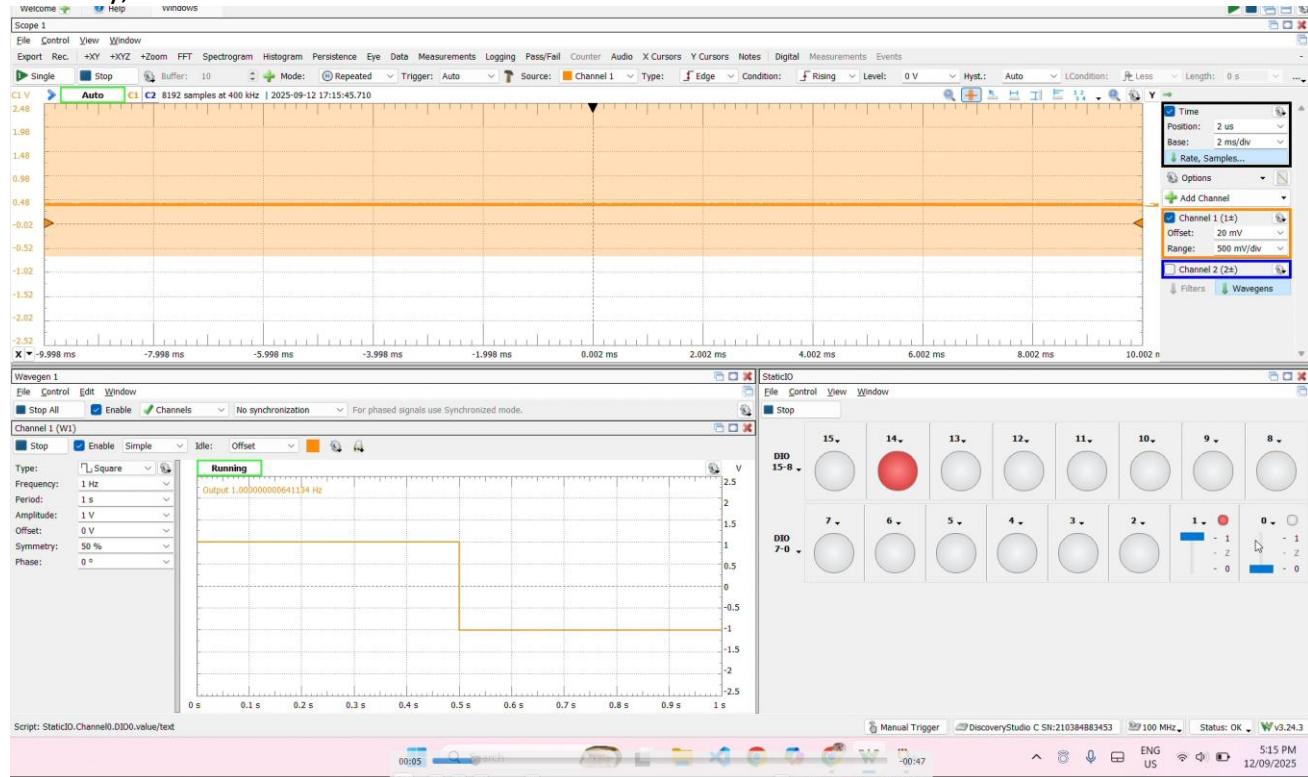


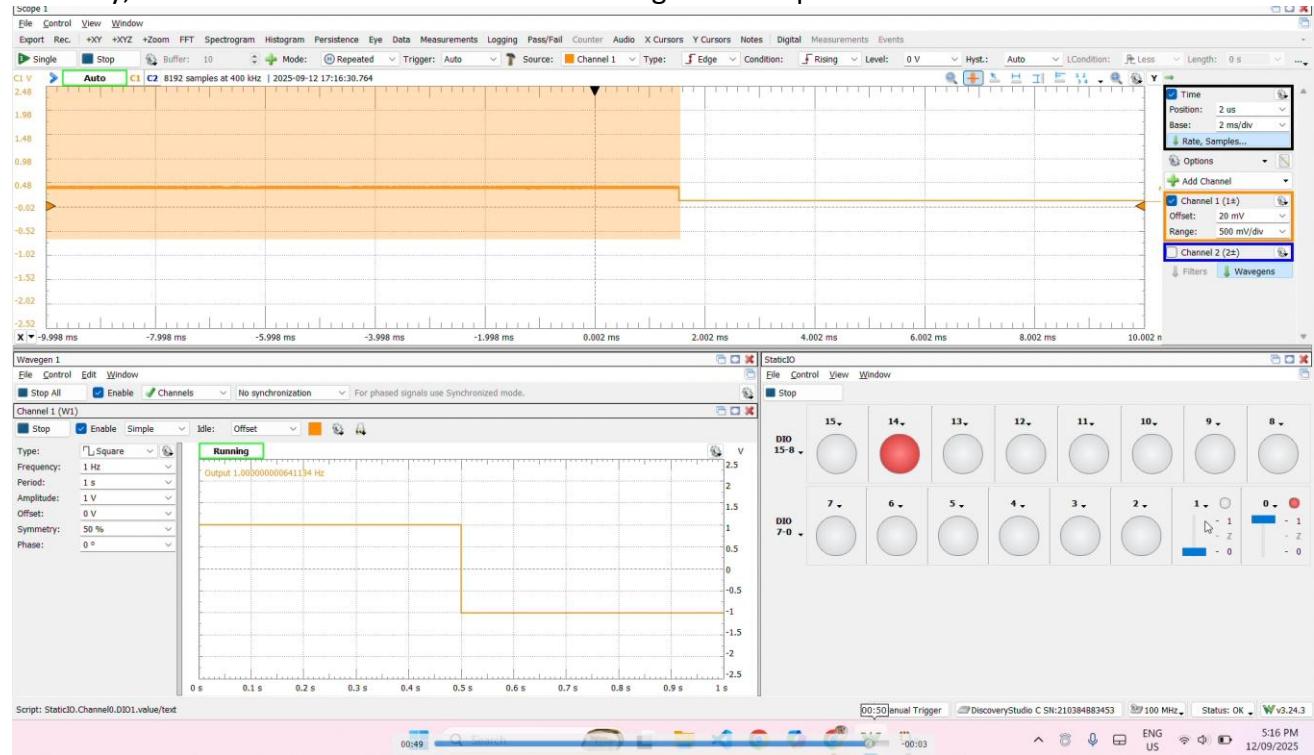
Figure: Output from the circuit when both A and B are equal to 0

Similarly, under the conditions A= 0 and B = 1

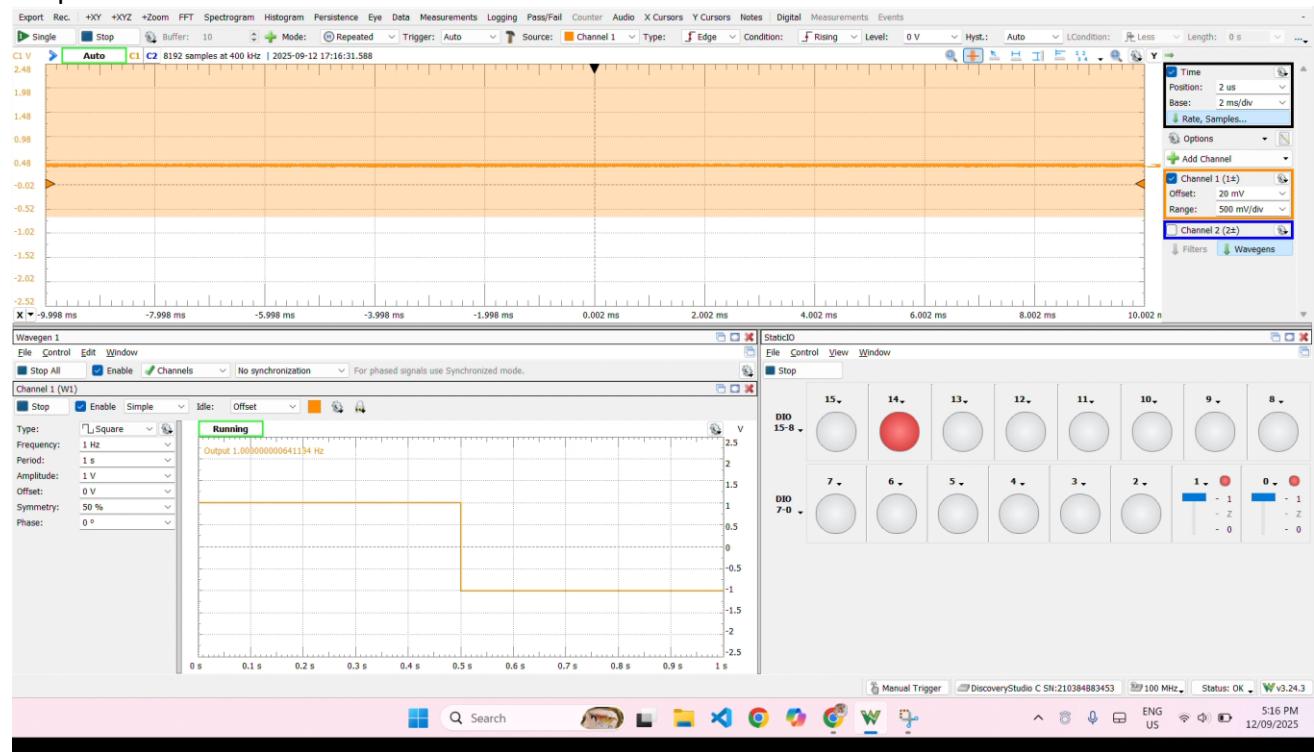


UNIVERSITY OF CANBERRA
INTRODUCTION TO COMPUTER ENGINEERING (8223/10096)
TUTORIAL WEEK 7 Assignment Template

Similarly, Under the conditions A= 1 and B =0 we get the output to be 0



Similarly on A=1 and B= 1 we get the output to be 1 which is the toggled output of the previous output



1.4 Answer question 5.

What does this circuit do?

Answer: The circuit behaves as a controlled JK flip flop where the inputs A and B determine whether the JK flip flops sets, resets, toggles or holds the previous states.

1.5 State the purpose of W1.

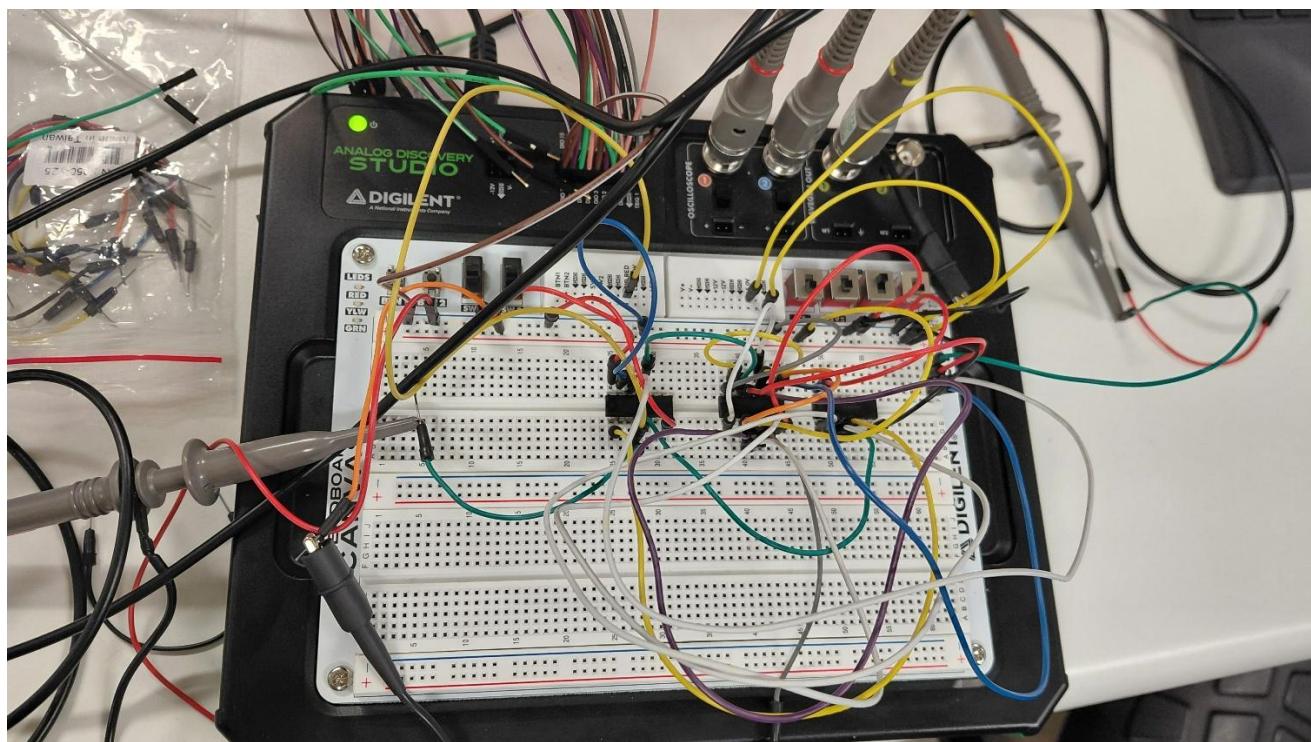
Answer: W1 here acts as a manual switch which manually generates the clock signals. When we toggle W1 to 1, it provides a rising edge and when changed to 0 it provides a falling edge, in our case, we have manually set it to ground.

2. Hardware Implementation Second Sequential Circuit (25 marks)

Materials required:

1. IC 7408 2 input AND gate
2. IC 7476 dual JK flipflop
3. Multimeter
4. Bread board

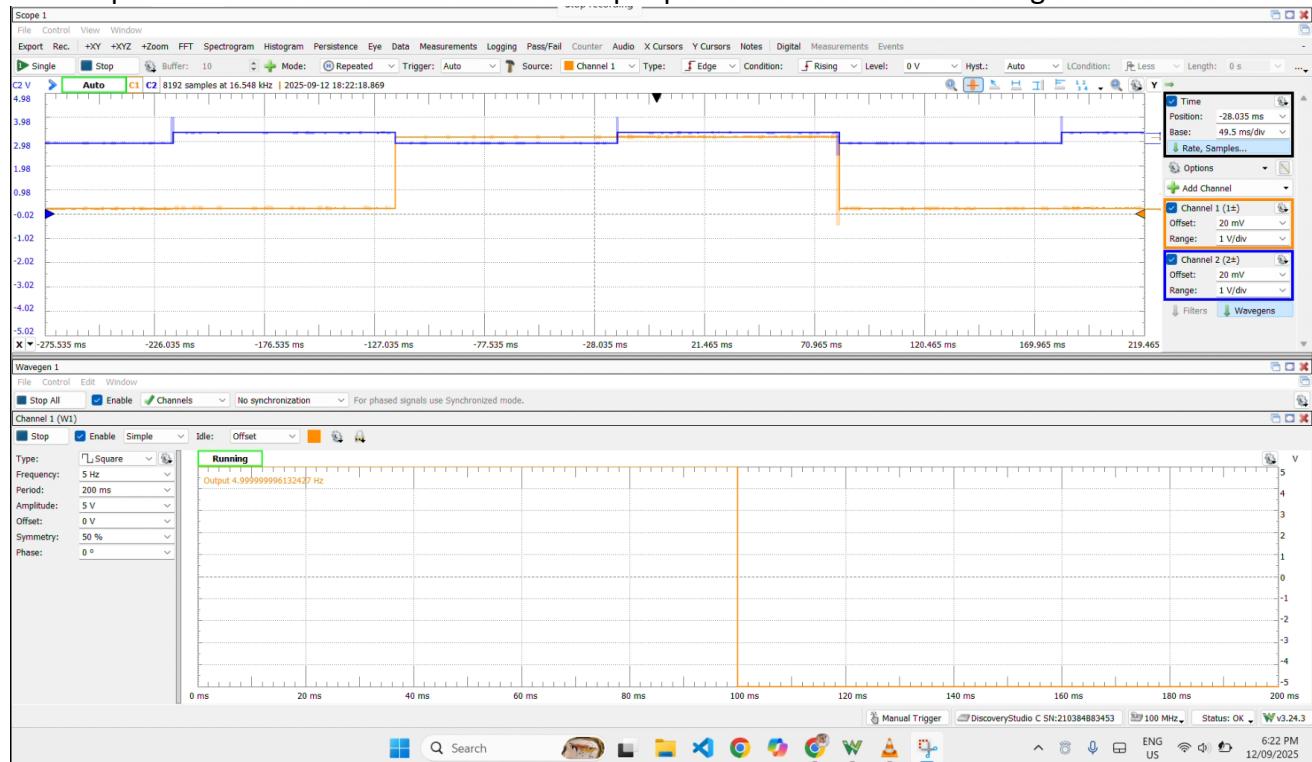
The circuit was implemented with two dual JK flip flops and was obtained as shown in the image below:



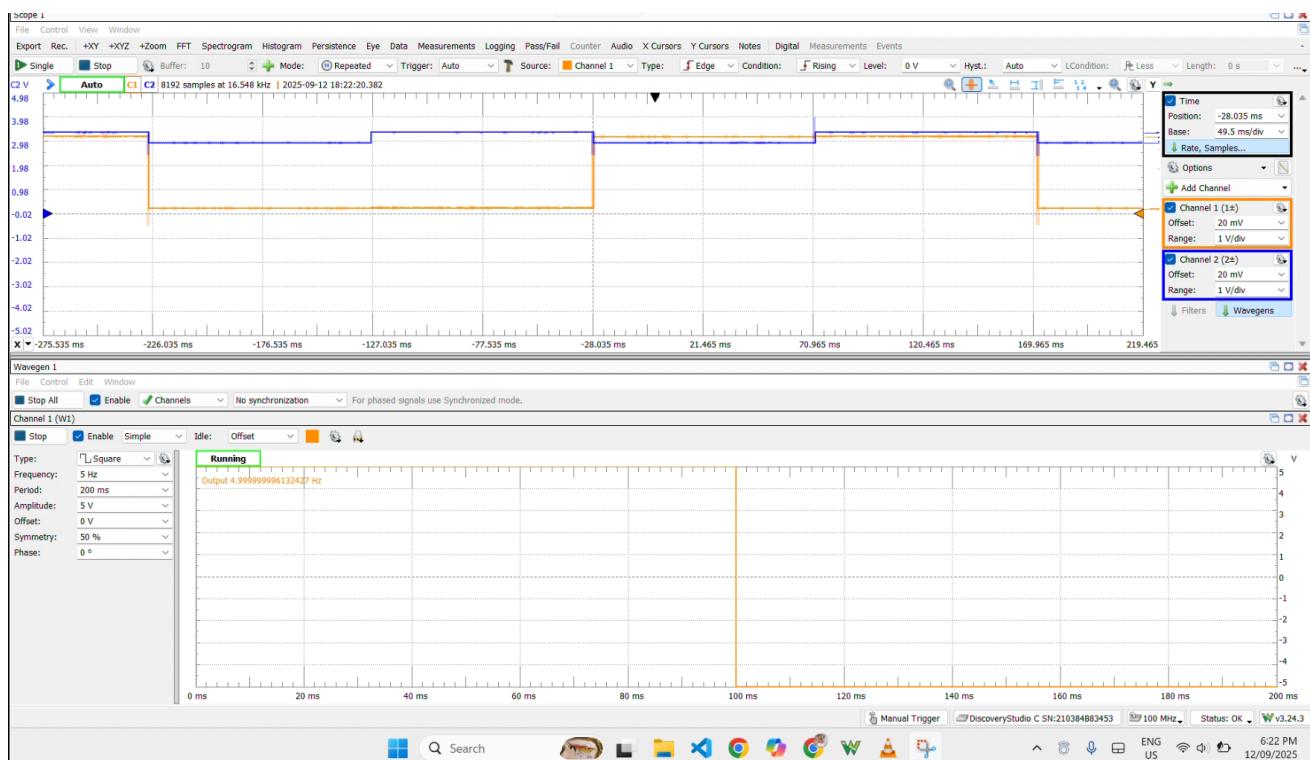
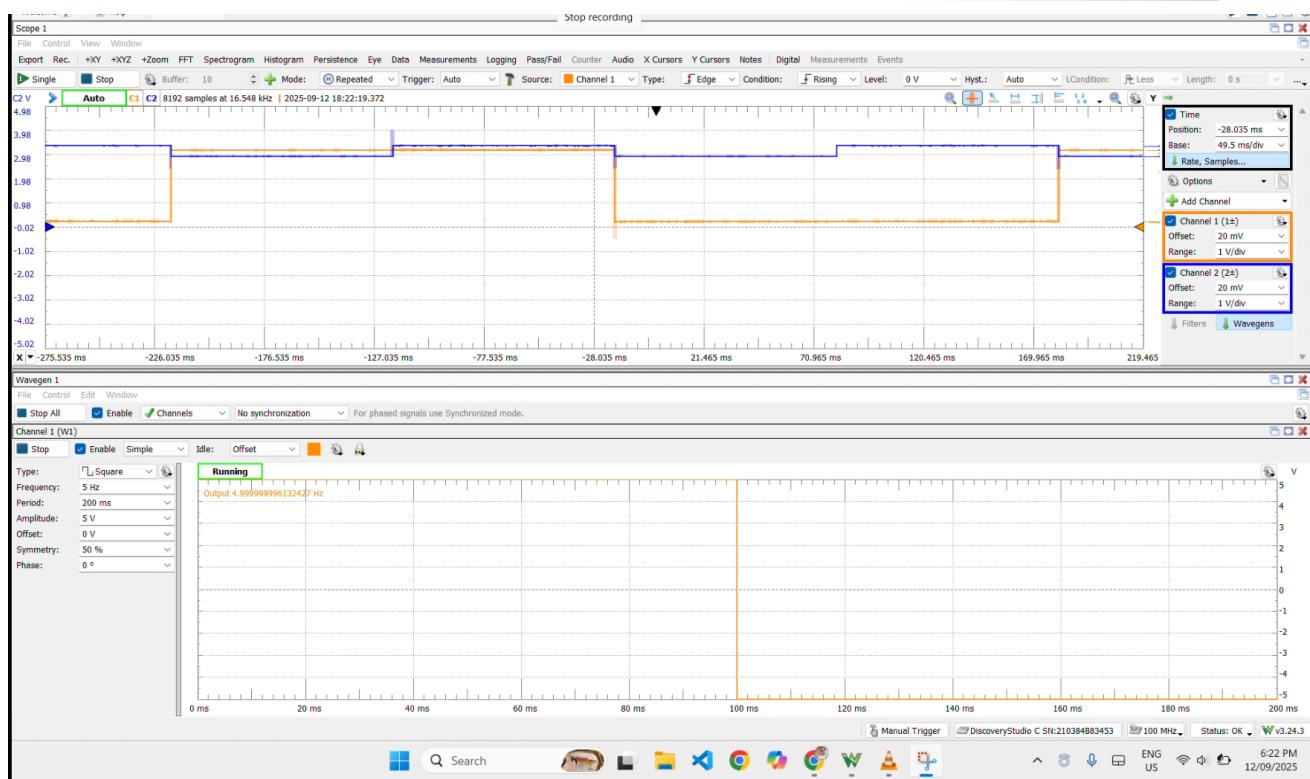
2.2 Measure and record the signal from the corresponding outputs.

The circuit was constructed, and the output signals were observed in waveforms application. The following outputs were obtained under different conditions:

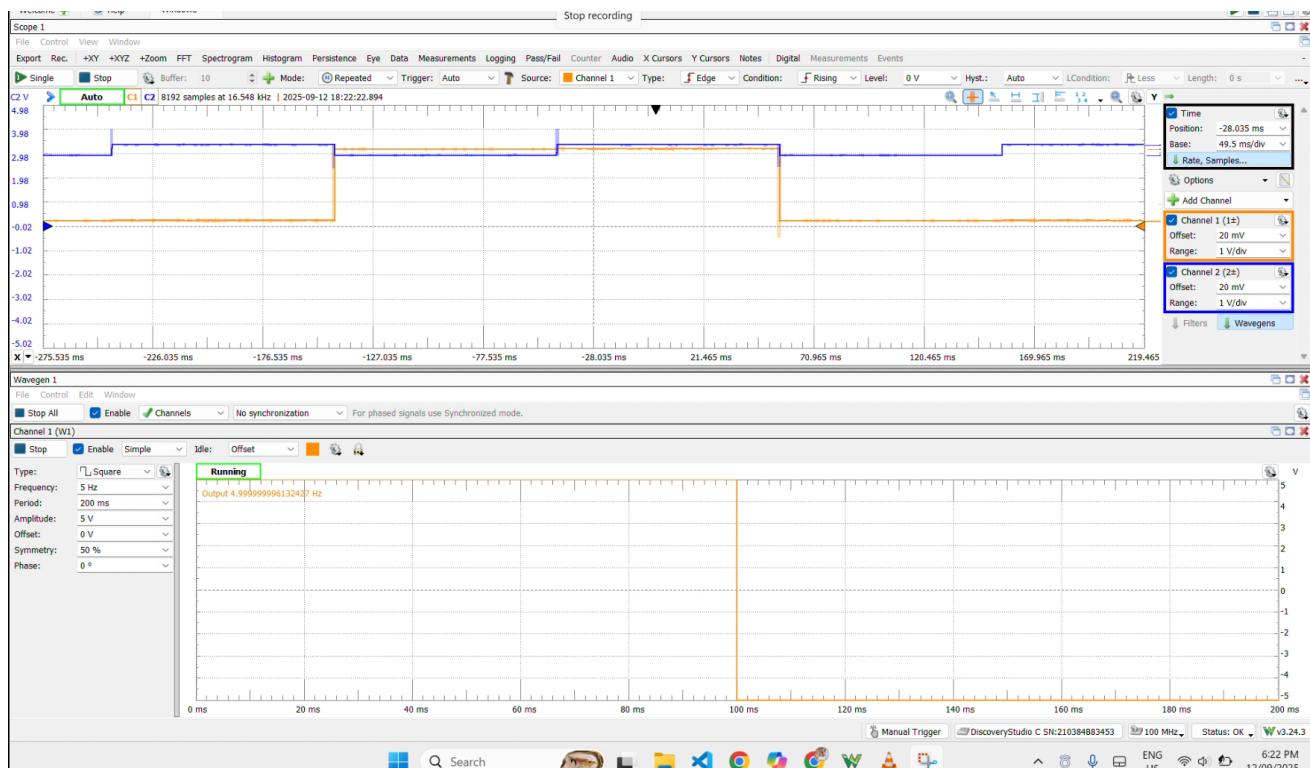
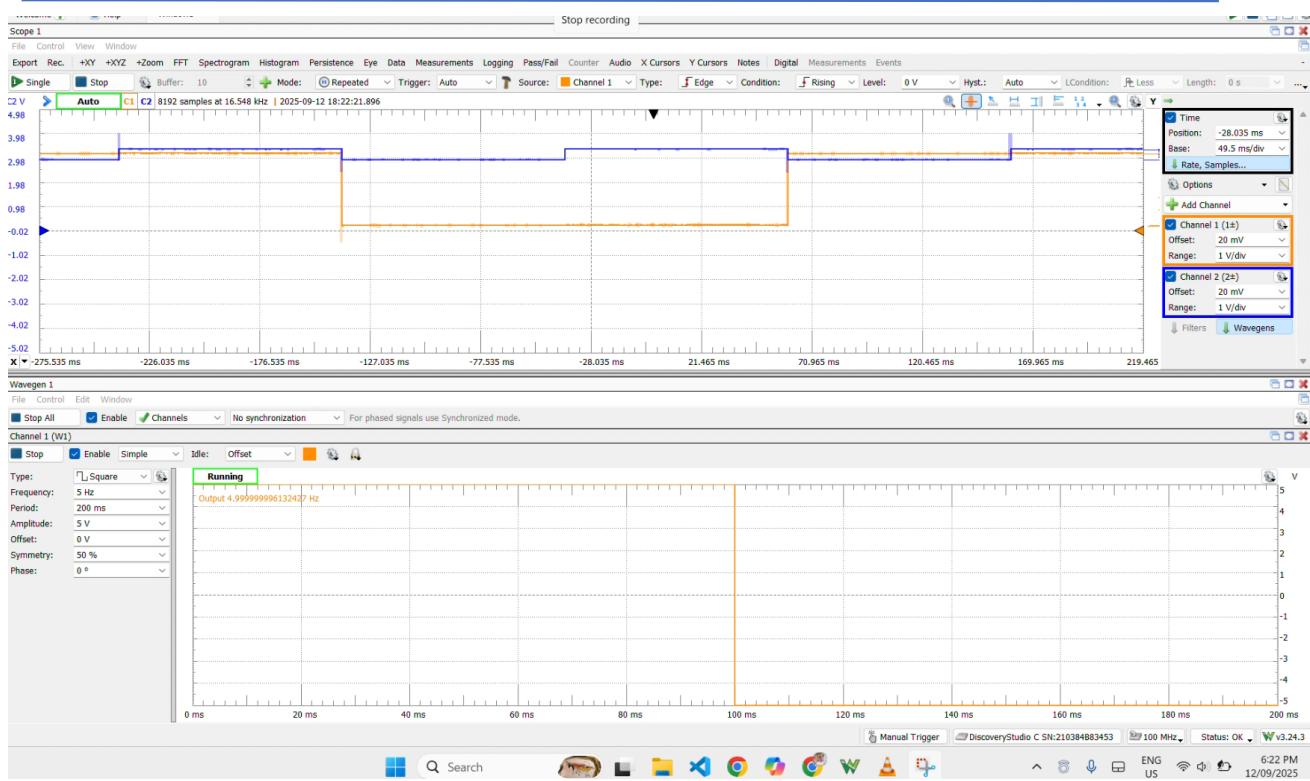
The outputs were observed from the two JK flipflops where we obtained the signals as:



UNIVERSITY OF CANBERRA
INTRODUCTION TO COMPUTER ENGINEERING (8223/10096)
TUTORIAL WEEK 7 Assignment Template



UNIVERSITY OF CANBERRA
INTRODUCTION TO COMPUTER ENGINEERING (8223/10096)
TUTORIAL WEEK 7 Assignment Template



From the above snapshots, it is clearly observed that the period of the signal obtained from second JK flipflop is exactly half of the one obtained from the first flip flop.

2.3 State the purpose of the circuit.

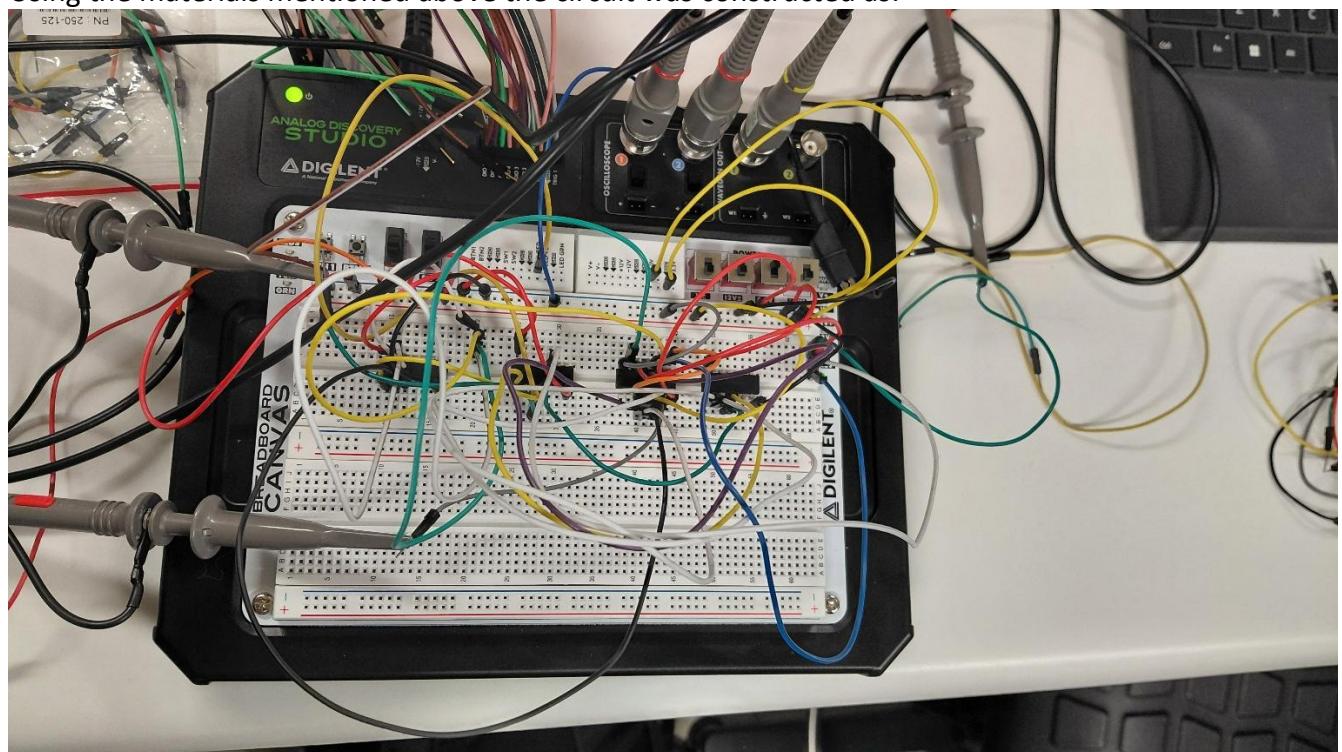
Answer: The circuit acts as a 3-bit asynchronous counter which counts the binary numbers from 0 to 7 representing the 8 states. All the flip flops have different clocks and hence are synchronous. Here the output of one flip flop serves as a clock for the next flip flop.

3. Hardware Implementation Third Sequential Circuit (25 marks)

Materials required:

1. IC7400 2 input NAND gate
2. IC7480 2 input AND gate
3. IC7476 dual JK flip flop
4. Bread board

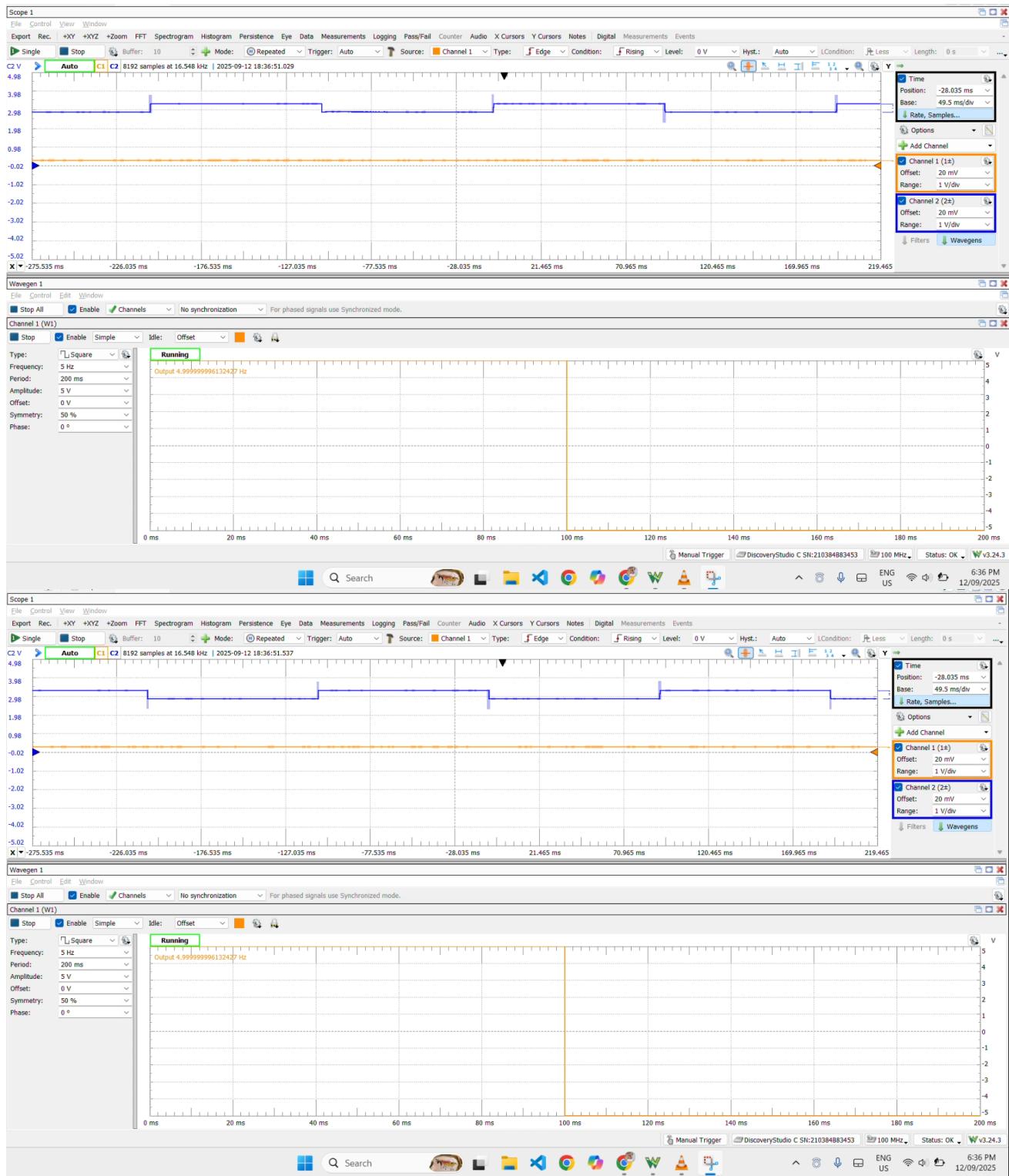
Using the materials mentioned above the circuit was constructed as:



3.2 Measure and record the signal from the corresponding outputs.

The circuit was simulated, and the signals were observed and were obtained as follows:

UNIVERSITY OF CANBERRA
INTRODUCTION TO COMPUTER ENGINEERING (8223/10096)
TUTORIAL WEEK 7 Assignment Template



The output obtained from the hardware simulation was not as per the desired output to be obtained. This error was resulted due to the error in IC which caused the issue.

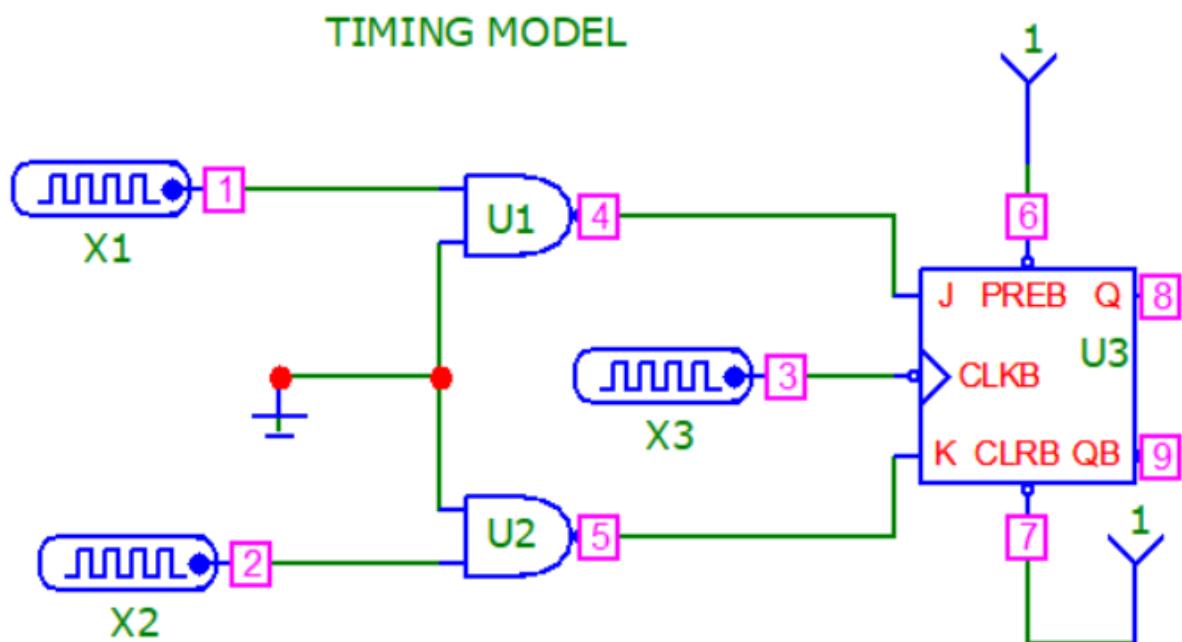
3.3 State the purpose of the circuit.

Answer: The circuit represents a three-bit synchronous counter where all the JK flip flops are provided with the same clock. The circuit represents a counter where the leftmost flip flop represents the least significant bit and the rightmost flip flop represents the most significant bit.

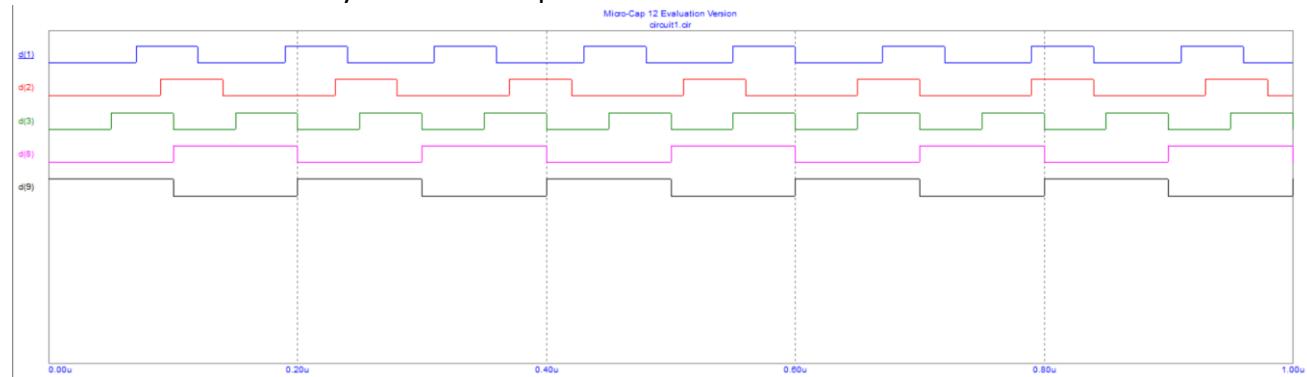
4. Circuit Simulation in Micro-Cap 12 (25 marks)

The circuit was also constructed in micro-cap and the circuit was simulated. The circuits on simulation yielded the following outputs:

For circuit 1:

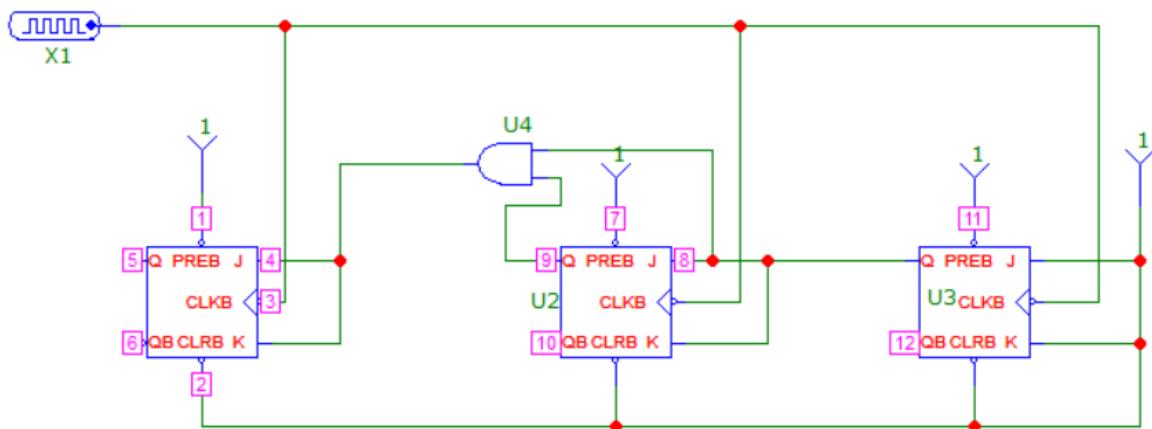


The circuit on simulation yielded the output as follows:

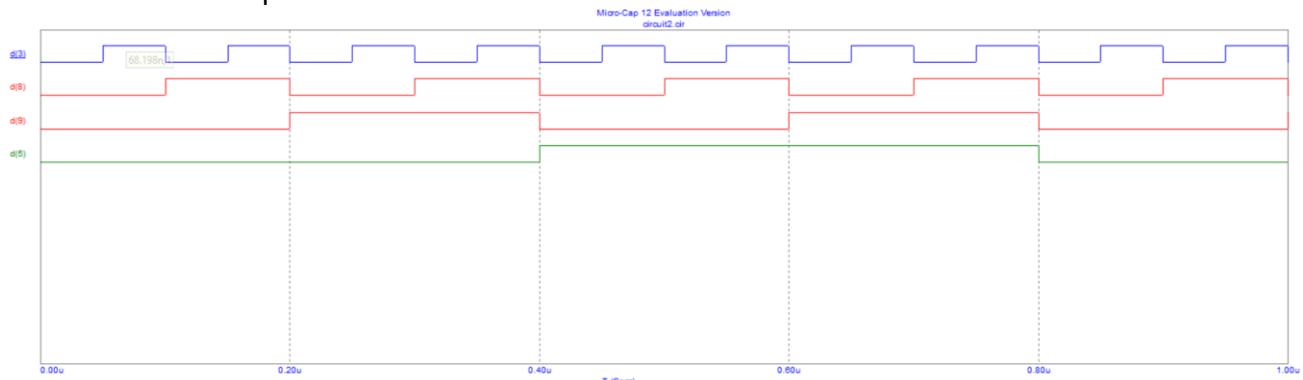


The signals D1, D2 and D3 represent the clock and two inputs A and B:
The output Q is represented by D8 and the complement of Q is represented by D9.
The signal represents the behavior of JK flip flops where the signal is high when both J and K are high. Similarly, on J=0 and K=1 the circuit yields output 0.

For circuit 2:

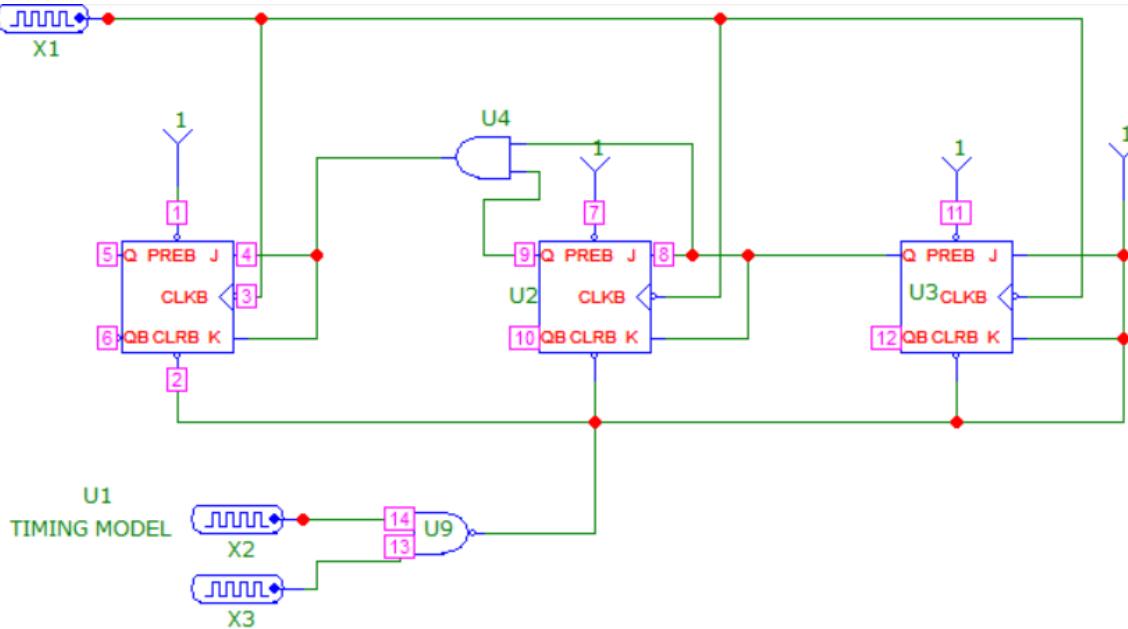


For circuit 2 the output is obtained as:

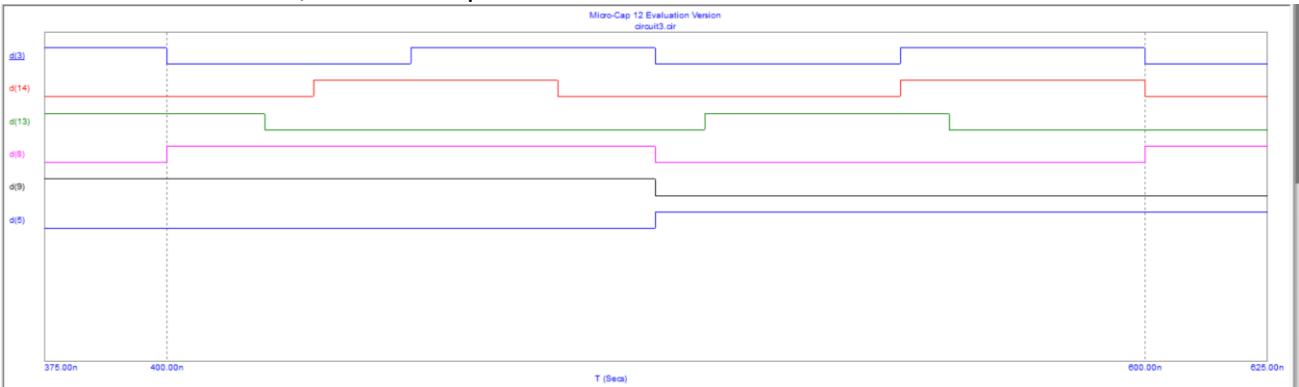


The signal D1 is regarded as the clock. The output from two flip flops are observed and the signals represent a three-bit counter. The signal outputs represent the counting from 0 to 7 which represent the behavior of three-bit asynchronous counters.

For circuit 3



The circuit is simulated, and the output is obtained as:



The simulation represents the behavior of three-bit synchronous counter. The output signals represent the counting through the signals of 0 to 7 which represent the behavior of the synchronous three-bit counter.

Hence, the outputs from the hardware implementation and the simulation through microcap match and show the same behavior.

REFERENCES

- [1] Floyd, Th.L. Digital Fundamentals, Pearson, 2015
- [2] Waveforms Reference Manual : https://mil.ufl.edu/3701/docs/Waveforms_tutorial.pdf