Checkpoint 3

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In this checkpoint, 32 32-bit regfiles are built by using D-flip-flop and tri-state buffers.

Read and write operation can be achieved.

ctrl\_writeEnable is the wirte enable signal,

ctrl\_readRegA, ctrl\_readRegB is the select read input.

ctrl\_writeReg is the select write input.

data\_writeReg is the data needed to be written.

data\_readRegA, data\_readRegB are the output.