EXPERIMENT - 7

OBJECTIVE

Study of 4 bit Asynchronous up-down counter

EQUIPMENT NEEDED

Components	Quantity
1) IC 7473 Dual Jk flip flop	2
2) IC 7408 2 input AND Gate	3

THEORY

Flip-Flop

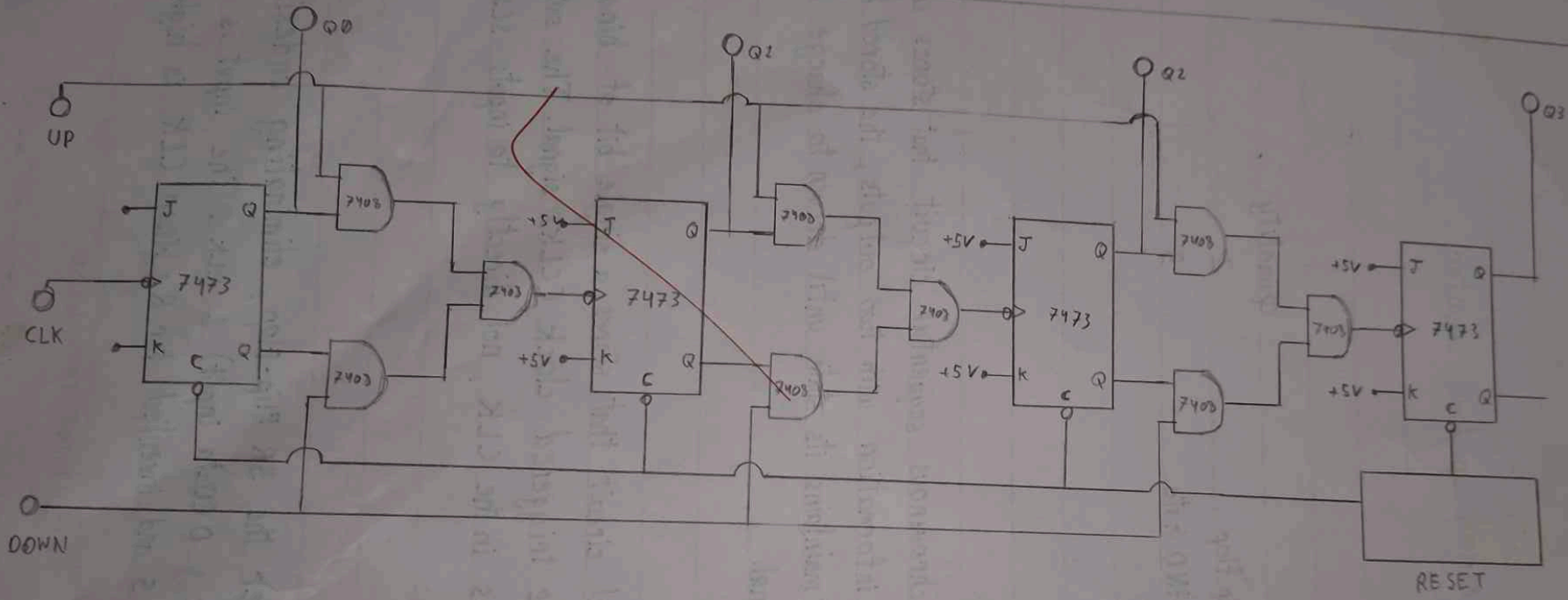
An edge-trigged synchronous sequential circuit that stores a single bit of binary information with two outputs; the stored bit, & its complement. It maintains its state until driven to change by an input ~~register~~ signal.

SR Flip-Flop

A clocked sequential circuit that stores a single bit of binary controlled by an edge triggered clock (CLK) signal. The output responds to changes in the CLK, not directly to inputs S(Set) & R(Reset).

D Flip-Flop

An improvement over the SR Flip-Flop, eliminating undesirable states. It has 2 inputs; D(Data input) & CLK. The input is directly connected to S and inverted for R. When CLK is high, the


Q0
Q1
Q2
Q3
UP
CLK
DOWN
RESET
7473
7403
+5V
J
K
C
Q

D input is stored; When CLK is low, the previous state is maintained.

JK Flip-Flop

A Refinment of the SR Flip-Flop, eliminating ~~indete~~ indetermin-ate states. Inputs J & K act Like S & R, Respectively. J sets the flip flop, K Resets it, and when both are high, the output toggles to the complement of its previous state.

PROCEDURE

When Switch is pressed it indicates switch is in HIGH Position.
When Switch is unpressed it indicates switch is in LOW Position.

Up-Counter

1) Make connection as shown in figure
2) Connect +5v to pin 14 of IC 7408 & pin 4 of IC 7473 and GND to pin. 7 of IC 7408 & pin 10 of IC 7473.
3) Connect I1 to UP & I2 to DOWN. Here S1 & S2 will be input Switches
4) Connect I0 to Reset key which is connected to clear.
5) Set the input switches S0-S2 initially to LOW Position.
6) Connect MANUAL PULSER T2 (L-H-L) to CLK. Here it will act as a Manual Pulser switch.
7) Connect Q0 to O0, Q1 to O1, Q2 to Q2, Q3 to O3 of Logic Level indicator.
8) Switch ON THE Power
9) Set S0 & S1 to ~~LOW~~ HIGH & S2 to LOW
10) Observe output at LEDs & verify truth table.

INPUT		LED DRIVER			
S1	S2	LED 4	LED 3	LED 2	LED 1
L	L	L	L	L	L
H	L	L	L	L	H
H	L	L	L	H	L
H	L	L	L	H	H
H	L	L	H	L	L
H	L	L	H	L	H
H	L	L	H	H	L
H	L	L	H	H	H
H	L	H	L	L	L
H	L	H	L	L	H
H	L	H	L	H	L
H	L	H	L	H	H
H	L	H	H	L	L
H	L	H	H	L	H
H	L	H	H	H	L
H	L	H	H	H	H

Conclusion :

A 4-bit Asynchronous up-down counter is studied

Assessment of the Experiment / Assignment :

Timely Submission (07)	Presentation (06)	Understanding (12)	Total (25)	Signature of Teacher with date
07	06	11	24	14/10/24