EXP NO :- 2

26-08-2024

OBJECTIVE

Study of binary Adders
A. Half Adder
B. Full Adder

THEORY

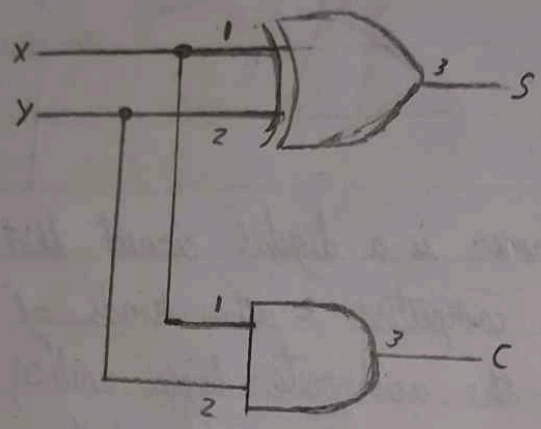
ADDER

In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers & other kinds of processor, adders are used not only in the arithemetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indicies, and simple.

HALF ADDER

Half adder is a combinational arithemetic circuit that adds two numbers & produces a sum bit (S) & carry bit (C) as the output. If A & B are the input bits, then sum bit(S) is the X-OR of A & B & the carry bit (C) will be the AND of A & B. From this it is clear that a half adder circuit can be easily constructed using 1 X-OR gate & 1 AND gate. Half adder is the simplest of all adder circuit, but it has a major disadvantage. The half adder can add only two bits (A & B) & has nothing to do with the carry if there is any in the input. So if the input to a half adder have a carry, then it will be neglected it & adds only the A & B bits. That means the binary addition process is not complete & that's why it is called a half adder.

A. HALF ADDER



Input 1 X	Input 2 Y	Theoretical		Practical	
		Sum	Carry	Sum	Carry
0	0	0	0	0	0
0	1	1	0	1	0
1	0	1	0	1	0
1	1	0	1	0	1

FULL ADDER

This type of adder is a little more difficult to implement than a half adder. The main difference between a half adder & a full adder is that the full adder has 3 inputs & two outputs. The first two inputs are A & B & the third input is an input carry designated as CIN. When a full adder logic is designed we will be able to string eight of them together to create a byte wide adder & cascade the carry bit from one adder to the next.
The output carry is designated COUT & the normal output is designated as S. Take a look at the truth table.

A. HALF ADDER

EQUIPMENT NEEDED

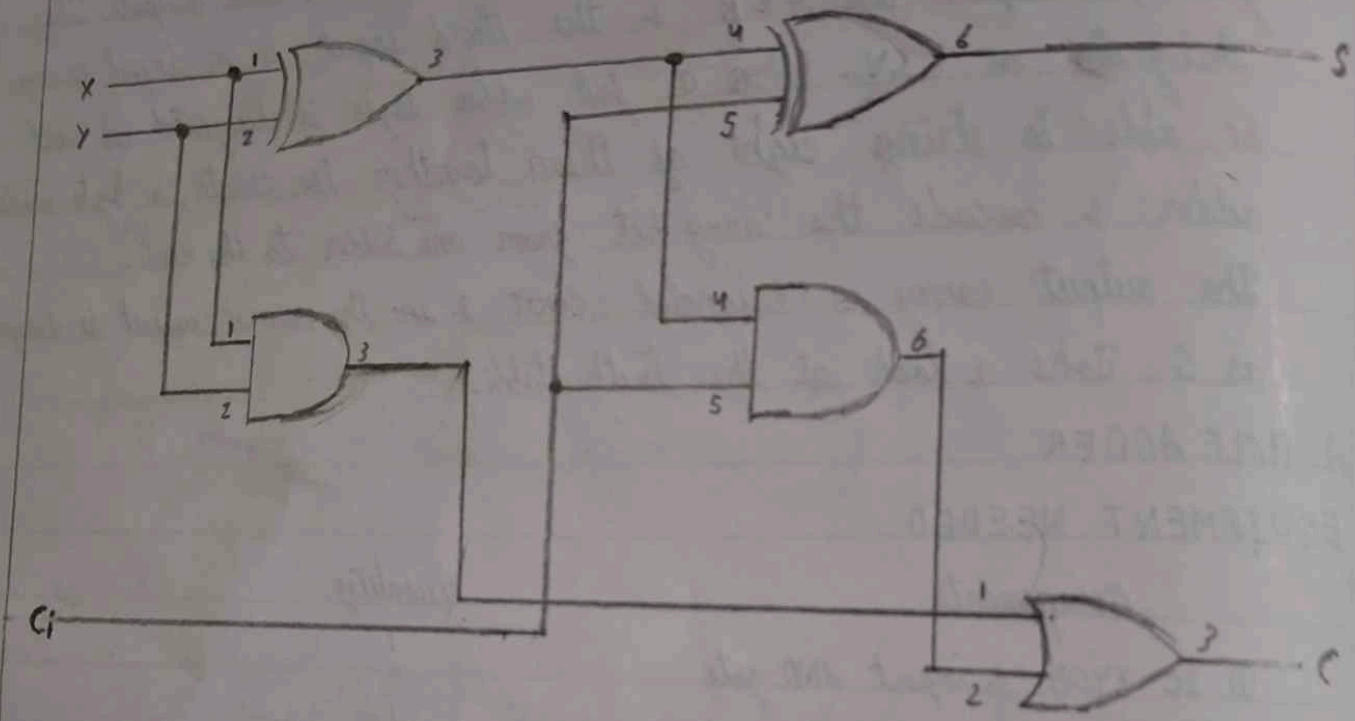
Components	Quantity
① IC 7408 2 input AND gate	1
② IC 7486 2 input XOR gate	1

PROCEDURE

When Switch is presed it indicates switch is in "HIGH" position
When Switch is impresed it indicates switch is in "LOW" position

1) Make connections on bread board as shown in figure
2) Connect +5V to pin no. 14 & GND to pin no 7 of IC 7408 & IC 7486.
3) Connect inputs X & Y (pins 1&2) of AND & XOR gate to the input switches 10 & 11 respectively.
4) Connect Sum(S) & Carry (C) to 00 & 01 of 10 bit LED indicator, respectively

B. FULL ADDER



Input 1 X	Input 2 Y	Input 3 C_i	Theoretical		Practical	
			Sum	Carry	Sum	Carry
0	0	0	0	0	0	0
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	1	0	1
1	1	0	0	1	0	1
1	1	1	1	1	1	1

5) Switch ON the kit.
6) Set the input switch S0 & S1 initially to LOW position.
7) Observe outputs S & C on LED L0 & L1 of 10 bits LED indicator, respectively.
8) Observe the output for different input combination as shown in truth table.
9) Verify truth table.

B. FULL ADDER

EQUIPMENT NEEDED

components	Quantity
① IC 7408 2 input AND gate	1
② IC 7432 2 input OR gate	1
③ IC 7486 2 input XOR gate	1

PROCEDURE

1) Make connections on bread board as shown in figure.
2) Connect +5v to pin 14 & GND to pin 7 of IC 7408, 7432 & 7486.
3) Connect inputs X & Y (pins 1&2) of AND & XOR gate to the inputs switches I2 & I3. respectively.
4) Connect C_i to input switch I4 as shown in figure
5) Connect Sum (S) & Carry out (CO) to O2 & O3 of 10 bit LED display, respectively.
6) Switch ON the kit.
7) Set the input switches S2, S3, & S4 initially to low position.

8) Observe outputs S & Co on led L2 & L3 of 10 bits LED display, respectively.
9) Observe the output for different input combination as shown in truth table
10) Verify truth table

OBSERVATION AND RESULT

Full adder can be implemented using two half adder. Adders are studied & truth tables are verified.

Conclusion :

Full Adder can be implemented using two half adder. Adders are studied & truth tables are verified

Assessment of the Experiment / Assignment :

Timely Submission (07)	Presentation (06)	Understanding (12)	Total (25)	Signature of Teahcer with date
07	06	11	24	21/9/24