OBJECTIVE Study of operation of all logic gotes

THEORY

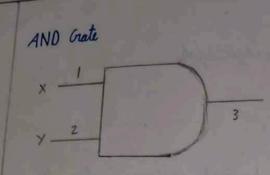
Legic gate is on idealized or physical Senice implementing a boolem function, that is, it performs a lagical aperation on one or more legic inputs & products a single lagic autput.

Depending on the contest, the term may refer to an ideal logic gate, one that has far instance yere rise time & unlimited for out, or it may refer to an nor ideal physical cluice.

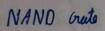
fogic gates are primarily implemental using diodes or transisters acting as electronic switches, but can also be constructed using electromagnetic relays (relay logic), physical logic, preumatic logic optics, malueles, or even nuchonical events elements. With amplification logic gates can be conseaded in the some way that boolean functions can be composed, allowing the construction of a physical model of all of boolean lagic, & therefore, all of the algorithms & model of all of boolean lagic, & therefore, all of the algorithms & model of all of boolean lagic, & therefore, all of the algorithms & model of all of boolean lagic, & therefore paid on logic.

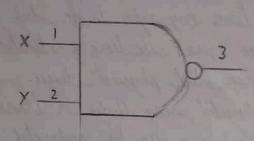
And Crate

The AND gote is a basic digital lagis gote that implements logic conjunction - it behaves according to the truth table to the right. A HIGH autput (1) results only if both the inputs to the AND gote are HIGH. If neither ar only one input to the AND gote is HIGH, a LOW output results.



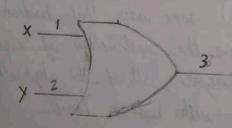
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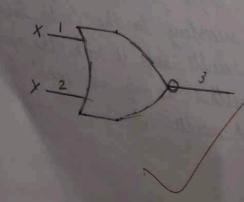
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OR Crate



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NOR crate



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NOT Grate (inverter)

The NOT gate is also known as an inverter; Simply because it changes the input to its opposite. The NOT gate accepts only one input s the output is the opposite of the input. In other words, a law vallage input (0) is converted to a high-vallage autput (1).

OR Crets

The OR gate is a gar digital lagic gate that implements lagical disjunction - it behaves according to the truth table to the right. A HIGH output result if one or both the inputs to the gate are HIGH. If neither are HIGH, a law output results.

NAIND crate

The Aligated AND, NOT AND, or NAND gate is the opposite of the digital AND gate, & behaves in a morn morner that corresponds to the opposite of AND gate, as shown in the table on the right.

A face (0) output results only if both the inputs to the gate are

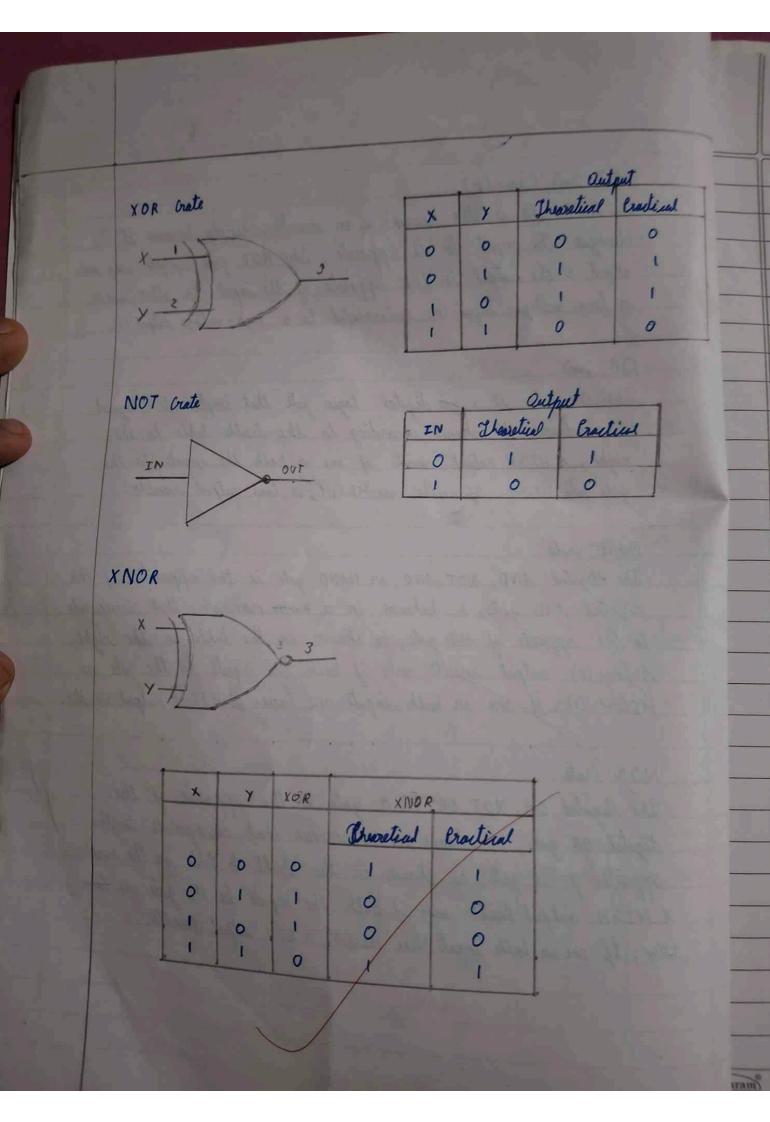
MIGH (1). If one or both inputs are law, A HIGH output results.

NOR Crate

The Meyated OR, NOT OR, NOR gate is the opposite of the digital OR gate, & behaves in a monner that corresponds to the appointe of OR gate, as shown in the truth to table on the right.

A HIGH output Results only if both the input to the gate are took LOW; If one or both inputs are HIGH, a LOW output Results.

ındaram



The XOR (sometimes EOR or EX-OR gate) is a go digital logic gate that implements an exclusive or; that is, a true output (1) result if one & only one, of the input to the gate is true (1). If both inputs are false or both are true, a false output Results.

XNOR Grate

The Megatist XOR, XNOR gute is the apposite of the XOR gate, & behaves in a mormer that corresponds to the apposite of the XOR gate, as shown in truth table. A High output results only if both the input to the gate are law or HIGH. A LOW output results if only one of the input or is high.

EQUIPMENT NEEDED

component	The first of the same of the same	quantity
	2 input AND chale	
	2 input OR Grate	
IC 7400	2 input IVANO Crate	1
	2 input NOR Grate	1
	2 input X-OR Crote	
	NOT crate	1

PROCEDURE

When Switch is pressed it indicates switch is in high position.
When Switch is appressed it indicate switch is in law position.

AND Grate

- 1) Clase IC 7408 on bread board.
- @ Connect +5v to pin no. 14 of IC 7408 & GIND to gin no. 7
- 3 connect input x & Y Cpins 122) of AND to the input smitches 102 respectively
- @ Connect inputs output of AND crate i.e gin na.03 to 00 of 10 autput bed LED indicators.
- (3) Switch on the kit.
- 6) set switches so 231 initially to law position.
- 3 Observe the output for diffront input combination as shown in truth table
- 1 Verify Truth Toble.

NANO Crate

- O Place IC 7400 on board Broad board
- @ Connect +sv to pin 14 of IC 7400 & GND to pin 7
- 3 Connect inputs X & Y (pins 182) of NAND gate the the input suntiches 10 & respectively
- (9) connect output of NAND gate 1.e pin 3 to 00 of 10 output LED indicator
- 3 switch on the kit
- 6) set switcher 50 % SI unitially to law position
 - 3 Oberus output of NAND crute on LED LO of 10 output LED indicates

- 1 Observe the autput for diffrent input combination as chaun in truth table.
- 1 Verify truth table.

OR crate

- 1 Clase IC 7432 on bread board
- @ Connect + sv to lin 14 of IC7432 & GND to jun na.7.
- 3 Connect input x x y (pin 1 x 2) of OR gate to the imput switcher 10 x 11 respectively
- 1 Connect output of OR gate i.e pin 3 to 00 of 10 autput LED indicater.
- 3 Switch on the & kit.
- O set the input suitcher so > sI initially to LOW position
- 3 Observe output of OR gote on LED LO of 10 output LED indicator
- 3 Observe the output for diffrent input combination as shown in truth table
- @ derify truth toble

NOR Crate

- 1) Clase IC 7402 on bread board.
- Office Connert +5v to pin 14 of IC 7402 & GND to pin 7.
- 3 Connect input x & y (pin 2 & 3) of NOR gate to the input switches
- @ Connect autput of NOR gate i.e pin 1 to 00 of 10 autput LED indicates
- 5 Switch on the kit
- 6 Set the input switches so 2 31 initially to LOW position
- 3 Observe output of NOR gute on LED LO of 10 output LED indicates
- (3) Observe the autput for different input combinations as chausen in

truth table.

(1) Verify truth table

XOR Grate

- O Place IC 7486 on bread board
- 1 Connect +5V to pin 14 of IC 7486 & GND to gin 7
- 3 Connect autput of XOR gate i.e pin 3 to 00 of 10 autput LED indicates
- (1) respectively
- 3 Switch on the kit
- 6) Set the input switches so & SI initially to LOW position
- 3 Observe output of KOR gate on led LOZZI of 10 output LED indicator
- 1 Observe the autput for diffrent input combination of shown in truth table
- 1 verify truth table.

NOT gate

- 10 clave IC 7404 on board bread board
- @ Connect +SV to pin 14 of IC 7404 & CNYD to pin 7
- 3 Connect inputs IN (pin 1) of NOT gute to the input switch 10.
- (a) Connect output of not NOT gate i.e pin 2 to 00 of 10 autput LED endicator
- (5) Switch on the Rit.
- (B) Set the input switch so to law initially.
- (7) Observe output of NOT gate on LED LO of 10 hits output
 LED indicator

8 Observe the in truth, 1 Verify truth	e entput for differ table. The table	ent input combi	ration as she	uun
RESULT			700	. 43
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working of all busic gate is studied & truth trable verified.

Assessment of the Experiment / Assignment :

Timely Submission (07)	Presentation (06)	Understanding (12)	Total (25)	Signature of Teahcer with date
07	06	11	24	ERC 26/8/24