VLSI System Design (Graduate Level)

Fall 2018

HOMEWORK III

REPORT

Must do self-checking before submission:

Compress all files described in the problem into one tar

All SystemVerilog files can be compiled under SoC Lab environment

All port declarations comply with I/O port specifications

Organize files according to File Hierarchy Requirement

No any waveform files in deliverables

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|  |  |
| --- | --- |
| Cache Architecture | |
| FSM(READ) | |
|  | |
| STATE EXPLANATION | |
| IDLE | Waiting state ,if there is any cpu read signal ,the next state will be check hit read |
| CHECK\_HIT\_READ | Check if the search in cache is hit or not  the hit condition will be (TA\_out==TA\_in )&&(single\_valid\_data)  if miss the next condition will be send read mem1  if hit the next condition will be IDLE |
| SEND\_READ\_MEM1~4 | The state will send the request to cpu wrapper to get data from main memory and the next state will be read\_mem |
| READ\_MEM1~4 | The state is waiting for the finsh of reading data from main memory after reading a cache line data(128bits) reading 4 times from main memory the next state will return to IDLE state |
| Detailed | Because when the design of CPU\_wrapper receive the request from cache ,it will active D\_wait at the same time thus it chould have two state ,one for sending the request signal  One for waiting the D\_wait signal to drop. |

|  |  |
| --- | --- |
| Cache Architecture | |
| FSM(READ) | |
|  | |
| STATE EXPLANATION | |
| IDLE | Waiting state ,if there is any cpu read signal ,the next state will be check hit write |
| CHECK\_HIT\_WRITE | Check if the search in cache is hit or not .  the hit condition will be (TA\_out==TA\_in )&&(single\_valid\_data).  if hit the next condition will be WRITE\_HIT and send the wrinting request to CPU\_wrapper rat the same time.  if hit the next condition will be WRITE\_MISS and send the wrinting request to CPU\_wrapperat the same time. |
| WRITE\_HIT | Check if writing operation to main memory is finish or not .  If finish it will return to IDLE |
| WRITE\_MISS | Check if writing operation to main memory is finish or not .  If finish it will return to IDLE |
| Detailed | Because when the design of CPU\_wrapper receive the request from cache ,it will active D\_wait at the same time thus it chould have two state ,one for sending the request signal  One for waiting the D\_wait signal to drop. |

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| --- |
| Waveform |

|  |  |
| --- | --- |
| Synthesize result(8ns) | |
| TIMING |  |

|  |  |
| --- | --- |
| AREA |  |
| POWER |  |

|  |  |
| --- | --- |
| APR | |
| Before Placement  Verify Geometric |  |
| Before Placement  Verify Connectivity |
| Post\_route  Setup\_verify |  |
| Post\_route  holdup\_verify |  |

|  |  |
| --- | --- |
| Post\_cts  Setup |  |
| Post\_cts  Holdup |  |
| ANTENNA  &  GEOMETRIC  CONNECTIVITY  &  VERIFY |  |

|  |
| --- |
| Floorplan\_View |
|  |
| Amoeba\_View |
|  |
| Physical\_view |
|  |

|  |  |
| --- | --- |
| Simulation | |
|  |  |
|  | **Syn0** |
| **Syn1** | **Syn2** |

|  |  |
| --- | --- |
| Superlint | |
|  | |
| Warning Explantion | File format 為命名沒有和module 同名 不影響合成  Coding style 是因為寫法習慣的問題 combination 電路中 會有接線來自 sequential 的區塊 不影響合成 一樣適合出flipflop |
| Superlint within 95% | / = >95% |

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| --- |
| 心得 |
|  |