VLSI System Design (Graduate Level)

Fall 2018

HOMEWORK III

REPORT

Must do self-checking before submission:

Compress all files described in the problem into one tar

All SystemVerilog files can be compiled under SoC Lab environment

All port declarations comply with I/O port specifications

Organize files according to File Hierarchy Requirement

No any waveform files in deliverables

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|  |
| --- |
| Cache 架構 |
|  |

|  |  |
| --- | --- |
| 合成結果(8ns) | |
| TIMING |  |
| AREA |  |
| POWER |  |

|  |  |
| --- | --- |
| APR | |
| Before Placement  Verify Geometric |  |
| Before Placement  Verify Connectivity |
| Post\_route  Setup\_verify |  |
| Post\_route  holdup\_verify |  |

|  |  |
| --- | --- |
| Post\_cts  Setup |  |
| Post\_cts  Holdup |  |
| ANTENNA  &  GEOMETRIC  CONNECTIVITY  &  VERIFY |  |

|  |
| --- |
| Floorplan\_View |
|  |
| Amoeba\_View |
|  |
| Physical\_view |
|  |

|  |  |
| --- | --- |
| Simulation | |
|  |  |
|  | **Syn0** |
| **Syn1** | **Syn2** |

|  |  |
| --- | --- |
| Superlint | |
|  | |
| Warning Explantion | File format 為命名沒有和module 同名 不影響合成  Coding style 是因為寫法習慣的問題 combination 電路中 會有接線來自 sequential 的區塊 不影響合成 一樣適合出flipflop |
| Superlint within 95% | / = >95% |

|  |
| --- |
| 心得 |
|  |