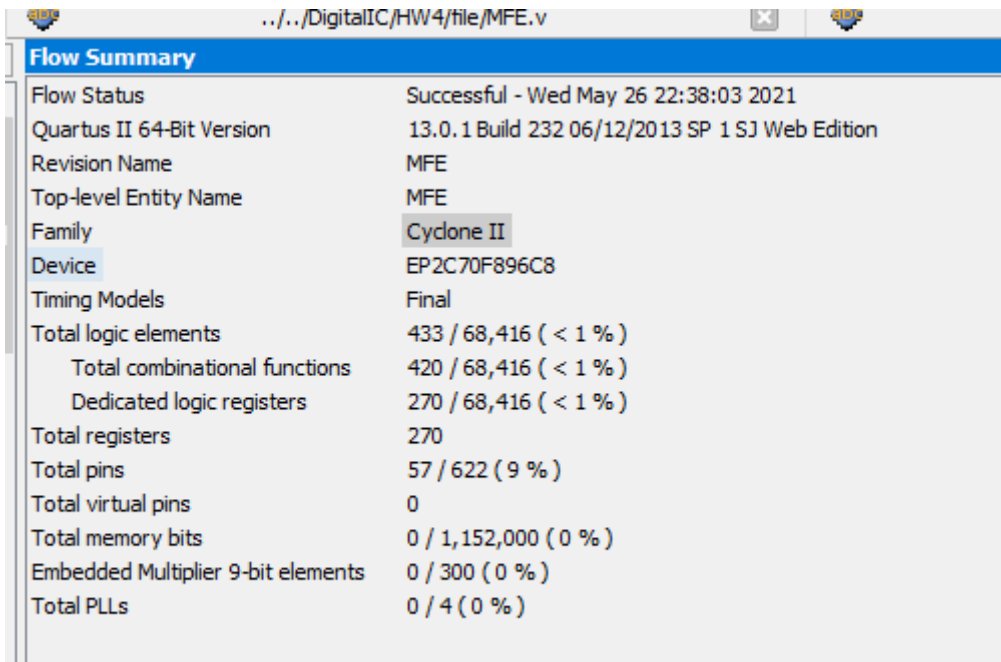
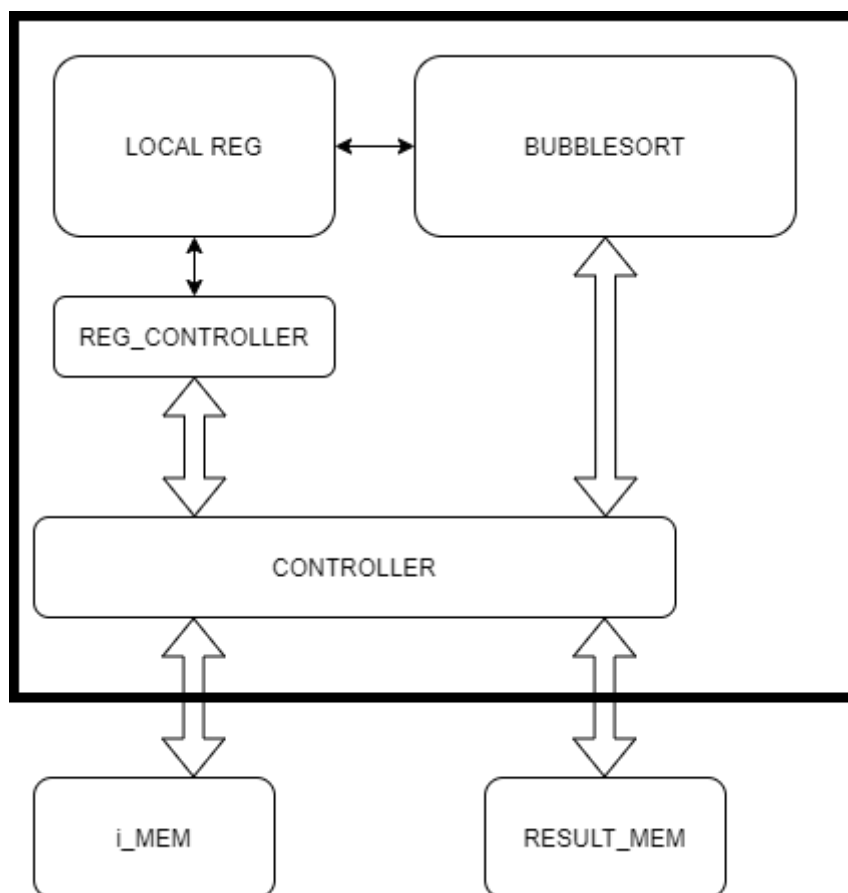
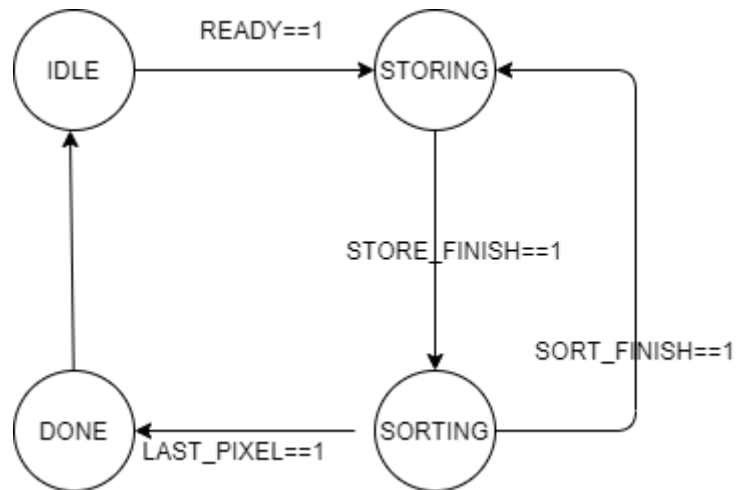


## 2021 Digital IC Design Homework 4

NAME	杜冠勳				
Student ID	N26094833				
Simulation Result					
Function al simulati on	Pass	Gate- level simulati on	Pass	Gate-level simulation time	simulation time 1204235391(ns) 12042353919(p)
<pre>SIM 4&gt; run -all ----- START!!! Simulation Start ..... ----- Result image is correct ! ----- ----- S U M M A R Y ----- Congratulations! Result image data have been generated successfully! The ----- ** Note: \$finish      : D:/DigitalIC/HW4/file/testfixture. Time: 8601675 ns  Iteration: 0  Instance: /testfixtur 1</pre>				(your post-sim result)	
Synthesis Result					
Total logic elements	423				
Total memory bit	0				
Embedded multiplier 9-bit element	0				
Clock width (Cycle)	35				
					

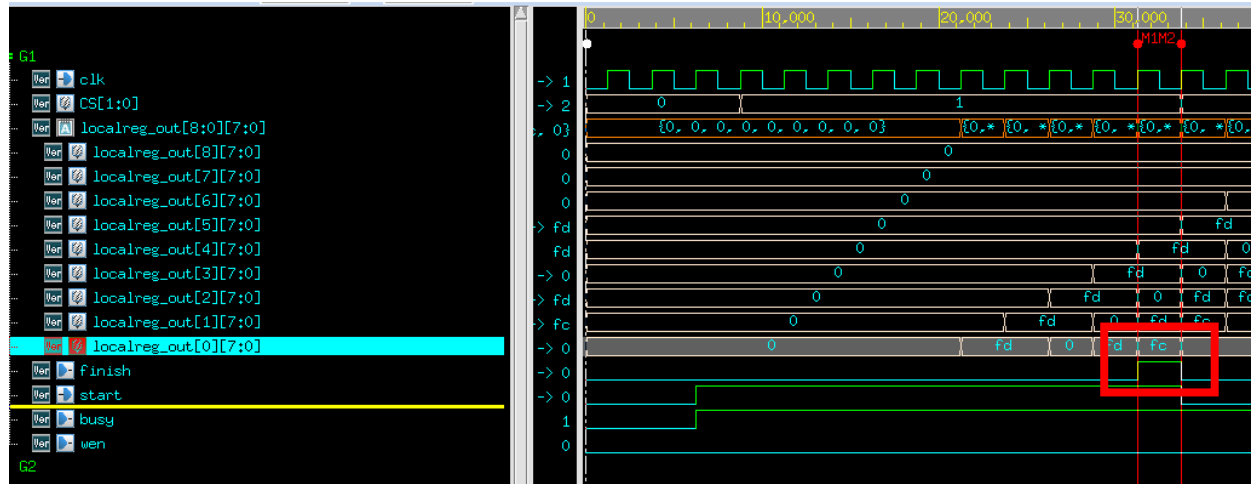
## Description of your design

運作流程  
 附圖為狀態機 一共有四個 STATE 接收到 READY 訊號時 會進入 STORING STATE 將要比較大小的 9 個點 存取進來 存完之後 發出 STORE\_FINISH 訊號 進入下一個 STATE SORTING 找尋中間值 找尋到之後 發出 SORT\_FINISH 訊號將結果存回 MEMORY 而當運算完最後 pixel 進入 DONE STATE

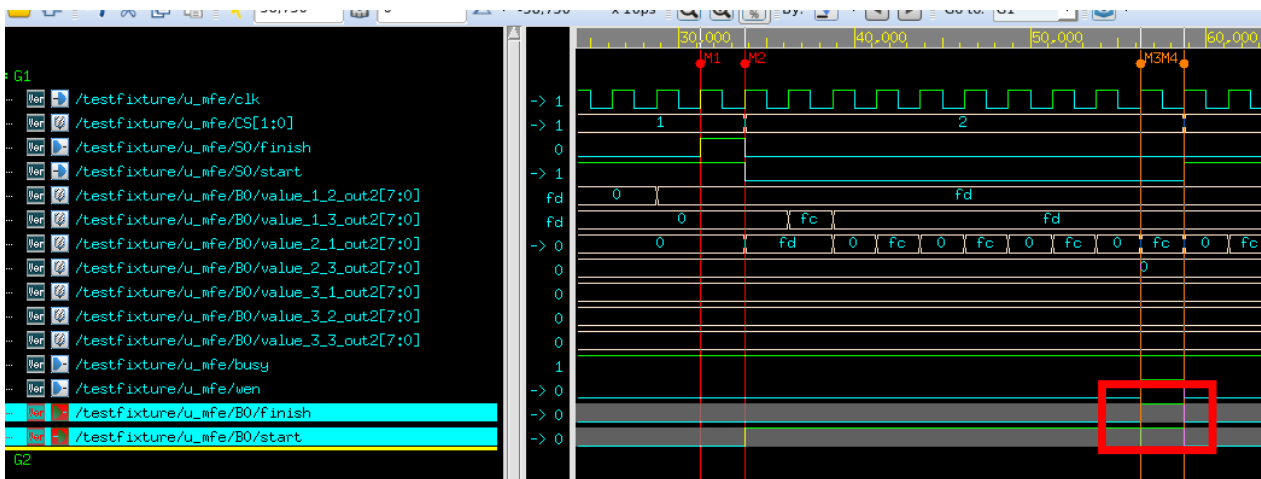


## 波行圖

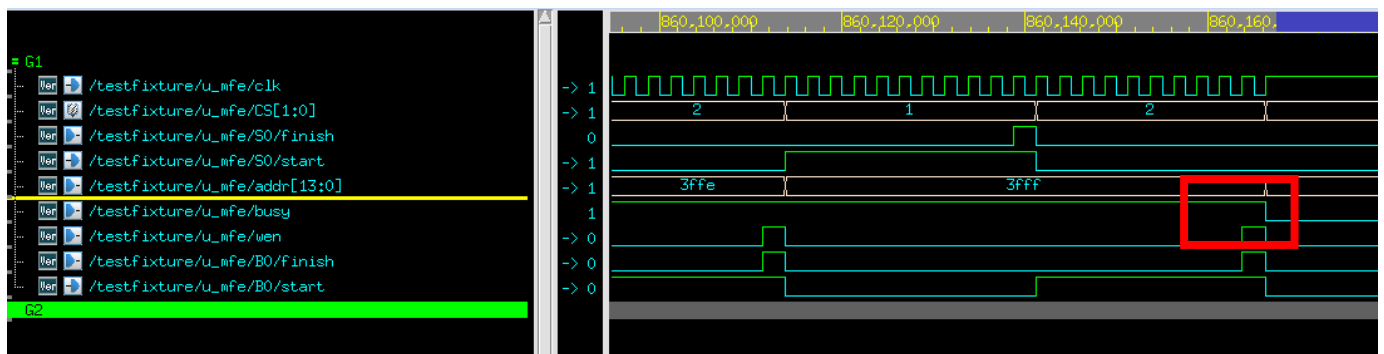
說明      當 ready 訊號來時 將 data 依序 存入 register 存滿 9 個值 拉起 訊號



說明      register 存滿 9 個值 拉起 finish 訊號 bubblesort 模塊 開始運作 若 尚未運算完所有 pixel ,busy 訊號不放下



說明      開始運作 所有運算結束後 進入 DONE STATE 將 busy 訊號 歸為 0



*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*