2021 Digital IC Design Homework 4

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| NAME | | 杜冠勳 | | | | | | |
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| **Simulation Result** | | | | | | | | |
| Functional simulation | Pass | | Gate-level simulation | Pass | | Gate-level simulation time | | simulation time (ns) |
|  | | | | | | | (your post-sim result) | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | | 498 | | | |
| Total memory bit | | | | | 0 | | | |
| Embedded multiplier 9-bit element | | | | | 0 | | | |
| Clock width (Cycle) | | | | |  | | | |
|  | | | | | | | | |

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| **Description of your design** |
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*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (longest gate-level simulation time in ns)*