2021 Digital IC Design Homework 4

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| NAME | | 杜冠勳 | | | | | | |
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| **Simulation Result** | | | | | | | | |
| Functional simulation | Pass | | Gate-level simulation | Pass | | Gate-level simulation time | | simulation time 12042354 (ns) |
|  | | | | | | | (your post-sim result) | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | | 498 | | | |
| Total memory bit | | | | | 0 | | | |
| Embedded multiplier 9-bit element | | | | | 0 | | | |
| Clock width (Cycle) | | | | |  | | | |
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| **Description of your design** | |
| 運作流程 | 附圖為狀態機 一共有四個 STATE 接收到 READY 訊號時 會進入 STORING STATE 將要比較大小的9個點 存取進來 存完之後 發出 STORE FINISH 訊號 進入下一個STATE SORTING 找尋中間值 找尋到之後 發出 SORT\_FINISH 訊號將結果存回 MEMORY 而當運算完最後pixel進入DONE STATE |
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| 波行圖 | | |
| 說明 | | 當ready 訊號來時 將data 依序 存入register 存滿 9 個值 拉起 訊號 |
|  | | |
| 說明 | register 存滿 9 個值 拉起 finish訊號 bubblesort 模塊 開始運作 若 尚未運算完所有pixel ,busy 訊號不放下 | |
|  | | |
| 說  明 | 開始運作 所有運算結束後 進入 DONE STATE將 busy 訊號 歸為0 | |
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*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (longest gate-level simulation time in ns)*