CAEN
Tools for Discovery

Electronic Instrumentation

PRELIMINARY

User Manual UM6697

DT5550W

Weeroc ASICs evaluation and DAQ system

Rev. 5 - March 2nd, 2022

Purpose of this User Manual

This User Manual contains the full description of the DT5550W motherboard for Weeroc ASICs Evaluation and Readout system.

Change Document Record

Date	Revision	Changes
November 6th, 2018	00	Initial release
March 6th, 2019	01	Modified **Ordering Options**
February 21st, 2020	02	Revised **DT5550W Readout Software**
June 8th, 2021	03	Revised **Hardware Description** and **Functional Description**
October 29th, 2021	04	General revision of safety notices
March 2nd, 2022	05	General revision

Symbols, abbreviated terms and notation

ADC	Analog to Digital Converter
FPGA	Field Programmable Gate Array
OEM	Original Equipment Manufacturer
OS	Operating system
PHA	Pulse Height Analysis
SBC	Single-Board Computer

Reference Document

[RD1] GD6520 - SCI-Compiler Quick Start Guide

[RD2] UM6519 - SCI-Compiler User Manual

[RD3] UM6698 – A55PETx User Manual

[RD4] UM7028 - A55CITx User Manual

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Limitation of responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

The information contained herein has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. CAEN spa reserves the right to modify its products specifications without giving any notice; for up to date information please visit www.caen.it.

MADE IN ITALY: We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (this is true for the boards marked "MADE IN ITALY", while we cannot guarantee for third-party manufactures).

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1 Introduction

The DT5550W is a **desktop programmable complete readout system, based on WeeROC (*) ASICs**. It is one of the CAEN programmable board designed to help users in building a customized acquisition system fitting the needs of their detectors and experimental conditions. The complete system is made of a motherboard hosting a programmable FPGA (DT5550W) and a piggyback board with up to 4 WeeROC ASICs (A55xxxx).

The device is designed to operate in laboratory environment under the supervision of skilled technicians.

The DT5550W can be used either as **evaluation system for WeeROC ASICs**, either as **full featured Readout System** for SiPM, PMT, SiPIN, SDD, GEM, etc. Depending on the chosen piggyback board, the system is equipped with a power supply for detector biasing and an adapter PCB exposing standard strip connectors, to easily connect any detector model to the board.

The DT5550W is fully supported by **SCI-Compiler,** a Windows-based graphical development system for **easy FPGA programming**. This tool allows to develop and compile the firmware code using graphical blocks which represents the functionalities needed for firmware implementation. SCI-Compiler automatically generates the VHDL firmware code starting only from logic blocks and virtual instruments that can be connected together in the GUI and, moreover, it generates C/C++/C#/Python Libraries for custom software development in Windows, Linux, MacOS, Android OS (refer to **[RD1]** and **[RD2]** for more details).

A complete, ready to use default firmware is provided for free and open source for each Piggyback Board. The default firmware has been developed to exploit all ASICs features, including the different readout methods supported by the ASICs. The user can open the default firmware design in SCI-Compiler and modify it in order to customize, for example, the trigger logic, the data processing or to integrate it in a larger system.
The SCI-Compiler license and one-year upgrade is included with the DT5550W.

The **DT5550W Readout Software** is the free and open source Windows-based software developed to perform acquisitions with the DT5550W. It works in conjunction with the DT5550W default firmware and it can be modified by the user according to the custom functions implemented in the firmware and for any other need. It allows to perform:

- List event readout (energy, time)
- Energy Spectrum measurements
- Time spectrum measurements
- Imaging with configurable detector shape
- System and ASIC configuration
- ASIC monitor signal probing

Available board models and accessories are listed below.

Motherboard	Description	Product Code
DT5550W	DT5550W - WeeROC ASICs Evaluation and DAQ System	WDT5550WXAAA
Piggyback Board Models	**Description**	**Product Code**
A55PET1	A55PET1 - Piggyback Board with 1 PETIROC chip	WW55PETI2AA1
A55PET2	A55PET2 - Piggyback Board with 2 PETIROC chip	WW55PETI2AA2
A55PET4	A55PET4 - Piggyback Board with 4 PETIROC chip	WW55PETI2AA4
A55CIT2	A55CIT2 - Piggyback Board with 2 CITIROC chip	WW55CITI1AA2
A55CIT4	A55CIT4 - Piggyback Board with 4 CITIROC chip	WW55CITI1AA4

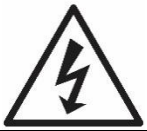
Table 1.1: table of available board models and accessories

(*) https://www.weeroc.com

2 Safety Notices

N.B. Read carefully the "Precautions for Handling, Storage and Installation" document provided with the product before starting any operation.

The following HAZARD SYMBOLS may be reported on the unit:

	Caution, refer to product manual
	Caution, risk of electrical shock
	Protective conductor terminal
	Earth (Ground) Terminal
	Alternating Current
	Three-Phase Alternating Current

The following symbol may be reported in the present manual:

	General warning statement

The symbol could be followed by the following terms:

- **DANGER**: indicates a hazardous situation which, if not avoided, will result in serious injury or death.
- **WARNING**: indicates a hazardous situation which, if not avoided, could result in death or serious injury.
- **CAUTION**: indicates a situation or condition that, if not avoided, could cause physical injury or damage the product and / or its environment.

To avoid potential hazards, use the product only as specified. Only qualified personnel should perform service procedures.
Avoid Electric Overload. To avoid electric shock or fire hazard, do not power a load outside of its specified range.
Avoid Electric Shock. To avoid injury or loss of life, do not connect or disconnect cables while they are connected to a voltage source.

Do Not Operate without Covers. To avoid electric shock or fire hazard, do not operate this product with covers or panels removed.
Do Not Operate in Wet/Damp Conditions. To avoid electric shock, do not operate this product in wet or damp conditions.
Do Not Operate in an Explosive Atmosphere. To avoid injury or fire hazard, do not operate this product in an explosive atmosphere.
Do Not Operate with Suspected Failures. If you suspect this product to be damaged, please contact Technical Support.

The mezzanine connector carries more than 250 I/O lines that can be grouped as:

- Digital 3.3V single ended I/O
- Digital 2.5V single ended I/O
- Digital differential 2.5V LVDS
- Analog differential Input
- Analog Common Mode Output
- I2C
- Power Supply
- Clock output

The following operating limits must be respected:

Net class	Connector	Unit	Min	Max
Power	/	Voltage	9 V	13 V
USER IO	LEMO	Voltage	-0.1 V	3.6 V
Digital lines	Mezzanine connector			
	Digital 3.3V	Voltage	0 V	3.5V
		Current		10 mA
	Digital 2.5V	Voltage	0 V	2.7 V
		Current		10 mA
	LVDS	Voltage	0.5 V	2.1 V
		Current		10 mA
		Common Mode		1.25 V
	I2C	Voltage	0	3.5 V
	Analog Differential Input	Voltage	0.45 V	1.55 V
		Common Mode	0.95 V	0.95 V
	Analog Common Mode Output	Current		6 mA
	Power 5V	Current		2 A
	Power 3.3V	Current		2 A
	Power 1.8V	Current		1 A
	Power 4V A	Current		600 mA
	Power -1V A	Current		600 mA
	Clock Output	Differential Impedance	80 Ω	120 Ω

Table 2.1: operating limits for DT5550W connectors.

WARNING: the piggyback connector lines are directly connected to the FPGA I/O. Violation in maximum absolute rating given in this document will likely destroy the FPGA.

THIS DEVICE SHOULD BE INSTALLED AND USED BY SKILLED TECHNICIAN ONLY OR UNDER HIS SUPERVISION

3 Block Diagram

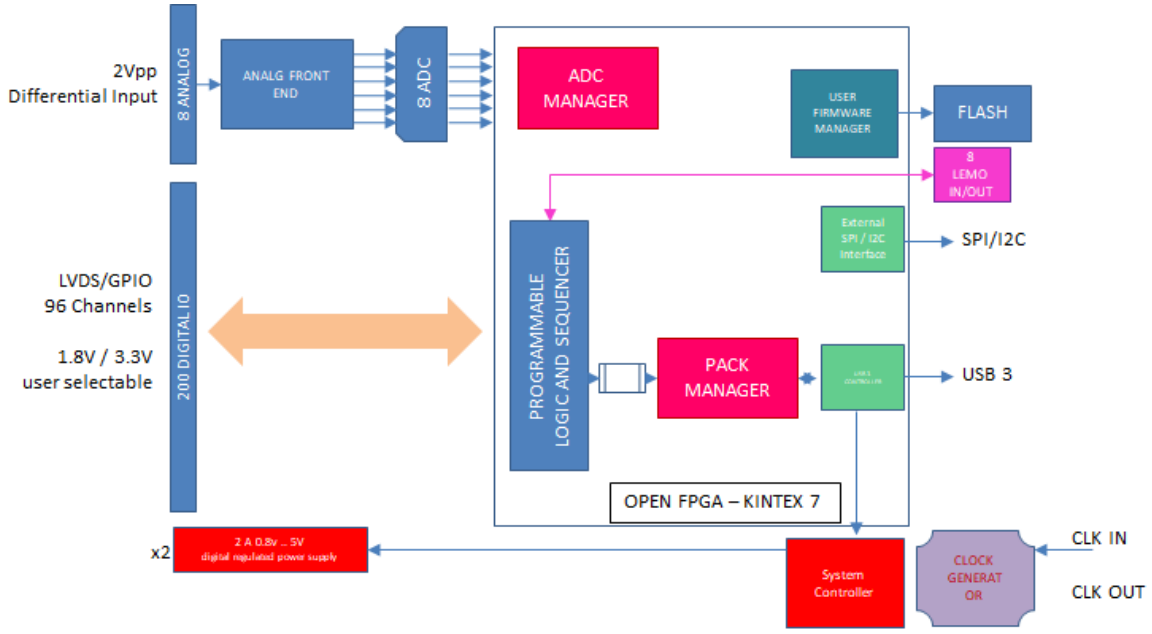


Figure 3.1: DT5550W Motherboard block diagram.

4 Technical Specifications

TECHNICAL		
POWER CONSUMPTION	With A55PET4 piggyback 1A @ 12 V (Typ.) With A55CIT4 piggyback 0.9A @ 12V (Typ.)	
ANALOG INPUT	**Channels** See related Piggyback User Manual Refer to the WeeROC ASIC datasheet for detailed information on the analog input stage	**Connector** See related Piggyback User Manual
BIAS VOLTAGE	CAEN A7585D Power Supply for SiPM available on A55PETx and A55CITx piggyback	
DIGITAL CONVERSION	Internal ASIC ADC or external 80 MS/s, 14-bit ADC	
CLOCK GENERATION	Clock source: internal/external On-board programmable PLL provides generation of the main board clocks from an internal (25 MHz local Oscillator) or external (CLK-IN connector) reference	
LEMO DIGITAL I/O	**CLOCK-IN (LEMO)** Z_{in} = 50 Ω Single-ended, 25 MHz, 3.3V **CLOCK-OUT (LEMO)** R_t = 50 Ω Single-ended, 25 MHz, 3.3V, 50mA	**GPIO 1…8 (LEMO)** General purpose programmable digital I/Os Single-ended, Z_{in} / R_t = 50 Ω
MEMORY	Common FIFO buffer	
TRIGGER	**Trigger Source** *Internal/External*: managed by the default firmware *Complex trigger logic*: implementable by the user on the open FPGA	**Trigger Propagation** Through programmable LEMO GPIO 1…8
TIMING RESOLUTION	*Default FW* Refer to the A55xxx piggyback manual	*Custom FW*: Defined by the firmware design
SYNCHRONIZATION	**Clock Propagation** LEMO CLOCK IN/OUT connectors	**Acquisition Synchronization** Through programmable LEMO GPIO 1…8
FPGA	**Open FPGA** Xilinx XC7K160T (Kintex-7 family)	
COMMUNICATION INTERFACE	**USB 3.0 – type B** USB 2.0 back compatibility Up to 240 MB/s transfer rate	
FIRMWARE	**Default** Standard ASICs readout	**Custom** Use SCI-Compiler to develop your own firmware! Firmware can be upgraded via USB 3.0 or micro-USB debugger (on-fly)
SOFTWARE	- **DT5550W Readout Software** to manage the default firmware - **SCI-Compiler** for custom firmware development	
MECHANICAL		
FORM FACTOR	Desktop bare PCB unit	
DIMENSIONS (H/W/L)	DT5550W + piggyback: 24/152/260 mm^3 (including connectors)	
ENVIRONMENTAL		
ENVIRONMENTAL	Indoor use	
OPERATING TEMPERATURE	Operating Temperature -20 °C ÷ 50 °C	
OPERATING HUMIDITY	25% ÷ 95% RH non condensing	
STORAGE TEMPERATURE	-30 °C ÷ +80 °C	
STORAGE HUMIDITY	5% ÷ 90% RH non condensing	
ALTITUDE	≤2000 m	
POLLUTION DEGREE	2	
OVERVOLTAGE CATEGORY	II	
EMC ENVIRONMENT	Commercial and light industrial	
IP DEGREE	IPX0 enclosure, not for wet location	
REGULATORY		
COMPLIANCE	• EMC: CE 2014/30/EU Electromagnetic compatibility Directive	

	• Safety: CE 2014/35/EU Low Voltage Directive

Table 4.1: technical specifications for the DT5550W

5 Packaging and compliancy

The DT5550W (composed by DT5550W motherboard and A55xxxx piggyback) is a desktop bare PCB board - 24/152/260 mm^3 (including connectors) H/W/L - The system is provided as OEM device without any enclosure in order to be easily integrated in the final experimental setup. Only a plexiglass covers the rear part of the board, providing a desk support.

The unit is inspected by CAEN before the shipment, and it is guaranteed to leave the factory free of mechanical or electrical defects.

When receiving the unit, the user is strictly recommended to inspect for any damage which may have occurred during transportation. Particularly, inspect for exterior damages like broken connectors and check that the panel is not scratched or cracked.

All packing material should be held on until the inspection has been completed. If damage is detected, the user must file a claim with the carrier immediately and notify CAEN.

Before installing the unit, make sure to read thoroughly the safety rules and installation requirements (Sec. Errore. L'origine riferimento non è stata trovata.), then place the package content onto your bench.

The content of the delivered package standardly consists of the part list shown in the table below (**Table 5.1**). All the official documentation, firmware updates, software tools, and accessories are available on *www.caen.it* at the product web page.

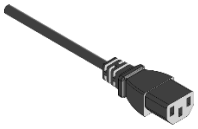
	Part	Description	Qty
	DT5550W	Weeroc ASICs evaluation and DAQ system	x1
	Power supply cable	Standard C13 power supply chord	x1
	AC/DC converter	220-110 V to 12V,60W AC/DC stabilized power supply with 2.1 mm type jack	x1
	USB 3.0 cable	USB 3.0 type A-microB I/O cable L=2MT	x1
	USB 2.0 cable	USB 2.0 type A-microB - I/O cable L=1.8MT	x1
	SCI-Compiler	USB Dongle for SCI-Compiler software **(if included in your order)**	x1
	User guide	UM6697 – DT5550W User Manual	x1

Table 5.1: delivered kit.

CAUTION: to manage the product, consult the operating instructions provided.

DT5550W is an ESD sensitive item. Handling without ESD protective covering shall be performed only into approved ESD Protected Area (EPAs)

DT5550W complies with EMC directive only if installed in a CE marked system

It is recommended to:

- Inspect containers for damage during shipment. Report any damage to the freight carrier for possible insurance claims.
- Check that all the components received match those listed on the enclosed packing list. (CAEN cannot accept responsibility for missing items unless we are notified promptly of any discrepancies.)
- Open shipping containers; be careful not to damage contents.
- Inspect contents and report any damage. The inspection should confirm that there is no exterior damage to the unit such as broken knobs or connectors and that the front panel and display face are not scratched or cracked. Keep all packing material until the inspection has been completed.
- If damage is detected, file a claim with carrier immediately and notify CAEN service.
- If equipment must be returned for any reason, carefully repack equipment in the original shipping container with original packing materials if possible. Please contact CAEN service.
- If equipment is to be installed later, place equipment in original shipping container and store in a safe place until ready to install

DO NOT SUBJECT THE ITEM TO UNDUE SHOCK OF VIBRATIONS

DO NOT BUMP, DROP OR SLIDE SHIPPING CONTAINERS

DO NOT LEAVE ITEMS OR SHIPPING CONTAINERS UNSUPERVISED IN AREAS WHERE UNTRAINED PERSONNEL MAY MISHANDLE THE ITEMS

USE ONLY ACCESSORIES WICH MEET THE MANUFACTURER SPECIFICATIONS

SCI-Compiler License

R5560SE is compatible with SCI-Compiler ([RD1][RD2]), the Windows-based CAEN ***firmware generator and compiler*** for ***easy FPGA programming.*** It is an **automatic code generator** that, starting from a graphical block diagram, generates a VHDL piece of code that implements the required function. The software uses a prebuilt library set containing macroblocks implementing complex functions (MCA, Oscilloscope, Digitizer, TDC) that the user can connect one with each other. SCI-Compiler is also able to generate C libraries and drivers to be used in **Windows**, **Linux** and **macOS** for DAQ software implementation.

Note: SCI-Compiler full version works upon the purchase of a license, contact CAEN at info@caen.it for more information.

Note: a trial version of SCI-Compiler is available for free on the CAEN website. It has no time limit but does not allow the user to generate any firmware code nor save his/her block-diagram design.

Full version of SCI-Compiler is accessible after activation of the **software license** on CAEN website using the SERIAL NUMBER and an ACTIVATION key provided together with the USB Dongle. The USB Dongle must be plugged into the PC to run SCI-Compiler full version. The generated firmware can be uploaded on each compatible board that has been activated with a **SCI-Compiler Runtime license** on CAEN website. Refer to **[RD1]** and **[RD2]** for more details.

Figure 5.1: SCI-Compiler USB Dongle and keys for license activation.

Note: user is not allowed to use the code generated by the SCI-Compiler on boards different from R5560SE. Even using a small part of the code generate by the SCI-Compiler on a custom design board or other products is an explicit violation of the license terms and it is an offense against CAEN S.p.A and Nuclear Instruments S.R.L.

6 PID (Product Identifier)

PID is the CAEN product identifier, an incremental number greater than 10000 that is unique for each product. The PID is on a label affixed to the product (**Fig. 6.1**) and it is even stored in an on-board non-volatile memory readable via readout software (see Chap**. DT5550W Readout Software**).

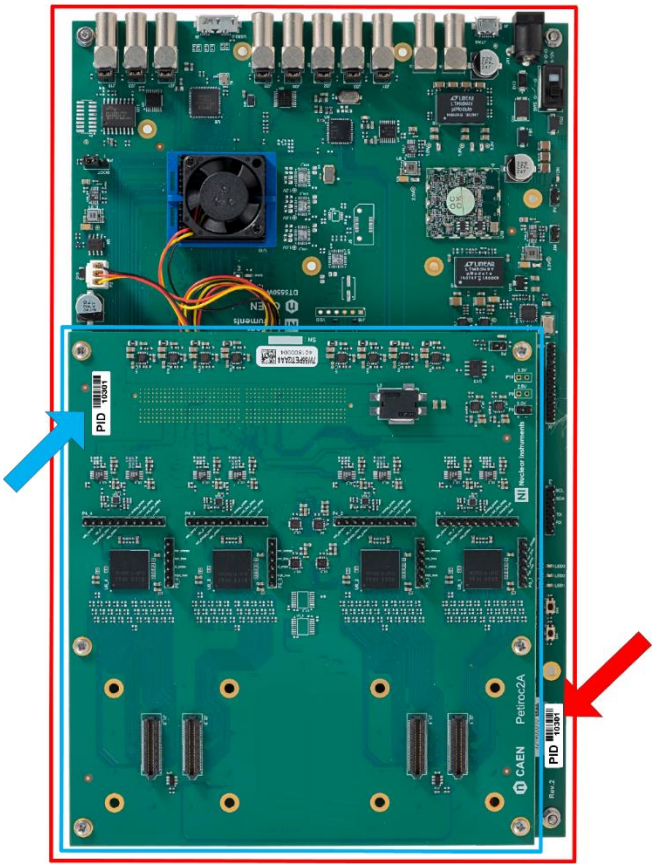


Fig. 6.1:PID location. The red arrow points to the DT5550W motherboard PID, while the blue one points to the piggyback board PID.

7 Power Requirements

The DT5550W is powered by an external 220-110 V to 12V, 60W AC/DC stabilized power supply provided with the board and included in the delivered kit, together with a standard wall IEC C13 power chord.

Note: using a different power supply source, like battery or linear type, it is recommended the source to provide +12 V and 2A; the power jack is a 2.1 mm type, a suitable cable is the RS 656-3816 type (or similar)

WARNING: the maximum operating voltage is 12.8V while the minimum is 9V.

8 Cooling Management

The DT5550W board can operate in the temperature range -20 + 50 °C.

An air flow fan is installed onboard, onto the FPGA. The user must take in care to provide a proper cooling to the board with external fan if the board is used in an enclosure or if the board is installed in a setup with poor air flow.
Excessive temperature will, in first instance, reduce the performance and the quality of the measurements and can also damage the board.

Please do not stop fan operation to avoid FPGA overheating. If in a single rack tower, multiple units are installed, please consider external fans or rack mounted air conditioning system.

If the board is stored in cold environmental, please check for water condensation before power on.

The board has not been tested for radiation hardness. High energy particle can be source of soft error and can damage the FPGA. If used in strong proton or neutron beams, arrange proper shielding or remote the sensor with a custom cable.

9 Installing the device

- Connect the power supply to the input 2.1 mm power jack
- Set the onboard switch to ON position

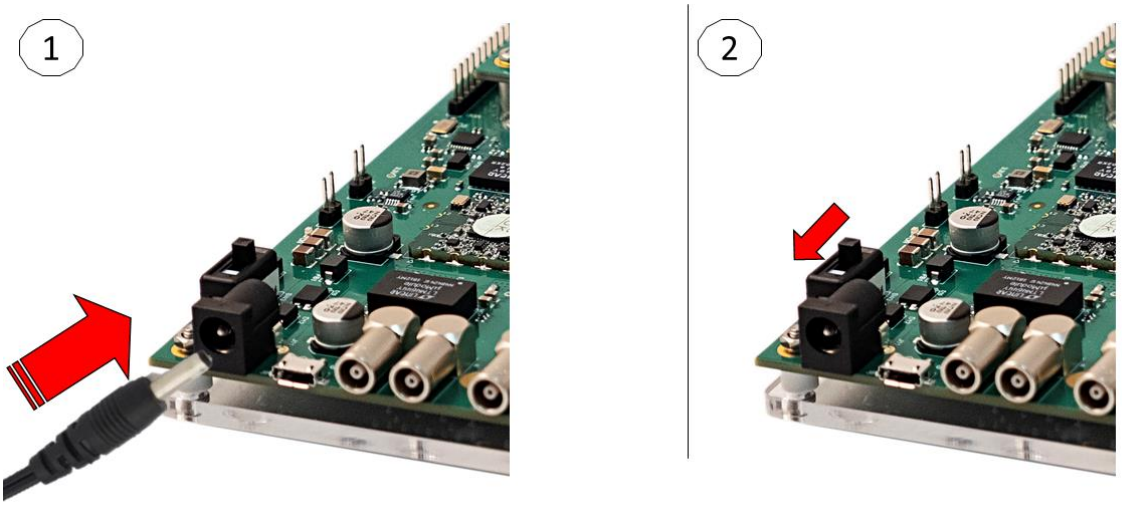


Fig. 9.1: installing the DT5550W.

ONLY QUALIFIED PERSONNEL SHOULD PERFORM INSTALLATION, OPERATIONS

DO NOT INSTALL THE EQUIPMENT SO THAT IT IS DIFFICULT TO OPERATE THE ON/OFF SWITCH ONBOARD

IT IS RECOMMENDED THAT THE SWITCH OR CIRCUIT-BREAKER IS NEAR THE EQUIPMENT

THE SAFETY OF ANY SYSTEM THAT INCORPORATES THE DEVICE IS UNDER THE RESPONSIBILITY OF THE ASSEMBLER OF THE SYSTEM

DT5550W is an ESD sensitive item. Handling without ESD protective covering shall be performed only into approved ESD Protected Area (EPAs)

DT5550W complies with EMC directive only if installed in a CE marked system

Do not use the device and contact technical support if one of these situations is verified:
- Enclosure integrity is compromised
- Insulation of HV chord is damaged (if present)
- The indication led or display is not performing as required (e.g. led not working, display with incorrect graphic)
- Fans are not working (if present)

10 Hardware Description

The DT5550W is a system meant to be used as a fully-equipped DAQ board or as an evaluation board for WeeROC ASICs

In order to maximize the flexibility, the system is divided in two board:

- **Motherboard**: an FPGA based system with a user programmable FPGA, USB 3.0 communication interface, an 80 MS/s, 14-bit ADC and a mezzanine connector with more than 200 digital I/O to provide interconnection between the FPGA and the ASICs.

- **Piggyback board**: a board equipped with one, two or four ASICs, detector connectors and, eventually, a power supply module for detector biasing.

Thanks to the mezzanine connector, a single motherboard can be used in conjunction with each one of the piggyback boards. The piggyback can be easily replaced removing 6 screws.

Note: CAEN provides the piggyback boards for WeeROC ASICs. User can design a custom piggyback board in order to readout custom ASICs.

The following piggyback boards are available for the DT5550W system:

Piggyback board model	ASICs	Channels	Detector
A55PET1	1x PETIROC2A	32	SiPM
A55PET2	2x PETIROC2A	64	SiPM, SiPM Matrix
A55PET4	4x PETIROC2A	128	SiPM, SiPM Matrix
A55CIT2	2x CITIROC1A	64	SiPM, SiPM Matrix
A55CIT4	4x CITIROC1A	128	SiPM, SiPM Matrix

Table 10.1: table of the available piggyback boards

Note: a detailed description of the chosen piggyback model can be found in the correspondent User Manual.

DT5550W Motherboard

The DT5550W motherboard is the board responsible for the processing of signals coming from the ASICs as well as for the interface with the host PC. It is equipped with an open Xilinx Kintex7 FPGA to be used for custom firmware development and with an 8-channel, 80 MS/s, 14-bit ADC, mainly used for ASICs multiplexed signals readout.

In the following picture the most important components and connectors of the DT5550W motherboard are highlighted.

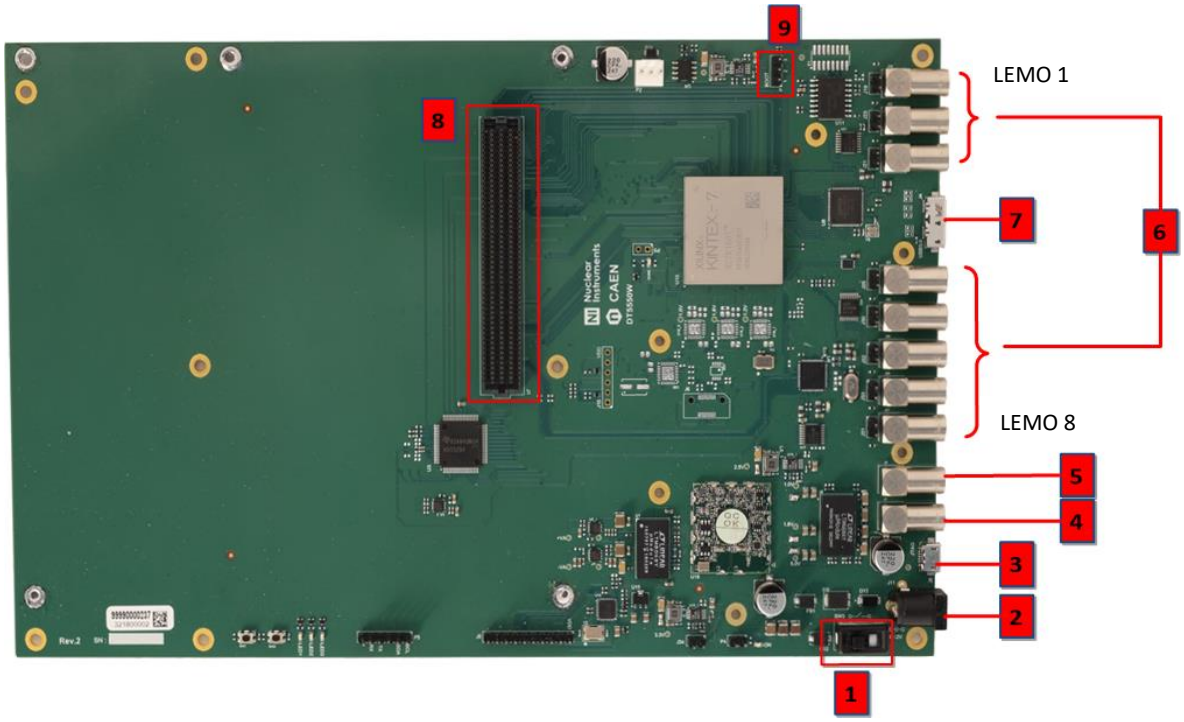


Figure 10.1: general view of the DT5550W board without any piggyback connected. The main components and connectors are highlighted.

Number	Connector	Description
1	n/a	**ON/OFF switch**
2	**2.1 mm female jack**	**Power Socket** (+12 V)
3	**Micro-USB 2.0**	**JTAG connector.** This port allows to connect directly to the FPGA to perform a fast firmware download, writing directly in the volatile configuration memory in a couple of seconds.
4	**LEMO**	**CLK IN** - accepts a 25MHz, 3.3V signal, 50 Ω input impedance.
5	**LEMO**	**CLK OUT** - provides a 25MHz, 3.3V signal (can be used to drive a 50Ω coaxial cable).
6	**LEMO**	**General Purpose I/Os**. The firmware defines their function. The direction (input/output) can be configured couple by couple. *These I/Os can be used to provide external trigger, Veto or board to board synchronization signals*. Input connectors can operate in high impedance mode or at 50 Ω by inserting the related jumper in the header behind the connector.
7	**USB3.0 type micro-B**	**Communication port** - allows high speed data transfer to the computer. Communication bus is back compatible with USB 2.0. Maximum transfer speed in USB3.0 mode is 200 MB/s while in USB2.0 is 24 MB/s.
8	**Samtec SEAF-50-06.5-L-08-1-A-K-TR**	**Mezzanine connector -** 8 column, 64 rows, BGA array connector used to plug one of the provided CAEN piggyback boards.
9	**Wurth WR-PHD male 1row vertical 2.54mm 3ways**	**Bootloader**– The jumper position must be changed with the board switched off. The jumper must be placed in position 1-2 to boot the FPGA in bootloader mode for firmware upgrade, while position 2-3 is for normal operation (see PCB serigraphy).

Table 10.2: DT5550W connectors description

Note: for those users willing to build a custom piggyback, the mezzanine connector schematic and pinout is provided upon request by contacting CAEN Support Service.

Digital conversion

The DT5550W motherboard hosts an 8 Channels, 80 MS/s, 14-bit ADC (Texas Instruments ADS5294). This is used for two main purposes:

- analog readout of the ASIC analog multiplexed outputs (see **Analog Multiplexed Readout** for more details)
- monitor of the ASIC analog probe.

Several Weeroc ASICs can be configured in order to generate a monitor output on an analog pin. The monitor allows to probe several internal signals like: preamplifier output, CR-RC output, TDC ramp of each channel.

The data between the FPGA and the ADC are transferred on a 1 GHZ, 16 lanes, serial bus.
The ADC input dynamic is 2Vpp; the single ended signals swing from 0.5V to 1.5V. The common mode reference is provided by the ADC and it is equal to 0.95V.
All 8 analog inputs of the ADC are routed to the mezzanine connector as differential line, as well as the common mode reference (VCM).

Weeroc ASICs have single-ended analog outputs. Therefore, an active DC-coupled conversion circuit is used to connect the ASIC output with the ADC input.

If using SCI-Compiler to develop a custom firmware, the user should not worry about configuring the ADC for data readout: the SCI-Compiler provides a virtual block for each analog input, already set for data readout.

User must take in account that the ADC has in internal pipeline. The pipeline introduces a delay of 15 clock cycles. The FPGA has an internal delay of 2 units. Each delay unit is equal to 12.5 ns. Digital data has no delay; that means that analog data are not synchronous with digital signals. In order to synchronize analog and digital signals, delay elements to all digital signals are added at firmware level.

Clock scheme

The DT5550W has a versatile clock scheme. A Texas Instruments CDCE62005 clock generator is used in order to generate the clock signal for all devices on the board. Onboard clock is provided to the ADC. Other clock signals are connected to the piggyback connector (two clocks) and one to the FPGA.

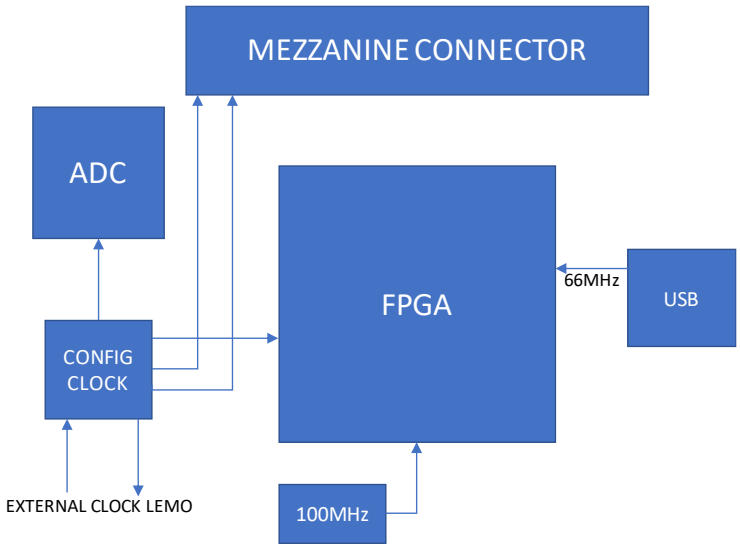


Figure 10.2: clock distribution scheme on the DT5550W board.

The clock frequency is programmed via firmware using a dedicated SPI bus between the FPGA and the clock generator. The frequency depends on the target project. For example, for Petiroc ASIC a 40MHz LVDS and a 160 MHz LVDS are generated on the lines connected to the piggyback connector and a 160 MHz clock is fed to the FPGA. For Citiroc ASIC a 25 MHz clock is fed to the ADCs and the system clock is 125 MHz.

Unless modifying the VHDL firmware code generated by the SCI-Compiler, user cannot change the clock frequency. We recommend not to change the clock frequency because it will likely make the system unstable.

It is possible to disable piggyback clock output at firmware level, if needed. If, for example, the Petiroc is used in photon counting mode (see **Functional Description**), the clock is not necessary, and it would only have the effect of increasing the noise in the chip. It is also possible to select the internal clock or the external clock as system clock source. The clocks customization cannot be performed at runtime but only prior the firmware compilation.

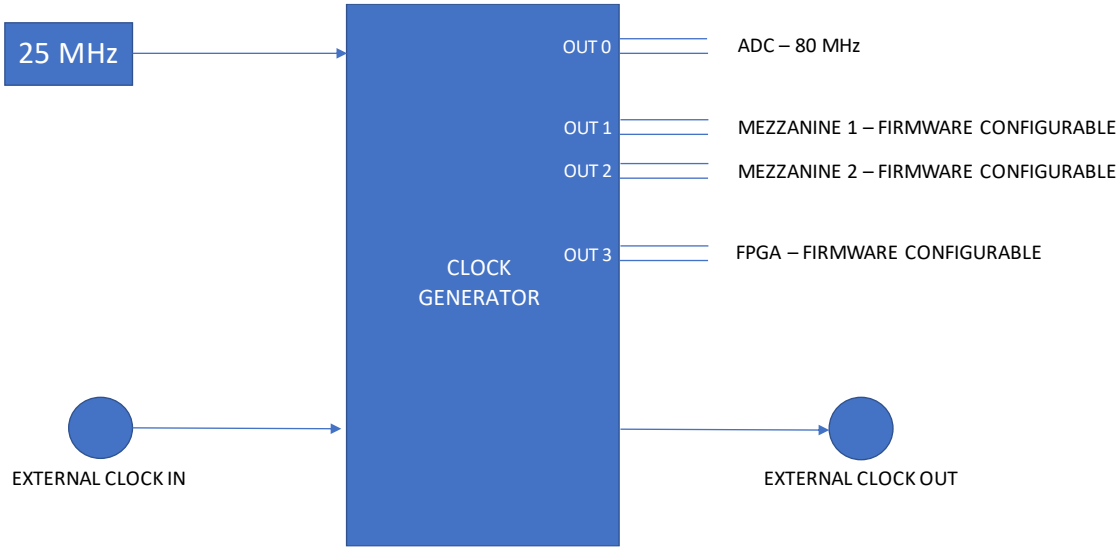


Figure 10.3: scheme of the clock generator. The external clock signal must be a 25 MHz, low jitter, 3.3V CMOS input. The external clock output is a CMOS 3.3V 25 MHz square wave. The clock output is able to drive a 50 Ω terminated cable.

11 Functional Description

The DT5550W supports four different readout methods:

- Digital readout of ADCs integrated in the ASICs (for example the PETIROC)
- Analog multiplexed ASICs (for example the CITIROC)
- Photon counting mode (all ASICs)
- TDC mode (all ASICs)

Note: in general, the **DT5550W Readout Software supports one readout mode for each ASIC: if a fully digital readout is available for a specific ASIC, DT5550W Readout Software will use it** because it maximizes the amount of information that can be extract from a specific ASIC. We provide the source code of both the software application and firmware (designed with SCI-Compiler) so that the user can easily customize them in order to integrate at best the DT5550W using the preferred readout system.

Digital Readout

ASICs like Petiroc have an integrated ADC/TDC and are able to provide the result of the measurement as a binary serialized stream. *The serial bit-stream contains for each channel the trigger information, the time of arrival and the charge information*.
The stream is high speed serialized (for Petiroc 160 Mbit/s) and a dedicated logic must be used in order to convert the stream in parallel information of hit/time/energy. The digital readout is implemented deserializing the serialized bit-stream which contains the measurement results generated by the ASIC. The SCI-Compiler integrates the appropriate digital readout for all supported ASICs. User can simply use SCI-Compiler to program the FPGA and deserialized data will be available in the user firmware.
For Petiroc ASIC, for example, a trigger signal from the ASIC starts the readout process inside the FPGA. The FPGA start the ASIC ADC converter using that "Start_Conv" signal. When the conversion is completed the ASIC sets the "TransmitOn" signal. The FPGA then starts to sample the 80 MHz data stream and deserialize it. *The deserialized data contains the energy/time/position for all the cannels of the ASIC and generate an event*. Events from all channels are pushed in a common FIFO buffer and are directly read out by the DT5550W Readout Software using the USB 3.0 communication port of the DT5550W board.

An example of the ASIC readout process and the data serialization is shown in the schemes below.

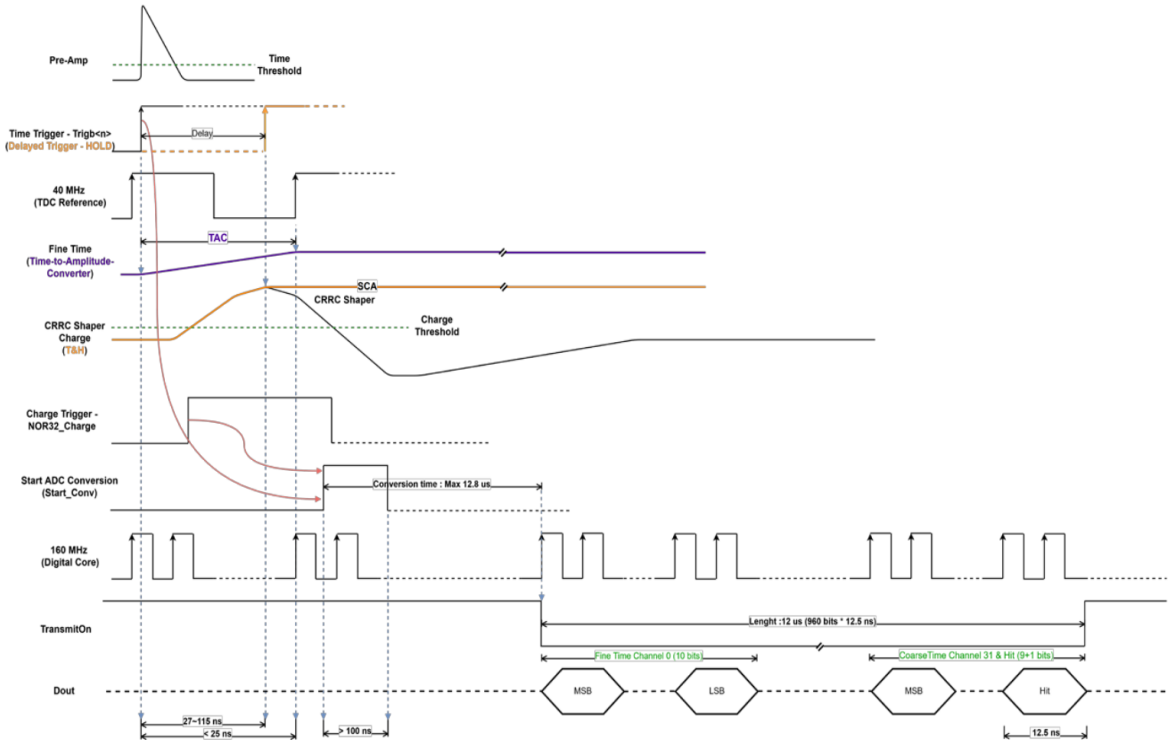


Figure 11.1: the readout scheme of WeeROC PETIROC, where data serialization process is shown.

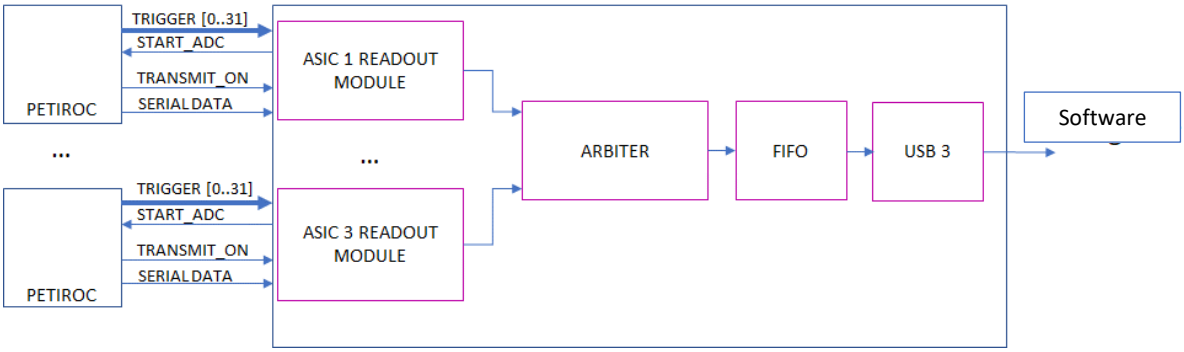


Figure 11.2: the readout of deserialized data with DT5550W Readout Software.

Analog Multiplexed Readout

ASICs like Citiroc have not an integrated ADC. The ASIC performs just a Sample and Hold operation on each channel. The energy of each channel is then multiplexed on a single analog output. The typical signal processing is shown in the scheme below.

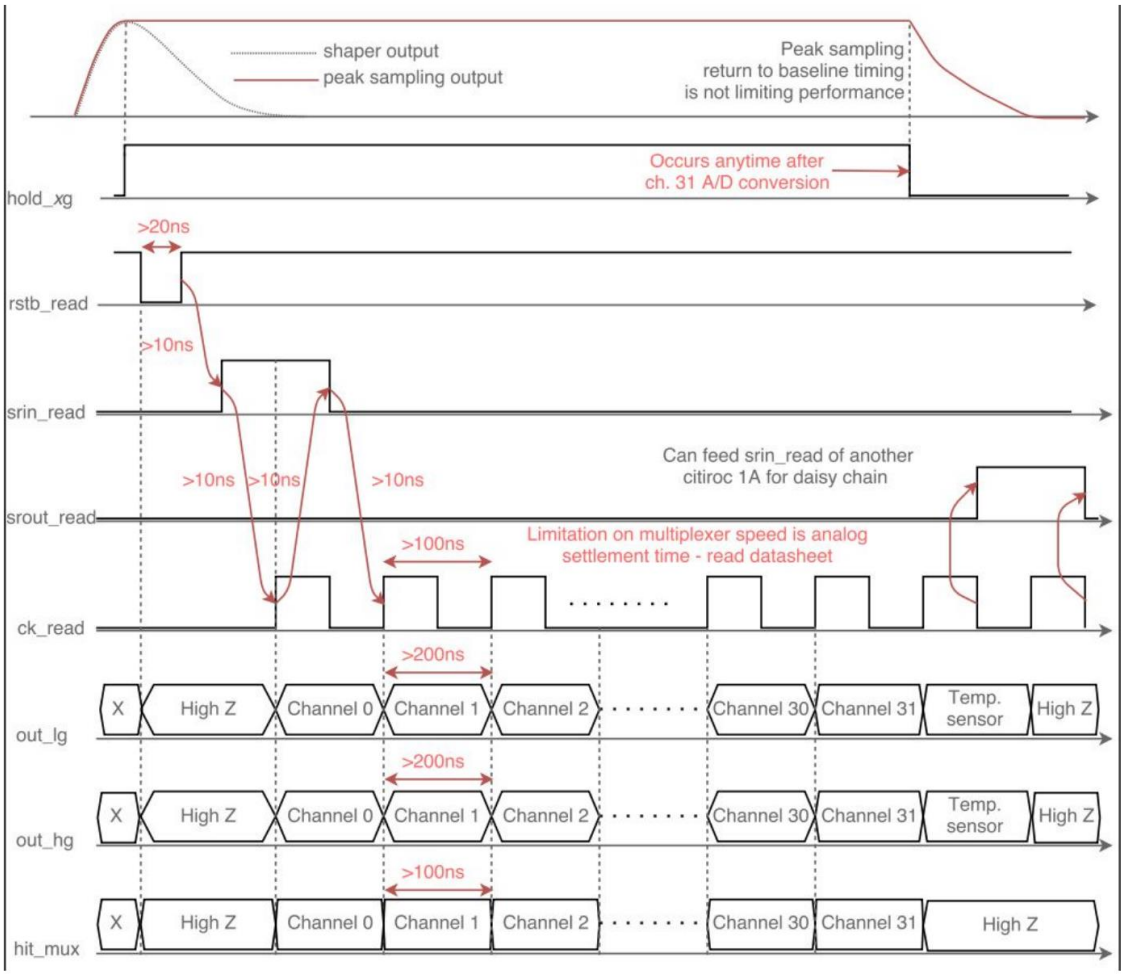


Figure 11.3: the readout scheme of WeeROC CITIROC, where analog multiplexed data are available as outputs.

In order to decode the ASIC energy information, the analog signal must be sampled with an external ADC; it is important to properly control the ASIC analog shift register in order to synchronize the analog information with a specific channel (refer to WeeROC ASIC datasheets for more details).

For Weeroc ASICs, there are two digital lines to control the analog shift register:

- srin_read: user must load a '1' at the beginning of the read procedure in order to select the first channel
- ck_read: user must generate a number of clock cycles equal to the number of channels plus one in order to shift out the analog information.

The analog information is provided on the out_charge_mux output (for CITIROC there are two outputs: high/low gain). At the same time on the hit_mux (or trigb_mux) output the multiplexed triggers are available, providing a coarse timestamp for the correspondent charge events. ***The FPGA timestamps the events with a resolution of 12.5 ns***.
The analog data conversion is done on the DT5550W motherboard by mean of the 80 MS/s 14-bit ADC. Digital data are available in the FPGA as a 80MHz 16-bit data stream with a pipeline delay of 15 clock cycles.

For each supported ASIC an Analog Readout SCI-Compiler Virtual Block is available, in order to easily build a working firmware to readout the IC. The block internally compensates the ADC pipeline delay and synchronously control the ASIC shift register and ADC sampling. User can also directly interface with the ADC output and write its own decoding block. Digital data can be read out by the DT5550W Readout Software using the USB3 communication port of the DT5550W board.

The typical analog multiplexed signals readout is shown in the scheme below.

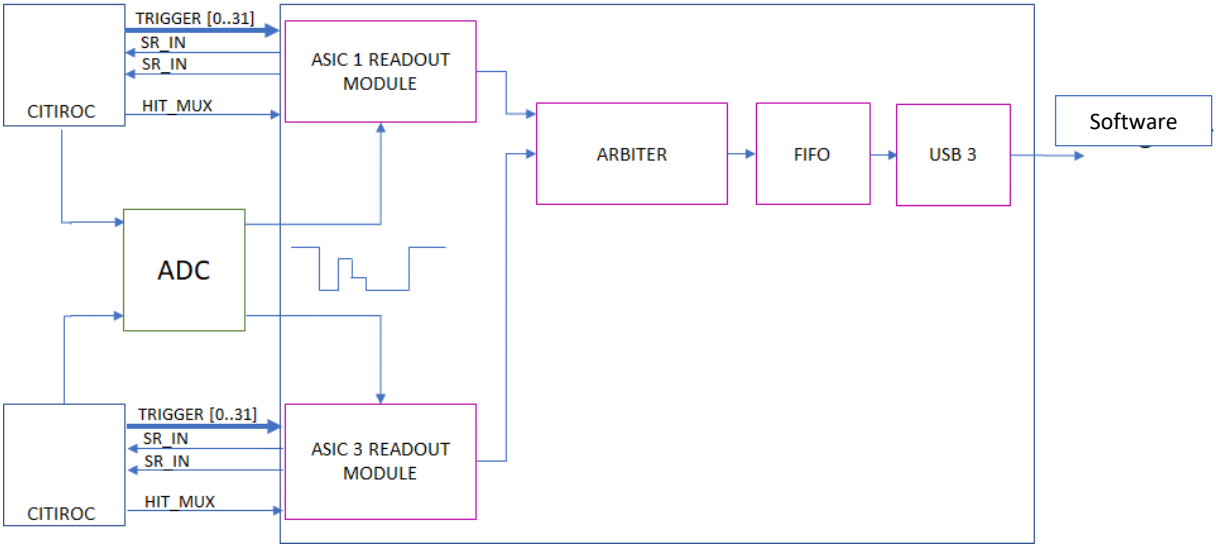


Figure 11.4: scheme of the readout process of analog multiplexed signals for WeeROC CITIROC.

Photon Counting Mode

If the charge information is not required, it is possible to work in photon counting mode.

In this mode the firmware just counts the transitions of the channels trigger output pins: the ASIC works in fully asynchronous digital mode and no internal ADC/TDC is enabled. Only the ASIC fast shaper and comparator are used.

A custom firmware could allow to work in photon counting, giving the user the possibility to read the number of photons per channel from the beginning of the run and the list (energy of a series of events) in a specific integration window opened by a start signal. The start signal could be generated by an internal periodic signal or by an external signal provided, for example, on the LEMO4. This window width could be set between 100ns and 4s. The internal start signal frequency can be set between 1Hz and 1MHz.

The readout scheme of DT5550W and ASIC operating in photon counting mode is shown below.

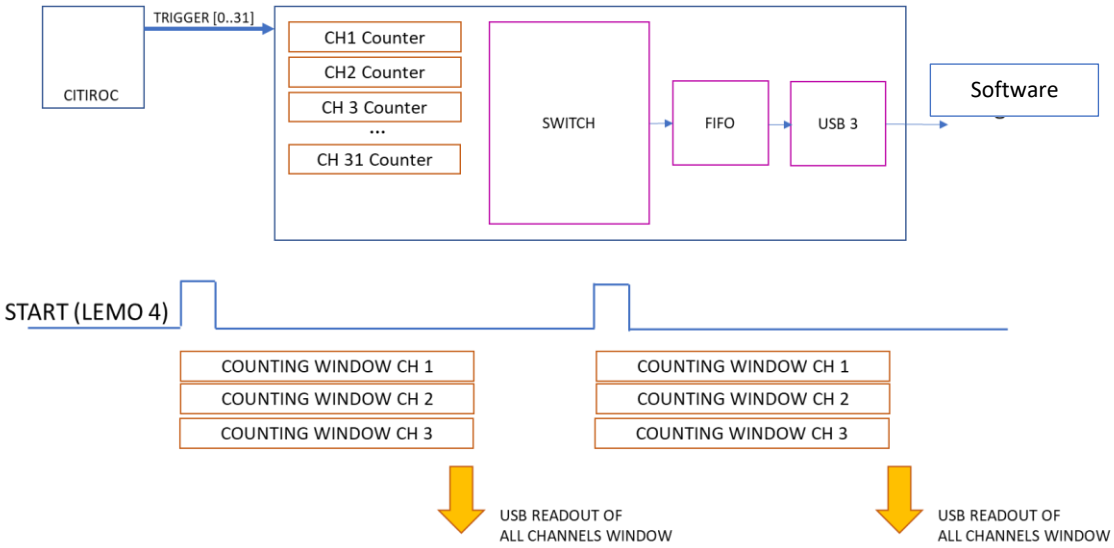


Figure 11.5: readout scheme of DT5550W and ASIC operating in photon counting mode.

TDC Mode

TDC mode is similar to the photon counting mode: the ASIC works in fully asynchronous digital mode and no internal ADC/TDC is enabled. The FPGA timestamps the toggling trigger line with a resolution of 0.5 ns; a 48bit timestamp is generated and transferred in list mode to the readout software.

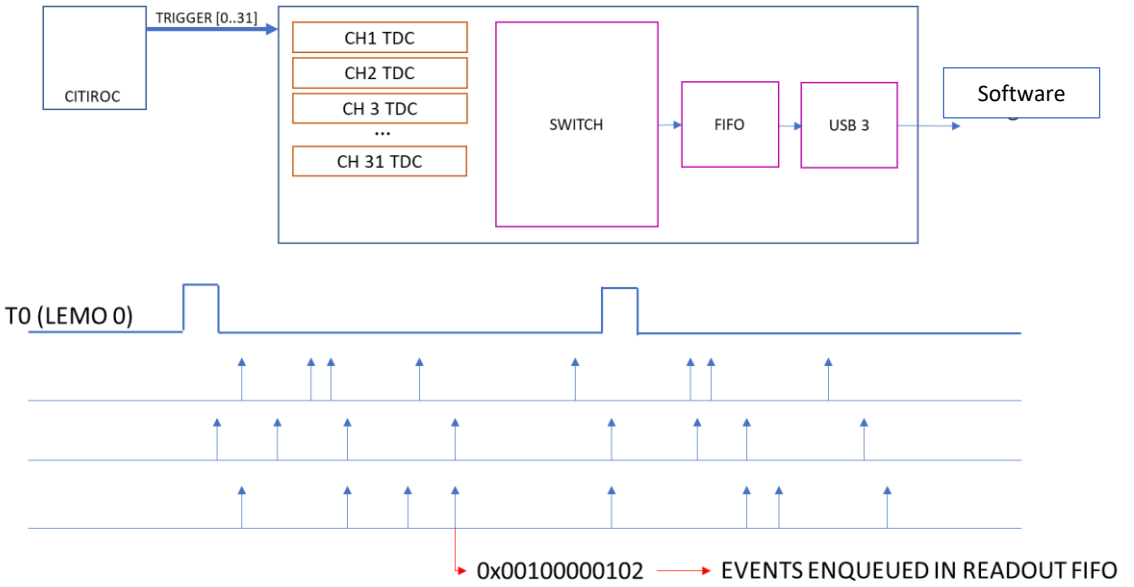


Figure 11.6: readout scheme of DT5550W and ASIC operating in TDC mode.

12 Drivers & Libraries

The DT5550W uses the standard FTDI FT60X driver (D3XX Driver) for USB 3.0 connection. We decided not to customize the device driver in order to preserve the portability of the driver on Windows/Linux/MacOS/Android OS. Drivers for these operating systems can be downloaded from FTDI web page:

http://www.ftdichip.com/Drivers/D3XX.htm

Follow the FTDI driver installation guide to install the device driver.

Note: upon installation of SCI-Compiler or DT5550W Readout Software, the drivers for DT5550W will be automatically installed in your Windows OS.

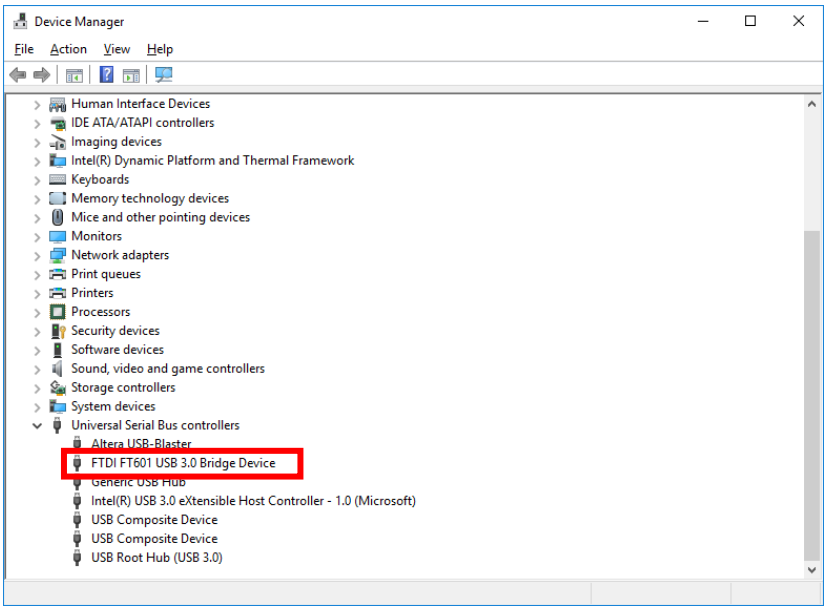


Figure 12.1: the Windows Device Manager showing up the DT5550W as FTDI FT601 USB3.0 Bridge Device

Libraries for C/C++/C#/Python are generated by SCI-Compiler when firmware code is compiled. The libraries can be used for custom software development on Windows/Linux/MacOS/Android. Libraries related to the default firmware are provided within the DT5550W Readout Software open source code.

13 Firmware and Upgrade

The DT5550W is a programmable platform with open FPGA. It is designed in order to encourage the user to develop his own custom firmware using the SCI-Compiler software **[RD2]**.

For users who want to implement a fully working readout system using one of the available piggyback board, a full working (default) firmware is provided for each piggyback board. Default firmware are complex full featured solution and are developed not as basic example to be modified with SCI-Compiler but as **DAQ readout system firmware**. For each piggyback, simpler firmware examples are also provided in order to introduce the user to his custom firmware development. Default firmware functionalities are given in the table below.
All default firmware work in conjunction with DT5550W Readout Software, which implements readout and data analysis functionalities.

Note: if the DT5550W is ordered with a specific piggyback board, it comes with the default firmware for that specific piggyback already preloaded. Refer to the specific piggyback User Manual for the functionalities of the default firmware. If the DT5550W is ordered without a specific piggyback it comes without a firmware. Only the bootloader is loaded in the flash memory.

It is possible to change the firmware using the firmware upgrader tool, included in both SCI-Compiler and DT5550W Readout Software installation setup.
The firmware upgrade tool interfaces with the FPGA bootloader in order to load the firmware in the DT5550W flash memory. In order to enter the FPGA in bootloader mode, the "bootloader" jumper must be inserted in position 1-2, as shown in **Figure 13.1**.

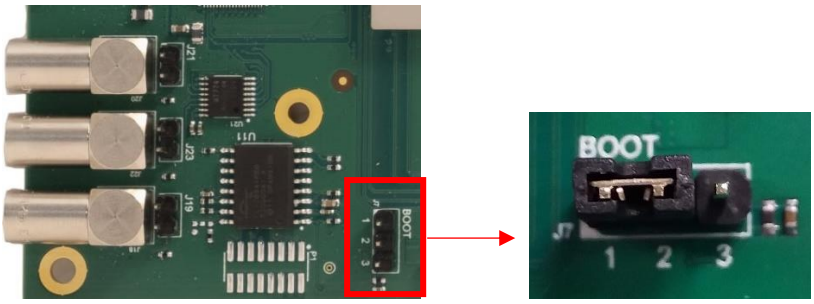
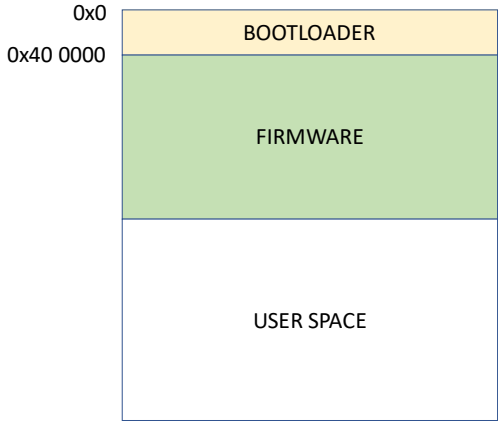


Figure 13.1: the bootloader jumper connector of DT5550W. The jumper must be inserted in position 1-2 with the board switched off.

The DT5550W mounts a QSPI 512 Mbit flash S25FL512S. The first 4 Mbytes are used for the bootloader. At start-up bootloader is always loaded. If the bootloader jumper is not inserted, the bootloader reconfigure on fly the FPGA to load the firmware at address 0x40 0000.
The firmware size depends on the complexity of the project. Always enable bitstream compression: this option is by default enabled in SCI-Compiler default firmware.

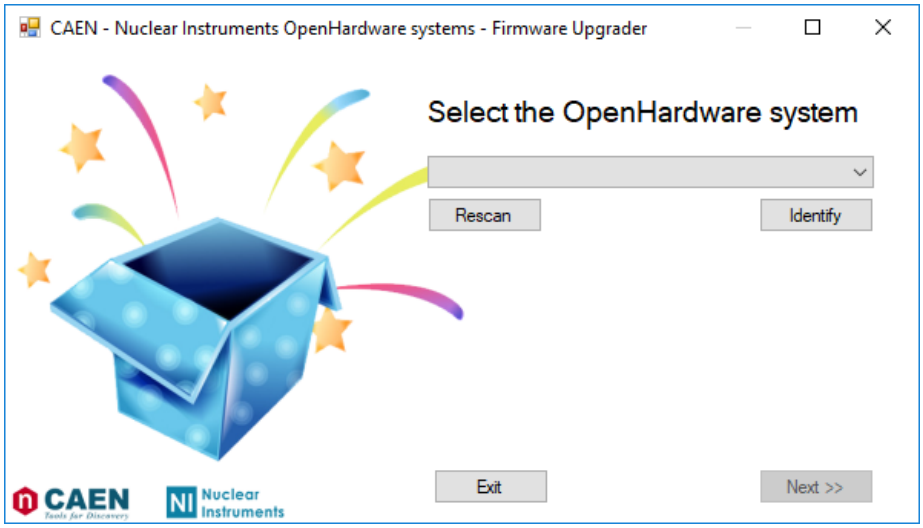


In order to upgrade the firmware, follow the steps below:

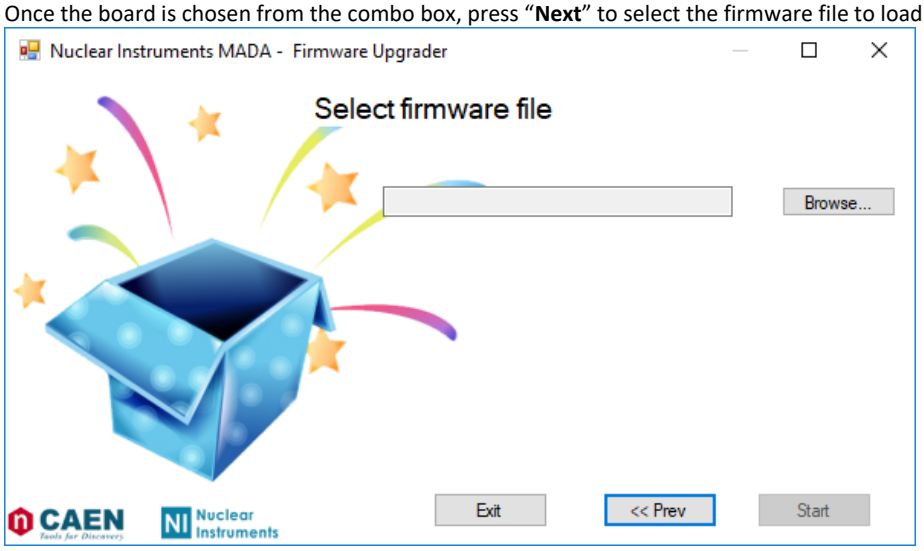
- **Insert the bootloader jumper in position 1-2**, with the board switched off
- Power on the board

- Launch the ***Open Hardware Upgrader***

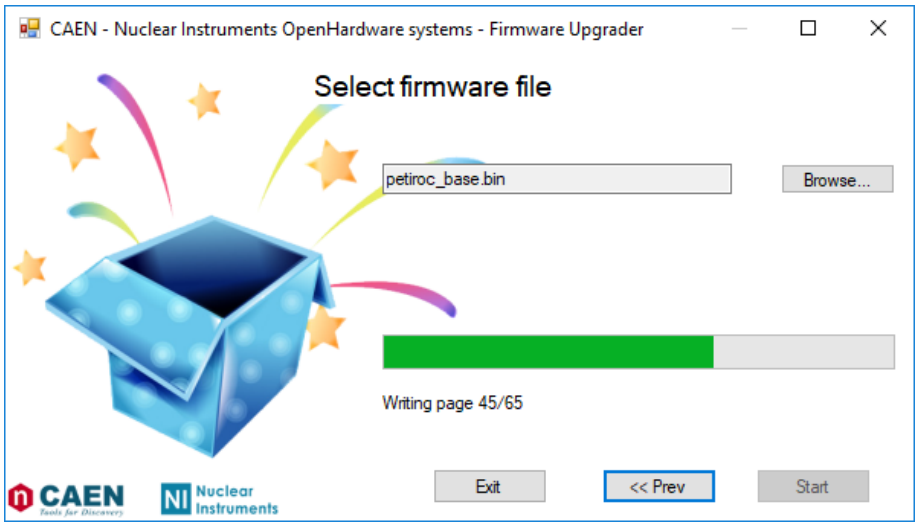
- A wizard will guide you in the firmware upgrade process. All supported hardware connected by USB to the computer will be listed in the combo box. **Select the hardware** you want to load the firmware on. Pushing identify a led on the selected device will start to blink



- Once the board is chosen from the combo box, press "**Next**" to select the firmware file to load.



- **Load the .bin file,** containing the firmware code and press the "**Start"** button.



- When the firmware is fully loaded a message invites the user to **power cycle the board** in order to load the new firmware.

- Remember to **move the bootloader jumper in position 2-3**, in order to allow the board to run in default mode and load the firmware from the flash memory.

WARNING: There is no way for the system to recognize if a firmware is correct for a given hardware. For example, a firmware designed for another compatible board can be loaded on a DT5550W but it can damage the board. In the same way it is possible to load a firmware to read Petiroc while a Citiroc piggyback board is connected. User must check the hardware target for a specific firmware BEFORE load it on the flash memory.

Note: the latest release of the DT5550W default firmware is available on CAEN website at the relative product page. You can load it on the board using the OpenHardware -Firmware Upgrader, following the procedure described above.

Note: it is possible to upgrade the firmware in the volatile FPGA memory, using SCI-Compiler and the micro-USB port on the DT5550W (refer to **[RD2]** for more details). In this way it is possible to connect directly to the FPGA and perform a **fast firmware upgrade**. Using the mini-USB port, the firmware is written in a volatile way directly into the FPGA in a couple of seconds (against about few minutes with bootloader flash tool): a power cycle will reload the firmware stored in the flash memory. This can be useful during development time.

14 DT5550W Readout Software

DT5550W Readout Software is a **free and open-source** software developed for **Windows OS** to operate **in conjunction with the default firmware** of the DT5550W, in order to provide a ready-to-use solution.

The software implements typical features needed to acquire and process data in nuclear spectroscopy and particle physics:

- Simultaneous readout of up to 4 Weeroc ASICs
- Energy measurements
- Time of flight measurements
- Online Cluster reconstruction between multiple ASICs, based on timestamp
- Imaging
- Energy and time spectra plot
- Event list mode readout (energy, time, position)
- Monitor of the analog signals
- High Voltage management (if available on the piggyback board)
- Data saving in ASCII format

Note: not all listed features are implemented for each ASIC model and for each readout mode. When not available, the related tabs are disabled in the software GUI.

The software is distributed both as compiled application and as source code. The source code is written in VB.NET and C# and it can be easily customized by the user to adapt to a custom firmware and for any other need. In order to recompile the DT5550W Readout Software, a free version of Visual Studio .NET 2015 or later must be installed on the user's PC.

The software uses a SDK which makes available the methods and proprietary structures of each ASIC model supported. Depending on the ASIC, the software automatically uses the correct functions. The SDK is distributed open source as VB.NET project written in C# and compiled as a DLL.

Note: the communication is managed by the *niusb3_core.dll* library, which can be compiled also under Linux OS. The user can extend the support for his custom readout software in Linux, implementing the C# functions not available in the DLL.

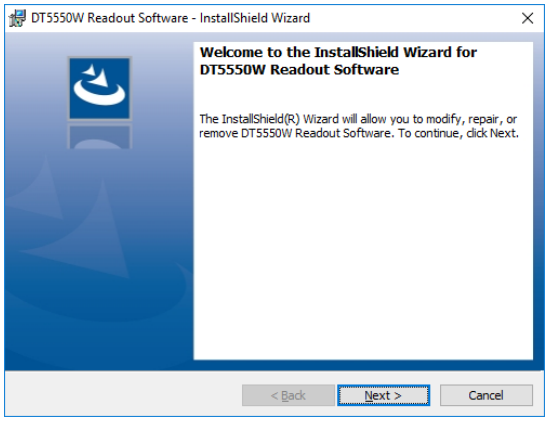
Software installation

DT5550W Readout Software is compliant with Windows 10-64bit

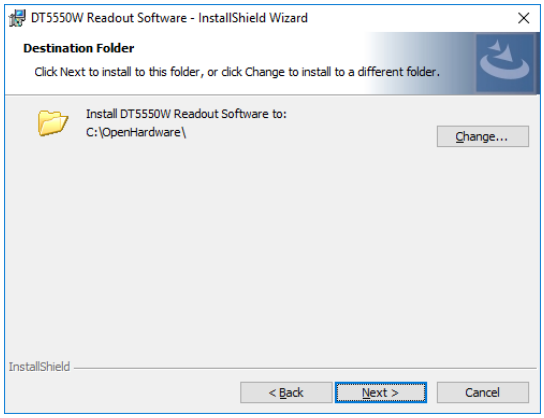
Note: The software is standalone and does not require the prior installation of any library

In order to install the DT5550W Readout Software, follow the steps below:

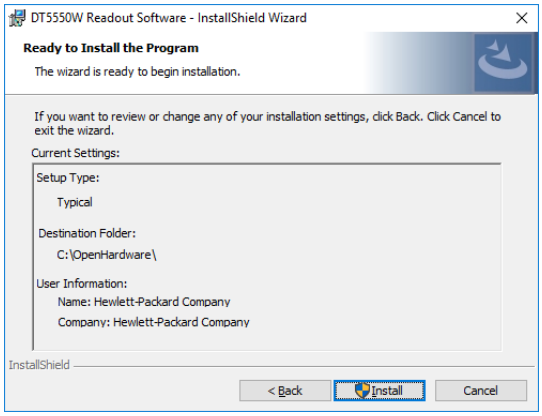
- Download the software package from the DT5550W product page on the CAEN website (**login required**)
- Unzip and run the executable as administrator.
- A setup wizard will start. **Press "Next" to continue.**



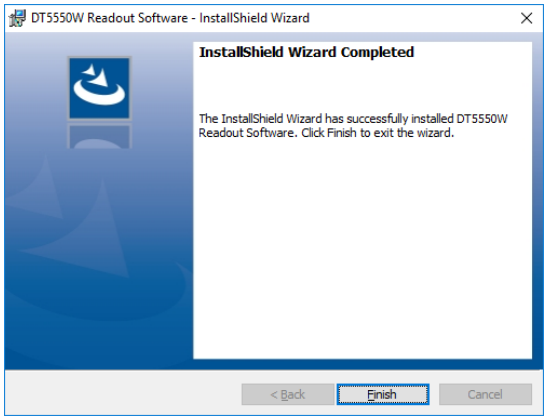
- Choose the destination folder and **press "Next".**



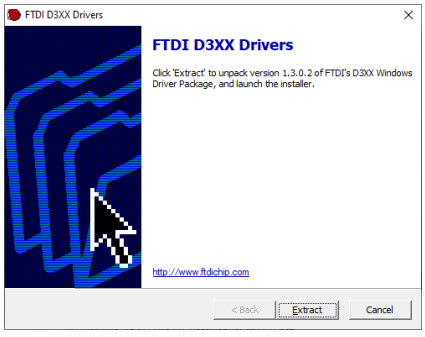
- **Click "Install"** to complete software installation.

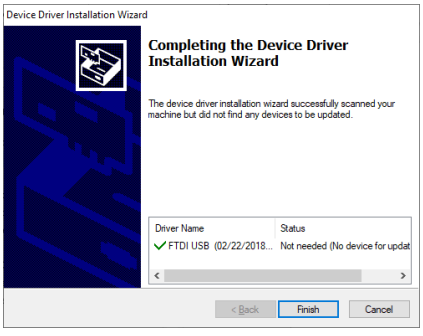


- Wait until installation is completed and press "**Finish**" to complete the setup.



- Follow the instruction to install the FTDI USB drivers





- Now it is possible to launch the DT5550W Readout software from the Windows programs menu.

Board Connection

After launching the software, the "Connection" window will open, and the user is asked to connect a board specifying the connection parameters:

- *Device*: selection of the serial number of the DT5550W board to be connected, choosing from a combo box.
- *ASIC model*: allows to specify the ASIC model (PETIROC, CITIROC,…). In *Auto* mode, the software automatically detects the ASIC mounted on the piggyback board.
- *ASIC count:* allows to specify the number of ASICs. In *Auto* mode, the software automatically detects the number of ASICs mounted on the piggyback board.

Note: At the moment, the software does not support connection to multiple boards: multiple instances of the software must be opened to manage acquisitions on each board.

Press *Connect* to establish a connection with the specified parameters and *Refresh* to update the list of devices listed in the Combo box or the ASIC model/count.

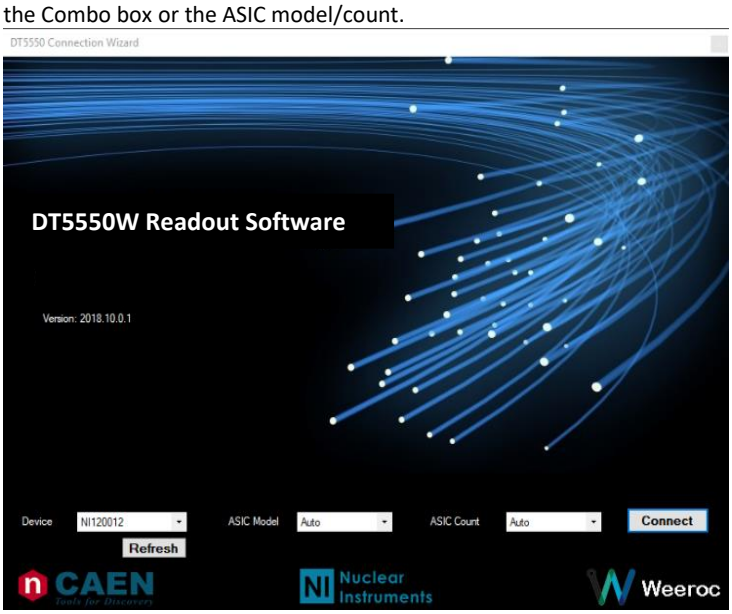


Figure 14.1: the "Connection" window at start-up of the DT5550W Readout Software

Software GUI Description

After successful connection, the main window will appear. The window is divided in five areas, as highlighted in **Figure 14.2**:

- Menu and Control Toolbar
- Main Working Area, with different tabs available
  - Spectrum
  - Time Distribution
  - Hit per Channel
  - Analog Monitor
  - ASIC Monitor
  - Settings
  - Mapping
- Event Display Area
- Log Area
- DAQ Status Bar

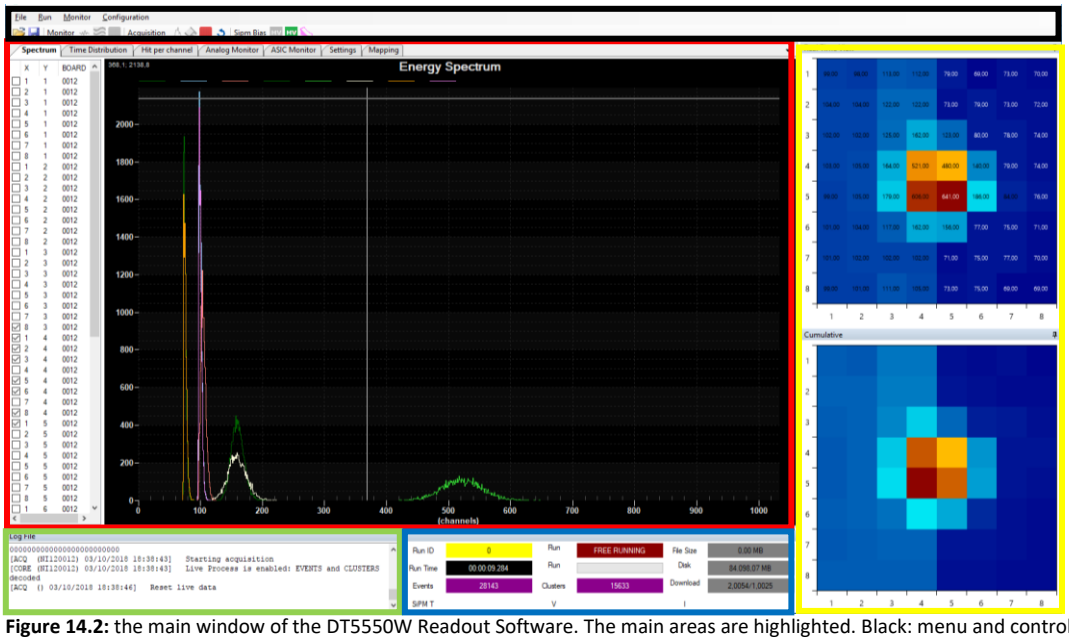


Figure 14.2: the main window of the DT5550W Readout Software. The main areas are highlighted. Black: menu and control toolbar. Red: main working area. Yellow: event display area. Green: log area. Blue: DAQ status.

Note: not all listed tabs and functions are implemented for each ASIC model and for each readout mode. When not available, the related tabs are disabled in the software GUI.

Menu and Control Toolbar

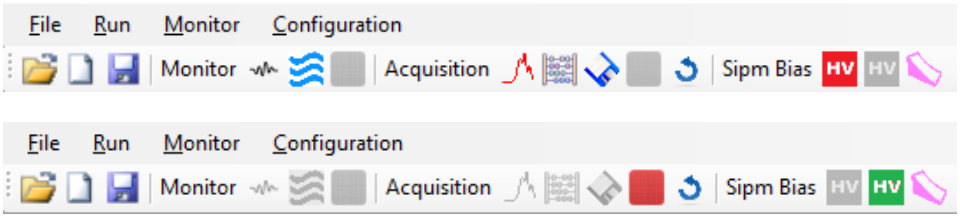


Figure 14.3: the Menu and Control Toolbar of the DT5550W Readout Software, before (top) and during (bottom) acquisition.

The *Menu and Control Toolbar* contains the following buttons:

- Open: open a configuration file
- Save: save a configuration file

Monitor (Oscilloscope acquisition configuration)

- Single Shot: acquire a single waveform in the oscilloscope
- Wave: start continuous acquisition of waveforms on the oscilloscope
- Stop: stop the oscilloscope acquisition

Acquisition

- Spectrum: start energy/time acquisition according to the ASIC settings (no data saving)
- Abacus (CITIROC only): start photon counting acquisition according to the ASIC settings
- Save: start energy/time or photon counting acquisition according to the ASIC settings and dump data on file.
- Stop: stop current acquisition
- Reset: reset the online spectra

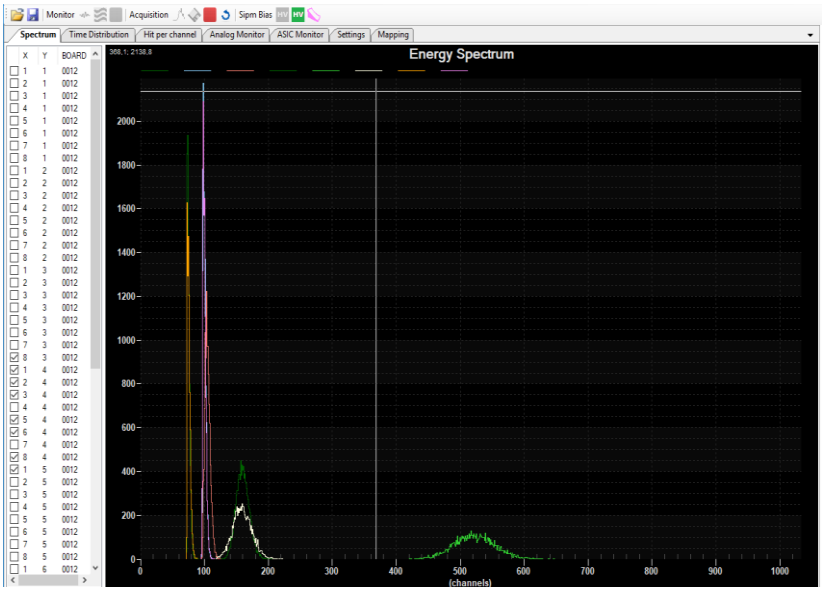
SiPM Bias (available for A55PETx and A55CITx)

- ❖ Turns ON/OFF the SiPM Power Supply. The Voltage is selected in the *Settings* tab. It is not possible to change the Voltage status during acquisition.
- ❖ DCR, to open the channel counts monitor

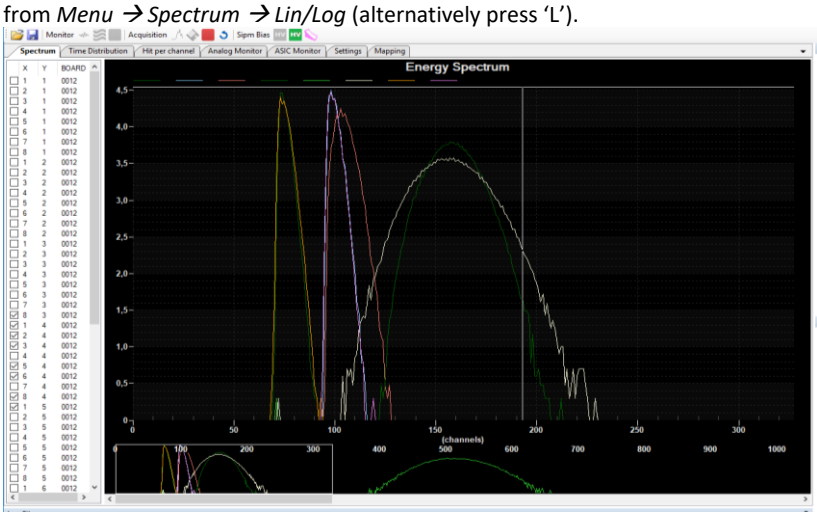
Main Working Area

The *Main Working Area* hosts all the tabs related to the ASICs settings, configuration of the acquisition and online plots (spectra, oscilloscope, …). Tabs can change depending on the ASIC model. The main tabs are:

- ***Energy/EnergyLG/EnergyHG***, to visualize the energy spectrum channel by channel. The number of bins of the spectrum depends on the ASIC model (for PETIROC, 102 bins).
  The spectrum of multiple channels can be displayed on the same plot, by checking the relative checkboxes in the channels list on the left of the tab. The channels are listed as element of a matrix (X-Y coordinates) reproducing the detector shape.
  Also the sum spectrum, realized summing all energy values of all channels. It is possible to set a scaling factor in the *Settings* for this spectrum.



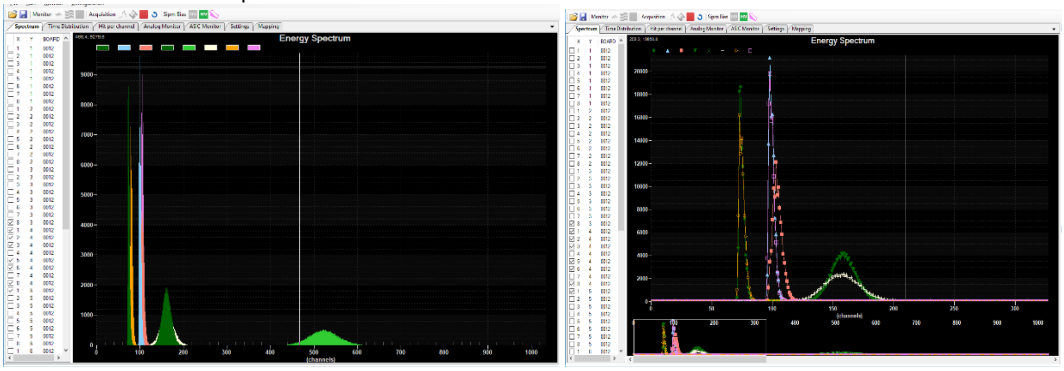
It is possible to zoom in the spectrum with keyboard command and then the mouse to drag on the interested area: rectangular zoom (press 'Z'), horizontal zoom (press 'H'), vertical zoom (press 'V'), unzoom (press 'U').
The spectrum can be displayed in bot linear and semi-log scale. It is possible to switch between the two modes from *Menu* → *Spectrum* → *Lin/Log* (alternatively press 'L').



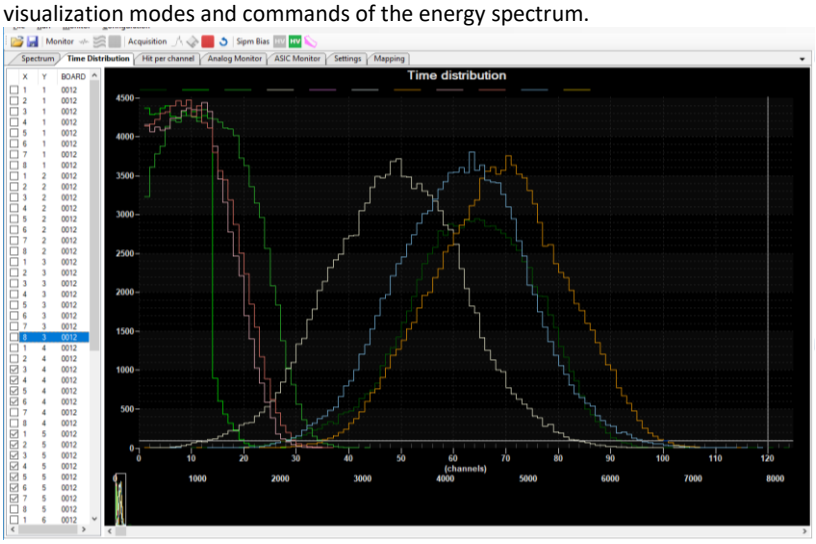
It is also possible to change the plot type: press 'O' to cycle between plot modes. Available plot modes are:

- Step
- Line
- Line with interpolation
- Bar
- Area
- Area with interpolation
- Dot

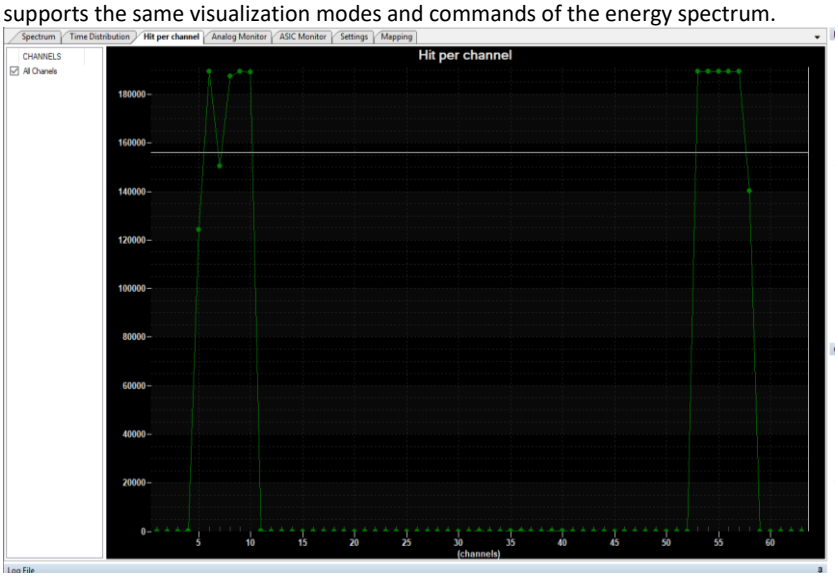
- Dot with Line
- Dot with interpolation



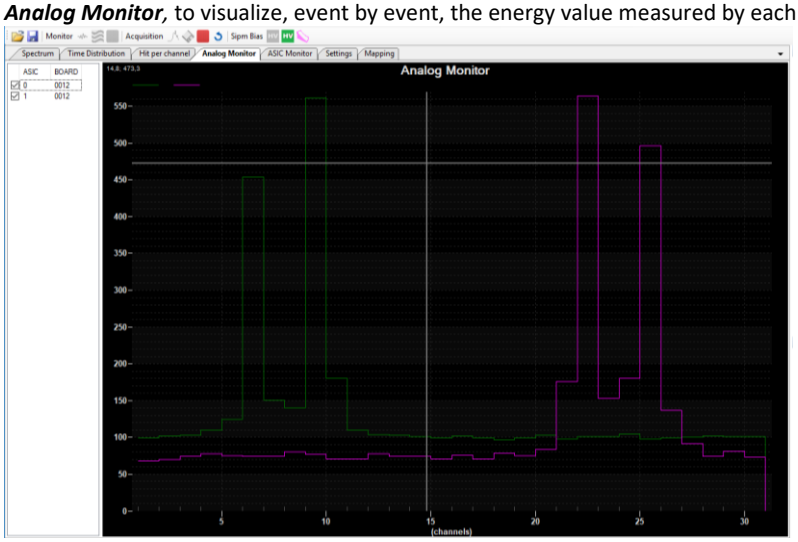
❖ ***Time Distribution,*** to visualize the time-of-flight spectrum with respect to a T0 signal or to the ASICs first triggering channel within an event packet (depends on the ASIC model and the *Settings*). It supports the same visualization modes and commands of the energy spectrum.



❖ ***Hit per channel,*** to visualize the number of triggers detected on each channel from the acquisition start. It supports the same visualization modes and commands of the energy spectrum.



- ***Analog Monitor***, to visualize, event by event, the energy value measured by each ASIC channel.



- ***ASIC Monitor***, to probe the internal ASIC signals. Specific for each ASIC model, refer to the related A55xxxx Piggyback Board User Manual.

- ***Scan***, to perform the scanning of some ASICs parameters and view the results on plot (works with A55CITx piggyback only)

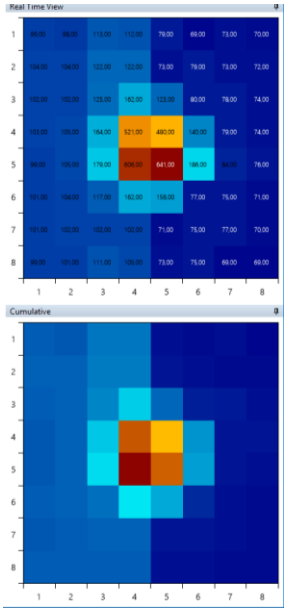
- ***Settings***, to set the specific parameters of each ASIC and configure the acquisition. Specific for each ASIC model, refer to the related A55xxxx Piggyback Board User Manual.

- ***Mapping***, to define the association between the pixels of the detectors and the ASIC channels. Refer to Sect.

Each panel can be undocked and moved externally to the software window.

Note: the tabs which are specific for each ASIC model (such as the *Settings*) are detailed in the related piggyback board User Manual.

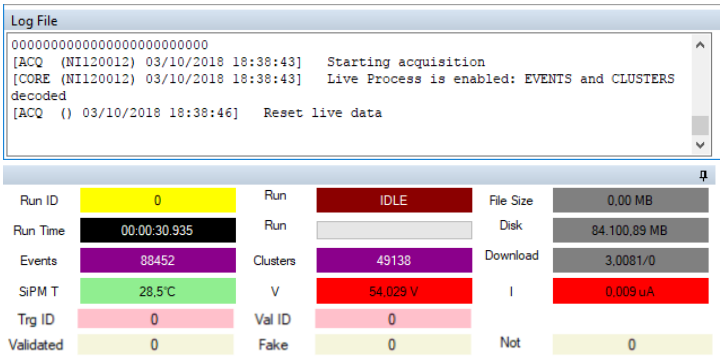
Imaging



In the *Imaging* area, the results of energy acquisition are shown as real-time and cumulative image. The real-time image shows the energy acquired on each channel event by event, while the cumulative image shows the sum of the energy channel by channel, acquired during the entire run.

It is possible to ZOOM in the image using the mouse wheel. Press ‘a’ on the keyboard to perform a zoom to fit.

Log Area and DAQ Status Bar



In the *Log Area*, are reported all the interactions of the software with the board, included the bitstream sent to the ASICs. In this way, it is possible to capture a configuration to be used on a custom board.

In the *DAQ Status Bar*, the acquisition status and stats are reported, included the high voltage status (when available on the piggyback board) , the piggyback temperature sensors value and validation parameters

After board connection, the *Log Area* shows, in the first lines, the model of the detected piggyback board, the number of ASICs, the serial number and the firmware version loaded on the motherboard.

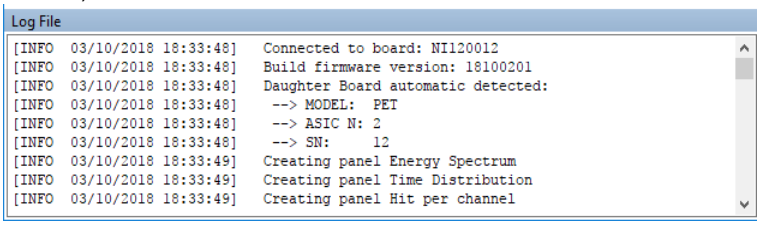


Figure 14.4: the *Log Area* after board connection. In this case, a PETIROC piggyback with two chips is detected.

How to perform an acquisition

Before starting an acquisition, the user should set all the relevant parameters in the *Settings* tab. Refer to the specific piggyback User Manual for a detailed description of the settings.

The acquisition is started pressing the correspondent button in the *Menu and Control Toolbar (Acquisition section)*. The Spectrum icon starts an acquisition without data saving, while the Floppy Disk icon starts an acquisition with data saving in the specified file format.

After pressing the Floppy Disk icon, the *Start Run* window automatically opens. In this menu it is possible to specify the data saving folder and compile the logbook, with the relevant acquisition parameters, the date and other annotations. It is also possible to set the Target mode for the acquisition: in *Free running* the acquisition must be stop manually, in *Run Time* the user must specify a target time at which the acquisition is stopped, in *Cluster Number* the user must specify the target number of events in a cluster. It is possible to choose the acquisition *Mode* between *Spectroscopy* and *Photon counting* (A55CITx piggyback only), in order to save energy/time or counts data respectively.

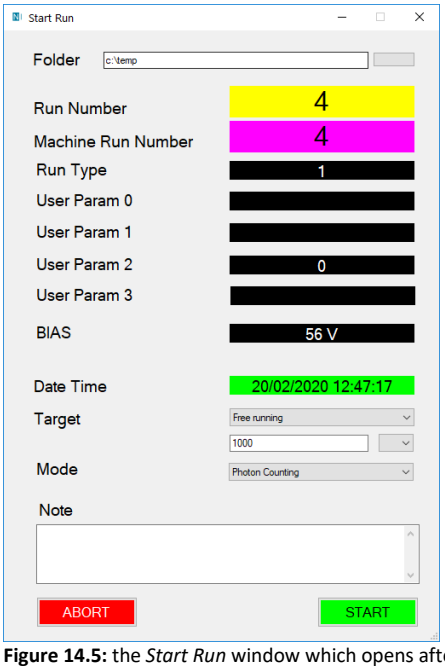


Figure 14.5: the *Start Run* window which opens after the acquisition with data saving is started.

After setting the fields in the *Start Run* window, press 'Start' to effectively start the board acquisition with specified parameters, press 'Abort' to return to the main software window.

After the acquisition is started, the user can visualize on plots the results of the acquisition, using the tabs described in the previous paragraphs.

How to remap a detector geometry

In order to map the channels of the ASIC directly on the pixel position of a detector, the DT5550W Readout Software uses a configurable conversion map, which can be set in the *Mapping* tab.

The map is a 2D grid, with configurable dimensions, in order to reproduce the physical shape of the detector. Once the dimensions are established, it is possible to associate each cell of the matrix to a specific ASIC channel in a specific board. All this information is used to reconstruct the image in the *Event Display* area.

It is possible to configure the number of rows and columns of the grid. The Resize button can be used to redefine the dimensions of the grid, the *Default* button restores the standard dimension of the map according to the number of ASICs installed on the piggyback board, the *Board Layout* button restores the default channel-pixel assignment.

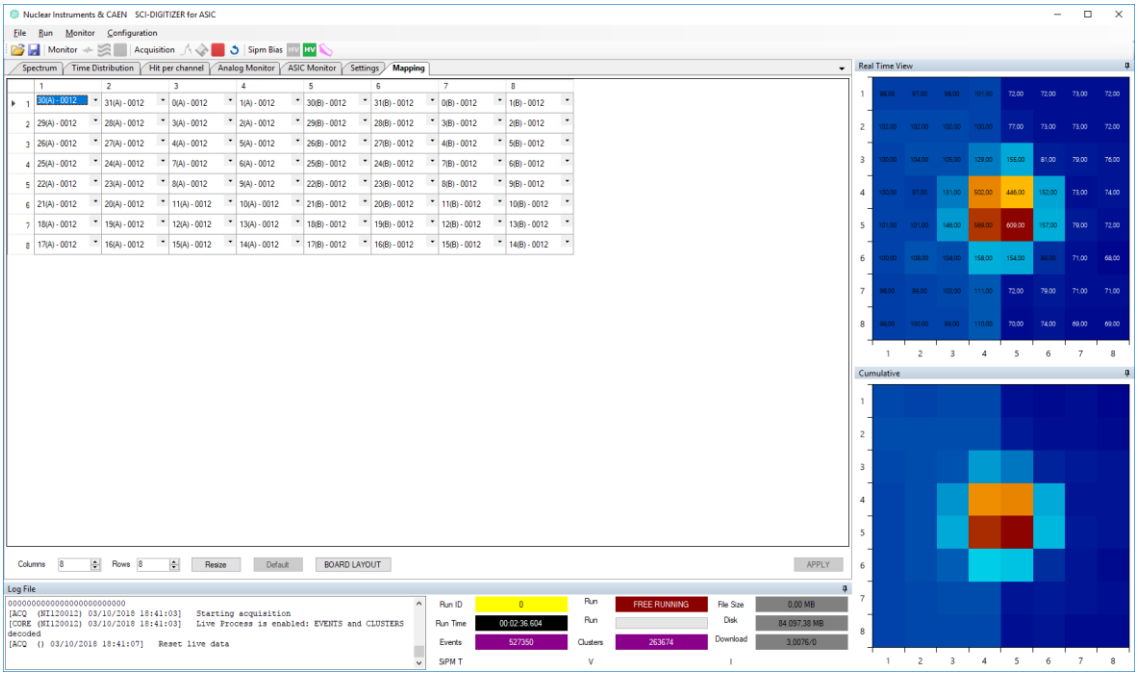
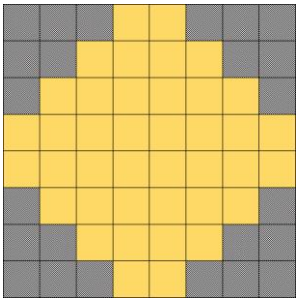


Figure 14.6: the *Mapping* tab, to associate the ASIC channels to detector pixels.

In order to modify the channel-pixel mapping, it is sufficient to click on the desired cell of the grid and select one of the ASIC channels from the combo box. It is possible not to assign any ASIC channel to a cell of the grid: this is particularly useful to obtain a reproduction of a non-square detector. The pixels which are not assigned to any channels will always count a zero energy.



The user must press *Apply* to assign the mapping grid.

15 Instructions for Cleaning

The equipment may be cleaned with compressed air spray, isopropyl alcohol or deionized water and air dried.

Cleaning the Touchscreen

In order to clean the touchscreen (if present), wipe the screen with a towelette designed for cleaning monitors or with a clean cloth moistened with water.
Do not use sprays or aerosols directly on the screen; the liquid may seep into the housing and damage a component. Never use solvents or flammable liquids on the screen.

Cleaning the air vents

It is recommended to occasionally clean the air vents (if present) on all vented sides of the board. Lint, dust, and other foreign matter can block the vents and limit the airflow. Be sure to unplug the board before cleaning the air vents and follow the general cleaning safety precautions.

General cleaning safety precautions

CAEN recommends cleaning the device using the following precautions:

1) Never use solvents or flammable solutions to clean the board.
2) Never immerse any parts in water or cleaning solutions; apply any liquids to a clean cloth and then use the cloth on the component.
3) Always unplug the board when cleaning with liquids or damp cloths.
4) Always unplug the board before cleaning the air vents (if present)
5) Wear safety glasses equipped with side shields when cleaning the board

16 Device decommissioning

After its intended service, it is recommended to perform the following actions:

- Detach all the signal/input/output cable
- Wrap the device in its protective packaging
- Insert the device in its packaging (if present)

THE DEVICE SHALL BE STORED ONLY AT THE ENVIRONMENT CONDITION SPECIFIED IN THE MANUAL, OTHERWISE PERFORMANCE AND SAFETY WILL BE NOT GUARANTEED

17 Disposal

The disposal of the equipment must be managed in accordance with Directive 2012/19 / EU on waste electrical and electronic equipment (WEEE).

The crossed bin symbol indicates that the device shall not be disposed with regular residual waste.

18 Technical Support

CAEN makes available the technical support of its specialists for request concerning the software and the hardware. Use the support form available at the following link:

https://www.caen.it/support-services/support-form/

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