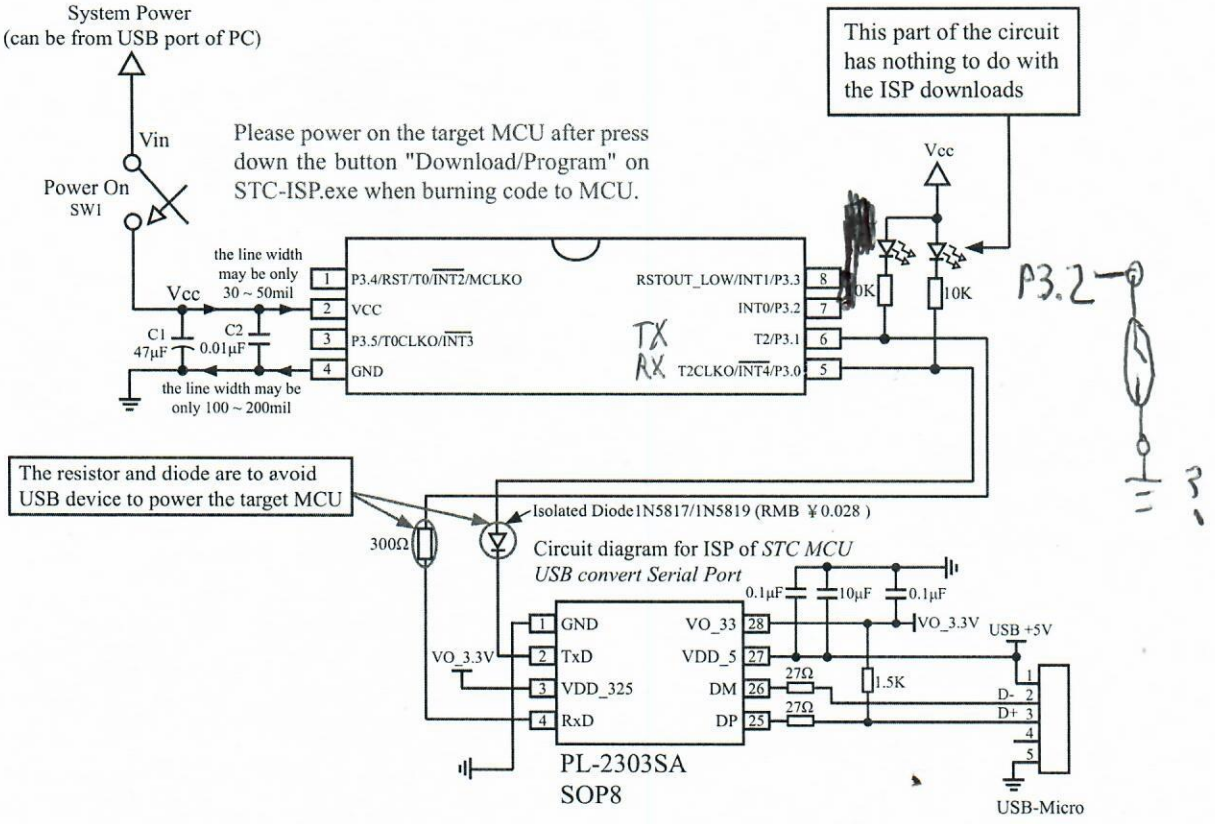
6.2 Application Circuit Diagram for ISP using USB Chip PL-2303SA to convert Serial Port

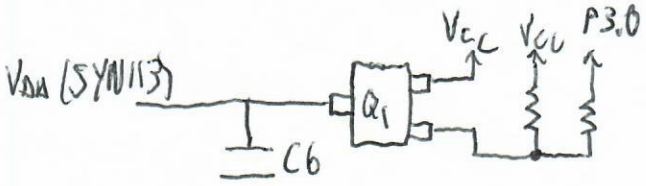


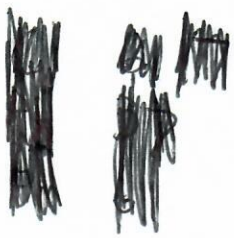
Internal hghly reliable Reset, External reset circuit can be completely removed.

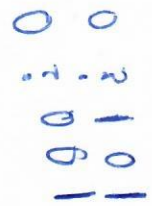
P3.4/RST/T0/INT2/MCLKO pin factory defaults to the I/O port, which can be set as RST reset pin(active high) through the STC-ISP programmer.

Internal high-precise R/C clock(±3%), ±1% temperature drift (-40℃~+85℃) while ±0.6% in normal temperature (-20℃~+65℃). External expensive crysal can be completely removed.

Recommend to add decoupling capacitor C1(47μF) and C2(0.1μF) between Vcc and Gnd that can remove power noise and improve the anti-interference ability.



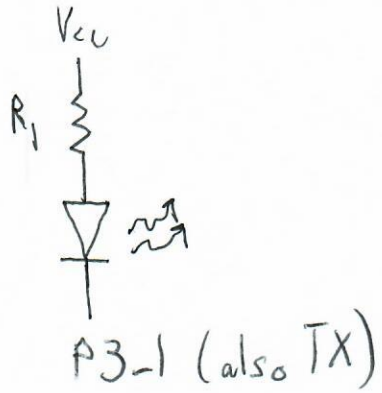




7. Pin Descriptions of STC15F101W series MCU

MNEMONIC	Pin Number (SOP8/DIP8/DFN8)	DESCRIPTION	
P3.0/$\overline{INT4}$ /T2CLKO	5	P3.0	common I/O port PORT3[0]
		$\overline{INT4}$	External interrupt 4, which only can be generated on falling edge. $\overline{INT4}$ supports power-down waking-up
		T2CLKO	T2 Clock Output The pin can be configured for T2CLKO by setting INT_CLKO[2] bit /T2CLKO
P3.1/T2	6	P3.1	common I/O port PORT3[1]
		T2	External input of Timer/Counter 2
P3.2/INT0	7	P3.2	common I/O port PORT3[2]
		INT0	External interrupt 0, which both can be generated on rising and falling edge. INT0 only can generate interrupt on falling edge if IT0 (TCON.0) is set to 1. And, INT0 both can generate interrupt on rising and falling edge if IT0 (TCON.0) is set to 0.
P3.3/INT1/ RSTOUT_LOW	8	P3.3	common I/O port PORT3[3]
		INT1	External interrupt 1, which both can be generated on rising and falling edge. INT1 only can generate interrupt on falling edge if IT1 (TCON.2) is set to 1. And, INT1 both can generate interrupt on rising and falling edge if IT1 (TCON.2) is set to 0. INT1 supports power-down waking-up
		RSTOUT_LOW	the pin output low after power-on and during reset, which can be set to output high by software
P3.4/RST/T0/ $\overline{INT2}$/MCLKO	1	P3.4	common I/O port PORT3[4]
		RST	Reset pin. A high on this pin for at least two machine cycles will reset the device.
		T0	External input of Timer/Counter 0
		$\overline{INT2}$	External interrupt 2, which only can be generated on falling edge. $\overline{INT2}$ supports power-down waking-up
		MCLKO	Master clock output; the output frequency can be MCLK/1, MCLK/2 and MCLK/4. The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator.
P3.5/T0CLKO/ $\overline{INT3}$	3	P3.5	common I/O port PORT3[5]
		T0CLKO	T0 Clock Output The pin can be configured for T0CLKO by setting INT_CLKO[0] bit /T0CLKO
		$\overline{INT3}$	External interrupt 3, which only can be generated on falling edge. $\overline{INT3}$ supports power-down waking-up
Vcc	2	The positive pole of power	
Gnd	4	The negative pole of power, Gound	

Sense and Drive the World



SYN113/SYN115 Datasheet

(300-450MHz ASK Transmitter)

Version 1.0