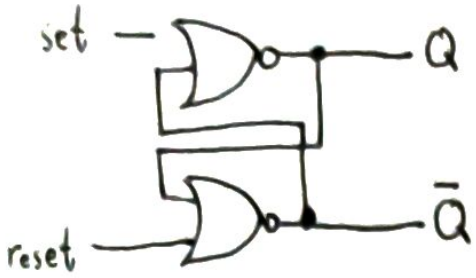
# Flip-Flops & Registers

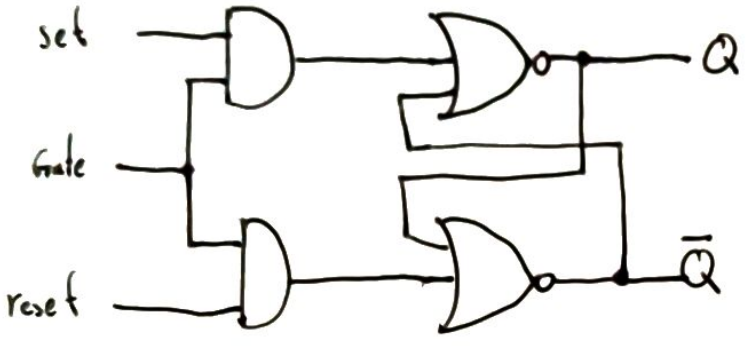
## S-R Flip-flop - data storage circuit




Function table

| set | Reset | Q | $\bar{Q}$ |
|---|---|---|---|
| 0 | 0 | Hold condition | |
| 0 | 1 | Flip-flop reset | |
| 1 | 0 | Flip-flop set | |
| 1 | 1 | Not used | |

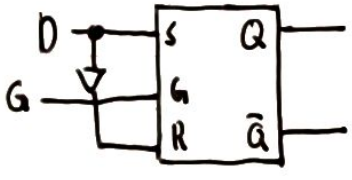
## Gated S-R Flip-flop




If gate = 0, set-reset is disabled & output was the previous output.
If gate = 1 set-reset is read

async = Output immediately to input change.
Sync = Operates sequentially with control input. (like the gate input / clock)

## Gated D-Flip-flop




D-Latch : To be latched means for the output to follow the previous output after the gate or clock input goes to low.