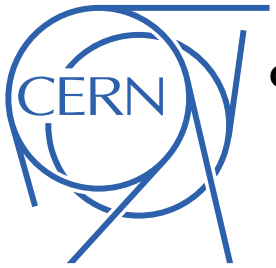

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Technical Specifications
Gennum GN4124 Core For FMC Projects

July 2010

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Abstract

This technical specification describes the HDL controller for Gennum GN4124 chip. It provides a Wishbone master for control and status registers access and a DMA controller for high speed data transfers.

Revision History

Version	Date	Notes
0.1	10-06-2010	Initial release
0.2	12-07-2010	First draft

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Introduction

This specification describes how the core work internally. For each internal block, we give a summary description of its function. The figure 1 show the core with all main blocks.

The structure of this cores and some signals names are based on Gennum cores *Lambo* and *Lotus*.

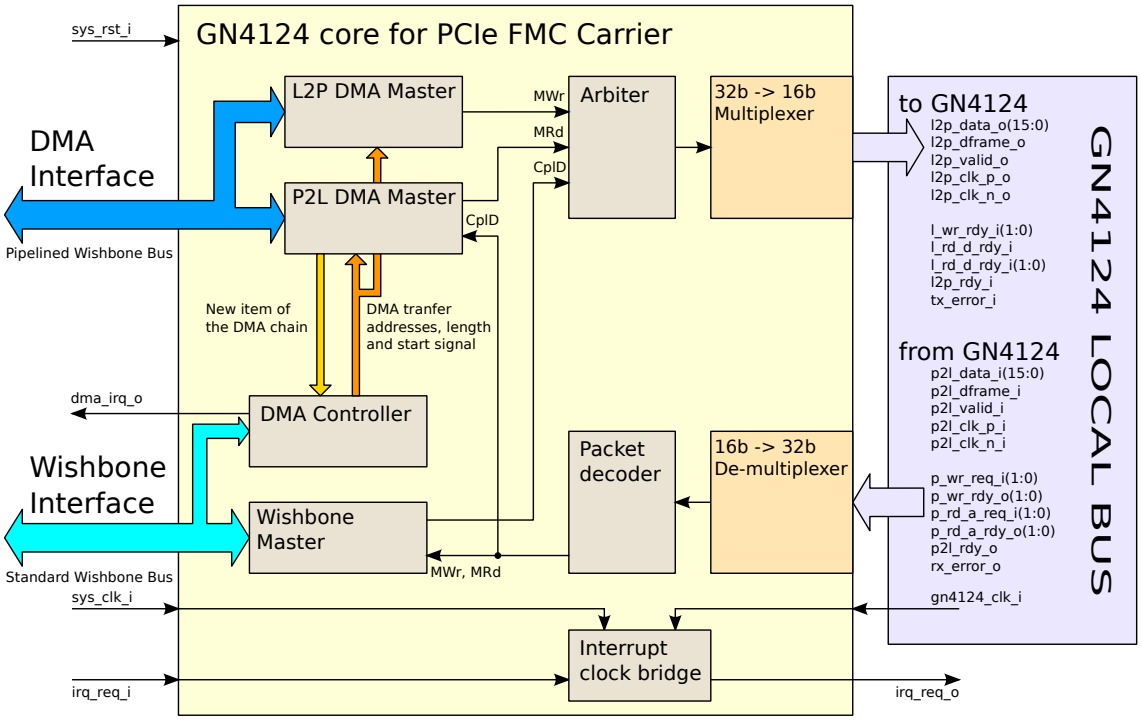

Figure 1: GN4124 core for PCIe FMC carrier

1 De-multiplexer

This block takes the double data rate 16-bit P2L (PCI Express to Local Bus direction) bus from the GN4124 device and converts it to a single data rate 32-bit bus for use inside the GN4124 core.

2 Multiplexer

It takes the internal single data rate 32 bit data and transmits it as double data rate 16-bit data on the L2P (Local Bus to PCI Express direction) bus.

3 Packet decoder

This block extracts header information, address, data, byte enables, and timing controls of the packets from the GN4124 chip. It provides signals like :

- Type of packet (target read request, target write request, master read completion ...)
- Begin of packet
- Address that will increment with data
- Data
- End of packet

4 Wishbone master

The Wishbone master implements a master for the Wishbone interconnection bus. It transforms a PCIe write into a Wishbone write and a PCIe read into a Wishbone read. Only single word reads and writes are supported. PCI express burst are divided in sigle reads and writes.

Data are coming from the packet decoder. Wishbone signals are generated and the master waits for an acknowledge. The incoming requests are saved in a FIFO. The FIFO depth is 16. The Wishbone master is allowing the GN4124 chip to send a request only if the FIFO is empty. The latency of the transfer between the GN4124 chip and the Wishbone master makes this FIFO necessary.

5 DMA controller

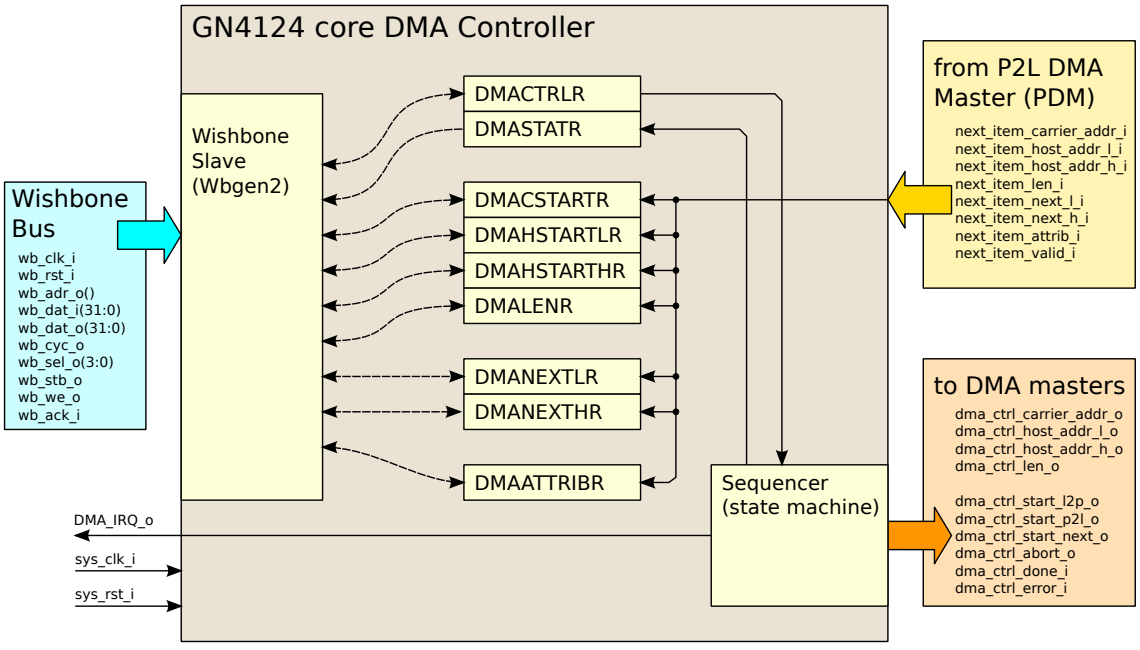

Figure 2: DMA controller

The DMA controller is a Wishbone slave controlled from the PCI Express host with the Wishbone master (see the functional specification). The figure 2 shows the internal of the DMA controller.

The transfer starts when the first bit (LSB) of the DMACTRLR register is asserted. One of the two signals, `dma_ctrl_start_L2P_o` and `dma_ctrl_start_P2L_o`, is set to '1' for one clock cycle. The `dma_ctrl_start_L2P_o` signal controls the DMA L2P master that performs transfers from the carrier

to the PCI Express host and the `dma_ctrl_start_P2L_o` signal controls the DMA P2L master that performs transfers from the PCI Express host to the carrier.

The DMA controller waits for the `dma_ctrl_done_i` signal from one of the two DMA masters that indicates the end of the transfer. The `dma_ctrl_error_i` signal indicates the end of the transfer if an error occurs.

After the end of a transfer, if this transfer is not the last, the controller ask to the P2L DMA master the new item of the DMA chain. The `next_item_valid_i` signal indicates that the DMA master can read the new DMA chain item from the P2L DMA master and starts the new cycle

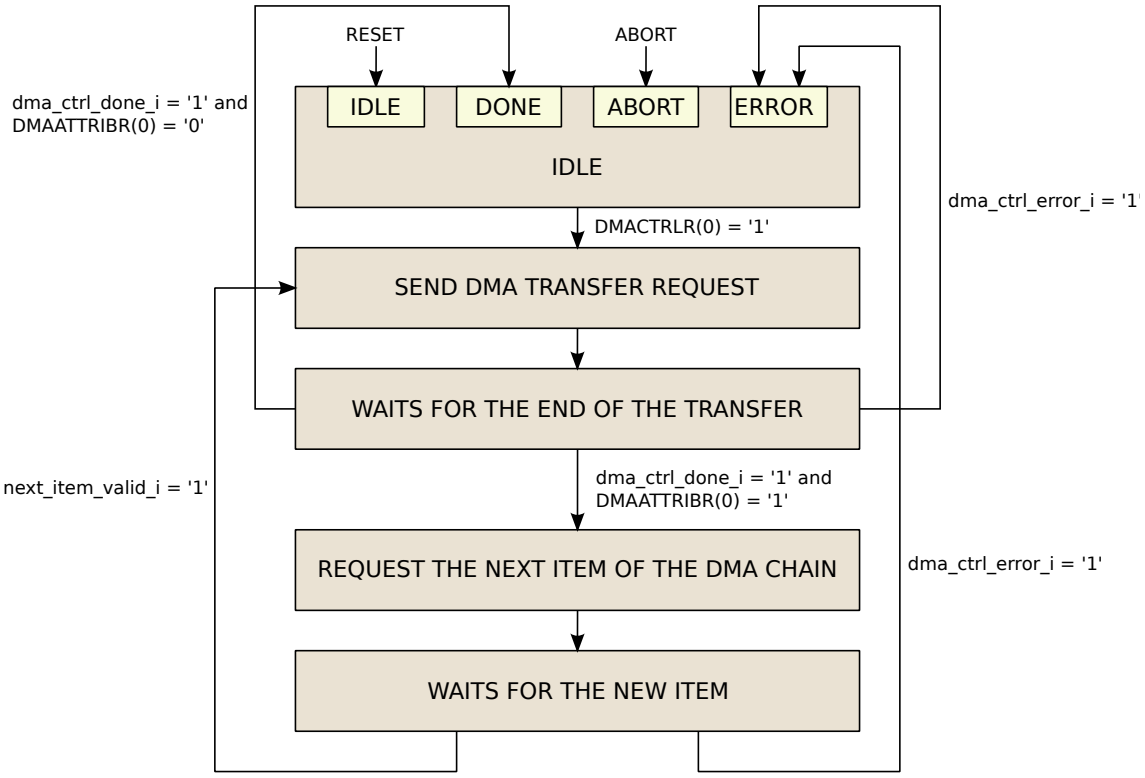

Figure 3: DMA controller state machine

6 L2P DMA Master

The L2P DMA master performs data transfers from the PCI Express host to the FMC carrier. The transfer is split in small blocks of data. The length of this blocks can be configured.

The L2P DMA master sends a master read request on the DMA interface and waits for answer. This transfer is clocked by the `sys_clk_i` signal. The received data are stocked in a FIFO.

When a block of data is in the FIFO, the DMA master sends a master write request to the PCI Express host. This operation is clocked by the GN4124 Local Bus Clock.

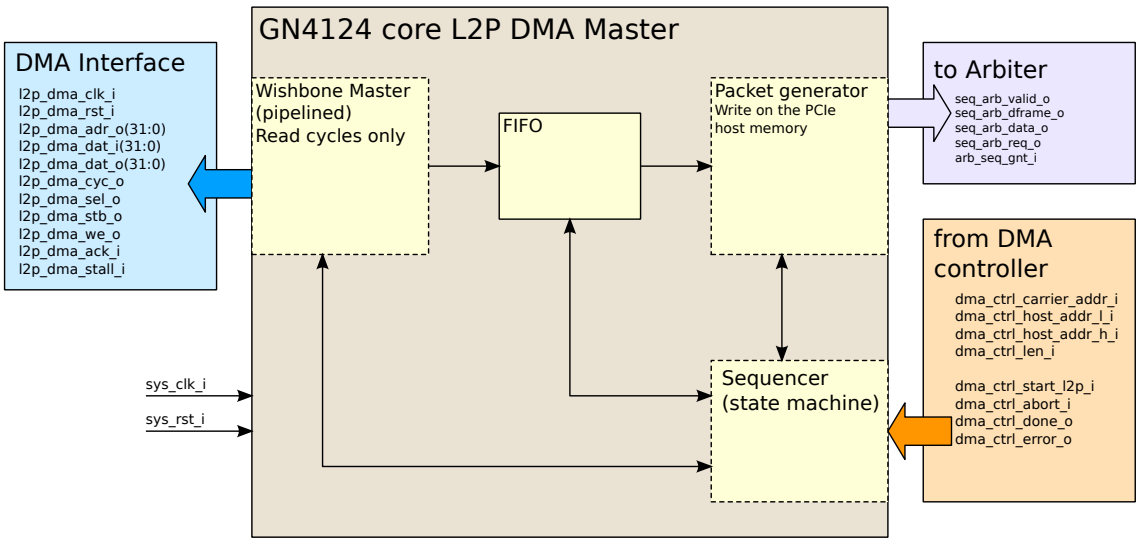

Figure 4: L2P DMA master

7 P2L DMA Master

The P2L DMA master performs data transfers from the FMC carrier to the memory of the PCI Express host. The transfer is split in small blocks of data. The length of this blocks can be configured.

The P2L DMA master sends a memory read request toward the GN4124 chip and waits for the answer. This operation is clocked by the GN4124 Local Bus Clock. The received data are stocked in a FIFO.

When a block of data is in the FIFO, the DMA master starts a master write cycle on the DMA interface of this block. This transfer is clocked by the `sys_clk_i` signal.

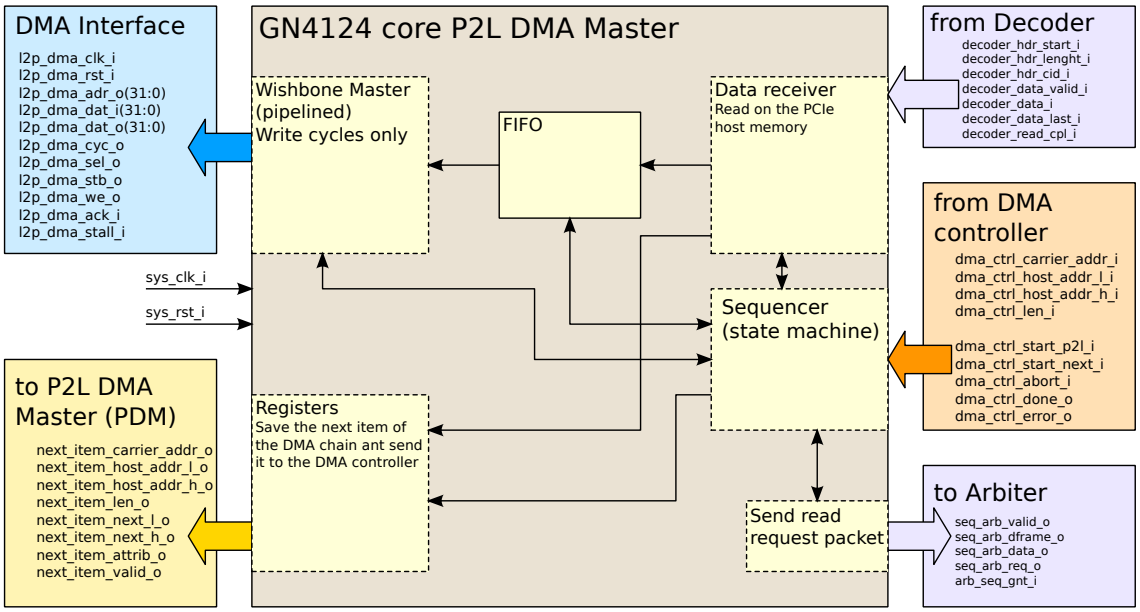

Figure 5: L2P DMA master

8 Arbiter

Arbitrate between Wishbone master and the two DMA masters. The arbiter is waiting for a request signal from one of this blocks and it grants the bus to the first requester until the end of the packet.

The highest priority is for Wishbone master.

9 Interrupt clock bridge

It transforms input interrupt one-tick-long pulse clocked by `sys_clk_i` in a one-tick-long pulse clocked by the GN4124 local bus clock.