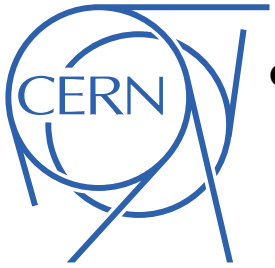

ORGANISATION EUROPÉENNE POUR LA RECHERCHE NUCLÉAIRE
EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

CERN BE-CO-HT

Functional Specifications
Gennum GN4124 Core For FMC Projects

May 2010

Edited by:
Simon Deprez

Checked by:

Abstract

This functional specification describes the HDL controller for Gennum GN4124 chip. This chip is used on the PCI express FMC carrier. It provides a Wishbone master for control and status registers access and a DMA controller for high speed data transfers.

Revision History

Version	Date	Notes
0.1	21-05-2010	Initial release

Contents

List of Figures

Introduction

1 PCIe FMC carrier

The PCIe FMC carrier[1] will be associated with several FMC[2] mezzanines.

Each FMC mezzanine used with the PCIe FMC carrier will need a specific HDL configuration. The HDL code should be generic for reuse the carrier specific modules with other the FMC mezzanines.

The communication between modules is essentially based on the Wishbone bus.

2 GN4124 core for PCIe FMC carrier

This core provides a Wishbone master to access control registers and read status. The Wishbone[3] bus is used for almost all communications between modules. The different soft cores are reusable.

A simple DMA master is used for high speed data transfers of mezzanine card acquisitions.

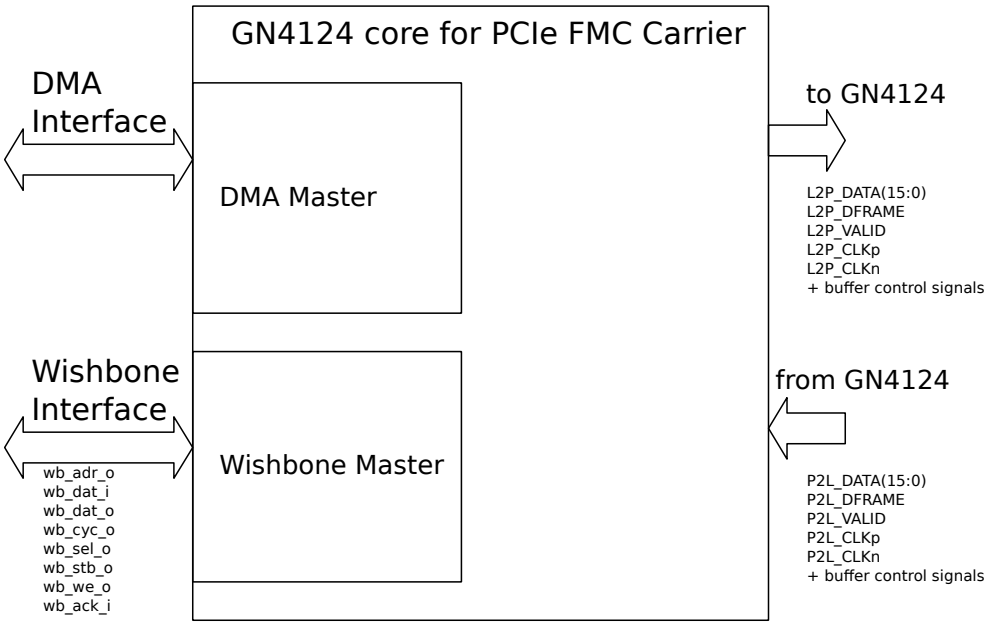

Figure 1: GN4124 core for PCIe FMC carrier

2.1 GN4124 Local Bus Interface

The GN4124 is a 4-lane PCI express to local bus bridge that is designed to work with a FPGA device to provide an high speed serial access for an application.

[1] See http://www.ohwr.org/projects/fmc-pci-carrier.
[2] See VITA FMC standard: http://www.vita.com/fmc.
[3] See http://opencores.org/downloads/wbspec_b3.pdf.

The GN412x PCI Express family Reference Manual[4] (52624-0 June 2009) describes the local bus interface at page 40.

The data exchange is based on PCI express packets, but with incomplete and simplified headers.

2.2 DMA Interface

The DMA interface is composed of two Wishbone-like bus without acknowledge mechanism. One performs application to host communications and the second, the host to application communications.

For the FMCADC100M14b4cha[5] card, the first communication direction only is used.

2.3 Wishbone interface

The Wishbone master transforms PCIe write into Wishbone write and a PCIe read into a Wishbone read. This Wishbone master should provide burst reads and writes.

WISHBONE DATASHEET for the 32-bit MASTER with 8-bit granularity		
Description	Specification	
General description	Wishbone master controlled by PCI express	
Supported cycles	MASTER, READ/WRITE MASTER, BLOCK READ/WRITE	
Data port, size: Data port, granularity: Data port, maximum operand size Data transfer ordering: Clock frequency constraints:	32-bit 8-bit 32-bit Big endian and/or little endian 100 MHz (Gennum IP local clock)	
Supported signal list and cross reference to equivalent WISHBONE signals	Signal Name CLK_O CYC_O STB_O ADR_O(10..0) DAT_I(31..0) DAT_O(31..0) WE_O ACK_I	WISHBONE Equiv. CLK_I CYC_O STB_O ADR_O() DAT_I() DAT_O() WE_O ACK_I

2.4 Interrupts

The interrupt signal is directly wired to GN4124 chip GPIO. When configured, the chip sends the MSI (Message Signaled Interrupts) to the host.

[4] See http://my.gennum.com/mygennum/view.php/gn4124-gullwing.
[5] See the FMCADC100M14b4cha HDL specification: http://www.ohwr.org/attachments/147/adc100m14b4cha.pdf.