CprE 381, Computer Organization and Assembly Level Programming

Team Contract – Project Part 2

Project Teams Group #: _Section C, Group 4_____

Team Members: _____Owen Jewell_____

_____Corey Heithoff_____

_____Luca Cano_____

_____ Jason Di Giovanni _____

Course Goals: *List and acknowledge the goals of your individual team members. Examples may include:*

- Pass the class
- Mostly try to minimize the number of lost points (follow the rubric diligently)
- learn about computer architecture
- know enough to understand the security risks posed by hardware primitives

Team Expectations:

- **Conduct:** Show up to group meetings with a good attitude and be willing to put in your share of the work.

- **Communication:** Snapchat group chat. Communicate as needed, and try to respond within the day. If urgent, try to respond within 2 hours.

- **Group conventions:** Do files as needed on a file by file basis. GitHub repo to manage code base and version control. Files names should be enough to know what it is. Commenting when needed for complex systems. Systems can be created as a project to compile and simulate easily. Push to own branch and check functionality before merging into main.

- **Meetings:** Monday 1:00 pm - 2:30 pm TLA (Work together in person)
  Thursday 3:30 pm - 5:00 pm TLA (Work on whatever responsibilities)

- **Peer Evaluation Criteria:**
  - Communication
  - Commit frequencies to git
  - Availability/Attendance to meetings
  - Timely completion of responsibilities

Role Responsibilities:

11/05/24 = Night before the start of the second lab section (Week 11)
11/12/24 = Night before the start of the third lab section (Week 12)
11/19/24 = Night before the start of the fourth lab section (Week 13)
11/22/24 = Project 2 due 11:59 pm

Lab Part		Estimated Time	Design		Test	
			Lead	**Deadline**	**Lead**	**Deadline**
Soft ware-Sche duled Pipel ine	Control Signals	0.5 hr	Corey	11/05/24	Luca	11/07/24
	Datapath	3 hr	Corey	11/05/24	Luca	11/07/24
	Testing	3 hr	Jason	11/12/24	Owen	11/14/24
	Synthesis (human effort)	0.5 hr	Jason	11/12/24	Owen	11/14/24
Hard ware-Sche duled Pipel ine	Pipeline Register Update	1 hr	Luca	11/12/24	Owen	11/14/24
	Data Hazard Avoidance	4 hr	Owen	11/12/24	Corey	11/14/24
	Control Hazard Avoidance	2-6 hr based on group size	Corey	11/12/24	Jason	11/14/24
	Integration (Hardware-Schedule Pipeline)	3 hr	Luca	11/19/24	Corey	11/22/24
	Testing	3 hr	Owen	11/19/24	Jason	11/22/24
	Synthesis	0.5 hr	Owen	11/19/24	Jason	11/22/24

*Estimated Time is given as a **very rough** guide for even distribution of tasks assuming you've already read through the lab document and have the prerequisite knowledge. Please note that to be done properly, the test programs will require significant time investment, but will result in a much stronger final design.*

Integrity of Work: *Do not delete the following.* We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

Student Signature ___Corey Heithoff_____ **Date** ___10/30/24_____

Student Signature ___Luca Cano_____ **Date** ___10/30/24_____

Student Signature ___Jason Di Giovanni_____ **Date** ___10/30/24_____

Student Signature ____Owen Jewell_____ **Date** _____10/30/24_____