CprE 381, Computer Organization and Assembly Level Programming

Team Contract – Project Part 1

Project Teams Group: _____Section C, Group 4_____

Team Members: _____Luca Cano_____
_____Owen Jewell_____
_____Corey Heithoff_____
_____Jason Di Giovanni_____

Course Goals: *List and acknowledge the goals of your individual team members.*

- Pass the class
- Mostly try to minimize the number of lost points (follow the rubric diligently)
- learn about computer architecture
- know enough to understand the security risks posed by hardware primitives

Team Expectations:

- **Conduct:** Show up to group meetings with a good attitude and be willing to put in your share of the work.

- **Communication:** Snapchat group chat. Communicate as needed, and try to respond within the day. If urgent, try to respond within 2 hours.

- **Group conventions:** Do files as needed on a file by file basis. GitHub repo to manage code base and version control. Files names should be enough to know what it is. Commenting when needed for complex systems. Systems can be created as a project to compile and simulate easily. Push to own branch and check functionality before merging into main.

- **Meetings:** Monday 11:00 am - 12:30 pm TLA (Work together in person)
  Thursday 3:30 pm - 5:00 pm TLA (Work on whatever responsibilities)

- **Peer Evaluation Criteria:**
  - Communication
  - Commit frequencies to git
  - Availability/Attendance to meetings
  - Timely completion of responsibilities

Role Responsibilities:

10/08/24 = Night before the start of the second lab section (Week 7)
10/15/24 = Night before the start of the third lab section (Week 8)
10/22/24 = Night before the start of the fourth lab section (Week 8)
10/25/24 = Project 1 due 11:59 pm

Lab Part	Estimated Time	Design		Test	
		Lead	Timeline	Lead	Timeline
High-level design	1 hr	Corey	10/08/24	Luca	10/15/24
Test programs	4 hr	Owen/Jason	10/08/24	Corey	10/15/24
Control logic	2 hr	Luca	10/08/24	Corey	10/15/24
Fetch logic	3 hr	Corey	10/08/24	Luca	10/15/24
Barrel shifter	2 hr	Owen	10/08/24	Luca	10/15/24
ALU integration + Misc updates	2 hr	Luca	10/15/24	Jason	10/20/24
High-level integration	4 hr	Corey	10/20/24	Owen	10/22/24
Synthesis (human effort)	1.5 hr	Jason	10/22/24	Corey	10/22/24

*Estimated Time is given as a **very rough** guide for even distribution of tasks assuming you've already read through the lab document and have the prerequisite knowledge. Depending on your group's skill and prerequisite knowledge, some tasks may take disproportionately long or short. For your future planning, track this – for future prelabs you will be asked to note why past tasks took longer than expected and how you might avoid such issues in the future.*

Integrity of Work: *Do not delete the following.* We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

Student Signature _____Owen Jewell_____ **Date** ___10/02/24_____

Student Signature _____Luca Cano_____ **Date** ___10/02/24_____

Student Signature _____Corey Heithoff_____ **Date** ____10/02/24_____

Student Signature _____Jason Di Giovanni_____**Date** ____10/09/24_____