GPIO and GPTM Timer Registers

List of Several TM4C Registers by Name (DATASHEET ACRONYM): C MACRO NAME

See also **tm4c123gh6m.h system header file**

GPIO

GPIO Data (GPIODATA): GPIO_PORTx_DATA_R
GPIO Direction (GPIODIR): GPIO_PORTx_DIR_R
GPIO Digital Enable (GPIODEN): GPIO_PORTx_DEN_R
GPIO Alternate Function Select (GPIOAFSEL): GPIO_PORTx_AFSEL_R
GPIO Port Control (GPIOPCTL): GPIO_PORTx_PCTL_R
GPIO Analog Mode Select (GPIOAMSEL): GPIO_PORTx_AMSEL_R
GPIO Run Mode Clock Gating Control (RCGCGPIO): SYSCTL_RCGCGPIO_R
GPIO Peripheral Ready (PRGPIO): SYSCTL_PRGPIO_R

GPIO Interrupt Sense (GPIOIS): GPIO_PORTx_IS_R
GPIO Interrupt Both Edges (GPIOIBE): GPIO_PORTx_IBE_R
GPIO Interrupt Event (GPIOIEV): GPIO_PORTx_IEV_R
GPIO Interrupt Mask (GPIOIM): GPIO_PORTx_IM_R
GPIO Raw Interrupt Status (GPIORIS): GPIO_PORTx_RIS_R
GPIO Masked Interrupt Status (GPIOMIS): GPIO_PORTx_MIS_R
GPIO Interrupt Clear (GPIOICR): GPIO_PORTx_ICR_R

NVIC

NVIC Interrupt Set Enable (ENx): NVIC_ENx_R
NVIC Interrupt Priority (PRIx): NVIC_PRIx_R

GPTM

Listed for Timer A (substitute “B” for “A” for Timer B)
GPTM Configuration (GPTMCFG): TIMER#_CFG_R
GPTM Timer A Mode (GPTMTAMR): TIMER#_TAMR_R
GPTM Control (GPTMCTL): TIMER#_CTL_R
GPTM Timer A Interval Load (GPTMTAILR): TIMER#_TAILR_R
GPTM Timer A Match (GPTMTAMATCHR): TIMER#_TAMATCHR_R
GPTM Timer A Prescale (GPTMTAPR): TIMER#_TAPR_R
GPTM Timer A Prescale Match (GPTMTAPMR): TIMER#_TAPMR_R
GPTM Timer A (GPTMTAR): TIMER#_TAR_R
GPTM Timer A Value (GPTMTAV): TIMER#_TAV_R
GPTM Timer Run Mode Clock Gating Control (RCGCTIMER): SYSCTL_RCGCTIMER_R
GPTM Peripheral Ready (PRTIMER): SYSCTL_PRTIMER_R

GPTM Interrupt Mask (GPTMIMR): TIMER#_IMR_R
GPTM Raw Interrupt Status (GPTMRIS): TIMER#_RIS_R
GPTM Masked Interrupt Status (GPTMMIS): TIMER#_MIS_R
GPTM Interrupt Clear (GPTMICR): TIMER#_ICR_R

Datasheet Table 23-5. GPIO Pins and Alternate Functions

I/O	Pin	Analog Function	Digital Functions (GPIOPCTL PMCx Bit Field Encoding)							
			1	2	3	4	5	6	7	8
PA0	17	-	U0RX	-	-	-	-	-	-	CAN1RX
PA1	18	-	U0TX	-	-	-	-	-	-	CAN1TX
PA2	19	-	-	SSI0CLK	-	-	-	-	-	-
PA3	20	-	-	SSI0FSS	-	-	-	-	-	-
PA4	21	-	-	SSI0RX	-	-	-	-	-	-
PA5	22	-	-	SSI0TX	-	-	-	-	-	-
PA6	23	-	-	-	I2C1SCL	-	M1PWM2	-	-	-
PA7	24	-	-	-	I2C1SDC	-	M1PWM3	-	-	-
PB0	45	USB0ID	U1RX	-	-	-	-	-	T2CCP0	-
PB1	46	USB0VB	U1TX	-	-	-	-	-	T2CCP1	-
PB2	47	-	-	-	I2C0SCL	-	-	-	T3CCP0	-
PB3	48	-	-	-	I2C0SDC	-	-	-	T3CCP1	-
PB4	58	AIN10	-	SSI2CLK	-	M0PWM2	-	-	T1CCP0	CAN0RX
PB5	57	AIN11	-	SSI2FSS	-	M0PWM3	-	-	T1CCP1	CAN0TX
PB6	1	-	-	SSI2RX	-	M0PWM0	-	-	T0CCP0	-
PB7	4	-	-	SSI2TX	-	M0PWM1	-	-	T0CCP1	-
PC0	52	-	SWCLK	-	-	-	-	-	T4CCP0	-
PC1	51	-	SWDIO	-	-	-	-	-	T4CCP1	-
PC2	50	-	TDI	-	-	-	-	-	T5CCP0	-
PC3	49	-	TDO SWO	-	-	-	-	-	T5CCP1	-
PC4	16	C1-	U4RX	U1RX	-	M0PWM6	-	IDX1	WT0CCP0	U1RTS
PC5	15	C1+	U4TX	U1TX	-	M0PWM7	-	PHA1	WT0CCP1	U1CTS
PC6	14	C0+	U3RX	-	-	-	-	PHB1	WT1CCP0	USB0EPEN
PC7	13	C0-	U3TX	-	-	-	-	-	WT1CCP1	USB0PFLT
PD0	61	AIN7	SSI3CLK	SSI1CLK	I2C3SCL	M0PWM6	M1PWM0	-	WT2CCP0	-
PD1	62	AIN6	SSI3FSS	SSI1FSS	I2C3SDC	M0PWM7	M1PWM1	-	WT2CCP1	-
PD2	63	AIN5	SSI3RX	SSI1RX	-	M0FAULT0	-	-	WT3CCP0	USB0EPEN
PD3	64	AIN4	SSI3TX	SSI1TX	-	-	-	IDX0	WT3CCP1	USB0PFLT
PD4	43	USB0DM	U6RX	-	-	-	-	-	WT4CCP0	-
PD5	44	USB0DP	U6TX	-	-	-	-	-	WT4CCP1	-
PD6	53	-	U2RX	-	-	M0FAULT0	-	PHA0	WT5CCP0	-
PD7	10	-	U2TX	-	-	-	-	PHB0	WT5CCP1	NMI
PE0	9	AIN3	U7RX	-	-	-	-	-	-	-
PE1	8	AIN2	U7TX	-	-	-	-	-	-	-
PE2	7	AIN1	-	-	-	-	-	-	-	-
PE3	6	AIN0	-	-	-	-	-	-	-	-
PE4	59	AIN9	U5RX	-	I2C2SCL	M0PWM4	M1PWM2	-	-	CAN0RX
PE5	60	AIN8	U5TX	-	I2C2SDC	M0PWM5	M1PWM3	-	-	CAN0TX
PF0	28	-	U1RTS	SSI1RX	CAN0RX	-	M1PWM4	PHA0	T0CCP0	NMI
PF1	29	-	U1CTS	SSI1TX	-	-	M1PWM5	PHB0	T0CCP1	-
PF2	30	-	-	SSI1CLK	-	M0FAULT0	M1PWM6	-	T1CCP0	-
PF3	31	-	-	SSI1FSS	CAN0TX	-	M1PWM7	-	T1CCP1	-
PF4	5	-	-	-	-	-	M1FAULT0	IDX0	T2CCP0	USB0EPEN

Bai book tables for Timer CCP Pins

Table 9.7 General Purpose Timers CCP pins distributions

Timers	Up/Down Counter	Even CCP Pins	Odd CCP Pins
16/32-bit Timer 0	**Timer A**	T0CCP0	-
	Timer B	-	T0CCP1
16/32-bit Timer 1	**Timer A**	T1CCP0	-
	Timer B	-	T1CCP1
16/32-bit Timer 2	**Timer A**	T2CCP0	-
	Timer B	**-**	T2CCP1
16/32-bit Timer 3	**Timer A**	T3CCP0	-
	Timer B	**-**	T3CCP1
16/32-bit Timer 4	**Timer A**	T4CCP0	-
	Timer B	-	T4CCP1
16/32-bit Timer 5	**Timer A**	T5CCP0	-
	Timer B	-	T5CCP1
32/64-bit Wide Timer 0	**Timer A**	WT0CCP0	-
	Timer B	-	WT0CCP1
32/64-bit Wide Timer 1	**Timer A**	WT1CCP0	-
	Timer B	-	WT1CCP1
32/64-bit Wide Timer 2	**Timer A**	WT2CCP0	-
	Timer B	**-**	WT2CCP1
32/64-bit Wide Timer 3	**Timer A**	WT3CCP0	-
	Timer B	**-**	WT3CCP1
32/64-bit Wide Timer 4	**Timer A**	WT4CCP0	-
	Timer B	**-**	WT4CCP1
32/64-bit Wide Timer 5	**Timer A**	WT5CCP0	-
	Timer B	**-**	WT5CCP1

Table 9.8 General Purpose Timers signals and GPIO pins distributions (Part I).

GPTM Pin	GPIO Pin	Pin Type	Pin Function
T0CCP0	**PB6 (7)** **PF0 (7)**	I/O	16/32-Bit Timer 0 Capture/Compare/PWM 0.
T0CCP1	**PB7 (7)** **PF1 (7)**	I/O	16/32-Bit Timer 0 Capture/Compare/PWM 1.
T1CCP0	**PB4 (7)** **PF2 (7)**	I/O	16/32-Bit Timer 1 Capture/Compare/PWM 0.
T1CCP1	**PB5 (7)** **PF3 (7)**	I/O	16/32-Bit Timer 1 Capture/Compare/PWM 1.
T2CCP0	**PB0 (7)** **PF4 (7)**	I/O	16/32-Bit Timer 2 Capture/Compare/PWM 0.
T2CCP1	**PB1 (7)**	I/O	16/32-Bit Timer 2 Capture/Compare/PWM 1.
T3CCP0	**PB2 (7)**	I/O	16/32-Bit Timer 3 Capture/Compare/PWM 0.
T3CCP1	**PB3 (7)**	I/O	16/32-Bit Timer 3 Capture/Compare/PWM 1.
T4CCP0	**PC0 (7)**	I/O	16/32-Bit Timer 4 Capture/Compare/PWM 0.
T4CCP1	**PC1 (7)**	I/O	16/32-Bit Timer 4 Capture/Compare/PWM 1.
T5CCP0	**PC2 (7)**	I/O	16/32-Bit Timer 5 Capture/Compare/PWM 0.
T5CCP1	**PC3 (7)**	I/O	16/32-Bit Timer 5 Capture/Compare/PWM 1.

These are the same as Datasheet Table 11-1 and Table 11-2.

Bai book Table 5.10. IRQ Numbers, ISR Names, NVIC Priority Registers

Vector Address	Exception Number	IRQ Number	ISR Name in Startup_TM4C123.s	NVIC Macros for Priority Register	Priority Bits
0x00000038	14	–2	PendSV_Handler	NVIC_SYS_PRI3_R	23–21
0x0000003C	15	–1	SysTick_Handler	NVIC_SYS_PRI3_R	31–29
0x00000040	16	0	GPIOA_Handler	NVIC_PRI0_R	7–5
0x00000044	17	1	GPIOB_Handler	NVIC_PRI0_R	15–13
0x00000048	18	2	GPIOC_Handler	NVIC_PRI0_R	23–21
0x0000004C	19	3	GPIOD_Handler	NVIC_PRI0_R	31–29
0x00000050	20	4	GPIOE_Handler	NVIC_PRI1_R	7–5
0x00000054	21	5	UART0_Handler	NVIC_PRI1_R	15–13
0x00000058	22	6	UART1_Handler	NVIC_PRI1_R	23–21
0x0000005C	23	7	SSI0_Handler	NVIC_PRI1_R	31–29
0x00000060	24	8	I2C0_Handler	NVIC_PRI2_R	7–5
0x00000064	25	9	PWM0_Fault_Handler	NVIC_PRI2_R	15–13
0x00000068	26	10	PWM0_0_Handler	NVIC_PRI2_R	23–21
0x0000006C	27	11	PWM0_1_Handler	NVIC_PRI2_R	31–29
0x00000070	28	12	PWM0_2_Handler	NVIC_PRI3_R	7–5
0x00000074	29	13	QEI0_Handler	NVIC_PRI3_R	15–13
0x00000078	30	14	ADC0SS0_Handler	NVIC_PRI3_R	23–21
0x0000007C	31	15	ADC0SS1_Handler	NVIC_PRI3_R	31–29
0x00000080	32	16	ADC0SS2_Handler	NVIC_PRI4_R	7–5
0x00000084	33	17	ADC0SS3_Handler	NVIC_PRI4_R	15–13
0x00000088	34	18	WDT0_Handler	NVIC_PRI4_R	23–21
0x0000008C	35	19	TIMER0A_Handler	NVIC_PRI4_R	31–29
0x00000090	36	20	TIMER0B_Handler	NVIC_PRI5_R	7–5
0x00000094	37	21	TIMER1A_Handler	NVIC_PRI5_R	15–13
0x00000098	38	22	TIMER1B_Handler	NVIC_PRI5_R	23–21
0x0000009C	39	23	TIMER2A_Handler	NVIC_PRI5_R	31–29
0x000000A0	40	24	TIMER2B_Handler	NVIC_PRI6_R	7–5
0x000000A4	41	25	COMP0_Handler	NVIC_PRI6_R	15–13
0x000000A8	42	26	COMP1_Handler	NVIC_PRI6_R	23–21
0x000000AC	43	27	COMP2_Handler	NVIC_PRI6_R	31–29
0x000000B0	44	28	SYSCTL_Handler	NVIC_PRI7_R	7–5
0x000000B4	45	29	FLASH_Handler	NVIC_PRI7_R	15–13
0x000000B8	46	30	GPIOF_Handler	NVIC_PRI7_R	23–21
0x000000BC	47	31	GPIOG_Handler	NVIC_PRI7_R	31–29
0x000000C0	48	32	GPIOH_Handler	NVIC_PRI8_R	7–5
0x000000C4	49	33	UART2_Handler	NVIC_PRI8_R	15–13

See also Datasheet Table 2-9 for the remaining IRQ Interrupt Numbers.

Bai book tables for NVIC Enable and Priority Registers

See also register descriptions in datasheet.

Note: In Table 5.13, some peripheral names are not shown because columns in the table are intentionally omitted by the textbook author for brevity. However, the bits can be determined using the IRQ number and/or the datasheet descriptions. In Tables 5.12 and 5.13, not all registers are listed (others are in the datasheet).

Table 5.13 Relationship between each bit on interrupt enable register and related peripheral.

Enable Register	32 Enable Bits								
	0	1	2	3	4	5	6 - 29	30	31
NVIC_EN0_R	PORTA	PORTB	PORTC	PORTD	PORTE	UART0	.....	PORTF	PORTG
NVIC_EN1_R	PORTH	UART2	SSI1	Timer3A	Timer3B	I2C1	.....	UART6	UART7
NVIC_EN2_R	...	...	...	...	I2C2	I2C3	.....	WTimer0A	WTimer0B
NVIC_EN3_R	WT1A	WT1B	WT2A	WT2B	WT3A	WT3B	.....	GPIOQ2	GPIOQ3

Table 5.12 Most popular Priority Registers used in the TM4C123GH6PM NVIC.

Priority Register	Priority Bits				Address
	31 – 29	23 - 21	15 - 13	7 - 5	
NVIC_PRI0_R	GPIO Port D	GPIO Port C	GPIO Port B	GPIO Port A	0xE000E400
NVIC_PRI1_R	SSI0, Rx Tx	UART1, Rx Tx	UART0, Rx Tx	GPIO Port E	0xE000E404
NVIC_PRI2_R	PWM Gen 1	PWM Gen 0	PWM Fault	I2C0	0xE000E408
NVIC_PRI3_R	ADC Seq 1	ADC Seq 0	Quad Encode	PWM Gen 2	0xE000E40C
NVIC_PRI4_R	Timer 0A	Watchdog	ADC Seq 3	ADC Seq 2	0xE000E410
NVIC_PRI5_R	Timer 2A	Timer 1B	Timer 1A	Timer 0B	0xE000E414
NVIC_PRI6_R	Comp 2	Comp 1	Comp 0	Timer 2B	0xE000E418
NVIC_PRI7_R	GPIO Port G	GPIO Port F	Flash Control	System Contrl	0xE000E41C
NVIC_PRI8_R	Timer 3A	SSI1, Rx Tx	UART2, Rx Tx	GPIO Port H	0xE000E420
NVIC_PRI9_R	CAN0	Quad Encod 1	I2C1	Timer 3B	0xE000E424
NVIC_PRI10_R	Hibernate	Ethernet	CAN2	CAN1	0xE000E428
NVIC_PRI11_R	uDMA Error	uDMA Soft Tfr	PWM Gen 3	USB0	0xE000E42C
NVIC_SYS_PRI3_R	SysTick	PendSV	--	Debug	0xE000ED20