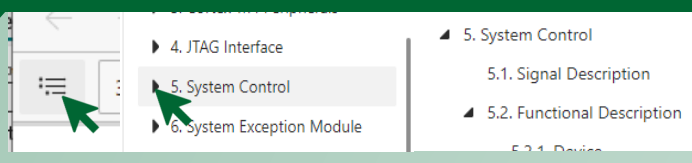
Navigating the TIVA Datasheet

So, you want to use the datasheet better?

Download It

- In-text hyperlinks
- Navigation side-bar

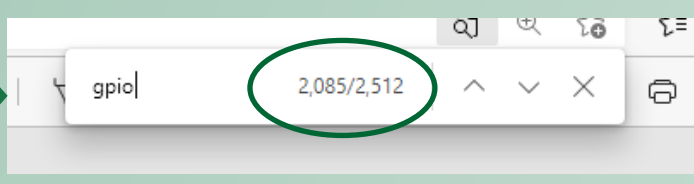


Skim It

Don't read it from cover to cover like a textbook.

CTRL-F Carefully

Too many results. There are more efficient ways to navigate



Know Chapters

⇒ 5 System Control
⇒ 10 GPIO
⇒ 11 Timers
⇒ 13 ADC
⇒ 20 PWM

Locate Tables

⇒ 10-2 GPIO alternate functions
⇒ 11-2 Timers

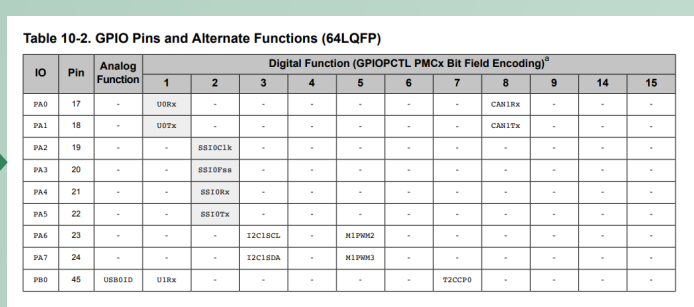


Table 10-2. GPIO Pins and Alternate Functions (64LQFP)

IO	Pin	Analog Function	Digital Function (GPIOPCTL PMCx Bit Field Encoding)[a]										
			1	2	3	4	5	6	7	8	9	14	15
PA0	17	-	U0Rx	-	-	-	-	-	-	CAN1Rx	-	-	-
PA1	18	-	U0Tx	-	-	-	-	-	-	CAN1Tx	-	-	-
PA2	19	-	-	SSI0Clk	-	-	-	-	-	-	-	-	-
PA3	20	-	-	SSI0Fss	-	-	-	-	-	-	-	-	-
PA4	21	-	-	SSI0Rx	-	-	-	-	-	-	-	-	-
PA5	22	-	-	SSI0Tx	-	-	-	-	-	-	-	-	-
PA6	23	-	-	-	I2C1SCL	-	M1PWM2	-	-	-	-	-	-
PA7	24	-	-	-	I2C1SDA	-	M1PWM3	-	-	-	-	-	-
PB0	45	USB0ID	U1Rx	-	-	-	-	-	T2CCP0	-	-	-	-

Register Maps

Looking for a certain register?

- Map before each register description section
- Page numbers hyperlinked
- Find address offsets easily

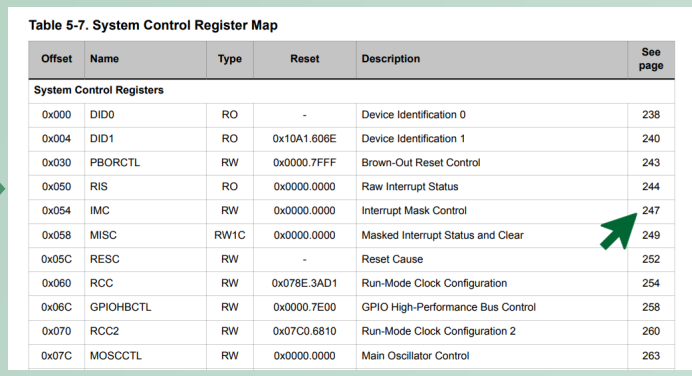


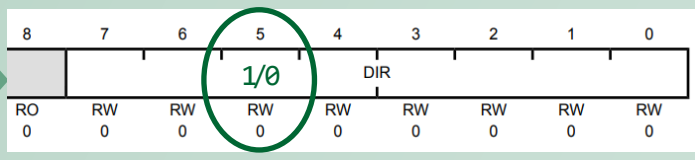
Table 5-7. System Control Register Map

Offset	Name	Type	Reset	Description	See page
System Control Registers					
0x000	DID0	RO	-	Device Identification 0	238
0x004	DID1	RO	0x10A1.606E	Device Identification 1	240
0x030	PBORCTL	RW	0x0000.7FFF	Brown-Out Reset Control	243
0x050	RIS	RO	0x0000.0000	Raw Interrupt Status	244
0x054	IMC	RW	0x0000.0000	Interrupt Mask Control	247
0x058	MISC	RW1C	0x0000.0000	Masked Interrupt Status and Clear	249
0x05C	RESC	RW	-	Reset Cause	252
0x060	RCC	RW	0x078E.3AD1	Run-Mode Clock Configuration	254
0x06C	GPIOHBCTL	RW	0x0000.7E00	GPIO High-Performance Bus Control	258
0x070	RCC2	RW	0x07C0.6810	Run-Mode Clock Configuration 2	260
0x07C	MOSCCTL	RW	0x0000.0000	Main Oscillator Control	263

Register Fields

Setting bit to 1/0 ? ..... ex. PB5 DIR

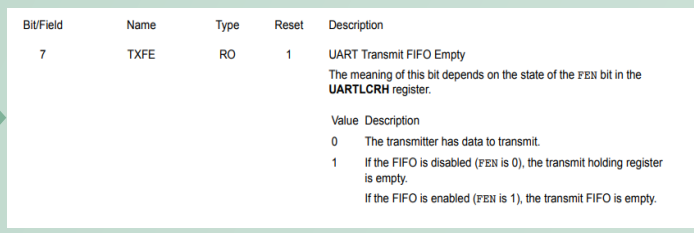
- Find its bit field with the register diagram... ex. 5
- Use it for at-a-glance checking your mask values ..... ex. 0b100000 or 0x20



Register Description

Should you set the bit to 1 or 0?

- Look under the register diagram for the description
- Last column states what happens with a 1 or a 0

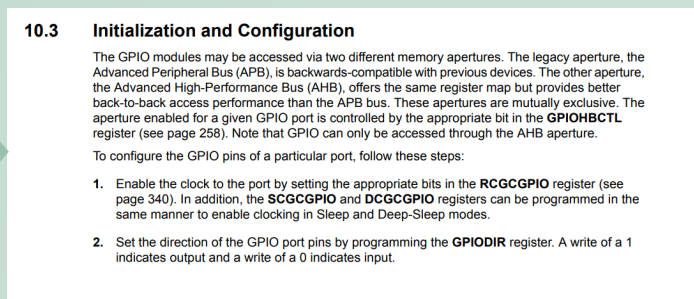


Bit/Field	Name	Type	Reset	Description
7	TXFE	RO	1	UART Transmit FIFO Empty The meaning of this bit depends on the state of the FEN bit in the **UARTLCRH** register. Value Description 0 The transmitter has data to transmit. 1 If the FIFO is disabled (FEN is 0), the transmit holding register is empty. If the FIFO is enabled (FEN is 1), the transmit FIFO is empty.

Initialization Steps

Need to write an init function?

- Instructions at the beginning of each section
- Registers to use, Bits to set, Order to do it in



10.3 Initialization and Configuration

The GPIO modules may be accessed via two different memory apertures. The legacy aperture, the Advanced Peripheral Bus (APB), is backwards-compatible with previous devices. The other aperture, the Advanced High-Performance Bus (AHB), offers the same register map but provides better back-to-back access performance than the APB bus. These apertures are mutually exclusive. The aperture enabled for a given GPIO port is controlled by the appropriate bit in the **GPIOHBCTL** register (see page 258). Note that GPIO can only be accessed through the AHB aperture.

To configure the GPIO pins of a particular port, follow these steps:

1. Enable the clock to the port by setting the appropriate bits in the **RCGCGPIO** register (see page 340). In addition, the **SCGCGPIO** and **DCGCGPIO** registers can be programmed in the same manner to enable clocking in Sleep and Deep-Sleep modes.
2. Set the direction of the GPIO port pins by programming the **GPIODIR** register. A write of a 1 indicates output and a write of a 0 indicates input.