ECEN 454

LAB 7

NAME: Jason Gilman

UIN: 126006979

SECTION: 511

TA: Guaynu Gao

Part A

area

```
****************************************
Report : area
Design : cruisecontrol
Version: O-2018.06-SP3
Date   : Wed Oct 28 19:35:10 2020
****************************************

Library(s) Used:

    iit018_stdcells (File: /home/ugrads/j/jasongilman/ecen454/synthesis/iit018_stdcells.db)

Number of ports:                          58
Number of nets:                          355
Number of cells:                         304
Number of combinational cells:           282
Number of sequential cells:               20
Number of macros/black boxes:              0
Number of buf/inv:                        73
Number of references:                     18

Combinational area:               8543.000000
Buf/Inv area:                     1576.000000
Noncombinational area:            1920.000000
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 10463.000000
Total area:                 undefined
```

Constraints

```
****************************************
Report : constraint
        -all_violators
        -verbose
Design : cruisecontrol
Version: O-2018.06-SP3
Date   : Wed Oct 28 19:34:00 2020
****************************************

This design has no violated constraints.
```

Register count = 20

Netlist

```
////////////////////////////////////////////////////////////
// Created by: Synopsys DC Expert(TM) in wire load mode
// Version   : O-2018.06-SP3
// Date      : Wed Oct 28 19:38:20 2020
////////////////////////////////////////////////////////////


module cruisecontrol_DW01_inc_0 ( A, SUM );
  input [7:0] A;
  output [7:0] SUM;

  wire   [7:2] carry;

  HAX1 U1_1_6 ( .A(A[6]), .B(carry[6]), .YC(carry[7]), .YS(SUM[6]) );
  HAX1 U1_1_5 ( .A(A[5]), .B(carry[5]), .YC(carry[6]), .YS(SUM[5]) );
  HAX1 U1_1_4 ( .A(A[4]), .B(carry[4]), .YC(carry[5]), .YS(SUM[4]) );
  HAX1 U1_1_3 ( .A(A[3]), .B(carry[3]), .YC(carry[4]), .YS(SUM[3]) );
  HAX1 U1_1_2 ( .A(A[2]), .B(carry[2]), .YC(carry[3]), .YS(SUM[2]) );
  HAX1 U1_1_1 ( .A(A[1]), .B(A[0]), .YC(carry[2]), .YS(SUM[1]) );
  INVX1 U1 ( .A(A[0]), .Y(SUM[0]) );
  XOR2X1 U2 ( .A(carry[7]), .B(A[7]), .Y(SUM[7]) );
endmodule


module cruisecontrol_DW01_inc_1 ( A, SUM );
  input [7:0] A;
  output [7:0] SUM;

  wire   [7:2] carry;

  HAX1 U1_1_6 ( .A(A[6]), .B(carry[6]), .YC(carry[7]), .YS(SUM[6]) );
  HAX1 U1_1_5 ( .A(A[5]), .B(carry[5]), .YC(carry[6]), .YS(SUM[5]) );
  HAX1 U1_1_4 ( .A(A[4]), .B(carry[4]), .YC(carry[5]), .YS(SUM[4]) );
  HAX1 U1_1_3 ( .A(A[3]), .B(carry[3]), .YC(carry[4]), .YS(SUM[3]) );
  HAX1 U1_1_2 ( .A(A[2]), .B(carry[2]), .YC(carry[3]), .YS(SUM[2]) );
  HAX1 U1_1_1 ( .A(A[1]), .B(A[0]), .YC(carry[2]), .YS(SUM[1]) );
  INVX2 U1 ( .A(A[0]), .Y(SUM[0]) );
  XOR2X1 U2 ( .A(carry[7]), .B(A[7]), .Y(SUM[7]) );
endmodule
```

```
  HAX1 U1_1_1 ( .A(A[1]), .B(A[0]), .YC(carry[2]), .YS(SUM[1]) );
  INVX2 U1 ( .A(A[0]), .Y(SUM[0]) );
  XOR2X1 U2 ( .A(carry[7]), .B(A[7]), .Y(SUM[7]) );
endmodule


module cruisecontrol ( clk, reset, throttle, set, accel, coast, cancel, resume,
       brake, speed, cruisespeed, cruisectrl );
  output [7:0] speed;
  output [7:0] cruisespeed;
  input clk, reset, throttle, set, accel, coast, cancel, resume, brake;
  output cruisectrl;
  wire   n297, n298, n299, n300, n301, n302, n303, n304, n305, n306, n307,
         n308, n309, n310, n311, n312, N49, N62, N64, N66, N120, N122, N123,
         N124, N125, N126, N127, N138, N139, N140, N141, N142, N143, N144,
         N145, N155, N156, N157, N158, N159, N160, N161, N162, N181, N182, n2,
         n3, n4, n5, n6, n7, n8, n9, n18, n19, n20, n21, n24, n25, n26, n27,
         n29, n30, n31, n32, n35, n36, n37, n38, n39, n41, n42, n44, n45, n46,
         n48, n49, n51, n52, n54, n55, n57, n61, n64, n65, n66, n67, n68, n70,
         n72, n73, n75, n77, n78, n80, n82, n83, n85, n87, n88, n90, n91, n92,
         n93, n94, n95, n97, n100, n102, n104, n105, n107, n108, n111, n112,
         n113, n114, n115, n116, n118, n119, n121, n122, n123, n124, n125,
         n126, n128, n129, n130, n131, n132, n133, n134, n135, n137, n138,
         n139, n140, n141, n142, n143, n144, n145, n146, n147, n148, n149,
         n150, n151, n152, n153, n154, n155, n156, n158, n159, n160, n161,
         n162, n163, n164, n165, n166, n167, n168, n169, n170, n171, n172,
         n173, n174, n175, n176, n177, n178, n179, n182, n187, n189, n191,
         n193, n195, n197, n199, n201, n203, n205, n207, n209, n210, n211,
         n212, n213, n214, n215, n216, n217, n218, n219, n220, n221, n222,
         n223, n224, n225, n226, n227, n228, n229, n230, n231, n232, n233,
         n234, n235, n236, n237, n238, n239, n240, n241, n242, n243, n244,
         n245, n246, n247, n248, n249, n250, n251, n252, n253, n254, n255,
         n256, n257, n258, n259, n260, n261, n262, n263, n264, n265, n266,
         n267, n268, n269, n270, n271, n272, n273, n274, n275, n276, n277,
         n278, n279, n280, n281, n282, n283, n284, n285, n286, n287, n288,
         n289, n290, n291, n292, n293, n294, n295, n296;
  wire   [2:0] state;
  wire   [8:0] \r130/carry ;
```

Part B

Max_paths

```
****************************************
Report : timing
        -path_type full
        -delay_type max
        -slack_lesser_than 5.00
        -max_paths 3
        -sort_by slack
Design : cruisecontrol
Version: O-2018.06-SP3
Date   : Wed Oct 28 20:08:32 2020
****************************************


  Startpoint: cruisespeed_reg[6]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: cruisespeed[6]
              (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                                   Incr       Path
  -----------------------------------------------------------------------------
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  cruisespeed_reg[6]/CLK (DFFPOSX1)                       0.00       0.00 r
  cruisespeed_reg[6]/Q (DFFPOSX1)                         0.18       0.18 r
  U171/Y (INVX1)                                          0.27       0.44 f
  U170/Y (INVX8)                                          0.77       1.21 r
  cruisespeed[6] (out)                                    0.00       1.21 r
  data arrival time                                                  1.21

  clock clk (rise edge)                                  10.00      10.00
  clock network delay (ideal)                             0.00      10.00
  clock reconvergence pessimism                           0.00      10.00
  output external delay                                  -5.00       5.00
  data required time                                                 5.00
  -----------------------------------------------------------------------------
  data required time                                                 5.00
  data arrival time                                                 -1.21
  -----------------------------------------------------------------------------
  slack (MET)                                                        3.79
```

```
  Startpoint: cruisespeed_reg[0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: cruisespeed[0]
              (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                                   Incr       Path
  -----------------------------------------------------------------------------
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  cruisespeed_reg[0]/CLK (DFFPOSX1)                       0.00       0.00 r
  cruisespeed_reg[0]/Q (DFFPOSX1)                         0.14       0.14 r
  U179/Y (INVX1)                                          0.26       0.40 f
  U178/Y (INVX8)                                          0.77       1.17 r
  cruisespeed[0] (out)                                    0.00       1.17 r
  data arrival time                                                  1.17

  clock clk (rise edge)                                  10.00      10.00
  clock network delay (ideal)                             0.00      10.00
  clock reconvergence pessimism                           0.00      10.00
  output external delay                                  -5.00       5.00
  data required time                                                 5.00
  -----------------------------------------------------------------------------
  data required time                                                 5.00
  data arrival time                                                 -1.17
  -----------------------------------------------------------------------------
  slack (MET)                                                        3.83


  Startpoint: cruisespeed_reg[5]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: cruisespeed[5]
              (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                                   Incr       Path
  -----------------------------------------------------------------------------
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
```

```
  output external delay                                -5.00       5.00
  data required time                                               5.00
  ---------------------------------------------------------------------------
  data required time                                               5.00
  data arrival time                                               -1.17
  ---------------------------------------------------------------------------
  slack (MET)                                                      3.83


  Startpoint: cruisespeed_reg[5]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: cruisespeed[5]
              (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                                 Incr       Path
  ---------------------------------------------------------------------------
  clock clk (rise edge)                                 0.00       0.00
  clock network delay (ideal)                           0.00       0.00
  cruisespeed_reg[5]/CLK (DFFPOSX1)                     0.00       0.00 r
  cruisespeed_reg[5]/Q (DFFPOSX1)                       0.14       0.14 r
  U177/Y (INVX1)                                        0.23       0.37 f
  U176/Y (INVX8)                                        0.76       1.12 r
  cruisespeed[5] (out)                                  0.00       1.12 r
  data arrival time                                                1.12

  clock clk (rise edge)                                10.00      10.00
  clock network delay (ideal)                           0.00      10.00
  clock reconvergence pessimism                         0.00      10.00
  output external delay                                -5.00       5.00
  data required time                                               5.00
  ---------------------------------------------------------------------------
  data required time                                               5.00
  data arrival time                                               -1.12
  ---------------------------------------------------------------------------
  slack (MET)                                                      3.88

Warning: report_timing has satisfied the max_paths criteria. There are 31 further e
```

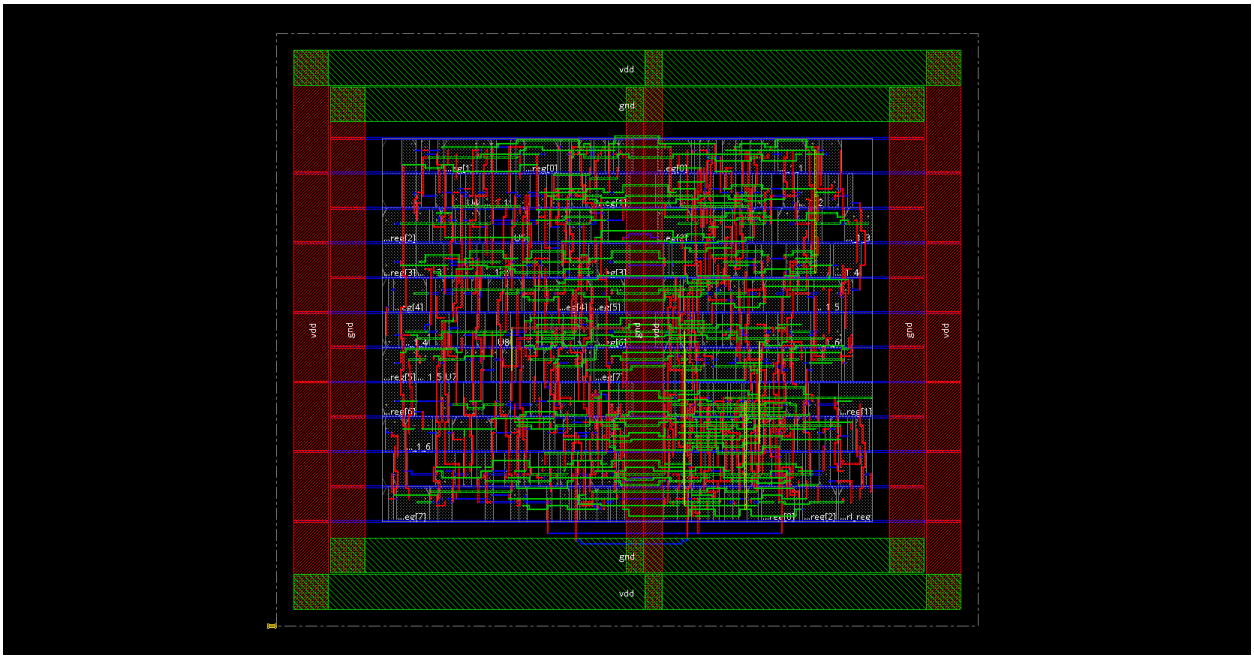
Min_paths

```
****************************************
Report : timing
        -path_type full
        -delay_type min
        -slack_lesser_than 5.00
        -max_paths 3
        -sort_by slack
Design : cruisecontrol
Version: O-2018.06-SP3
Date   : Wed Oct 28 20:07:28 2020
****************************************


  Startpoint: reset (input port clocked by clk)
  Endpoint: state_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                   Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                   0.00       0.00
  clock network delay (ideal)             0.00       0.00
  input external delay                    0.00       0.00 f
  reset (in)                              0.06       0.06 f
  U71/Y (OAI21X1)                         0.08       0.13 r
  state_reg[1]/D (DFFPOSX1)               0.00       0.13 r
  data arrival time                                  0.13

  clock clk (rise edge)                   0.00       0.00
  clock network delay (ideal)             0.00       0.00
  clock reconvergence pessimism           0.00       0.00
  state_reg[1]/CLK (DFFPOSX1)                        0.00 r
  library hold time                       0.00       0.00
  data required time                                 0.00
  -----------------------------------------------------------
  data required time                                 0.00
  data arrival time                                 -0.13
  -----------------------------------------------------------
  slack (MET)                                        0.13
```

```
  Startpoint: brake (input port clocked by clk)
  Endpoint: state_reg[0]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  input external delay                     0.00       0.00 f
  brake (in)                               0.06       0.06 f
  U44/Y (OAI21X1)                          0.08       0.14 r
  state_reg[0]/D (DFFPOSX1)                0.00       0.14 r
  data arrival time                                   0.14

  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  clock reconvergence pessimism            0.00       0.00
  state_reg[0]/CLK (DFFPOSX1)                         0.00 r
  library hold time                        0.00       0.00
  data required time                                  0.00
  -----------------------------------------------------------
  data required time                                  0.00
  data arrival time                                  -0.14
  -----------------------------------------------------------
  slack (MET)                                         0.13


  Startpoint: resume (input port clocked by clk)
  Endpoint: cruisectrl_reg
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  input external delay                     0.00       0.00 r
  resume (in)                              0.05       0.05 r
  U40/Y (AOI22X1)                          0.06       0.11 f
```

```
  library hold time                        0.00       0.00
  data required time                                  0.00
  -----------------------------------------------------------
  data required time                                  0.00
  data arrival time                                  -0.14
  -----------------------------------------------------------
  slack (MET)                                         0.13


  Startpoint: resume (input port clocked by clk)
  Endpoint: cruisectrl_reg
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  input external delay                     0.00       0.00 r
  resume (in)                              0.05       0.05 r
  U40/Y (AOI22X1)                          0.06       0.11 f
  U38/Y (OAI21X1)                          0.07       0.18 r
  cruisectrl_reg/D (DFFPOSX1)              0.00       0.18 r
  data arrival time                                   0.18

  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  clock reconvergence pessimism            0.00       0.00
  cruisectrl_reg/CLK (DFFPOSX1)                       0.00 r
  library hold time                        0.00       0.00
  data required time                                  0.00
  -----------------------------------------------------------
  data required time                                  0.00
  data arrival time                                  -0.18
  -----------------------------------------------------------
  slack (MET)                                         0.18

Warning: report_timing has satisfied the max_paths criteria. There
```

Part C



Total Wire Length = 9328 um

Total Number of Vias = 1436

Standard Cells = 302