ECEN 454

LAB 3

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SECTION: 511

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Cell18.spi

File Edit Format View Help

```
//Spice netlist for an inverter
simulator lang=spectre
subckt IV (input output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 output input VDD VDD tsmc18P w=wp l=lp
        M2 output input VSS VSS tsmc18N w=wn l=ln
ends IV

subckt NAND2 (input_A input_B output VDD VSS)
        parameters wp=.65u lp=.2u wn=.3u ln=.3u

        ;copy configuration from lab 2
        ;parameters defines width and length for below
        ;tsmc18P for PMOS
        ;tsmc18N for NMOS

        M1 output input_A VDD VDD tsmc18P w=wp l=lp
        M2 output input_B VDD VDD tsmc18P w=wp l=lp
        M3 output input_A wire1 VSS tsmc18N w=wn l=ln
        M4 wire1 input_B VSS VSS tsmc18N w=wn l=ln
ends NAND2

subckt XOR2 (input_A input_B output VDD VSS)
        parameters wp=.9u lp=.2u wn=.3u ln=.3u

        ;2 transistors per inverter
        M1 inv_A input_A VDD VDD tsmc18P w=wp l=lp
        M2 inv_A input_A VSS VSS tsmc18N w=wn l=ln
        M3 inv_B input_B VDD VDD tsmc18P w=wp l=lp
        M4 inv_B input_B VSS VSS tsmc18N w=wn l=ln

        ;copy schematic from lab2
        M5 wire1 input_B VDD VDD tsmc18P w=wp l=lp
        M6 output inv_A wire1 VDD tsmc18P w=wp l=lp
        M7 wire2 inv_B VDD VDD tsmc18P w=wp l=lp
        M8 output input_A wire2 VDD tsmc18P w=wp l=lp
        M9 output inv_A wire3 VSS tsmc18N w=wn l=ln
        M10 wire3 inv_B VSS VSS tsmc18N w=wn l=ln
        M11 output input_A wire4 VSS tsmc18N w=wn l=ln
        M12 wire4 input_B VSS VSS tsmc18N w=wn l=ln
ends XOR2
```

Inverter

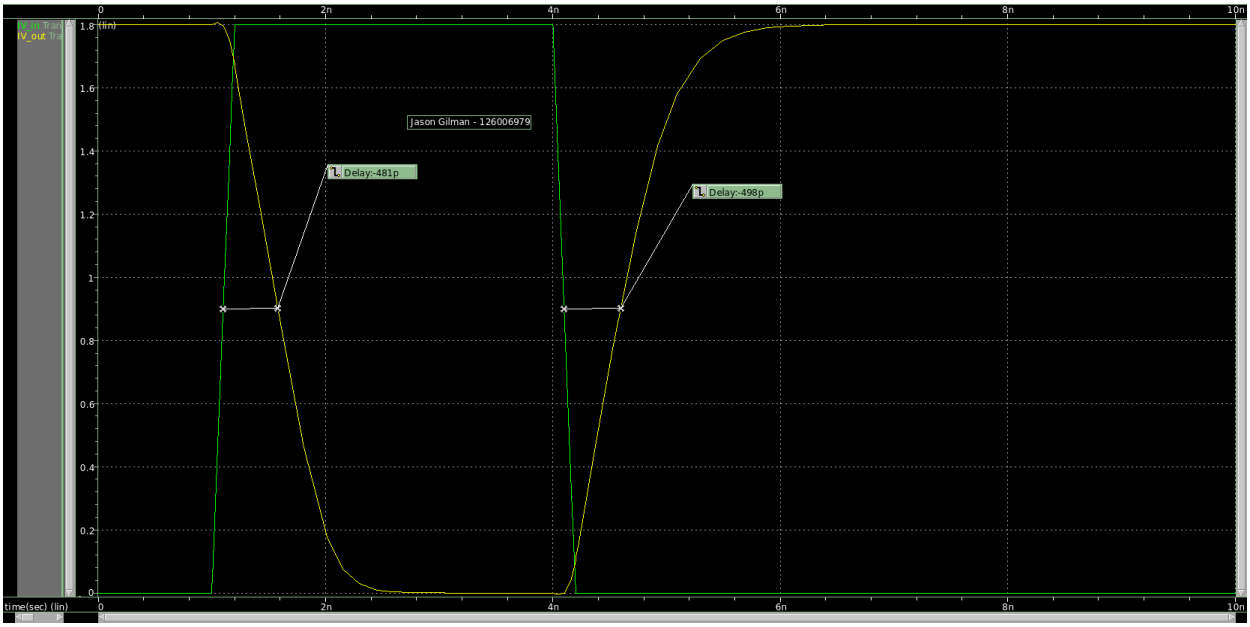
Inverter.spi

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/ecen454/cellcharacs/model18.spi"
include "~/ecen454/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (IV_in IV_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.3u ln=0.2u

R1 (IV_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save IV_in IV_out
```

Inverter_simcap.spi

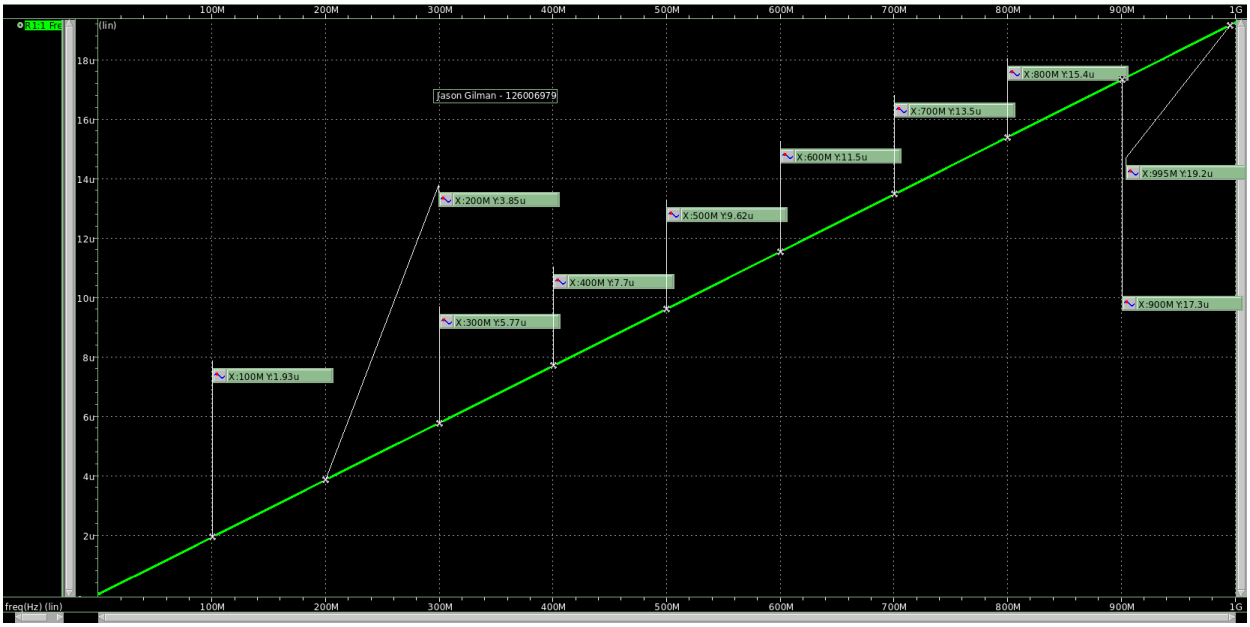
```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/ecen454/cellcharacs/model18.spi"
include "~/ecen454/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

acinput (IV_in 0) vsource dc=0 mag=1

R1 (IV_in IV_in1) resistor r=0

X1 (IV_in1 IV_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.3u ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```

Inverter delay



Capacitance (fF)	Rising Delay (p)	Falling Delay (p)	Error (%)
1	-27.1	-45.2	66.790
5	-57.7	-74.5	29.116
10	-85.5	-101	18.129
15	-109	-122	11.927
20	-131	-144	9.924
25	-153	-166	8.497
30	-175	-188	7.429
35	-197	-210	6.599
40	-219	-232	5.936
45	-240	-255	6.250
50	-262	-277	5.725
60	-306	-321	4.902
70	-351	-368	4.843
80	-393	-410	4.326
90	-439	-451	2.733
100	-481	-498	3.534

Inverter AC



Frequency (MHz)	Current (µA)	Capacitance (nF)
100	1.930	3.072
200	3.850	3.064
300	5.770	3.061
400	7.700	3.064
500	9.620	3.062
600	11.500	3.050
700	13.500	3.069
800	15.400	3.064
900	17.300	3.059
995	19.200	3.071

Sink Capacitance	3.064

NAND2

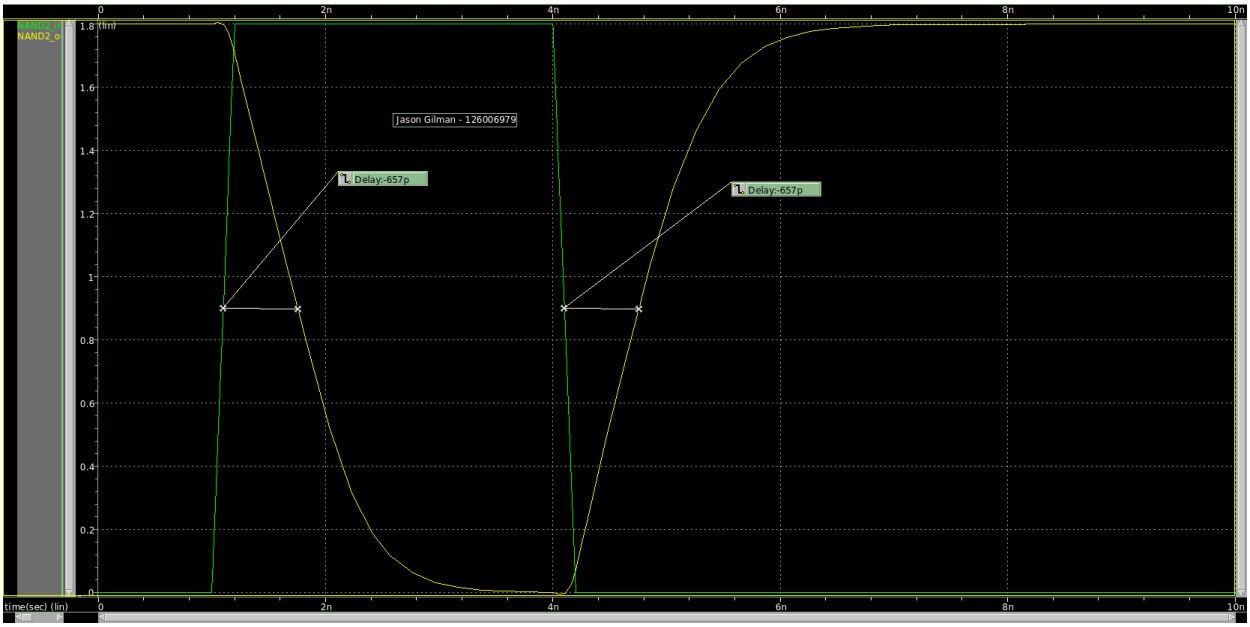
NAND2.spi

```
File  Edit  Format  View  Help
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/ecen454/cellcharacs/model18.spi"
include "~/ecen454/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (NAND2_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (NAND2_in vdd NAND2_out vdd gnd) NAND2 wp=0.65u lp=0.2u wn=0.3u ln=0.2u

R1 (NAND2_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save NAND2_in NAND2_out
```

NAND2_simcap.spi

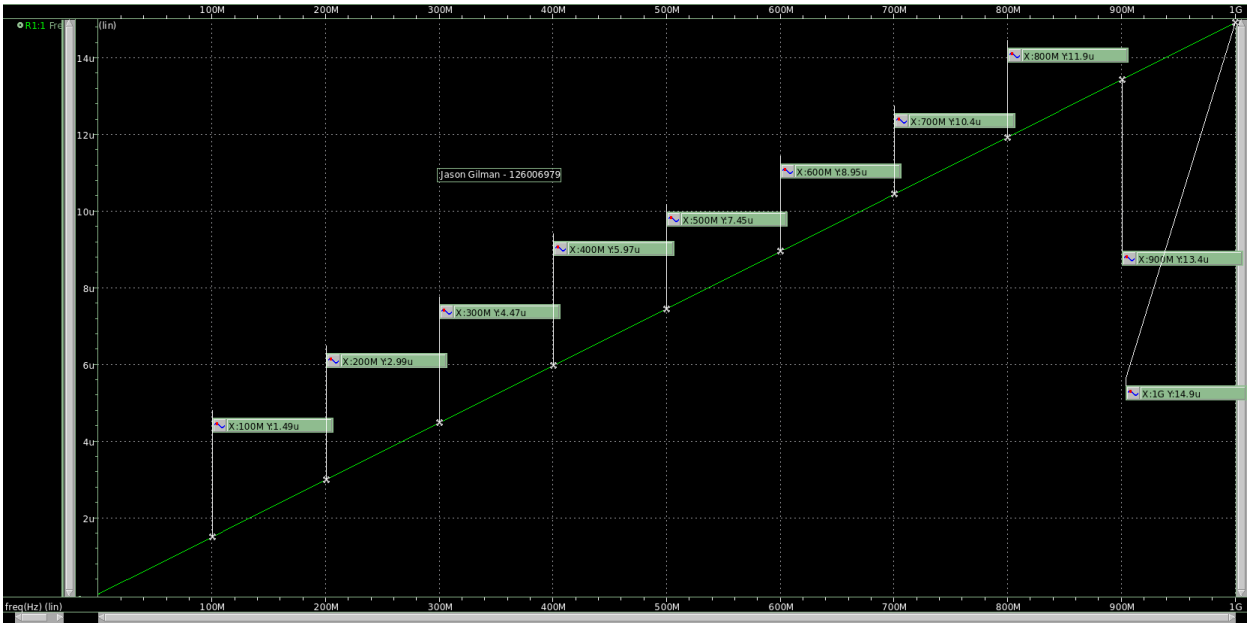
```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/ecen454/cellcharacs/model18.spi"
include "~/ecen454/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

acinput (NAND2_in 0) vsource dc=0 mag=1

R1 (NAND2_in NAND2_in1) resistor r=0

X1 (NAND2_in1 vdd NAND2_out vdd gnd) NAND2 wp=0.65u lp=0.2u wn=0.3u ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```

NAND2 Delay



Capacitance (fF)	Rising Delay (p)	Falling Delay (p)	Error (%)
1	-37.2	-56.2	51.075
5	-73.5	-89.8	22.177
10	-108	-121	12.037
15	-138	-150	8.696
20	-169	-180	6.509
25	-199	-210	5.528
30	-230	-240	4.348
35	-262	-271	3.435
40	-292	-299	2.397
45	-322	-331	2.795
50	-351	-360	2.564
60	-415	-418	0.723
70	-475	-477	0.421
80	-535	-537	0.374
90	-596	-596	0.000
100	-657	-657	0.000

NAND2 AC



Frequency (MHz)	Current (µA)	Capacitance (nF)
100	1.490	2.371
200	2.990	2.379
300	4.470	2.371
400	5.970	2.375
500	7.450	2.371
600	8.950	2.374
700	10.400	2.365
800	11.900	2.367
900	13.400	2.370
995	14.900	2.383

Sink Capacitance	2.373

XOR2

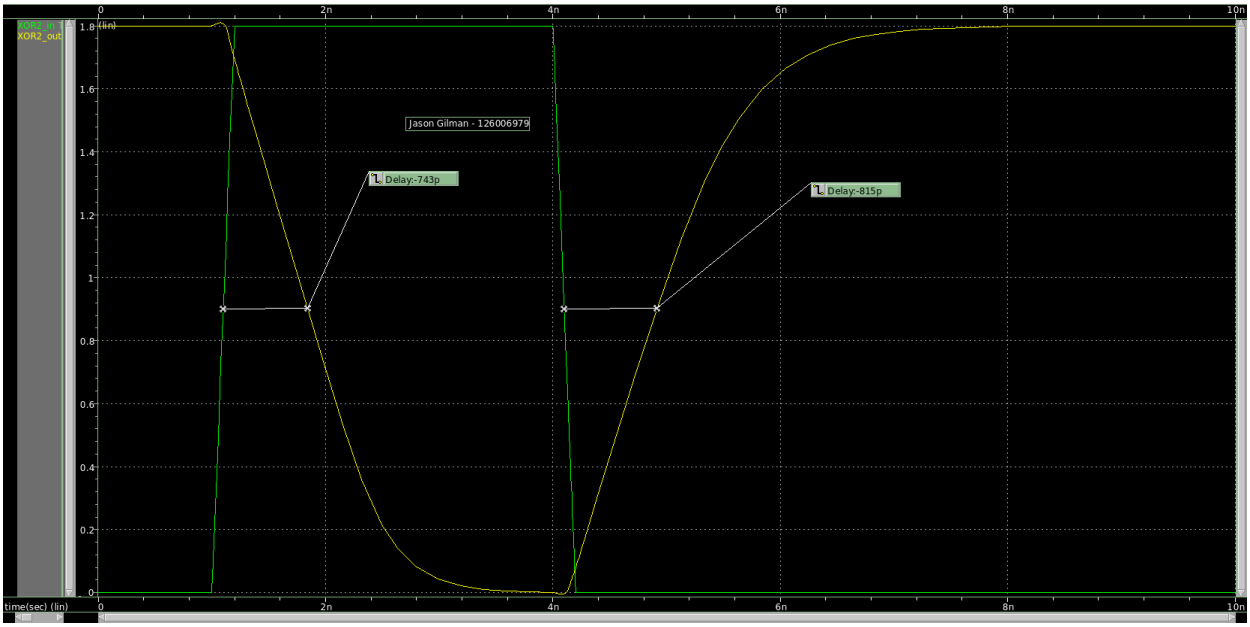
XOR2.spi

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/ecen454/cellcharacs/model18.spi"
include "~/ecen454/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (XOR2_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (XOR2_in vdd XOR2_out vdd gnd) XOR2 wp=1u lp=0.2u wn=0.2u ln=0.2u

R1 (XOR2_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save XOR2_in XOR2_out
```

XOR2_simcap.spi

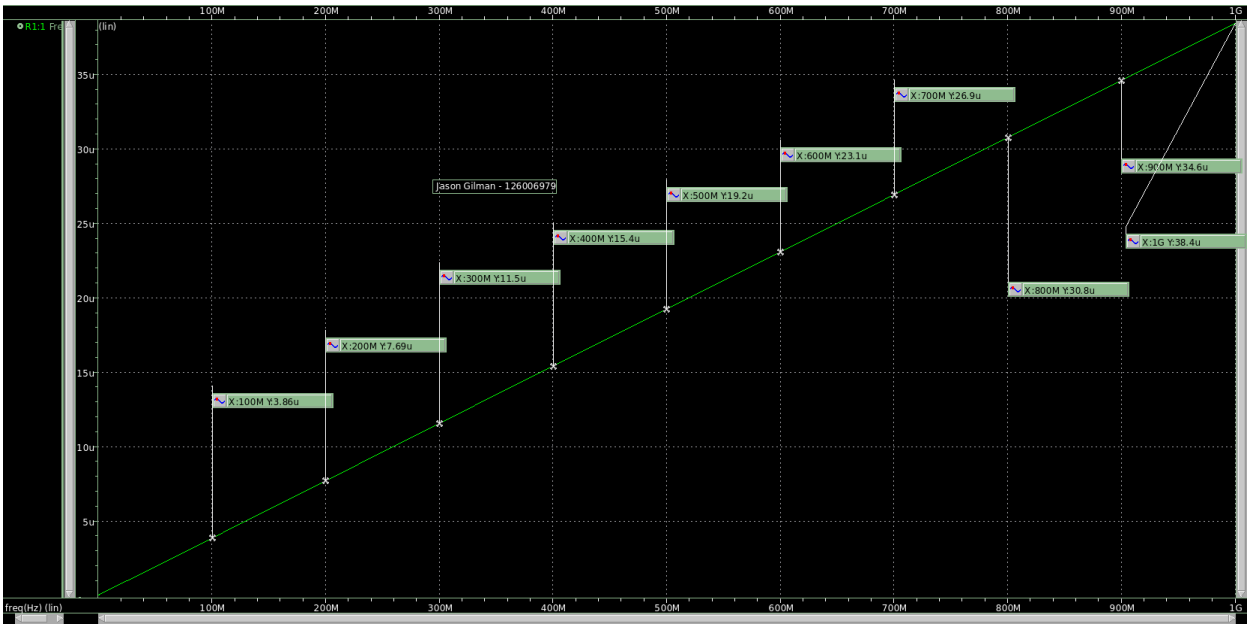
```
File  Edit  Format  View  Help
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/ecen454/cellcharacs/model18.spi"
include "~/ecen454/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

acinput (XOR2_in 0) vsource dc=0 mag=1

R1 (XOR2_in XOR2_in1) resistor r=0

X1 (XOR2_in1 vdd XOR2_out vdd gnd) XOR2 wp=0.9u lp=0.2u wn=0.3u ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```

XOR2 Delay



Capacitance (fF)	Rising Delay (p)	Falling Delay (p)	Error (%)
1	-39.8	-52.2	31.156
5	-72.5	-89.5	23.448
10	-110	-129	17.273
15	-146	-168	15.068
20	-181	-207	14.365
25	-217	-244	12.442
30	-252	-283	12.302
35	-288	-321	11.458
40	-323	-359	11.146
45	-358	-399	11.453
50	-393	-438	11.450
60	-463	-511	10.367
70	-533	-588	10.319
80	-604	-663	9.768
90	-673	-741	10.104
100	-743	-817	9.960

XOR2 AC



Frequency (MHz)	Current (µA)	Capacitance (nF)
100	3.860	6.143
200	7.690	6.120
300	11.500	6.101
400	15.400	6.127
500	19.200	6.112
600	23.100	6.127
700	26.900	6.116
800	30.800	6.127
900	34.600	6.119
995	38.400	6.142

Sink Capacitance	6.123