

ECEN 454

LAB 6

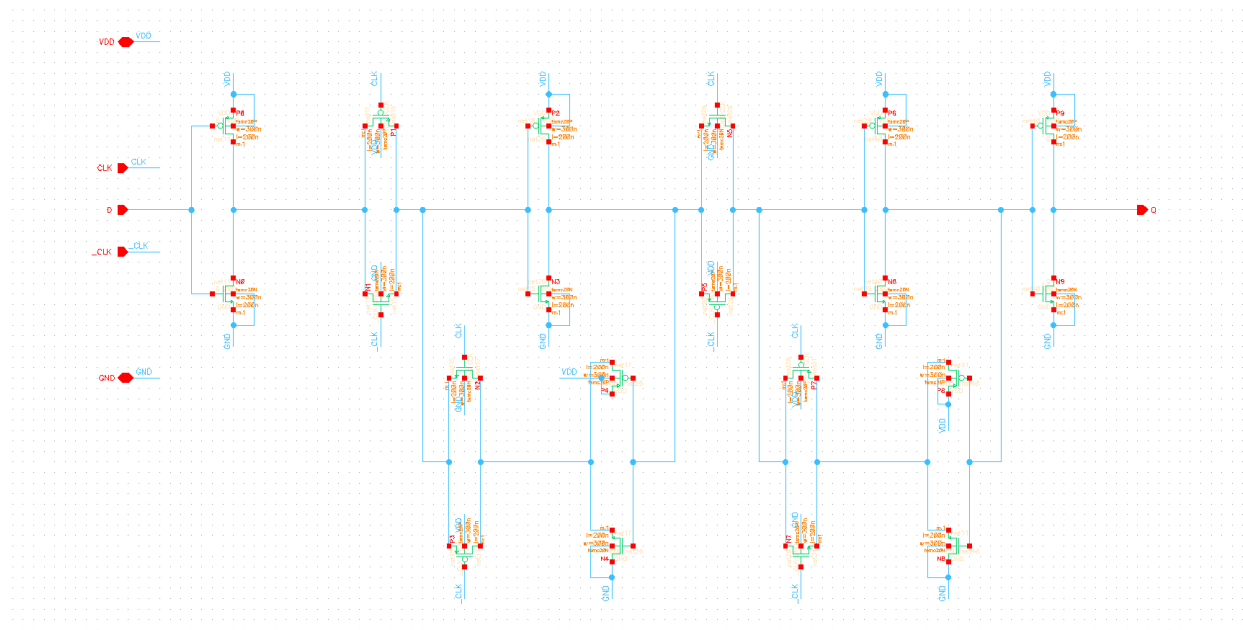
NAME: Jason Gilman

UIN: 126006979

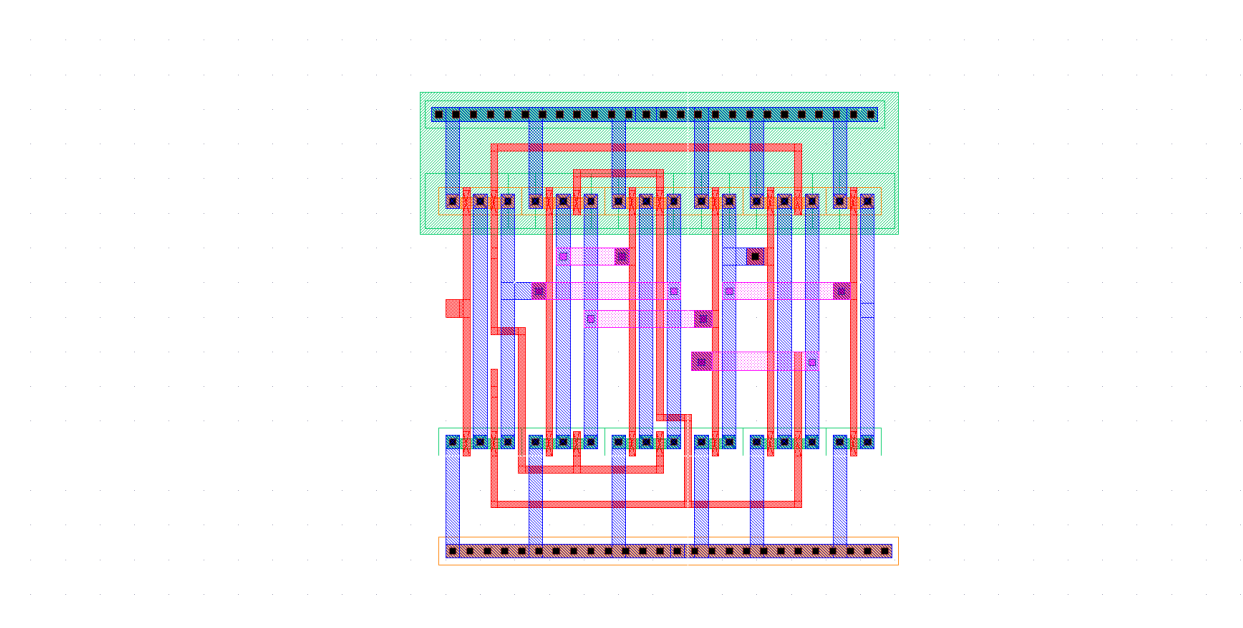
SECTION: 511

TA: Guaynu Gao

Flip-Flop Schematic



Flip-Flop Layout



LVS

```
@(#)CDS: LVS version 6.1.8-64b 08/04/2020 19:19 (cpgsrv11) $

Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/ugrads/j
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

Net-list summary for /home/ugrads/j/jasongilman/ecen454/LVS/layout/netlist
count
13          nets
6           terminals
10          pmos
10          nmos

Net-list summary for /home/ugrads/j/jasongilman/ecen454/LVS/schematic/netlist
count
13          nets
6           terminals
10          pmos
10          nmos

Terminal correspondence points
N10         N6         CLK
N11         N2         D
N7          N1         GND
N8          N3         Q
N12         N8         VDD
N9          N7         _CLK

Devices in the rules but not in the netlist:
cap nfet pfet nmos4 pmos4

The net-lists match.

              layout schematic
              instances
un-matched      0      0
rewired         0      0
size errors     0      0
pruned          0      0
active          20     20
total           20     20
```

N8	N3	Q
N12	N8	VDD
N9	N7	_CLK

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	20	20
total	20	20
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	13	13
total	13	13
	terminals	
un-matched	0	0
matched but		
different type	0	0
total	6	6

Probe files from /home/ugrads/j/jasongilman/ecen454/LVS/schematic

devbad.out:

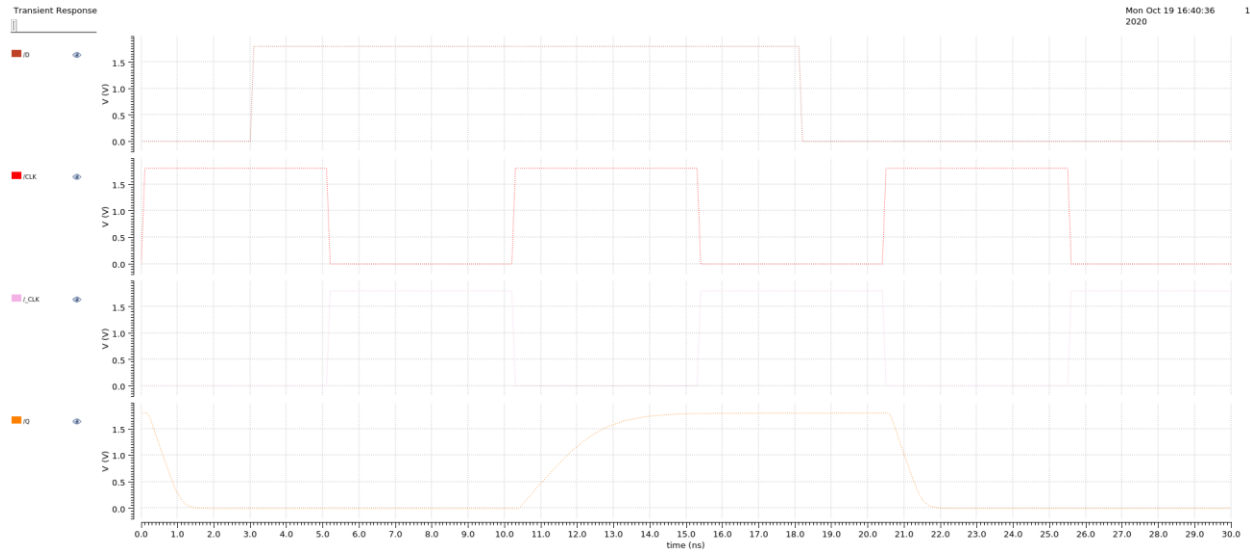
netbad.out:

mergenet.out:

termbad.out:

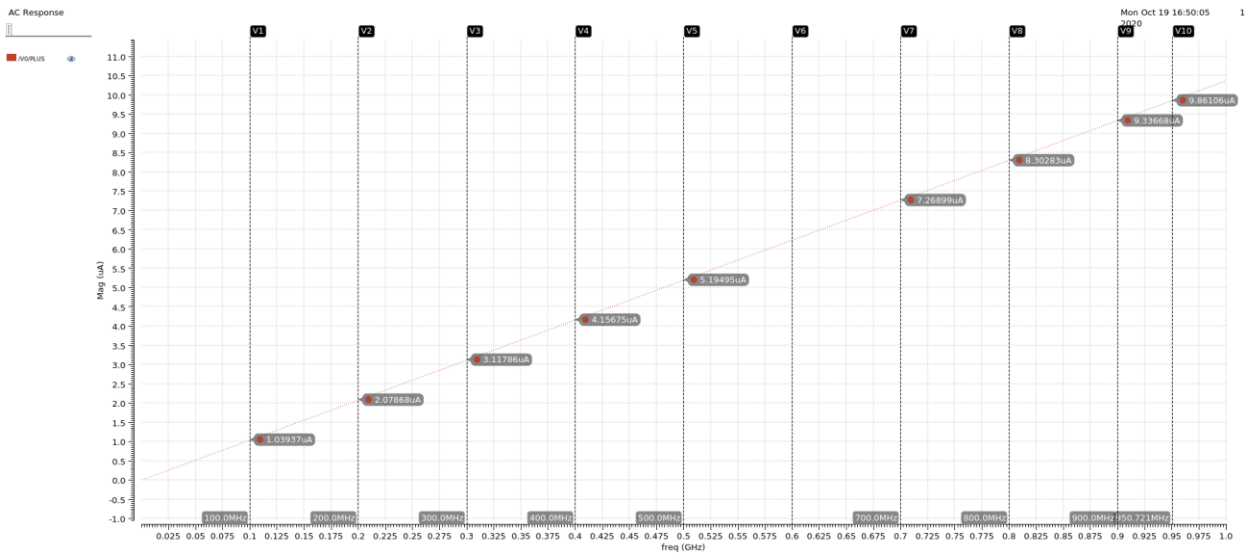
prunenet.out:

Waveform



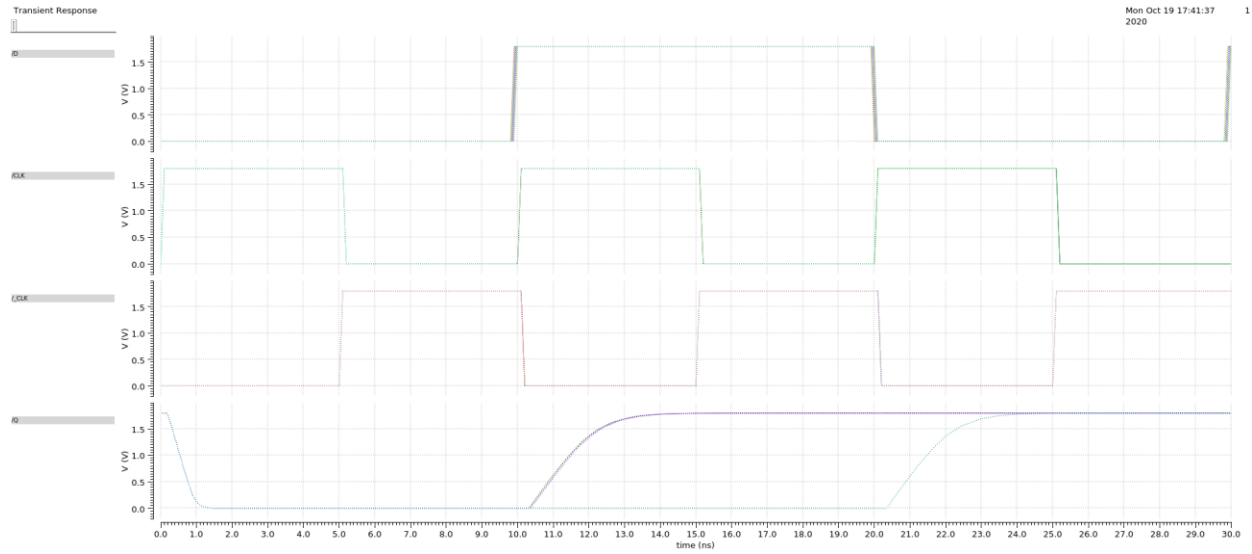
C = 100f F			Delay (ns)	C = 50f F			Delay (ns)
Rising	11.58229	10.25	1.33229	Rising	10.9964	10.25	0.7464
Falling	21.05861	20.45	0.60861	Falling	20.8393	20.45	0.3893
% error			0.543185	% error			0.47843
C = 90f F			Delay (ns)	C = 40f F			Delay (ns)
Rising	11.46	10.25	1.21	Rising	10.8803	10.25	0.6303
Falling	21.0148	20.45	0.5648	Falling	20.7955	20.45	0.3455
% error			0.5332231	% error			0.451848
C = 80f F			Delay (ns)	C = 30f F			Delay (ns)
Rising	11.34	10.25	1.09	Rising	10.7645	10.25	0.5145
Falling	20.97	20.45	0.52	Falling	20.7514	20.45	0.3014
% error			0.5229358	% error			0.414189
C = 70f F			Delay (ns)	C = 20f F			Delay (ns)
Rising	11.231	10.25	0.981	Rising	10.6475	10.25	0.3975
Falling	20.92699	20.45	0.47699	Falling	20.7066	20.45	0.2566
% error			0.5137717	% error			0.354465
C = 60f F			Delay (ns)	C = 10f F			Delay (ns)
Rising	11.11338	10.25	0.86338	Rising	10.53027	10.25	0.28027
Falling	20.88304	20.45	0.43304	Falling	20.65892	20.45	0.20892
% error			0.4984364	% error			0.254576

AC Simulation

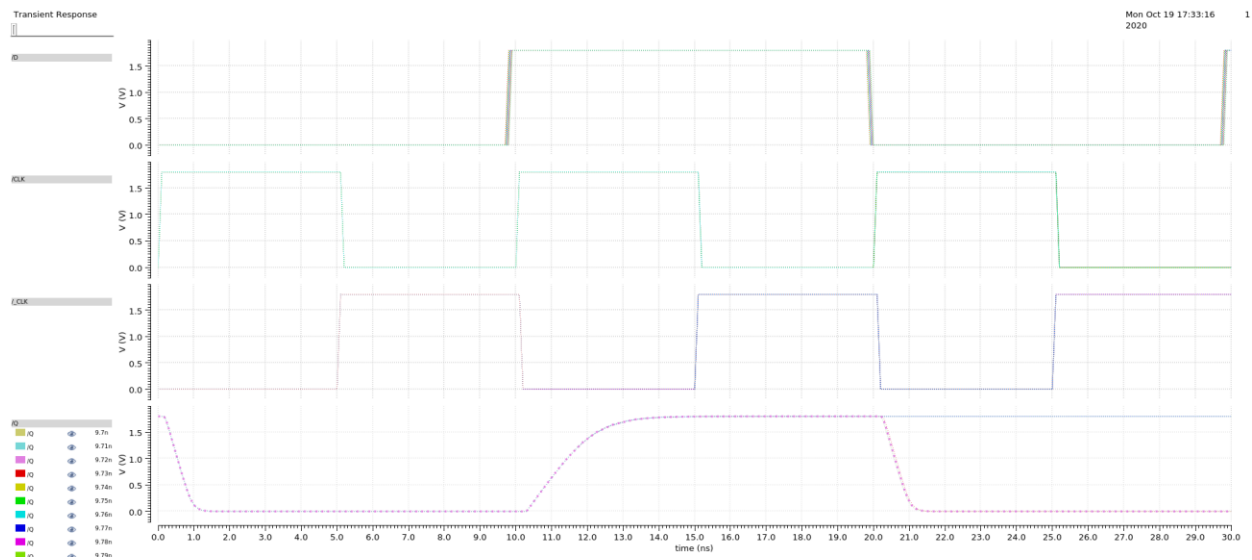


Mag (uA)	Freq (GHz)	Capacitance (fF)
1.03937	0.1	1.654208732
2.07868	0.2	1.654160986
3.11786	0.3	1.654076103
4.15675	0.4	1.653918274
5.19495	0.5	1.653603943
6.23274	0.6	1.653285633
7.26899	0.7	1.652708128
8.3028	0.8	1.651789577
9.33668	0.9	1.651087527
9.86106	1	1.569436443
Mean		1.644827535

Setup Time



Setup_r = .15ns



Setup_f = .28 ns

The Setup time is .28ns since it is the greatest value out of the setup rise and setup fall times.