ECEN 454

LAB 1

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SECTION: 511

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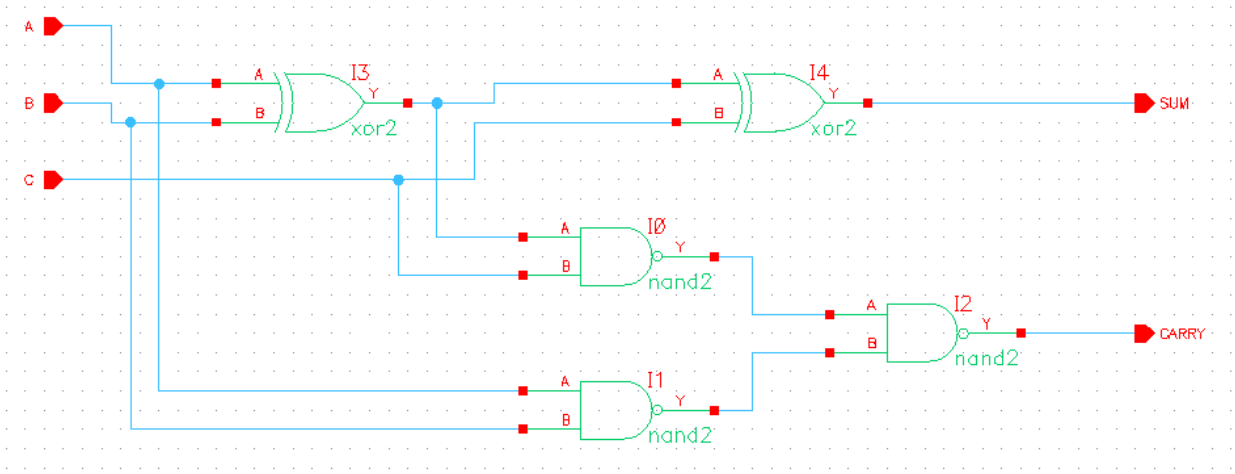
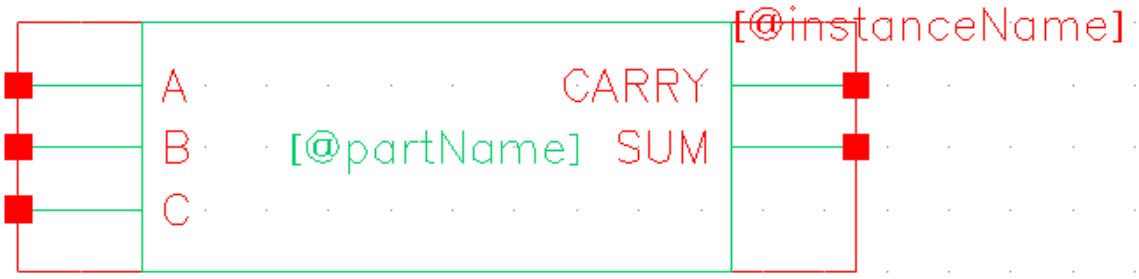
Fulladder:

Schematic - fulladder



Symbol - fulladder



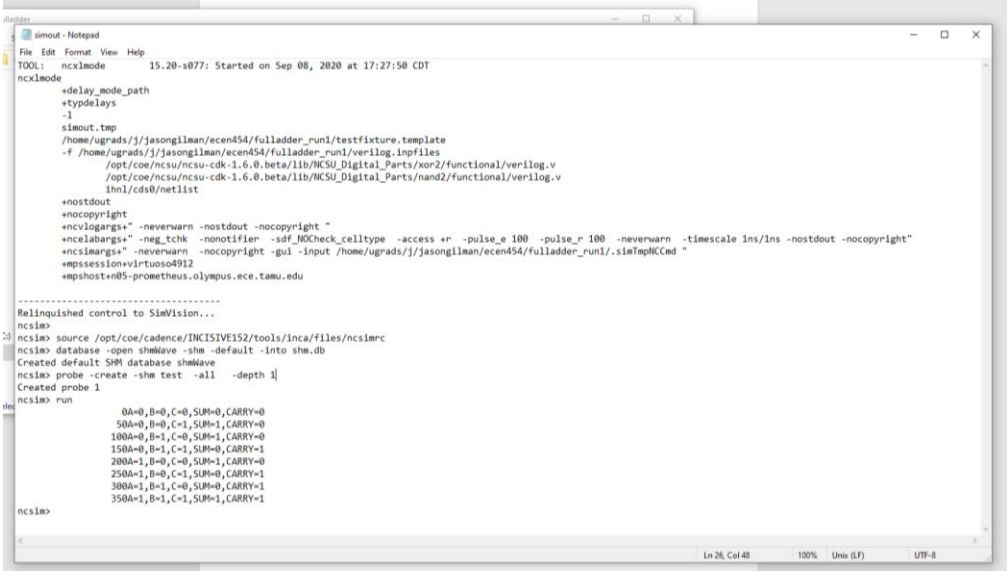
Testbench – fulladder

testfixture - Notepad

File Edit Format View Help

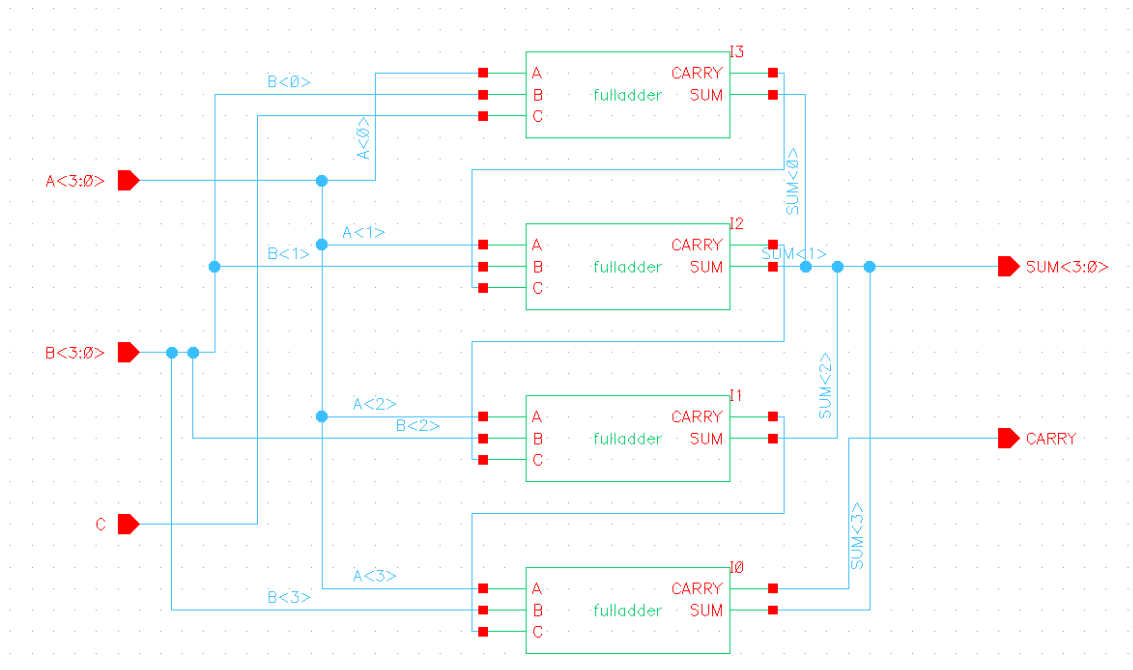
```
// Verilog stimulus file.
// Please do not create a module in this file.


// Default verilog stimulus.

initial
begin

      A = 1'b0; B = 1'b0; C = 1'b0;
   #50 A = 1'b0; B = 1'b0; C = 1'b1;
   #50 A = 1'b0; B = 1'b1; C = 1'b0;
   #50 A = 1'b0; B = 1'b1; C = 1'b1;
   #50 A = 1'b1; B = 1'b0; C = 1'b0;
   #50 A = 1'b1; B = 1'b0; C = 1'b1;
   #50 A = 1'b1; B = 1'b1; C = 1'b0;
   #50 A = 1'b1; B = 1'b1; C = 1'b1;
end

initial
$monitor($time,"A=%b,B=%b,C=%b,SUM=%b,CARRY=%b",A,B,C,SUM,CARRY);
```

Simulation Output - fulladder

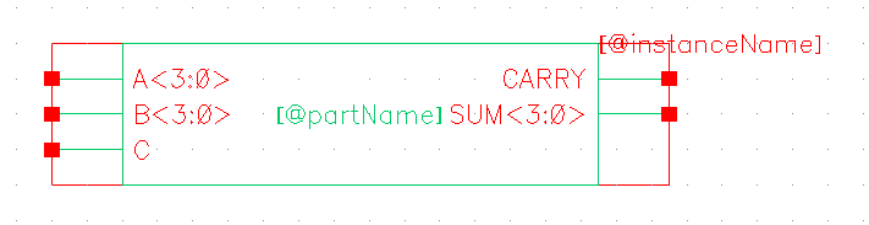


4-Bit-Adder:

Schematic – 4-bit-adder



Symbol – 4-bit-adder



Testbench – 4-bit-adder

File Edit Format View Help

```
// Verilog stimulus file.
// Please do not create a module in this file.


// Default verilog stimulus.

initial
begin

   A[3:0] = 4'b0000; B[3:0] = 4'b0000; C = 1'b0;
   #50 A[3:0] = 4'b1111; B[3:0] = 4'b1111; C = 1'b0;
   #50 A[3:0] = 4'b1010; B[3:0] = 4'b1010; C = 1'b1;
   #50 A[3:0] = 4'b0101; B[3:0] = 4'b0101; C = 1'b1;
end

initial
$monitor($time,"A=%b,B=%b,C=%b,SUM=%b,CARRY=%b",A,B,C,SUM,CARRY);
```

Simulation Output – 4-bit-adder

File Edit Format View Help

```
TOOL:   ncxlmode        15.20-s077: Started on Sep 08, 2020 at 19:35:01 CDT
ncxlmode
        +delay_mode_path
        +typdelays
        -l
        simout.tmp
        /home/ugrads/j/jasongilman/ecen454/4-bit-adder_run1/testfixture.template
        -f /home/ugrads/j/jasongilman/ecen454/4-bit-adder_run1/verilog.inpfiles
                /opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/xor2/functional/verilog.v
                /opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/nand2/functional/verilog.v
                ihnl/cds0/netlist
                ihnl/cds1/netlist
        +nostdout
        +nocopyright
        +ncvlogargs+" -neverwarn -nostdout -nocopyright "
        +ncelabargs+" -neg_tchk  -nonotifier  -sdf_NOCheck_celltype  -access +r  -pulse_e 100  -pulse_r 100  -neverwarn  -timescale 1ns/1ns -nostdout -nocopyright"
        +ncsimargs+" -neverwarn  -nocopyright -gui -input /home/ugrads/j/jasongilman/ecen454/4-bit-adder_run1/.simTmpNCCmd "
        +mpssession+virtuoso39880
        +mpshost+n05-prometheus.olympus.ece.tamu.edu

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Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test  -all   -depth 1
Created probe 1
ncsim> run
                  0A=0000,B=0000,C=0,SUM=0000,CARRY=0
                 50A=1111,B=1111,C=0,SUM=1110,CARRY=1
                100A=1010,B=1010,C=1,SUM=0101,CARRY=1
                150A=0101,B=0101,C=1,SUM=1011,CARRY=0
ncsim>
```
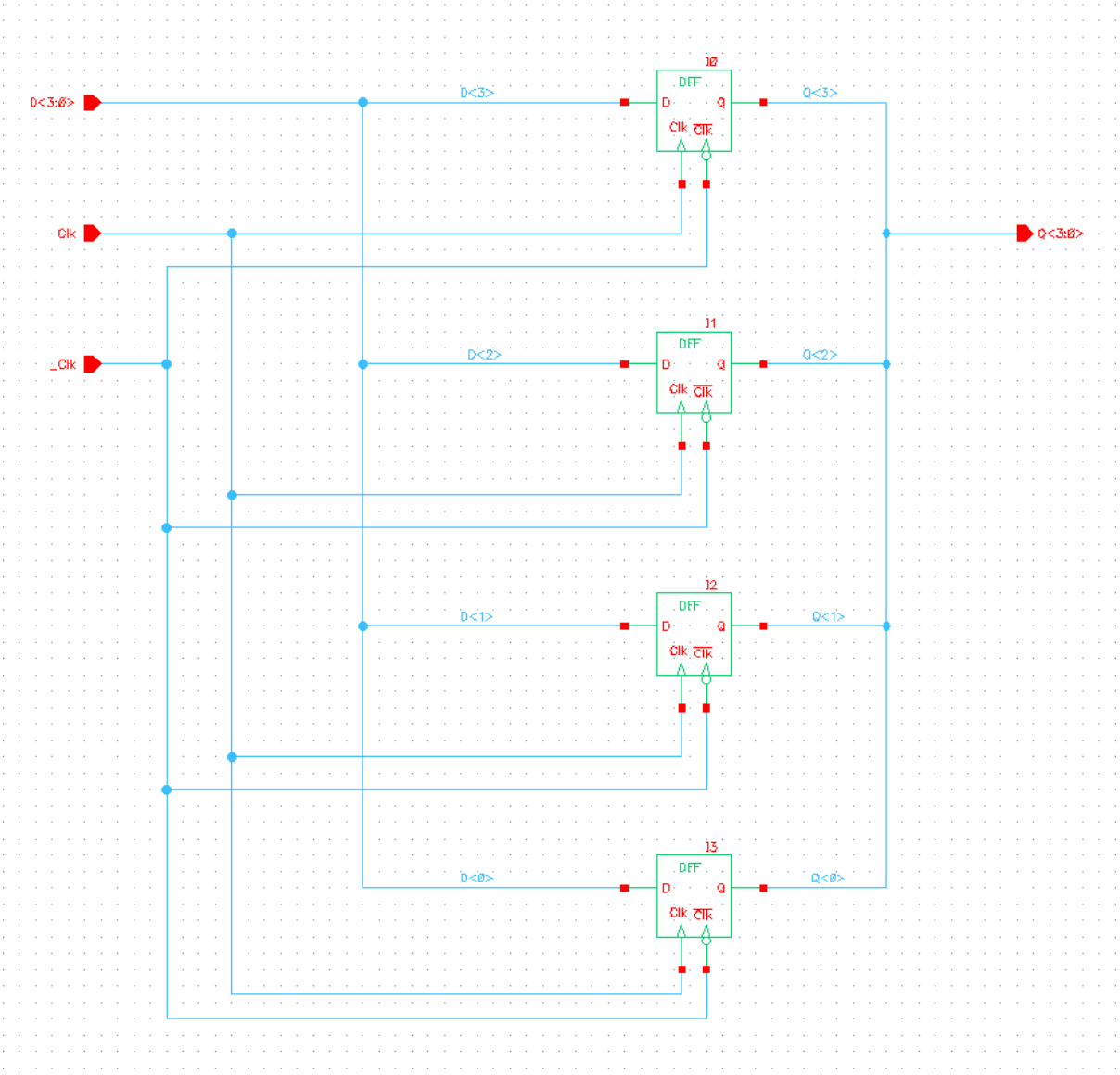
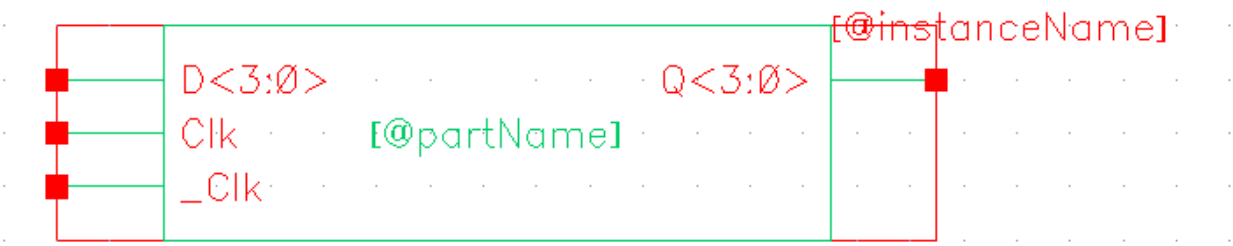

4-Bit-Register:

Schematic – 4-bit-register

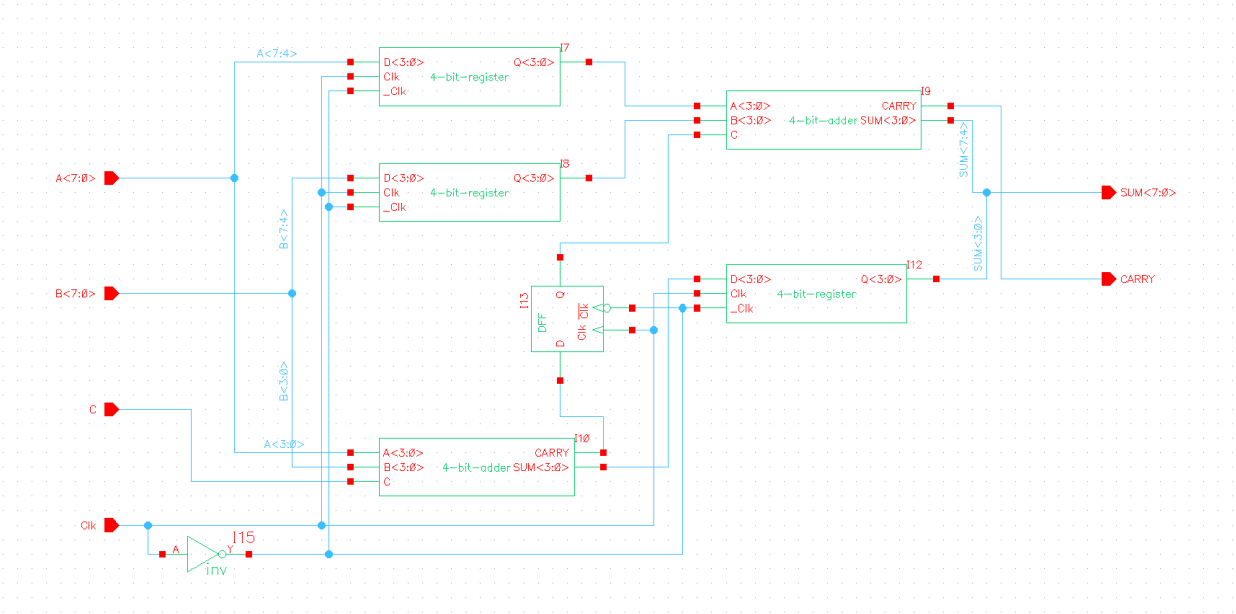


Symbol – 4-bit-register

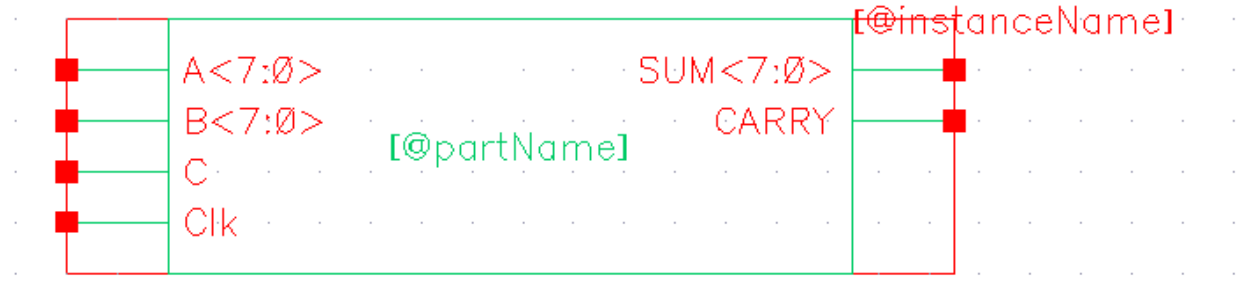


8-Bit-Adder:

Schematic – 8-bit-adder



Symbol – 8-bit-adder



Testbench – 8-bit-adder

testfixture - Notepad

File Edit Format View Help

```
// Verilog stimulus file.
// Please do not create a module in this file.


// Default verilog stimulus.

initial
$monitor($time," A=%b, B=%b, C=%b, Clk=%b, SUM=%b, CARRY=%b", A, B, C, Clk, SUM, CARRY);

always@(Clk)
   #25 Clk<=~Clk;

initial
begin

   A[7:0] = 8'b00000000; B[7:0] = 8'b00000000; C = 1'b0; Clk = 1'b0;

   #50 A[7:0] = 8'b01111110; B[7:0] = 8'b11100111; C = 1'b0;
   $monitor($time," A=%b, B=%b, C=%b, Clk=%b, SUM=%b, CARRY=%b", A, B, C, Clk, SUM, CARRY);

   #50 A[7:0] = 8'b11111111; B[7:0] = 8'b00000000; C = 1'b1;
   $monitor($time," A=%b, B=%b, C=%b, Clk=%b, SUM=%b, CARRY=%b", A, B, C, Clk, SUM, CARRY);

   #50 A[7:0] = 8'b10101010; B[7:0] = 8'b01010101; C = 1'b0;
   $monitor($time," A=%b, B=%b, C=%b, Clk=%b, SUM=%b, CARRY=%b", A, B, C, Clk, SUM, CARRY);

   #50 A[7:0] = 8'b10101010; B[7:0] = 8'b01010101; C = 1'b1;
   $monitor($time," A=%b, B=%b, C=%b, Clk=%b, SUM=%b, CARRY=%b", A, B, C, Clk, SUM, CARRY);

   #50 A[7:0] = 8'b11001100; B[7:0] = 8'b00110011; C = 1'b0;
   $monitor($time," A=%b, B=%b, C=%b, Clk=%b, SUM=%b, CARRY=%b", A, B, C, Clk, SUM, CARRY);

   #50 A[7:0] = 8'b11001100; B[7:0] = 8'b00110011; C = 1'b1;
   $monitor($time," A=%b, B=%b, C=%b, Clk=%b, SUM=%b, CARRY=%b", A, B, C, Clk, SUM, CARRY);

   #50
   $monitor($time," A=%b, B=%b, C=%b, Clk=%b, SUM=%b, CARRY=%b", A, B, C, Clk, SUM, CARRY);

   $finish;
end
```

Simulation Output – 8-bit-adder

File Edit Format View Help

```
                /opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/Dlatch/behavioral/verilog.v
                ihnl/cds0/netlist
                ihnl/cds1/netlist
                ihnl/cds2/netlist
                ihnl/cds3/netlist
                ihnl/cds4/netlist
        +nostdout
        +nocopyright
        +ncvlogargs+" -neverwarn -nostdout -nocopyright "
        +ncelabargs+" -neg_tchk  -nonotifier  -sdf_NOCheck_celltype  -access +r  -pulse_e 100  -pulse_r 100  -neverwarn  -timescale 1ns/1ns -nostdout -nocopyright"
        +ncsimargs+" -neverwarn  -nocopyright -gui -input /home/ugrads/j/jasongilman/ecen454/8-bit-adder_run1/.simTmpNCCmd "
        +mpssession+virtuoso39880
        +mpshost+n05-prometheus.olympus.ece.tamu.edu

---------------------------------------
Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test  -all   -depth 1
Created probe 1
ncsim> run
                  0 A=00000000, B=00000000, C=0, Clk=0, SUM=xxxxxxxx, CARRY=x
                 25 A=00000000, B=00000000, C=0, Clk=1, SUM=00000000, CARRY=0
                 50 A=01111110, B=11100111, C=0, Clk=0, SUM=00000000, CARRY=0
                 75 A=01111110, B=11100111, C=0, Clk=1, SUM=01100101, CARRY=1
                100 A=11111111, B=00000000, C=1, Clk=0, SUM=01100101, CARRY=1
                125 A=11111111, B=00000000, C=1, Clk=1, SUM=00000000, CARRY=1
                150 A=10101010, B=01010101, C=0, Clk=0, SUM=00000000, CARRY=1
                175 A=10101010, B=01010101, C=0, Clk=1, SUM=11111111, CARRY=0
                200 A=10101010, B=01010101, C=1, Clk=0, SUM=11111111, CARRY=0
                225 A=10101010, B=01010101, C=1, Clk=1, SUM=00000000, CARRY=1
                250 A=11001100, B=00110011, C=0, Clk=0, SUM=00000000, CARRY=1
                275 A=11001100, B=00110011, C=0, Clk=1, SUM=11111111, CARRY=0
                300 A=11001100, B=00110011, C=1, Clk=0, SUM=11111111, CARRY=0
                325 A=11001100, B=00110011, C=1, Clk=1, SUM=00000000, CARRY=1
Simulation complete via $finish(1) at time 350 NS + 0
./testfixture.verilog:40    $finish;
ncsim> ^C
ncsim> exit
TOOL:   ncxlmode        15.20-s077: Exiting on Sep 08, 2020 at 22:51:56 CDT  (total: 00:08:33)
```