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HW #3 - ECEN 449 - 508

1)a)

From the circuit diagram I get the following truth table:

|  |  |  |  |
| --- | --- | --- | --- |
| In1 | In2 | In3 | Out |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

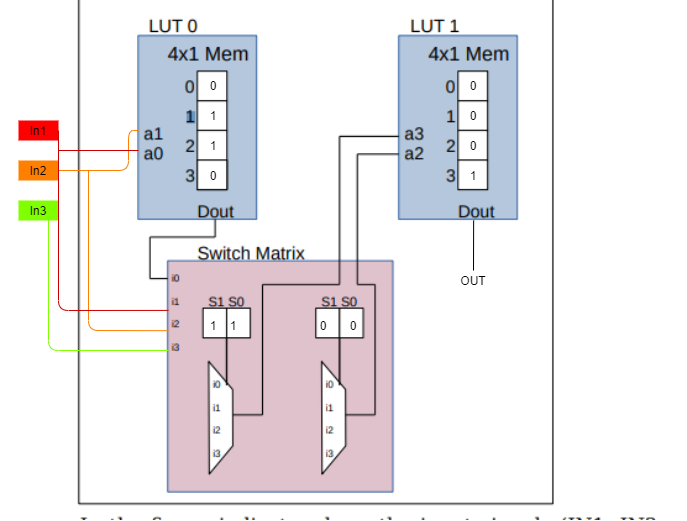
I want LUT0 to output (In1 XNOR (In2)’). This makes In1 = a0 = i1 and In2 = a1 = i2. Dout0 is found:

|  |  |  |
| --- | --- | --- |
| a0 | a1 | Dout0 = (a0 XNOR a1’) |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

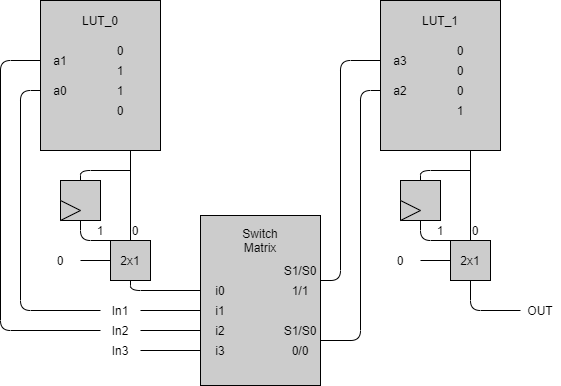
Since Dout0 = i0, I want LUT1 to find the expression of (i0 ^ In3), which makes In3 = a3 = i3 and i0 = a2. So I will need one switch to choose i0 and the other to choose i3 to make (i0 ^ i3). The following truth table shows the output of LUT1:

|  |  |  |
| --- | --- | --- |
| i0 = Dout0 = a2 | I3 = a3 | Dout1 = a2 ^ a3 |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Dout1 is equal to out from the circuit. All of the connections can be shown in the following figure:



1)b)



As shown in the diagram above, the mux’s are selected so that the flip-flop is not selected. This shows that the circuit has no sequential logic. The bitstream is as follows:

0110 0 11 00 0001 0

2)a)

To achieve the worst case delay through the inverter circuit, Tf must be engaged. This means that the initial value of IN2 in the worst case will be 1. The inverter will cause the signal to fall which will incur a delay of 2ps.

Next, the worst case delay through the XNOR circuit is achieved by triggering Tr. This means that we want the circuit to evaluate to 1. We know that the signal coming out of the inverter is 0, so to cause the XNOR to rise, IN1 must be equal to 0 in the worst case delay. The total worst case delay of the circuit coming out of the XNOR will be 7ps.

Regardless of whether the signal rises or falls, the delay of the AND gate is the same. This means that IN3 can either be 0 or 1, with the total worst case delay of the circuit being **10ps**.

2)b)

T\_min = 3ps + 2ps

F\_max = 1/T\_min = **2E11 Hz**