Energy Project
Group Report

Practical Engineering Design Solutions and Project Development (EEEE2046 UNUK)

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Faculty of Engineering

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1. Introduction

A dual switch forward converter was designed using PLECS to satisfy the requirements for rectification in a Switch Mode Power Supply (SMPS). The converter could rectify and step-down an AC input voltage supply and provide a DC output. Transformer ratio ($\frac{N_1}{N_2}$), the duty cycle (d), output voltage and current were considered in the design. Data sheets was checked to build non-ideal conditions. To obtain the more precise result, the max step size of simulation parameters is set to be 1e-7 because it should be the reciprocal of the switching frequency then divided by 100.

Values chosen and calculated for Ideal Converter:

Switching Frequency	100kHz
Duty Cycle	40%
Turns ratio of forward converter transformer (N_1/N_2)	1.75
Output Filter Inductor	25.6μH
Output Filter Capacitor	234.375μF
Output voltage ripple (peak to peak)	0.01

2. Calculations for Forward Converter

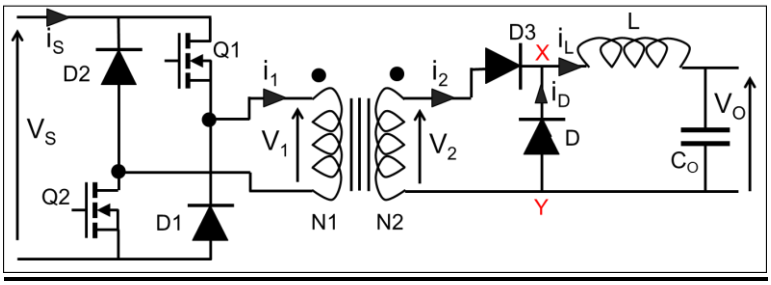

Figure 1 – Basic circuit of forward converter

The calculation was based on the circuit in Figure 1. The proper switching frequency was determined to be 100 kHz, because the MOSFET switch on and off would cause energy losses.

The duty cycle should not exceed 0.5 to prevent MOSFET damage. Moreover, the duty cycle should be lower than 0.45, because the duty cycle should not exceed the maximum duty cycle limit of real PWM output of 45%. Therefore, duty cycle was determined to be 0.4.

2.1 Turn Ratio: $\frac{N_1}{N_2} = 1.75$

The turns ratio of the transformer in the converter were determined by the output voltage (V_o), the input voltage (V_s) and duty cycle (d).

$$V_o = \frac{N_2}{N_1} d V_s \qquad \textit{Eqn.1}$$

$$\frac{N_2}{N_1} = \frac{8}{0.4 \times 35} = \frac{4}{7}$$

$$\frac{N_1}{N_2} = \frac{7}{4} = 1.75$$

2.2 Primary and secondary voltage: $V_1 = 35\ V, V_2 = 20\ V$

Secondary voltage was calculated as follows:

$$V_2 = \frac{N_2}{N_1} V_1 = \frac{4}{7} \times 35 = 20\ V \qquad \textit{Eqn.2}$$

2.3 Output Filter Inductor: L=25.6 μH, i_L=1.875 A

The load resistance at discontinuous output current threshold was 15% of P_{max}, so the minimum output current was:

$$I_{o(min)} = \frac{50 \times 0.15}{8} = 0.9375\ A \qquad \textit{Eqn.3}$$

The maximum output current was:

$$I_{o(max)} = \frac{50}{8} = 6.25\ A$$

Therefore, the output filter inductor could be calculated:

$$L = \frac{VTA}{\Delta i_L} \qquad \textit{Eqn.4}$$

$$T = T_{sw} = \frac{1}{f_{sw}} = \frac{1}{100000} = 10\ \mu s \qquad \textit{Eqn.5}$$

$$L = \frac{8 \times 10 \times 10^{-6} \times 0.4}{0.9375 \times 2} = 25.6\ \mu H$$

Therefore, the inductor current was:

$$i_L = \Delta i_L \times 2 = 0.9375 \times 2 = 1.875\ A \qquad \textit{Eqn.6}$$

2.4 Output filter capacitor: C=23.4μF

$$\Delta V_o = \frac{ITA}{C_o} \qquad \textit{Eqn.7}$$

$$C_o = \frac{ITA}{\Delta V_o} = \frac{0.9375 \times 0.5 \times 5 \times 10^{-6}}{0.01} = 234.375\ \mu F \qquad \textit{Eqn.8}$$

2.5 Load Resistance: $R_{Load} = 8.53\ \Omega,\ R_{Load} = 1.28\ \Omega$

When the load current was 0.9375 A:

$$R_{Load} = \frac{8}{0.9375} = 8.53\ \Omega \qquad \textit{Eqn.9}$$

When the load current was 6.25 A, R_{Load} also could be calculated by Eqn.9

$$R_{Load} = \frac{8}{6.25} = 1.28\ \Omega$$

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3. Simulation results under Ideal Conditions

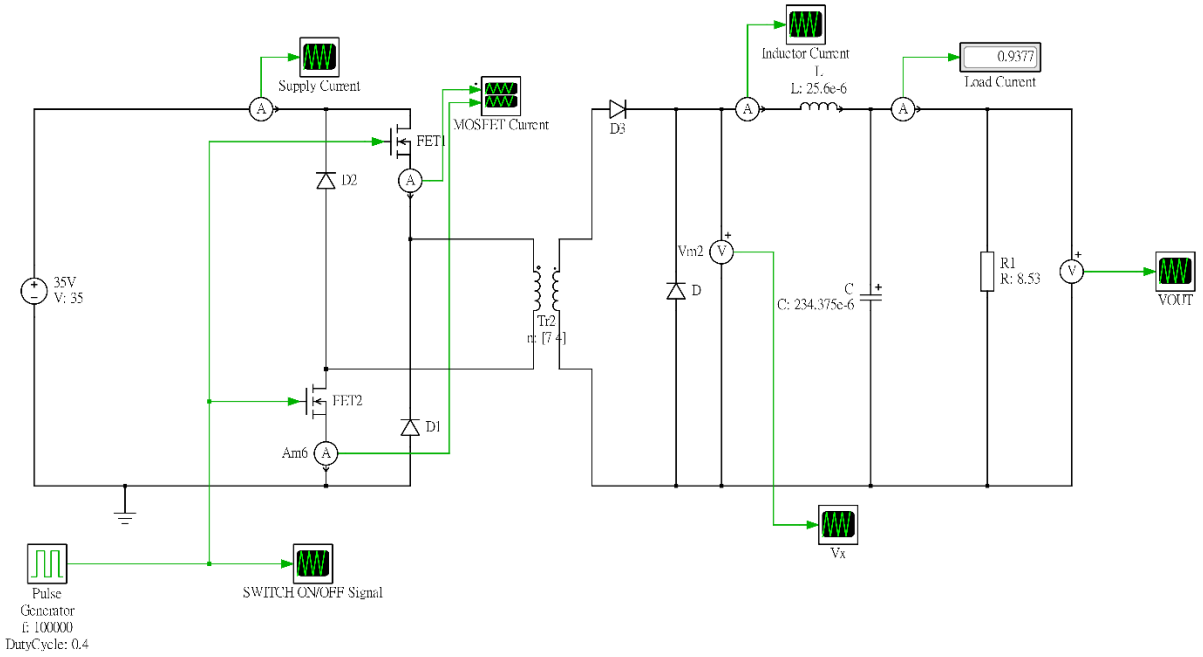

Figure 2- Ideal Model

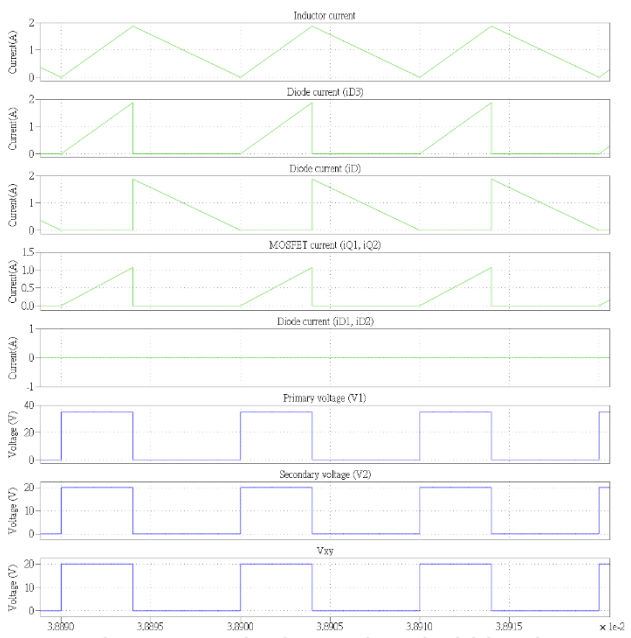

Figure 3 – Ideal DC Threshold load

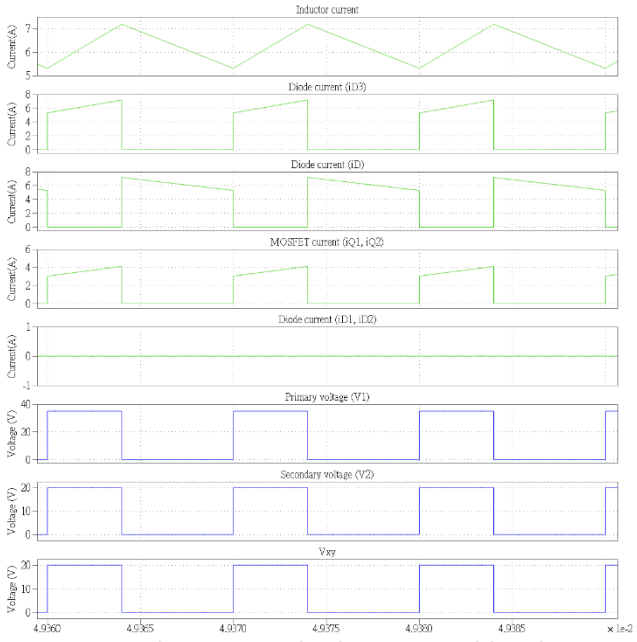

Figure 4 – Ideal DC Rated load

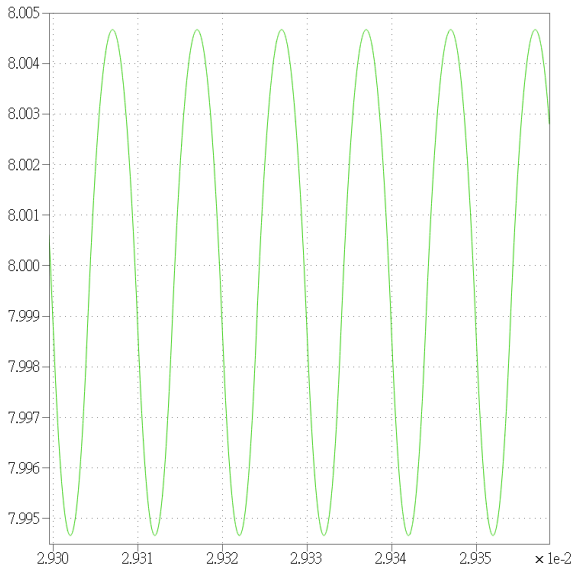

Figure 5 – Ideal DC Rated load V_o

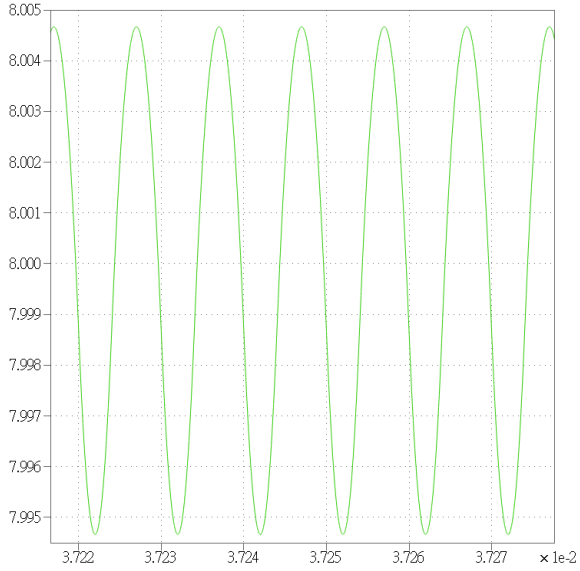

Figure 6 – Ideal DC Threshold load V_o

3.1 Comparison with the expected results

As shown in simulation results, the inductor current was 1.8756 A (from 0.000053 to 1.8756 A) under threshold load, and 1.8756 A (from 5.31 to 7.187 A) under rated load. Under both conditions, the output voltage was from 7.994 to 8.004 V and the ripple was under 0.01 V. The total result displayed were in line with expectations.

3.2 Effect of capacitor and inductor

In Figure 5 and Figure 6, the output voltage was 8V and the voltage ripple was 0.01 which could be influenced by the magnitude of the output capacitor. The larger the capacitance, the lower voltage ripple. The increase of the capacitance meant that more charge could be stored during each switching cycle, and thus the voltage ripple would be decreased because of a smaller change in voltage for a given amount of charge. For the inductor current ripple, the larger the inductance, the lower the current ripple and the voltage ripple. The increase of the inductance meant the rate of change of current was reduced. Therefore, the inductor current would rise more slowly during the "on" time and fall more slowly during the "off" time, resulting in less current ripple and less voltage ripple.

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4. Simulation results with non-ideal components in DC

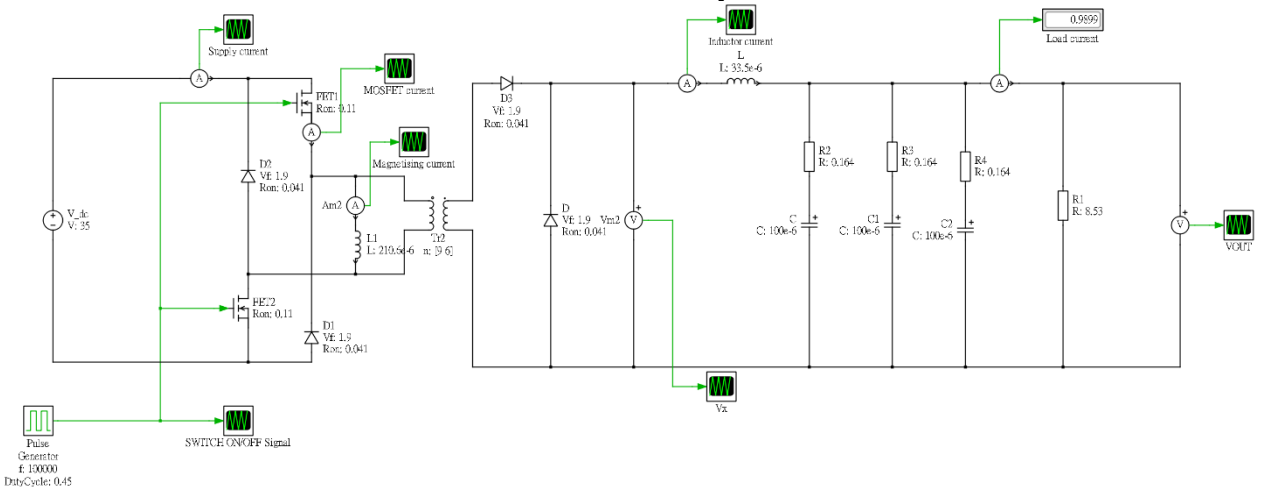

Figure 7 - Non-ideal Model

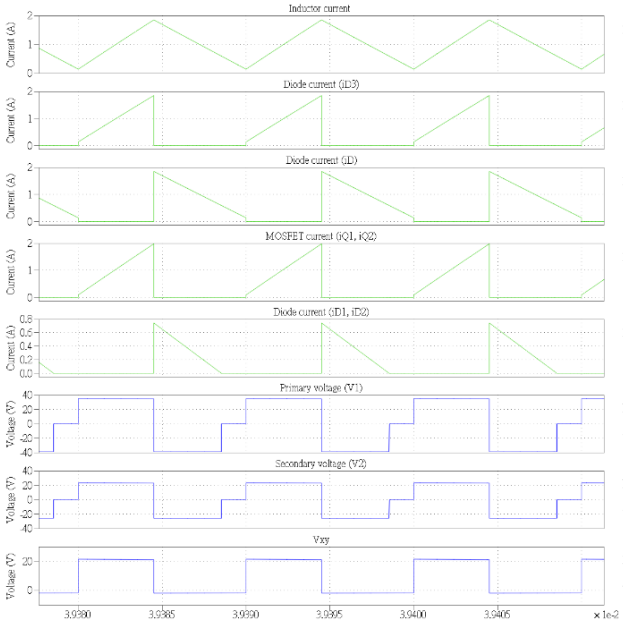

Figure 8 – Non-ideal Threshold load

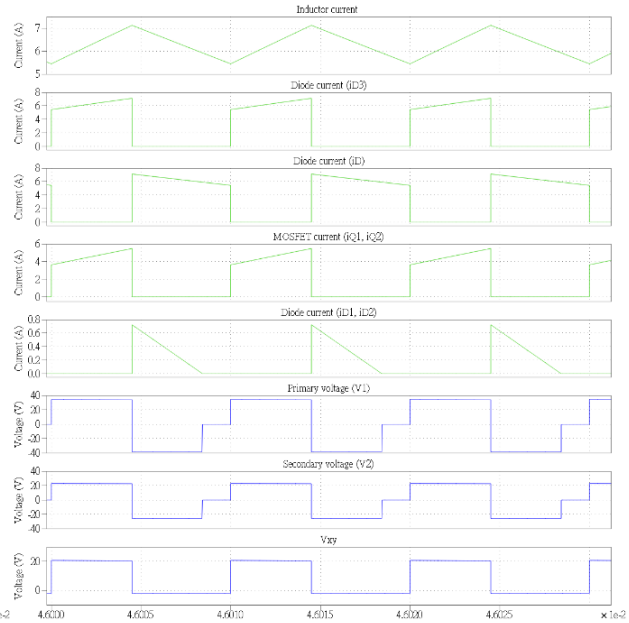

Figure 9 – Non-ideal Rated load

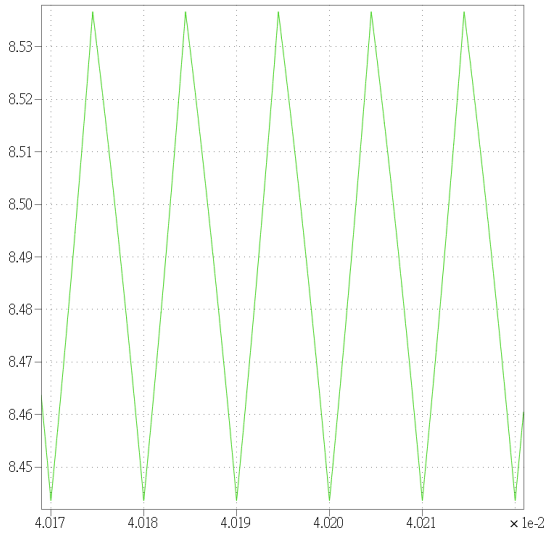

Figure 10 - Non-ideal Threshold load V_o

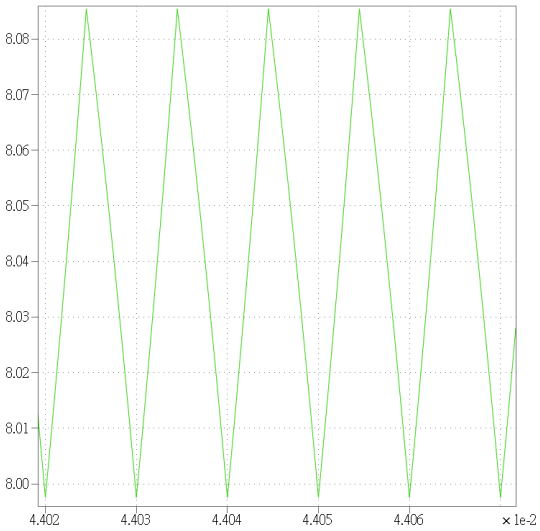

Figure 11 - Non-ideal Rated load V_o

The considerations of non-ideal components:

Diode	$V_f = 1.9\,V; R_{on} = 0.041\,\Omega$
MOSFET	$R_{on} = 0.11\,\Omega$
Magnetising Inductance	$L_{MAG} = 210.6\,\mu H$
Capacitor ESR	$R = 0.164\,\Omega$
Turn Ratio	9:6
Voltage ripple	0.09

Where V_f: Forward Voltage, R_{on}: On-resistance. All the value of the forward voltage and on-resistance above was based on the datasheet of the components.

4.1 Comparison with the expected results

Under the threshold load, the output voltage was in the range of 7.298 and 7.389 V and the ripple was 0.09035. The ripple of inductor current was 1.663. For the rated load, the output voltage was between 6.934 to 7.019 V and the ripple was 0.08554. The ripple of the inductor current was 1.6303. Both results show that the output voltage was lower than the expected voltage and the ripple was higher than the expected ripple. The inductor should not be too small, otherwise a plat would appear at the position of troughs.

4.2 Non-ideal components

4.2.1 Turn Ratio

The initial turn ratio was 7:4, but the turn ratio was changed to be 9:6 under the non-ideal model. The number of turns should consider the value of VTA (under the worst case). The worst case of VTA was under the duty cycle of 0.45, because the maximum duty cycle limit of actual PWM output was 0.45. The VTA was 0.00015543. From the datasheet, the maximum flux density was about 200 mT, and A_{core} was 97.1 mm^2. Thus, the number of the turn in primary could be calculated:

$$N = \frac{VTA}{\Delta B A_{core}} \qquad \textit{Eqn.10}$$

Therefore, the primary number of turns was 9 and the secondary number of turns was 6 because of the turn ratio 7:4. The turn ratio was changed to be 3:2.

4.2.2 Magnetising inductance L_{MAG}

From the datasheet, the inductance per turn squared (A_L) was 2600 nH. Thus, the magnetising inductance could be calculated by:

$$L_{MAG} = A_L N^2 \qquad \textit{Eqn.11}$$

The calculation result of L_{MAG} was 210.6 μH. The consideration of the magnetising inductance caused the current (iD_1, iD_2) in diode. The reason was that when the two MOSFET turn off, the magnetising current was transferred to D_1 and D_2.

4.2.3 Forward voltage and on-resistance

The forward voltage and on resistance in diodes as a result in the lower output voltage as more power was dissipated across the diode during its forward conduction. This could lead to increased heat generation and reduced overall efficiency of the converter. For the on-resistance in MOSFET, on-resistance determines the power losses and efficiency of the circuit because MOSFET was used as a switch in the converter. When the MOSFET was on, the on-resistance caused a voltage drop across the MOSFET, leading to power dissipation and heat generation. Therefore, the MOSFET needed a heatsink to dissipate the heat.

4.2.4 Equivalent Series Resistance (ESR) in capacitor

The ESR value of a capacitor caused a voltage drop across it, resulting in a reduction in the output voltage of the forward converter. Higher ESR value would cause the equivalent circuit more resistive. Hence, the voltage ripple on the output would be increased, leading to decreased efficiency and increased power dissipation. Additionally, in Figure 7, to minimize ESR, three capacitors were connected in parallel, instead of using a capacitor with large capacitance. It is because by parallel connection, the value of total capacitance was the sum of each capacitor, but the value of total ESR would be smaller as a result in the smaller ripple.

5. Simulation results with AC derived input

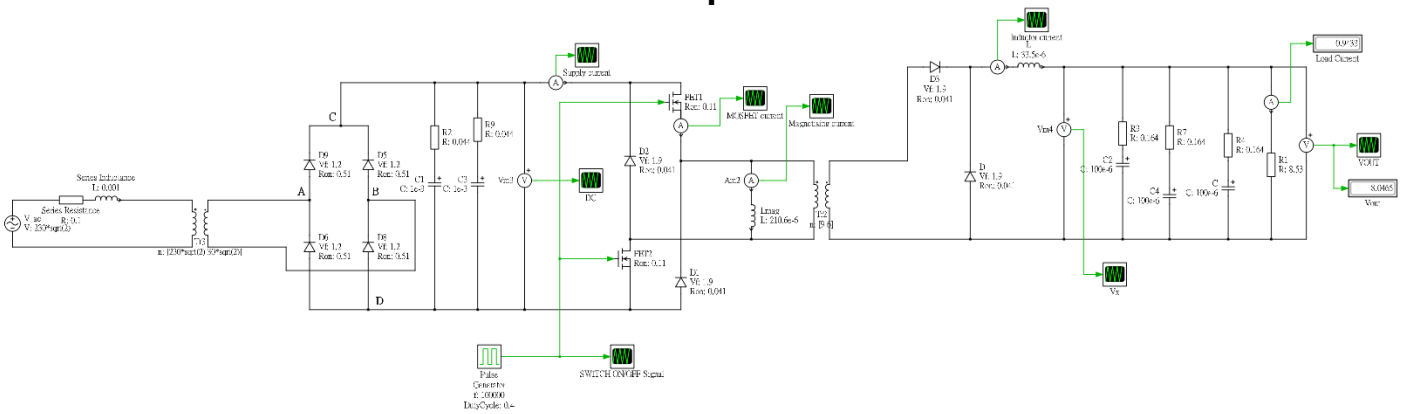

Figure 12 – Non-ideal conditions in AC input

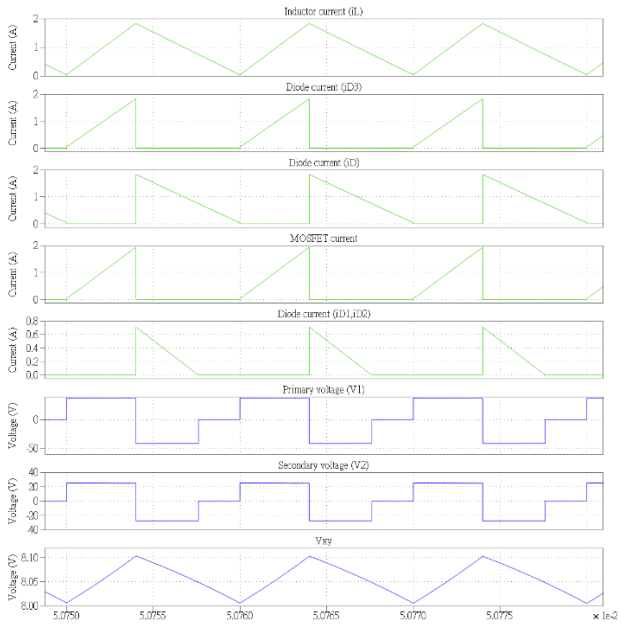

Figure 13 – Non ideal in AC Threshold load

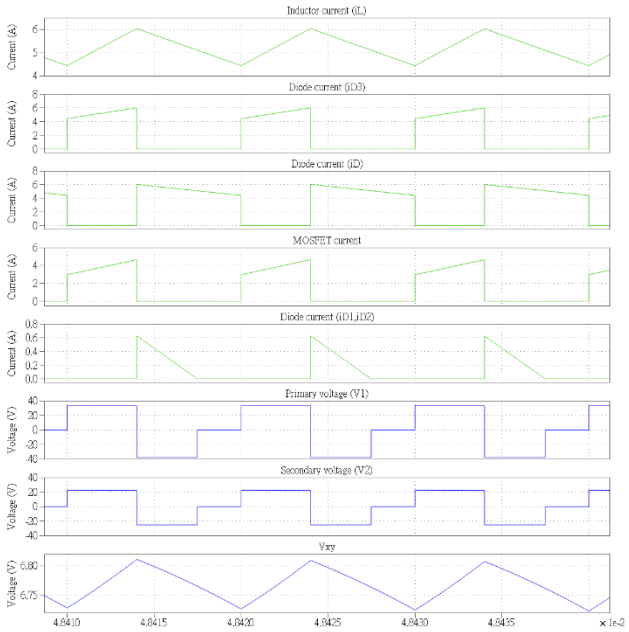

Figure 14 – Non-ideal in AC Rated load

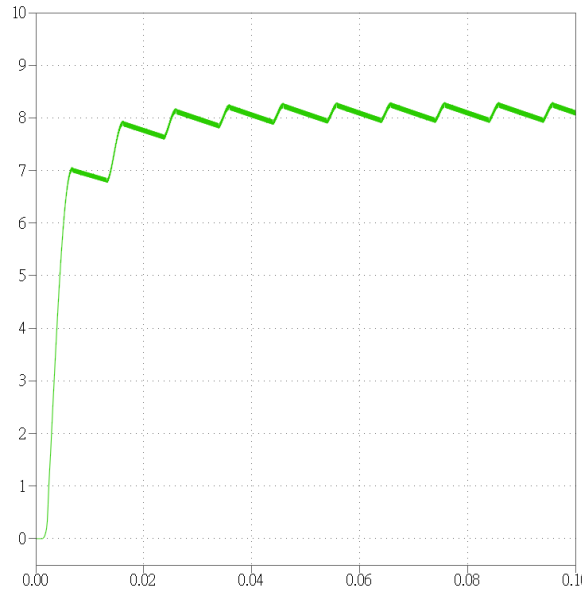

Figure 15 – Non-ideal in AC Threshold load V_o

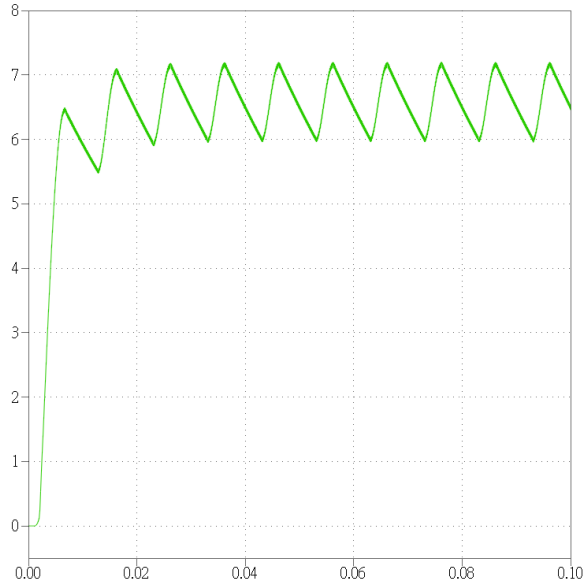

Figure 16 – Non-ideal in AC Rated load V_o

5.1 Design of non-ideal AC input

From the datasheet, the forward voltage of diode in rectifier is 1.2 V and on-resistance is 0.51 Ω. The series resistance of AC input is 0.1 Ω and the series inductance is 0.001 H. The output results with threshold load and rated load were in Figure 15 and Figure 16 respectively.

5.2 Working principle of AC input with full wave rectifier

For the AC input supply, an AC power source with RMS value of 230 V, 50 Hz was used. It was step down to 30V AC (RMS) by a transformer, which could also isolate the power

source and converter circuit. Hence, the damaging of one part would have less change to cause danger to the other part. Then a rectifier was used to convert the AC signal to DC signal.

In Figure 12, an AC source was connected to terminals A and B. When the voltage potential of A was higher than B, the current would flow from A to C through D9, and from D to B through D8. When the direction of AC source changes, the current would flow from D to A through D6, and from B to C through D5. Hence, for the load connected to terminals C and D, the direction of current would not change.

The direction of power supply was unified by rectifier, but the signal was not a flat, the output signal of rectifier was shown in the figure below.

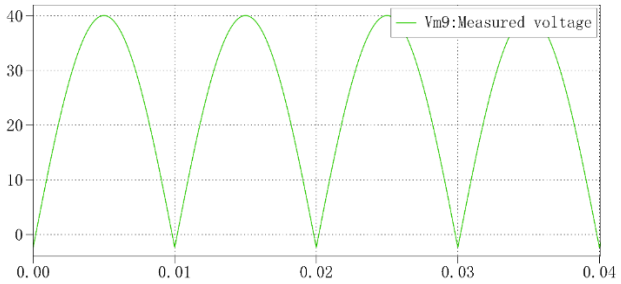

Figure 17 – DC output of rectifier

The change in voltage would cause ripple. To minimize the ripple, two capacitor was connected in parallel to serve as “smoothing” capacitor. When the input signal shown in Figure 17 approach the peak, the capacitor would charge. Then, when the input voltage decreased, the capacitor would discharge and serve as a voltage source, maintaining the voltage level. Hence, the voltage would be stabilized by the capacitor. Therefore, the ripple was decreased.

5.3 Non-ideal Transformer

There are copper loss iron loss and magnetic loss in non-ideal transformer. The winding resistance would cause a ESR in transformer. Additionally, not all of the flux would be transmitted to secondary winding, which would cause a leakage inductance connected in serial to the transformer. The ESR and the leakage inductance could be read from data sheet. To minimize the dissipation in ESR and leakage inductance, the current should be smaller.

5.4 Load resistance

The simulation results under threshold load and rated load were shown in Figure 15 and Figure 16. Compared threshold load to rated load, the DC offset was increased, and the ripple was narrowed. For the increase of DC offset, the increase of load resistance would cause a decrease of current in secondary circuit, which would lead to a current decrease in primary circuit. Hence, the current flowed into the ESR and diode would be smaller, which would lead to a lower voltage loss and voltage drop. Therefore, the average output voltage would increase. On the other hand, for the decrease of ripple, between two peeks, the capacitor would charge (when the rectifier output is larger than the voltage across the capacitor) and discharge (when the rectifier output is smaller than the voltage across the capacitor) to decrease the change rate of voltage. When the current was decreased the charge and discharge was slowed down, Hence, the rate of charging and discharging is

decreased, which would cause a smaller variety of voltage across capacitor. Thus, the ripple was decreased.

6. Gate Drive circuit

Gate Driver Circuit is required to turn on and turn off the MOSFETs as it provides logic input higher than the MOSFET threshold to control the switching of MOSFETs. The schematic of gate drive circuit was shown in Figure 18, the parameters were also labelled.

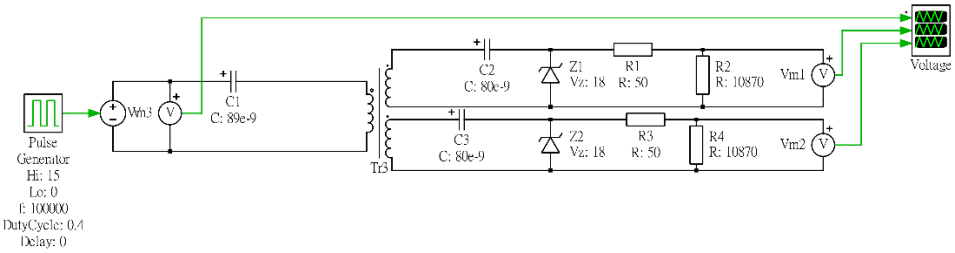

Figure 18 – Gate Drive circuit

In order to supply 15 V supply to fully turn on the MOSFET, TC4425A High-Speed Power MOSFET driver is required to amplify the 3-5 V signal generated from the UC3524A PWM signal generator to 15 V.

The details of how the circuit works and the function of each component would be discussed in this paragraph. Capacitor C_1 of 82 nF was added on the primary side to couple the signal between the gate driver IC and the transformer. The capacitor should not be too low, but higher capacitance would cause the transformer to saturate. Since the C_1 filtered the DC voltage the output side was lower than 15 V. Hence, capacitor C_2 was required to raise the output voltage, guaranteeing V_{gs} >> V_{th} for the whole on period. The capacitor would charge during the negative half cycle. Resistors R_1 and R_2 would form a time constant with C_2, which should not be too small. Hence, the capacitor was not fully discharged when the next negative half cycle reaches. When the positive half cycle reached, the capacitor could serve as a voltage supply, increasing the output voltage. Additionally, pull down R_2 and R_4 is applied to avoid the gate-source capacitance parasitical charging when the gate drive circuit was disconnected. Parasitical charging of gate capacitor could lead to a voltage higher than the expected, which could damage MOSFET. Finally, the Zener diode was applied to protect the MOSFET. The Zener diode would reverse biased when the output voltage reached 18 V. Hence, the output part was shorted when the output voltage reached 18 V. Therefore, a transient protection was provided by Zenner diode.

7. Summary

The design of a dual switch forward converter was accomplished successfully. The non-ideal situation was considered and an AC input supply was added to the final circuit. The vital simulation results were all shown and the important phenomenon such ripple and change in DC was discussed. A detailed explanation for each component was assigned to each circuit.