#### **Tomasulo Loop Example**

```
R1
Loop: LD
                     F0
                            \mathbf{0}
       MULTD
                     F4
                            F0
                                   F2
       SD
                     F4
                                   R1
                            0
       SUBI
                                   #8
                     R1
                            R1
       BNEZ
                            Loop
                     R1
```

- ☐ Assume Multiply takes 4 clocks
- □ Assume first load takes 8 clocks (cache miss?), second load takes 4 clocks (hit)
- ☐ To be clear, will show clocks for SUBI, BNEZ
- ☐ Reality, integer instructions ahead

Instru	uction s	status_				Exec	cutioı Write					
Instru	uction	j	k	iteration	Issue	comp	olete Result	_	Busy	Addr	ess	
LD	F0	0	R1	1				Load1	No			
MUL	TF4	F0	F2	1				Load2	No			
SD	F4	0	R1	1				Load3	No		Qi	
LD	F0	0	R1	2				Store1	No			
MUL	TF4	F0	F2	2				Store2	No			
SD	F4	0	R1	2				Store3	No			
Rese	rvation	Station	<u>1S</u>		S1	S2	RS for	RS for k	<b>(</b>			
	Time	Name	Busy	/ Op	Vj	Vk	Qj	Qk	Code	<i>:</i>		
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	No						SUBI	R1	R1	#8
	0	Mult2	No						BNEZ	ZR1	Loo	p
Regis	ster res	sult stati	<u>us</u>									
Clo	ck	R1		F0	F2	F4	F6	F8	F10	F12	2	F30



0

80

Qi

_						_					
<u>Instru</u>	<u>uction s</u>	<u>status</u>				Exec	cutioi Write				
Instru	uction	j	k	iteration	Issue	com	olete Result	_	Busy	Addı	ess
LD	F0	0	R1	1	1			Load1	Yes	80	
MUL <sup>*</sup>	TF4	F0	F2	1				Load2	No		
SD	F4	0	R1	1				Load3	No		Qi
LD	F0	0	R1	2				Store1	No		
MUL	TF4	F0	F2	2				Store2	No		
SD	F4	0	R1	2				Store3	No		
Rese	rvation	Station	<u>1S</u>		S1	S2	RS for	RS for I	(		
	Time	Name	Bus	у Ор	Vj	Vk	Qj	Qk	Code	<i>:</i>	
	0	Add1	No						LD	F0	0 R1
	0	Add2	No						MULT	Γ <b>F</b> 4	F0 F2
	0	Add3	No						SD	F4	0 R1
	0	Mult1	No						SUBI	R1	R1 #8
	0	Mult2	No						BNEZ	ZR1	Loop
Regis	ster res	ult stati	<u>us</u>								
Clo	ck	R1		F0	F2	F4	F6	F8	F10	F12	F30



Qi

80

Load1

Instruc	tion	<u>status</u>				Execution	o Write			
Instruc	ction	j	K	iteration	Issue	complet	e Result	_	Busy Add	ress
LD	F0	0	R1	1	1			Load1	Yes 80	
MULT	F4	F0	F2	1	2			Load2	No	
SD	F4	0	R1	1				Load3	No	Qi
LD	F0	0	R1	2				Store1	No	
MULT	F4	F0	F2	2				Store2	No	
SD	F4	0	R1	2				Store3	No	
Reserv	<u>vatio</u>	n Statior	<u>าร</u>		S1	S2	RS for	RS for k	(	
	Time	Name	Busy	<sup>,</sup> Ор	Vj	Vk	Qj	Qk	Code:	
	0	Add1	No						LD F0	0 R1
	0	Add2	No						MULT F4	F0 F2
	0	Add3	No						SD F4	0 R1
	0	Mult1	Yes	MULTD		R(F2)	Load1		SUBI R1	R1 #8
	0	Mult2	No						BNEZR1	Loop
Regist	er re	sult stat	<u>us</u>							
Cloc	k	R1		<i>F</i> 0	F2	F4	F6	F8	F10 F1	2 F30
2		80	Qi	Load1		Mult1				



Instruction s	status_				Execution	o Write					
Instruction	j	k	iteration	Issue	complet	e Result	_	Busy	Addı	ess	
LD F0	0	R1	1	1			Load1	Yes	80		
MULTF4	F0	F2	1	2			Load2	No			
SD F4	0	R1	1	3			Load3	No		Qi	
LD F0	0	R1	2				Store1	Yes	80	Mult	:1
MULTF4	F0	F2	2				Store2	No			
SD F4	0	R1	2				Store3	No			
Reservation	Statio	<u>ns</u>		S1	S2	RS for	RS for A	<b>(</b>			_
Time	Name	Busy	<sup>,</sup> Ор	Vj	Vk	Qj	Qk	Code:			
0	Add1	No						LD	F0	0	R1
0	Add2	No						<b>MULT</b>	F4	F0	F2
0	Add3	No						SD	F4	0	R1
0	Mult1	Yes	MULTD		R(F2)	Load1		SUBI	R1	R1	#8
0	Mult2	No						BNEZ	R1	Loo	p
Register res	sult stat	tus									
Clock	R1		F0	F2	F4	F6	F8	F10	F12	<u> </u>	F30
3	80	Qi	Load1		Mult1						



Note: MULT1 has no registers names in RS

Instruction	<u>status</u>				Execution	o Write				
Instruction	n <i>j</i>	k	iteration	Issue	complet	e Result	_	Busy A	<u>.ddr</u> e	ess
LD F0	0	R1	1	1			Load1	Yes	80	
MULTF4	F0	F2	1	2			Load2	No		
SD F4	0	R1	1	3			Load3	No		Qi
LD F0	0	R1	2				Store1	Yes	08	Mult1
MULTF4	F0	F2	2				Store2	No		
SD F4	0	R1	2				Store3	No		
Reservation	on Statio	<u>ns</u>		S1	S2	RS for	RS for A	<		
Tim	e Name	Busy	⁄ Ор	Vj	Vk	Qj	Qk	Code:		
	O Add1	No						LD F	0	0 R1
	O Add2	No						MULTF	4 F	F0 F2
	O Add3	No						SD F	4	0 R1
	0 Mult1	Yes	MULTD		R(F2)	Load1		SUBI F	R1 F	R1 #8
	0 Mult2	No						BNEZF	R1 I	_oop
Register r	esult sta	tus								
Clock	R1		<i>F0</i>	F2	F4	F6	F8	F10 F	-12.	F30
4	72	Qi	Load1		Mult1					



Instruction s	status_				Execution	oı Write			
Instruction	j	k	iteration	Issue	complet	e Result	_	Busy Ad	<u>ddr</u> ess
LD F0	0	R1	1	1			Load1	Yes 8	0
MULT F4	F0	F2	1	2			Load2	No	
SD F4	0	R1	1	3			Load3	No	Qi
LD F0	0	R1	2				Store1	Yes 8	0 Mult1
MULT F4	F0	F2	2				Store2	No	
SD F4	0	R1	2				Store3	No	
Reservation	Station	<u>18</u>		S1	S2	RS for	JRS for k	<	
Time	Name	Busy	<sup>,</sup> Ор	Vj	Vk	Qj	Qk	_Code:	
0	Add1	No						LD FO	0 R1
0	Add2	No						MULT F4	F0 F2
0	Add3	No						SD F4	0 R1
0	Mult1	Yes	MULTD		R(F2)	Load1		SUBI R	1 R1 #8
0	Mult2	No						BNEZR	1 Loop
Register res	sult stat	us							
Clock	R1		<i>F</i> 0	F2	F4	F6	F8	F10 F	12 F30
5	<b>72</b>	Qi	Load1		Mult1				



Instru	ction s	status_				Execution	Write					
Instru	ction	j	k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD	F0	0	R1	1	1			Load1	Yes	80		
MULT	F4	F0	F2	1	2			Load2	Yes	72		
SD	F4	0	R1	1	3			Load3	No		Qi	
LD	F0	0	R1	2	6			Store1	Yes	80	Mul	t1
MULT	F4	F0	F2	2				Store2	No			
SD	F4	0	R1	2				Store3	No			
Reser	vation	<b>Station</b>	<u>1S</u>		S1	S2	RS for	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load1		SUBI	R1	R1	#8
	0	Mult2	No						BNEZ	R1	Loo	p
Regis	ter res	sult stati	<u>JS</u>									
Cloc	k	R1		F0	F2	F4	F6	F8	F10	F12		F30
6		72	Qi	Load2		Mult1						

Note: F0 never sees Load1 result

Instru	ction s	status_				Execution	Write					
Instru	ction	j	k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD	F0	0	R1	1	1			Load1	Yes	80		
<b>MULT</b>	F4	F0	F2	1	2			Load2	Yes	72		
SD	F4	0	R1	1	3			Load3	No		Qi	
LD	F0	0	R1	2	6			Store1	Yes	80	Mul	t1
<b>MULT</b>	F4	F0	F2	2	7			Store2	No			
SD	F4	0	R1	2				Store3	No			
Reser	vation	<b>Station</b>	<u>1S</u>		S1	S2	RS for	RS for k	7			
	Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load1		SUBI	R1	R1	#8
	0	Mult2	Yes	MULTD		R(F2)	Load2		BNEZ	R1	Loo	p
Regis	ter res	sult state	<u>us</u>									
Cloc	k	R1		F0	F2	F4	F6	F8	F10	F12		F30
7		72	Qi	Load2		Mult2						

Note: MULT2 has no registers names in RS

Instruction s	status_				Execution	o Write					
Instruction	j	k	iteration	Issue	complet	e Result	_	Busy	Addı	ess	
LD F0	0	R1	1	1			Load1	Yes	80		
MULT F4	F0	F2	1	2			Load2	Yes	72		
SD F4	0	R1	1	3			Load3	No		Qi	
LD F0	0	R1	2	6			Store1	Yes	80	Mult1	
MULT F4	F0	F2	2	7			Store2	Yes	72	Mult2	
SD F4	0	R1	2	8			Store3	No			
Reservation	Station	<u>ns</u>		S1	S2	RS for	RS for I	k			
Time	Name	Busy	<sup>,</sup> Ор	Vj	Vk	Qj	Qk	Code	<i>.</i>		
0	Add1	No						LD	F0	0 R	1
0	Add2	No						MULT	F4	FO F	2
0	Add3	No						SD	F4	0 R	1
0	Mult1	Yes	MULTD		R(F2)	Load1		SUBI	R1	R1 #	8
0	Mult2	Yes	MULTD		R(F2)	Load2		BNEZ	ZR1	Loop	
Register res	sult stat	us									
Clock	R1		F0	F2	F4	F6	F8	F10	F12	2 F	<del>-</del> 30
8	<b>72</b>	Qi	Load2		Mult2						



Instruction s	status_				Execution	o Write					
Instruction	j	k	iteration	Issue	complet	e Result	_	Busy	Addı	ress	
LD F0	0	R1	1	1	9		Load1	Yes	80		
MULT F4	F0	F2	1	2			Load2	Yes	72		
SD F4	0	R1	1	3			Load3	No		Qi	
LD F0	0	R1	2	6			Store1	Yes	80	Mult	1
MULT F4	F0	F2	2	7			Store2	Yes	72	Mult	2
SD F4	0	R1	2	8			Store3	No			
Reservation	Statio	<u>ns</u>		S1	S2	RS for	RS for k	(			
Time	Name	Busy	<sup>,</sup> Ор	Vj	Vk	Qj	Qk	Code	<i>:</i>		
0	Add1	No						LD	F0	0	R1
0	Add2	No						MULT	F4	FO I	F2
0	Add3	No						SD	F4	0	R1
0	Mult1	Yes	MULTD		R(F2)	Load1		SUBI	R1	R1 ;	#8
0	Mult2	Yes	MULTD		R(F2)	Load2		BNEZ	ZR1	Loop	)
Register res	sult stat	:US									
Clock	R1		<i>F</i> 0	F2	F4	F6	F8	F10	F12	2	F30
9	64	Qi	Load2		Mult2						

Load1 completing; what is waiting for it?

<u>Instruct</u>	<u>ion status</u>	_			Execution	oi Write				
Instruct	ion <i>j</i>	k	iteration	Issue	complet	e Result	_	Busy	Addr	ess
LD F	0	0 R1	1	1	9	10	Load1	No		
MULTF	4 F	0 F2	1	2			Load2	Yes	72	
SD F	4	0 R1	1	3			Load3	No		Qi
LD F	0	0 R1	2	6	10		Store1	Yes	80	Mult1
MULTF	4 F	0 F2	2	7			Store2	Yes	72	Mult2
SD F	4	0 R1	2	8			Store3	No		
Reserva	ation Stati	<u>ons</u>		S1	S2	RS for	,RS for k	(		
7	N	_	_							
1	īme Name	e <u>Bus</u> j	/ Op	Vj	Vk	Qj	Qk	_Code	:	
,	0 Add1	Busy No	/ Op	Vj	Vk	Qj	Qk	Code	FO	0 R1
1		No	/ Op	Vj	<u>Vk</u>	Qj	Qk	7	F0	0 R1 F0 F2
,	0 Add1	No No	/ Op	Vj	<u>Vk</u>	Qj	<u>Qk</u>	LD	F0	_
1	0 Add1 0 Add2	No No	/ Op MULTD	<i>Vj</i> M(80)		Qj	Qk	LD MUL1	F0 F4	F0 F2
,	0 Add1 0 Add2 0 Add3	No No No Yes	MULTD	,		Qj Load2	Qk	LD MUL1 SD	F0 F4 F4 R1	F0 F2 0 R1
	<ul><li>0 Add1</li><li>0 Add2</li><li>0 Add3</li><li>4 Mult1</li></ul>	No No No Yes Yes	MULTD	,	R(F2)	•	Qk	LD MUL1 SD SUBI	F0 F4 F4 R1	F0 F2 0 R1 R1 #8
	0 Add1 0 Add2 0 Add3 4 Mult1 0 Mult2 r result st	No No No Yes Yes	MULTD	,	R(F2)	•	Qk F8	LD MUL1 SD SUBI BNEZ	F0 F4 F4 R1 ZR1	F0 F2 0 R1 R1 #8



Load2 completing; what is waiting for it?

Instru	ction	<u>status</u>				Executio	Write					
Instru	ction	j	k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD	F0	0	R1	1	1	9	10	Load1	No			
MULT	F4	F0	F2	1	2			Load2	No			
SD	F4	0	R1	1	3			Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	Mul	t1
MULT	F4	F0	F2	2	7			Store2	Yes	72	Mul	t2
SD	F4	0	R1	2	8			Store3	No			
Reser	rvatior	n Statio	<u>ns</u>		S1	S2	RS for	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code	_		
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	3	Mult1	Yes	MULTD	M(80)	R(F2)			SUBI	R1	R1	#8
	4	Mult2	Yes	MULTD	M(72)	R(F2)			BNEZ	:R1	Loo	p
Regis	ter re	<u>sult stat</u>	<u>us</u>									
Cloc	ck	R1		F0	F2	F4	F6	F8	F10	F12		F30
11		64	Qi	Load3		Mult2						

Instru	ction	status				Execution	Write					
Instru	ction	j	k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD	F0	0	R1	1	1	9	10	Load1	No			
MULT	F4	F0	F2	1	2			Load2	No			
SD	F4	0	R1	1	3			Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	Mul	t1
MULT	F4	F0	F2	2	7			Store2	Yes	72	Mul	t2
SD	F4	0	R1	2	8			Store3	No			
Reser	rvatior	Station	<u>าร</u>		S1	S2	RS for	RS for k	(			
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	2	Mult1	Yes	MULTD	M(80)	R(F2)			SUBI	R1	R1	#8
	3	Mult2	Yes	MULTD	M(72)	R(F2)			BNEZ	R1	Loo	p
Regis	ter res	sult stat	<u>us</u>									
Cloc	ck	R1		F0	F2	F4	F6	F8	F10	F12		F30
12		64	Qi	Load3		Mult2						

Instru	ction s	status_				Execution	Write					
Instru	ction	j	k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD	F0	0	R1	1	1	9	10	Load1	No			
<b>MULT</b>	F4	F0	F2	1	2			Load2	No			
SD	F4	0	R1	1	3			Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	Mul	t1
MULT	F4	F0	F2	2	7			Store2	Yes	72	Mul	t2
SD	F4	0	R1	2	8			Store3	No			
Reser	rvation	<b>Station</b>	<u>1S</u>		S1	S2	RS for	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	1	Mult1	Yes	MULTD	M(80)	R(F2)			SUBI	R1	R1	#8
	2	Mult2	Yes	MULTD	M(72)	R(F2)			BNEZ	R1	Loo	р
Regis	ter res	sult stati	<u>us</u>									
Cloc	ck	R1		F0	F2	F4	F6	F8	F10	F12		F30
13		64	Qi	Load3		Mult2						

Instru	ction s	status_				Execution	Write					
Instru	ction	j	k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD	F0	0	R1	1	1	9	10	Load1	No			
MULT	F4	F0	F2	1	2	14		Load2	No			
SD	F4	0	R1	1	3			Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	Mul	t1
MULT	F4	F0	F2	2	7			Store2	Yes	72	Mul	t2
SD	F4	0	R1	2	8			Store3	No			
Reser	vatior	Station	<u>าร</u>		S1	S2	RS for	RS for k	(			
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	FO	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD	M(80)	R(F2)			SUBI	R1	R1	#8
	1	Mult2	Yes	MULTD	M(72)	R(F2)			BNEZ	R1	Loo	p
Regis	ter res	sult stat	<u>us</u>									
Cloc	k	R1		F0	F2	F4	F6	F8	F10	<i>F</i> 12		F30
14		64	Qi	Load3		Mult2						

Mult1 completing; what is waiting for it?

Instruc	ction s	status				Execution	Write					
Instruc	ction	j	k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD	F0	0	R1	1	1	9	10	Load1	No			
<b>MULT</b>	F4	F0	F2	1	2	14	15	Load2	No			
SD	F4	0	R1	1	3			Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	Yes	08	M(8	0)*R(F
MULT	F4	F0	F2	2	7	15		Store2	Yes	72	Mult	t2
SD	F4	0	R1	2	8			Store3	No			
Reser	vation	Station	<u>IS</u>		S1	S2	RS for J	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:	•		
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	No						SUBI	R1	R1	#8
	0	Mult2	Yes	MULTD	M(72)	R(F2)			BNEZ	R1	Loo	р
Regist	ter res	ult statu	<u>IS</u>									
Cloc	k	R1		F0	F2	F4	F6	F8	F10	F12		F30
15		64	Qi	Load3		Mult2						

Mult2 completing; what is waiting for it?

Instru	ction s	status_				Execution	Write					
Instru	ction	j	k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD	F0	0	R1	1	1	9	10	Load1	No			
MULT	F4	F0	F2	1	2	14	15	Load2	No			
SD	F4	0	R1	1	3			Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	M(8	0)*R(F
MULT	F4	F0	F2	2	7	15	16	Store2	Yes	72	M(7	2)*R(7
SD	F4	0	R1	2	8			Store3	No			
Reser	vatior	Station	<u>าร</u>		S1	S2	RS for	RS for k				
	Time	A /			1.7	1.71	_ ·	$\sim$ 1	01 -			
	Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:			
		Add1	<i>Busy</i> No	Ор	VJ	VK	Qj	QK	LD	F0	0	R1
	0			Ор	VJ	VK	QJ	QK		F0	0 F0	R1 F2
	0	Add1	No	Ор	VJ	VK	Qj	QK	LD	F0		
	0 0 0	Add1 Add2	No No	MULTD	VJ	R(F2)	Load3	QK	LD MULT	F0 F4	F0 0	F2
	0 0 0	Add1 Add2 Add3	No No No		VJ			QK	LD MULT SD	F0 F4 F4 R1	F0 0	F2 R1 #8
Regis	0 0 0 0	Add1 Add2 Add3 Mult1	No No No Yes		VJ			QK	LD MULT SD SUBI	F0 F4 F4 R1	F0 0 R1	F2 R1 #8
Regis	0 0 0 0 0 ter res	Add1 Add2 Add3 Mult1 Mult2	No No No Yes		F2			F8	LD MULT SD SUBI BNEZ	F0 F4 F4 R1 R1	F0 0 R1 L00	F2 R1 #8

Instru	ction	status_				Execution	Write					
Instru	ction	j	k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD	F0	0	R1	1	1	9	10	Load1	No			
MULT	F4	F0	F2	1	2	14	15	Load2	No			
SD	F4	0	R1	1	3			Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	M(8	0)*R(F
MULT	F4	F0	F2	2	7	15	16	Store2	Yes	72	M(7	2)*R(7
SD	F4	0	R1	2	8			Store3	Yes	64	Mul	t1
Reser	vatior	Station	<u>าร</u>		S1	S2	RS for	RS for k				
	<del></del> -			_								
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:	•		
		Name Add1	<i>Busy</i> No	Ор	Vj	Vk	Qj	Qk	Code:	F0	0	R1
	0			Ор	Vj	Vk	Qj	Qk		F0	0 F0	R1 F2
	0	Add1	No	Ор	Vj	Vk	Qj	Qk	LD	F0		
	0 0 0	Add1 Add2	No No	<i>Op</i> MULTD	Vj	Vk R(F2)	Qj Load3	Qk	LD MULT	F0 F4	F0 0	F2
	0 0 0	Add1 Add2 Add3	No No No		Vj			Qk	LD MULT SD	F0 F4 F4 R1	F0 0	F2 R1 #8
Regis	0 0 0 0	Add1 Add2 Add3 Mult1	No No No Yes		Vj			Qk	LD MULT SD SUBI	F0 F4 F4 R1	F0 0 R1	F2 R1 #8
Regis	0 0 0 0 0 ter res	Add1 Add2 Add3 Mult1 Mult2	No No No Yes		F2			Qk F8	LD MULT SD SUBI BNEZ	F0 F4 F4 R1 R1	F0 0 R1 L00	F2 R1 #8

Instru	ction s	status_				Execution	Write					
Instru	ction	j	k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD	F0	0	R1	1	1	9	10	Load1	No			
MULT	F4	F0	F2	1	2	14	15	Load2	No			
SD	F4	0	R1	1	3	18		Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	M(8	0)*R(F
MULT	F4	F0	F2	2	7	15	16	Store2	Yes	72	M(7	2)*R(7
SD	F4	0	R1	2	8			Store3	Yes	64	Mult	t1
Reser	vatior	<b>Station</b>	<u>1S</u>		S1	S2	RS for	RS for k	-			
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:	•		
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						NALIL T			F2
									MULT	Γ4	F0	1 4
	0	Add3	No						SD	F4	0	R1
		Add3 Mult1		MULTD		R(F2)	Load3				0	
	0		No	MULTD		R(F2)	Load3		SD	F4 R1	0	R1 #8
Regis	0	Mult1	No Yes No	MULTD		R(F2)	Load3		SD SUBI	F4 R1	0 R1	R1 #8
Regis Cloc	0 0 ter res	Mult1 Mult2	No Yes No	MULTD F0	F2	R(F2)	Load3 F6	F8	SD SUBI	F4 R1 R1	0 R1 Loo	R1 #8 p

Instruc	ction s	status_				Execution	Write					
Instru	ction	j	k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD	F0	0	R1	1	1	9	10	Load1	No			
MULT	F4	F0	F2	1	2	14	15	Load2	No			
SD	F4	0	R1	1	3	18	19	Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	No			
MULT	F4	F0	F2	2	7	15	16	Store2	Yes	72	M(7	2)*R(7
SD	F4	0	R1	2	8			Store3	Yes	64	Mult	<u>:1</u>
Reser	vatior	<b>Station</b>	<u>ıs</u>		S1	S2	RS for	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load3		SUBI	R1	R1	#8
	0	Mult2	No						BNEZ	R1	Loo	р
Regist	ter res	sult statu	<u>us</u>									
Cloc	k	R1		F0	F2	F4	F6	F8	F10	F12		F30
19		56	Qi	Load3		Mult1						

Instruc	ction s	status_				Execution	Write					
Instru	ction	j	k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD	F0	0	R1	1	1	9	10	Load1	No			
MULT	F4	F0	F2	1	2	14	15	Load2	No			
SD	F4	0	R1	1	3	18	19	Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	No			
MULT	F4	F0	F2	2	7	15	16	Store2	Yes	72	M(7	2)*R(7
SD	F4	0	R1	2	8	20		Store3	Yes	64	Mult	t <b>1</b>
Reser	vation	<b>Station</b>	<u>IS</u>		S1	S2	RS for	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load3		SUBI	R1	R1	#8
	0	Mult2	No						BNEZ	R1	Loo	р
Regist	ter res	sult statu	<u>us</u>									
Cloc	k	R1		F0	F2	F4	F6	F8	F10	F12		F30
20		56	Qi	Load3		Mult1						

Instru	ction s	status_				Execution	Write					
Instru	ction	j	k	iteration	Issue	complete	Result		Busy	Addr	ess	
LD	F0	0	R1	1	1	9	10	Load1	No			
MULT	F4	F0	F2	1	2	14	15	Load2	No			
SD	F4	0	R1	1	3	18	19	Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	No			
MULT	F4	F0	F2	2	7	15	16	Store2	No			
SD	F4	0	R1	2	8	20	21	Store3	Yes	64	Mul	t1
Reser	vatior	Station	<u>าร</u>		S1	S2	RS for	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code.			
		<i>Name</i> Add1	<i>Busy</i> No	Ор	Vj	Vk	Qj	Qk	Code:	F0	0	R1
	0			Ор	Vj	Vk	Qj	Qk		F0	0 F0	R1 F2
	0	Add1	No	Ор	Vj	Vk	Qj	Qk	LD	F0		
	0 0 0	Add1 Add2	No No	<i>Op</i> MULTD	Vj	Vk R(F2)	Qj Load3	Qk	LD MULT	F0 F4	F0 0	F2
	0 0 0	Add1 Add2 Add3	No No No		Vj			Qk	LD MULT SD	F0 F4 F4 R1	F0 0	F2 R1 #8
Regis	0 0 0 0	Add1 Add2 Add3 Mult1	No No No Yes		Vj			Qk	LD MULT SD SUBI	F0 F4 F4 R1	F0 0 R1	F2 R1 #8
Regis:	0 0 0 0 0 ter res	Add1 Add2 Add3 Mult1 Mult2	No No No Yes		Vj F2			Qk F8	LD MULT SD SUBI	F0 F4 F4 R1 R1	F0 0 R1 L00	F2 R1 #8 p