Tomasulo Example Cycle 0

Instruction status					*Execution*	*Write*					
Instruction		*j*	*k*	*Issue*	*complete*	*Result*			Busy	Address	
LD	F6	34+	R2					Load1	No		
LD	F2	45+	R3					Load2	No		
MULT	F0	F2	F4					Load3	No		
SUBD	F8	F6	F2								
DIVD	F10	F0	F6								
ADDD	F6	F8	F2								

Reservation Stations				*S1*	*S2*	*RS for j*	*RS for k*
Time	*Name*	*Busy*	*Op*	*Vj*	*Vk*	*Qj*	*Qk*
0	Add1	No					
0	Add2	No					
0	Add3	No					
0	Mult1	No					
0	Mult2	No					

Register result status											
Clock			*F0*	*F2*	*F4*	*F6*	*F8*	*F10*	*F12*	...	*F30*
0		*FU*									

Latency: *load* 1, *add* 2, *multiply* 10 and *divide* 40 clock cycles

Tomasulo Example Cycle 1

Instruction status

Instruction		j	k	Issue	Execution complete	Write Result
LD	F6	34+	R2	1		
LD	F2	45+	R3			
MULTD	F0	F2	F4			
SUBD	F8	F6	F2			
DIVD	F10	F0	F6			
ADDD	F6	F8	F2			

	Busy	Address
Load1	Yes	34+R2
Load2	No	
Load3	No	

Reservation Stations

Time	Name	Busy	Op	S1 Vj	S2 Vk	RS for j Qj	RS for k Qk
0	Add1	No					
0	Add2	No					
	Add3	No					
0	Mult1	No					
0	Mult2	No					

Register result status

Clock		F0	F2	F4	F6	F8	F10	F12 ...	F30
1	FU				Load1				

Tomasulo Example Cycle 2

Instruction status

Instruction	j	k	Issue	Execution complete	Write Result
LD F6	34+	R2	1		
LD F2	45+	R3	2		
MULTD F0	F2	F4			
SUBD F8	F6	F2			
DIVD F10	F0	F6			
ADDD F6	F8	F2			

	Busy	Address
Load1	Yes	34+R2
Load2	Yes	45+R3
Load3	No	

Reservation Stations

Time	Name	Busy	Op	S1 Vj	S2 Vk	RS for j Qj	RS for k Qk
0	Add1	No					
0	Add2	No					
	Add3	No					
0	Mult1	No					
0	Mult2	No					

Register result status

Clock	F0	F2	F4	F6	F8	F10	F12 ...	F30
2 FU		Load2		Load1				

Note: Unlike 6600, can have multiple loads outstanding

Tomasulo Example Cycle 3

Instruction status

Instruction		j	k	Issue	Execution complete	Write Result
LD	F6	34+	R2	1	3	
LD	F2	45+	R3	2		
MULTD	F0	F2	F4	3		
SUBD	F8	F6	F2			
DIVD	F10	F0	F6			
ADDD	F6	F8	F2			

	Busy	Address
Load1	Yes	34+R2
Load2	Yes	45+R3
Load3	No	

Reservation Stations

Time	Name	Busy	Op	S1 Vj	S2 Vk	RS for j Qj	RS for k Qk
0	Add1	No					
0	Add2	No					
	Add3	No					
0	Mult1	Yes	MULTD		R(F4)	Load2	
0	Mult2	No					

Register result status

Clock		F0	F2	F4	F6	F8	F10	F12 ...	F30
3	FU	Mult1	Load2		Load1				

- Note: register names are removed ("renamed") in Reservation Stations; MULT issued vs. scoreboard
- Load1 completing; what is waiting for Load1?

Tomasulo Example Cycle 4

Instruction status					Execution	Write					
Instruction		j	k	Issue	complete	Result			Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD	F2	45+	R3	2	4			Load2	Yes	45+R3	
MULT	F0	F2	F4	3				Load3	No		
SUBD	F8	F6	F2	4							
DIVD	F10	F0	F6								
ADDD	F6	F8	F2								

Reservation Stations				S1	S2	RS for j	RS for k			
Time	Name	Busy	Op	Vj	Vk	Qj	Qk			
0	Add1	Yes	SUBD	M(34+R2)			Load2			
0	Add2	No								
	Add3	No								
0	Mult1	Yes	MULTD		R(F4)	Load2				
0	Mult2	No								

Register result status											
Clock			F0	F2	F4	F6	F8	F10	F12	...	F30
4		FU	Mult1	Load2		M(34+R2)	Add1				

- Load2 completing; what is waiting for it?

Tomasulo Example Cycle 5

Instruction status					Execution	Write						
Instruction		j	k	Issue	complete	Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MULT	F0	F2	F4	3				Load3	No			
SUBD	F8	F6	F2	4								
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2									

Reservation Stations				S1	S2	RS for j	RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk				
2	Add1	Yes	SUBD	M(34+R2)	M(45+R3)						
0	Add2	No									
	Add3	No									
10	Mult1	Yes	MULTD	M(45+R3)	R(F4)						
0	Mult2	Yes	DIVD		M(34+R2)	Mult1					

Register result status											
Clock			F0	F2	F4	F6	F8	F10	F12	...	F30
5		FU	Mult1	M(45+R3)		M(34+R2)	Add1	Mult2			

Tomasulo Example Cycle 6

Instruction status					Execution	Write					
Instruction		j	k	Issue	complete	Result			Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD	F2	45+	R3	2	4	5		Load2	No		
MULT	F0	F2	F4	3				Load3	No		
SUBD	F8	F6	F2	4							
DIVD	F10	F0	F6	5							
ADDD	F6	F8	F2	6							

Reservation Stations				S1	S2	RS for j	RS for k			
Time	Name	Busy	Op	Vj	Vk	Qj	Qk			
1	Add1	Yes	SUBD	M(34+R2)	M(45+R3)					
0	Add2	Yes	ADDD		M(45+R3)	Add1				
	Add3	No								
9	Mult1	Yes	MULTD	M(45+R3)	R(F4)					
0	Mult2	Yes	DIVD		M(34+R2)	Mult1				

Register result status										
Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
6	FU	Mult1	M(45+R3)		Add2	Add1	Mult2			

- Issue ADDD here vs. scoreboard?

Tomasulo Example Cycle 7

Instruction status					Execution	Write						
Instruction		j	k	Issue	complete	Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MULT	F0	F2	F4	3				Load3	No			
SUBD	F8	F6	F2	4	7							
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2	6								

Reservation Stations				S1	S2	RS for j	RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk				
0	Add1	Yes	SUBD	M(34+R2)	M(45+R3)						
0	Add2	Yes	ADDD		M(45+R3)	Add1					
	Add3	No									
8	Mult1	Yes	MULTD	M(45+R3)	R(F4)						
0	Mult2	Yes	DIVD		M(34+R2)	Mult1					

Register result status											
Clock			F0	F2	F4	F6	F8	F10	F12	...	F30
7		FU	Mult1	M(45+R3)		Add2	Add1	Mult2			

- Add1 completing; what is waiting for it?

Tomasulo Example Cycle 8

Instruction status					Execution	Write						
Instruction		j	k	Issue	complete	Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MUL	F0	F2	F4	3				Load3	No			
SUBD	F8	F6	F2	4	7	8						
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2	6								

Reservation Stations				S1	S2	RS for j	RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk				
0	Add1	No									
2	Add2	Yes	ADDD	M()-M()	M(45+R3)						
0	Add3	No									
7	Mult1	Yes	MULT	M(45+R3)	R(F4)						
0	Mult2	Yes	DIVD		M(34+R2)	Mult1					

Register result s											
Clock			F0	F2	F4	F6	F8	F10	F12	...	F30
8		FU	Mult1	M(45+R3)		Add2	M()-M()	Mult2			

Tomasulo Example Cycle 9

Instruction status											
Instruction		*j*	*k*	*Issue*	*Execution complete*	*Write Result*			Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD	F2	45+	R3	2	4	5		Load2	No		
MULTD	F0	F2	F4	3				Load3	No		
SUBD	F8	F6	F2	4	7	8					
DIVD	F10	F0	F6	5							
ADDD	F6	F8	F2	6							

Reservation Stations				*S1*	*S2*	*RS for j*	*RS for k*
Time	*Name*	*Busy*	*Op*	*Vj*	*Vk*	*Qj*	*Qk*
0	Add1	No					
1	Add2	Yes	ADDD	M()–M()	M(45+R3)		
0	Add3	No					
6	Mult1	Yes	MULTD	M(45+R3)	R(F4)		
0	Mult2	Yes	DIVD		M(34+R2)	Mult1	

Register result status										
Clock		*F0*	*F2*	*F4*	*F6*	*F8*	*F10*	*F12*	...	*F30*
9	*FU*	Mult1	M(45+R3)		Add2	M()–M()	Mult2			

Tomasulo Example Cycle 10

Instruction status											
Instruction		*j*	*k*	*Issue*	*Execution complete*	*Write Result*			Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD	F2	45+	R3	2	4	5		Load2	No		
MUL	F0	F2	F4	3				Load3	No		
SUBD	F8	F6	F2	4	7	8					
DIVD	F10	F0	F6	5							
ADDD	F6	F8	F2	6	10						

Reservation Stations				*S1*	*S2*	*RS for j*	*RS for k*
Time	*Name*	*Busy*	*Op*	*Vj*	*Vk*	*Qj*	*Qk*
0	Add1	No					
0	Add2	Yes	ADDD	M()–M()	M(45+R3)		
0	Add3	No					
5	Mult1	Yes	MULTD	M(45+R3)	R(F4)		
0	Mult2	Yes	DIVD		M(34+R2)	Mult1	

Register result status										
Clock			*F0*	*F2*	*F4*	*F6*	*F8*	*F10*	*F12*	...	*F30*
10		*FU*	Mult1	M(45+R3)		Add2	M()–M()	Mult2			

- Add2 completing; what is waiting for it?

Tomasulo Example Cycle 11

Instruction status					Execution	Write						
Instruction		j	k	Issue	complete	Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MUL	F0	F2	F4	3				Load3	No			
SUBD	F8	F6	F2	4	7	8						
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2	6	10	11						

Reservation Stations				S1	S2	RS for j	RS for k				
Time	Name	Bus	Op	Vj	Vk	Qj	Qk				
0	Add1	No									
0	Add2	No									
0	Add3	No									
4	Mult1	Yes	MULT	M(45+R3)	R(F4)						
0	Mult2	Yes	DIVD		M(34+R2)	Mult1					

Register result s												
Clock			F0	F2	F4	F6	F8	F10	F12	...	F30
11		FU	Mult1	M(45+R3)		(M-M)+M()	M()ĞM()	Mult2			

- Write result of ADDD here vs. scoreboard?

Tomasulo Example Cycle 12

Instruction status					Execution	Write						
Instruction		j	k	Issue	complete	Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MUL	F0	F2	F4	3				Load3	No			
SUBD	F8	F6	F2	4	6	7						
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2	6	10	11						

Reservation Stations				S1	S2	RS for j	RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk				
0	Add1	No									
0	Add2	No									
0	Add3	No									
3	Mult1	Yes	MULTD	M(45+R3)	R(F4)						
0	Mult2	Yes	DIVD		M(34+R2)	Mult1					

Register result status											
Clock			F0	F2	F4	F6	F8	F10	F12	...	F30
12		FU	Mult1	M(45+R3)		(M-M)+M()	M()–M()	Mult2			

- Note: all quick instructions complete already

Tomasulo Example Cycle 13

Instruction status					Execution	Write					
Instruction		j	k	Issue	complete	Result			Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD	F2	45+	R3	2	4	5		Load2	No		
MULTD	F0	F2	F4	3				Load3	No		
SUBD	F8	F6	F2	4	7	8					
DIVD	F10	F0	F6	5							
ADDD	F6	F8	F2	6	10	11					

Reservation Stations				S1	S2	RS for j	RS for k			
Time	Name	Busy	Op	Vj	Vk	Qj	Qk			
0	Add1	No								
0	Add2	No								
	Add3	No								
2	Mult1	Yes	MULTD	M(45+R3)	R(F4)					
0	Mult2	Yes	DIVD		M(34+R2)	Mult1				

Register result status										
Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
13	FU	Mult1	M(45+R3)		(M–M)+M()	M()–M()	Mult2			

Tomasulo Example Cycle 14

Instruction status					Execution	Write					
Instruction		j	k	Issue	complete	Result			Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD	F2	45+	R3	2	4	5		Load2	No		
MULT	F0	F2	F4	3				Load3	No		
SUBD	F8	F6	F2	4	7	8					
DIVD	F10	F0	F6	5							
ADDD	F6	F8	F2	6	10	11					

Reservation Stations				S1	S2	RS for j	RS for k			
Time	Name	Busy	Op	Vj	Vk	Qj	Qk			
0	Add1	No								
0	Add2	No								
0	Add3	No								
1	Mult1	Yes	MULTD	M(45+R3)	R(F4)					
0	Mult2	Yes	DIVD		M(34+R2)	Mult1				

Register result status										
Clock			F0	F2	F4	F6	F8	F10	F12 ...	F30
14		FU	Mult1	M(45+R3)		(M–M)+M()	M()–M()	Mult2		

Tomasulo Example Cycle 15

Instruction status					Execution	Write						
Instruction		j	k	Issue	complete	Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MULT	F0	F2	F4	3	15			Load3	No			
SUBD	F8	F6	F2	4	7	8						
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2	6	10	11						

Reservation Stations				S1	S2	RS for j	RS for k			
Time	Name	Busy	Op	Vj	Vk	Qj	Qk			
0	Add1	No								
0	Add2	No								
	Add3	No								
0	Mult1	Yes	MULTD	M(45+R3)	R(F4)					
0	Mult2	Yes	DIVD		M(34+R2)	Mult1				

Register result status										
Clock			F0	F2	F4	F6	F8	F10	F12 ...	F30
15		FU	Mult1	M(45+R3)		(M–M)+M()	M()–M()	Mult2		

- Mult1 completing; what is waiting for it?

Tomasulo Example Cycle 16

Instruction status					Execution	Write						
Instruction		j	k	Issue	complete	Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MULT	F0	F2	F4	3	15	16		Load3	No			
SUBD	F8	F6	F2	4	7	8						
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2	6	10	11						

Reservation Stations				S1	S2	RS for j	RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk				
0	Add1	No									
0	Add2	No									
	Add3	No									
0	Mult1	No									
40	Mult2	Yes	DIVD	M*F4	M(34+R2)						

Register result status											
Clock			F0	F2	F4	F6	F8	F10	F12	...	F30
16		FU	M*F4	M(45+R3)		(M–M)+M()	M()–M()	Mult2			

- Note: Just waiting for divide

Tomasulo Example Cycle 55

Instruction status					Execution	Write						
Instruction		j	k	Issue	complete	Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MULT	F0	F2	F4	3	15	16		Load3	No			
SUBD	F8	F6	F2	4	7	8						
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2	6	10	11						

Reservation Stations				S1	S2	RS for j	RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk				
0	Add1	No									
0	Add2	No									
	Add3	No									
0	Mult1	No									
1	Mult2	Yes	DIVD	M*F4	M(34+R2)						

Register result status											
Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
55	FU	M*F4	M(45+R3)		(M–M)+M()	M()–M()	Mult2			

Tomasulo Example Cycle 56

Instruction status					Execution	Write						
Instruction		j	k	Issue	complete	Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MUL	F0	F2	F4	3	15	16		Load3	No			
SUBD	F8	F6	F2	4	7	8						
DIVD	F10	F0	F6	5	56							
ADDD	F6	F8	F2	6	10	11						

Reservation Stations				S1	S2	RS for j	RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk				
0	Add1	No									
0	Add2	No									
	Add3	No									
0	Mult1	No									
0	Mult2	Yes	DIVD	M*F4	M(34+R2)						

Register result status											
Clock			F0	F2	F4	F6	F8	F10	F12	...	F30
56		FU	M*F4	M(45+R3)		(M–M)+M()	M()–M()	Mult2			

- Mult 2 completing; what is waiting for it?

Tomasulo Example Cycle 57

Instruction status					Execution	Write						
Instruction		j	k	Issue	complete	Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MUL	F0	F2	F4	3	15	16		Load3	No			
SUBD	F8	F6	F2	4	7	8						
DIVD	F10	F0	F6	5	56	57						
ADDD	F6	F8	F2	6	10	11						

Reservation Stations				S1	S2	RS for j	RS for k				
Time	Name	Busy	Op	Vj	Vk	Qj	Qk				
0	Add1	No									
0	Add2	No									
	Add3	No									
0	Mult1	No									
0	Mult2	No									

Register result status											
Clock			F0	F2	F4	F6	F8	F10	F12	...	F30
57		FU	M*F4	M(45+R3)		(M–M)+M()	M()–M()	M*F4/M			

- Again, in-order issue, out-of-order execution, completion

Compare to Scoreboard Cycle 62

Instruction status

Instruction		j	k	Issue	Read operand	Executi comple	Write Result
LD	F6	34+	R2	1	2	3	4
LD	F2	45+	R3	5	6	7	8
MULT	F0	F2	F4	6	9	19	20
SUBD	F8	F6	F2	7	9	11	12
DIVD	F10	F0	F6	8	21	61	62
ADDD	F6	F8	F2	13	14	16	22

Functional unit status

Time	Name	Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
	Integer	No								
	Mult1	No								
	Mult2	No								
	Add	No								
0	Divide	No								

Register result status

Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
62	FU									

- Why takes longer on Scoreboard/6600?