ELEC3500 - Xilinx Project Navigator Tutorial.

This tutorial is valid for Xilinx Project Navigator (ISE), ModelSim, Spartan6

Starting Xilinx Project Navigator

To start the Xilinx Project Navigator, click on the Start menu and select:

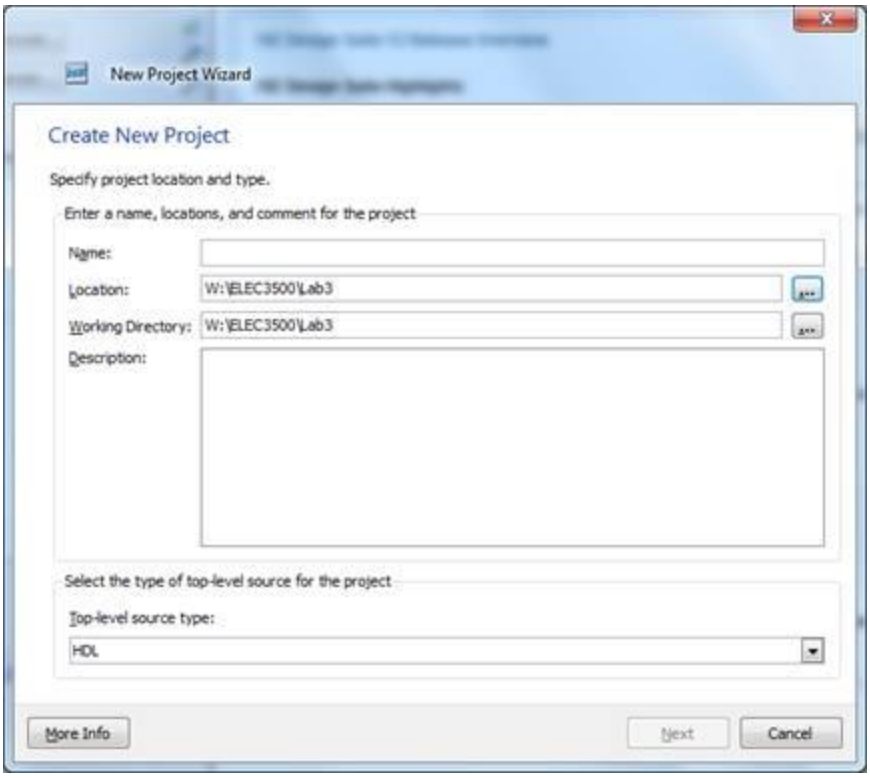
→ All Programs → Xilinx ISE Design Suite → ISE Design Tools → 32bit Project Navigator

Creating a new project

You will need to create a project for your design which can be done by choosing:

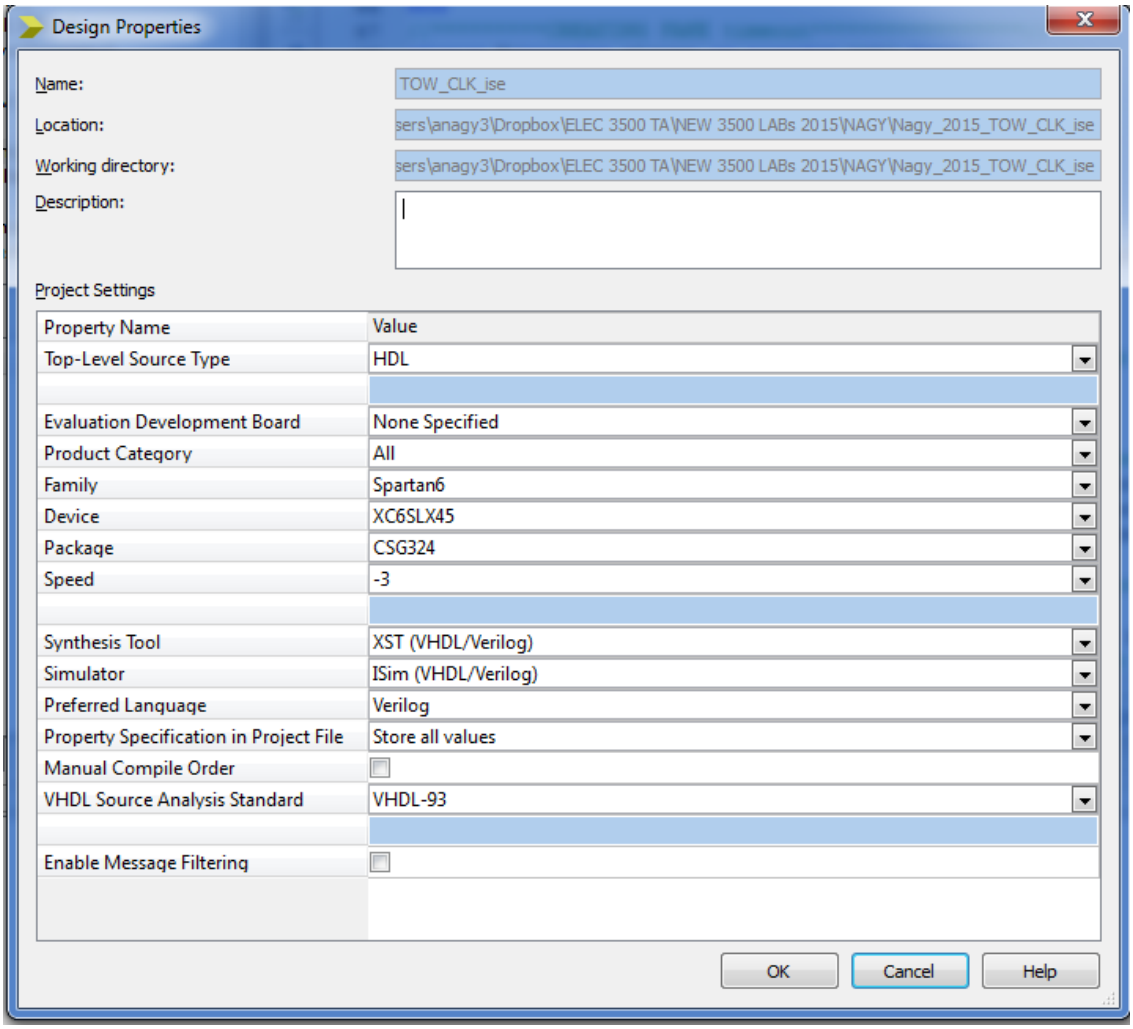
→ File → New Project…

The following window will open.



1. Name: Enter a project name (eg. Lab3).
2. Location: Select a project location on your W: drive (eg: W:\Elec3500\Lab3). Any directories will be built automatically.
3. Select HDL for the "Top-Level Source Type:"
4. Click Next.

Fill in the device information as shown in the figure below.



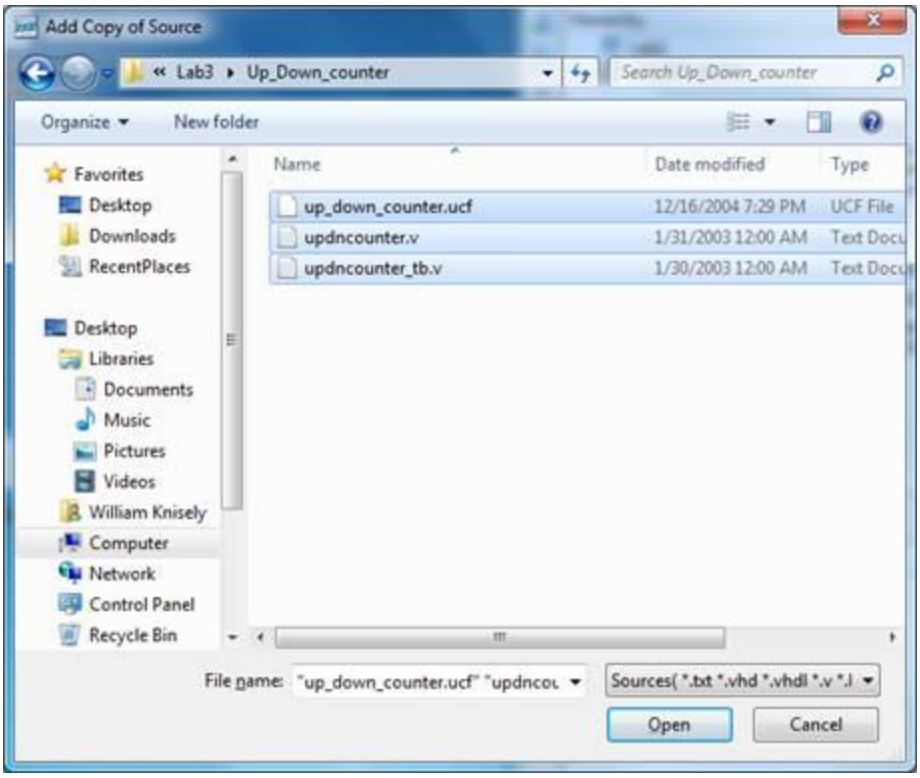
Click "Next" and review the settings to ensure they are correct.

Then.

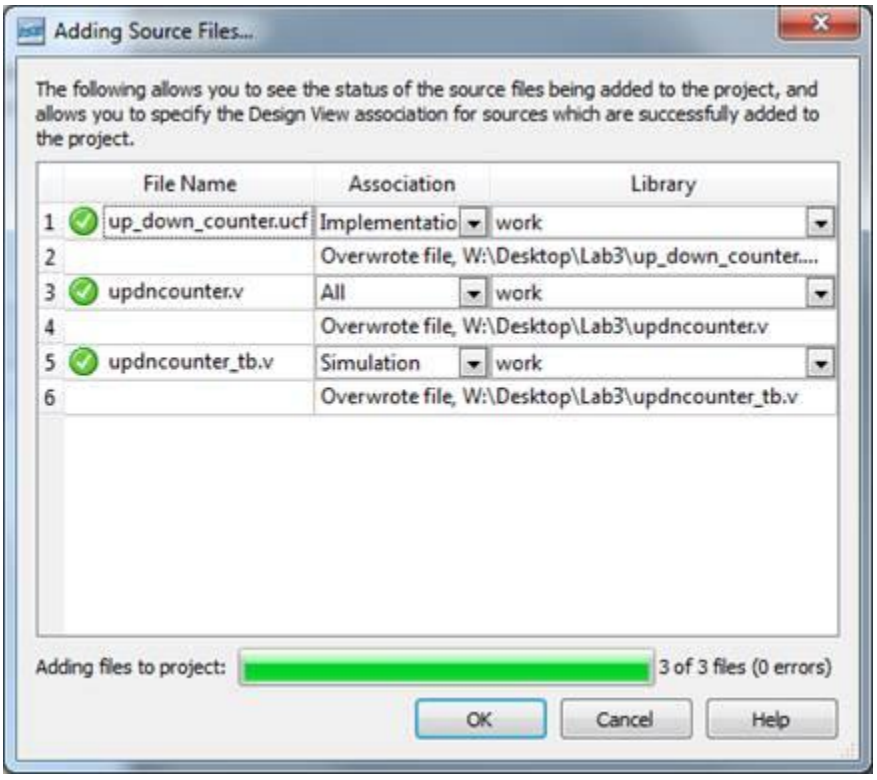
Click Finish.

The ISE Project Navigator window will be now active:

1. In the Design Panel under the Hierarchy view, right click the window. Select "Add Copy of Source…"
2. In the window that opens, shown below, navigate to P:\CourseNotes\ELEC3500\Lab3\Up_Down_counter
3. While holding the Ctrl key, select all 3 files.
4. Click Open.



The following window will open.

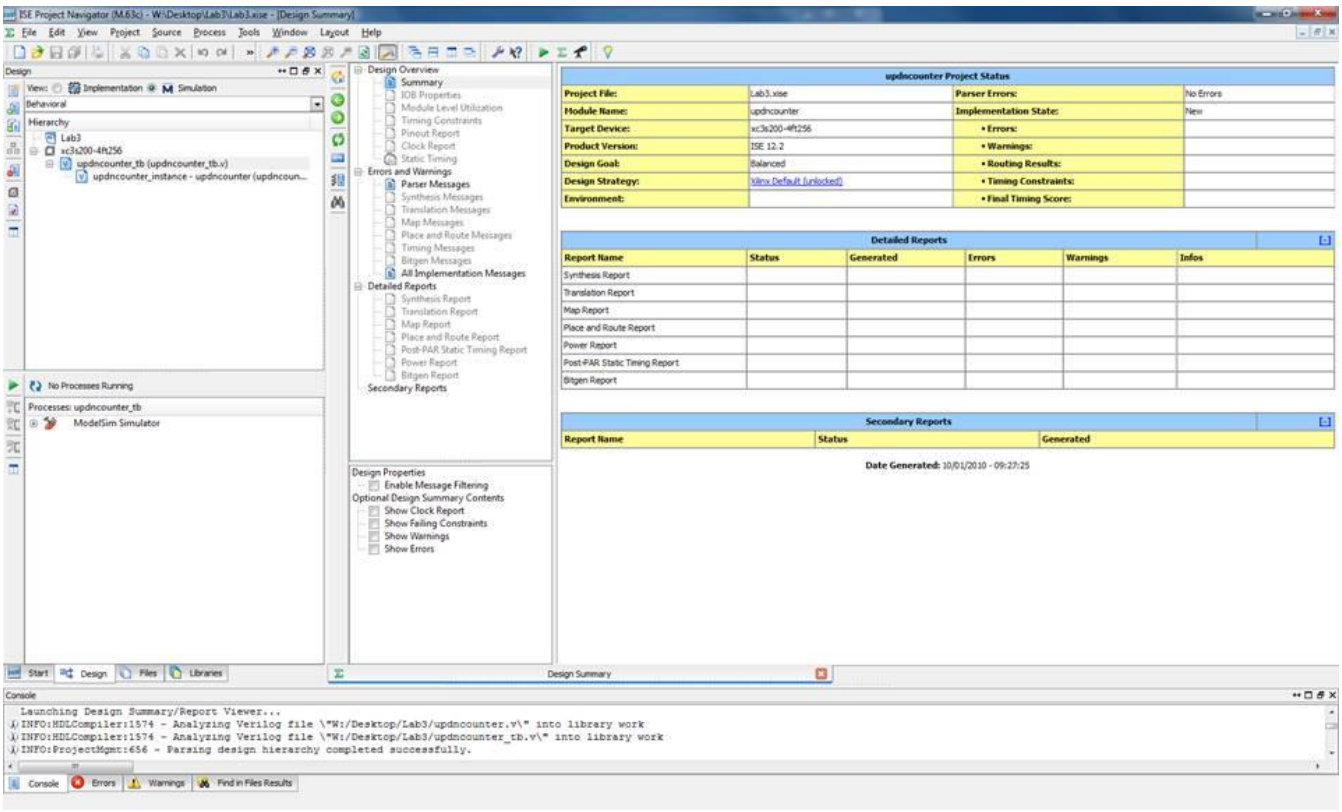


Ensure the entries are the same and click OK.

Note: When adding other files test benches should have a Simulation association, modules should be associated with All, and UCF files with Implementation.

Using ISE

The Project Navigator should look like the figure below:

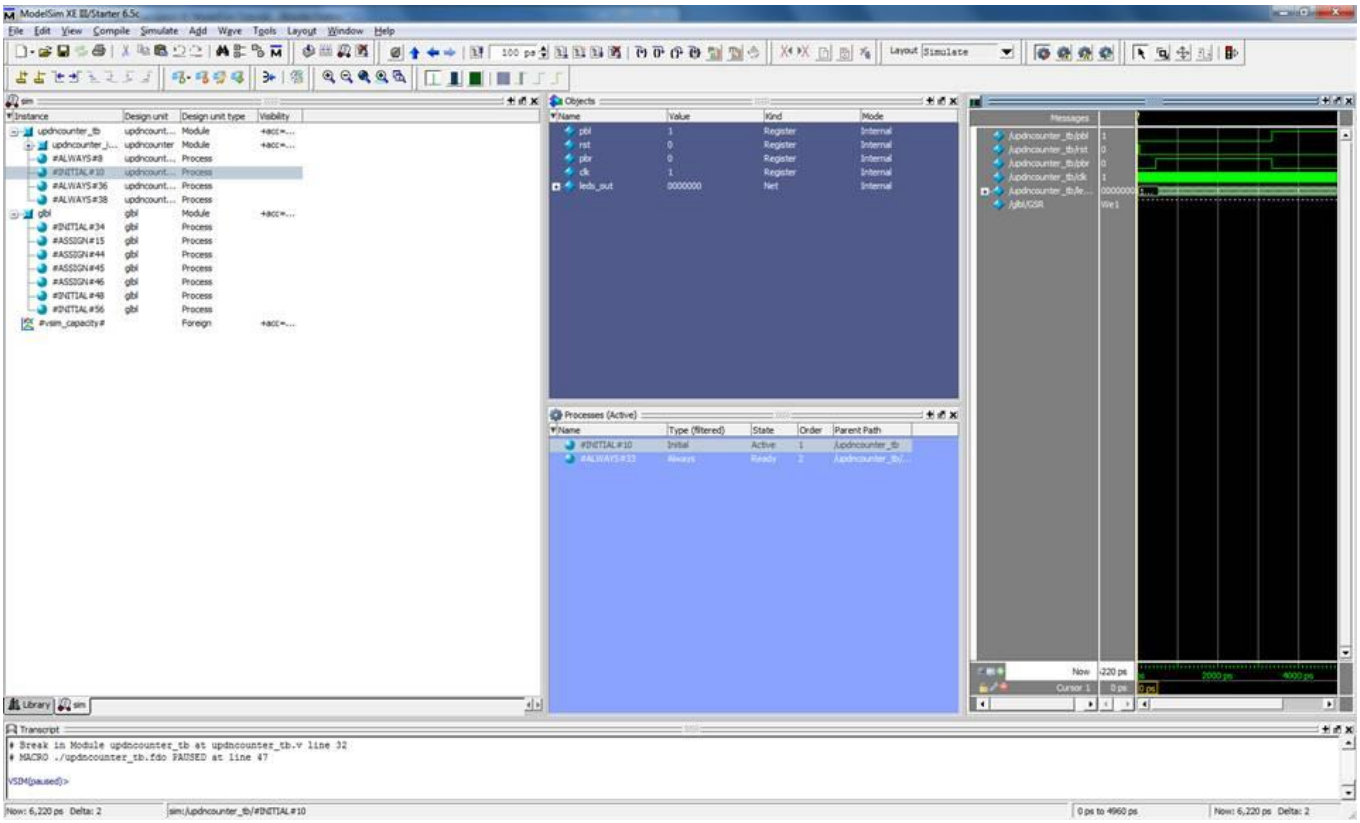


Behavioural Simulation of the design

You will simulate the design from the Project Navigator using ModelSim.

1. In the Design Panel, select the Simulation view.
2. From the drop down menu below the Simulation radial button, select Behavioural.
3. In the project Hierarchy pane select updncounter_tb (updncounter_tb.v).
4. In the Processes frame, double click Simulate Behavioral Model or click the Play button.

This will launch the ModelSim simulator to simulate your design. Several windows should open up.
ModelSim may request to associate files with ModelSim. Say **Yes**.
A dialog box will open and ask if you would like to finish. Click **No.**



The "wave" window displays the simulated waveforms. There are several buttons to change the zoom on the waveforms:

-  zoom out full
-  zoom out
-  zoom in
-  zoom to a box

Simulating the remaining cases

The default test bench only covers some cases. You will need to add the remaining cases.
You can edit the file in the Project Navigator text editor:

1. In the project Hierarchy frame, double-click on the test bench updncounter_tb (updncounter_tb.v) to open the text editor.
2. Make sure you save the changes to your test bench file after you have changed it.
3. Close the ModelSim program before running another simulation. You can only have one copy of ModelSim open at a time.
4. Re-simulate your design to verify that it works correctly.

Gate Level Simulation of the Design

Behavioural simulation results are based on the description of the circuit's operation in the verilog code. It does not simulate actual hardware operation. To do this you must run a gate level simulation:

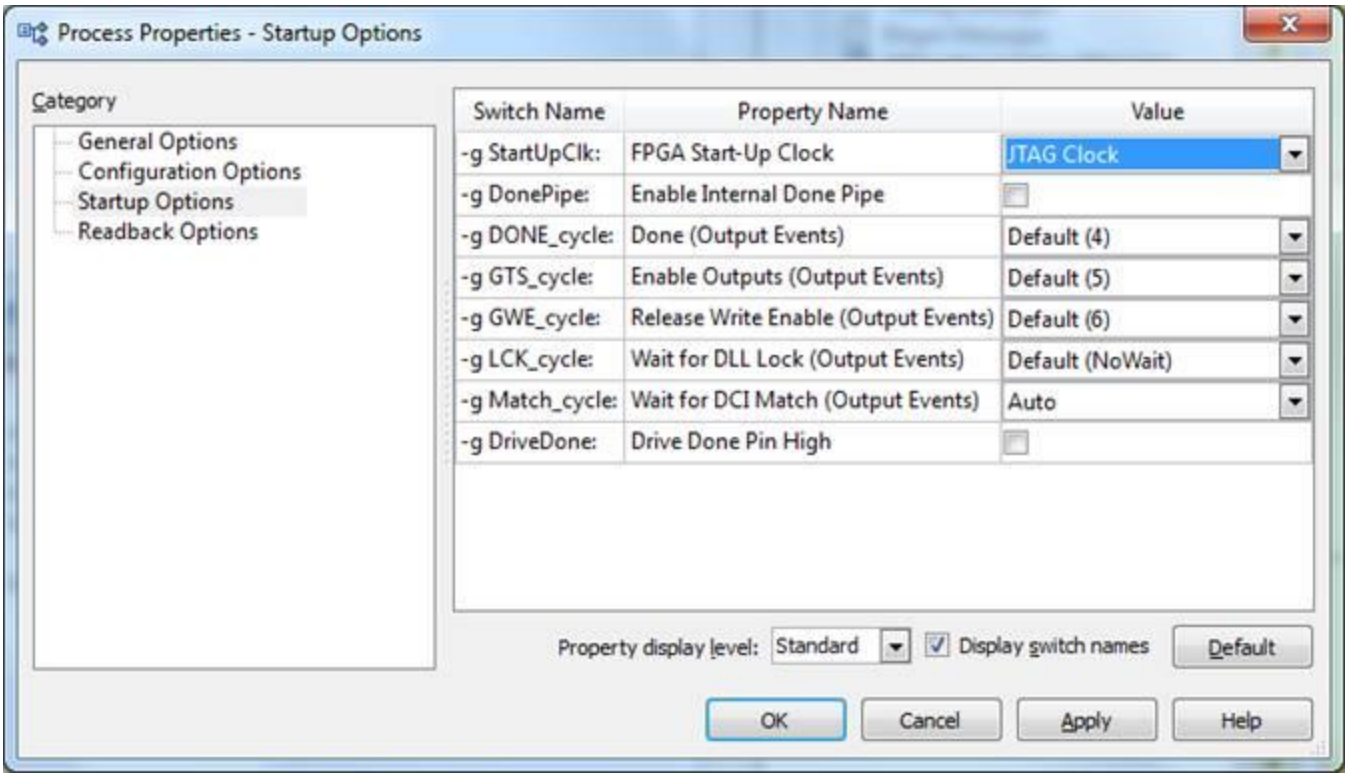
1. In the Design Panel, select the Simulation view.
2. From the drop down menu below the Simulation radial button, select Post-Route.
3. In the project Hierarchy pane select updncounter_tb (updncounter_tb.v).
4. In the Processes frame, double click Simulate Post-Place & Route Model or click the Play button.

Note that ISE will automatically synthesize the implementation/netlist files as well as perform other functions such as mapping and routing. You can see this in the Implementation pane by the green check marks indicating successful completion of each function. The gate level design will then be simulated in ModelSim. This may take somewhat longer than the behavioural simulation as the actual circuit is being simulated (not just its behavior).

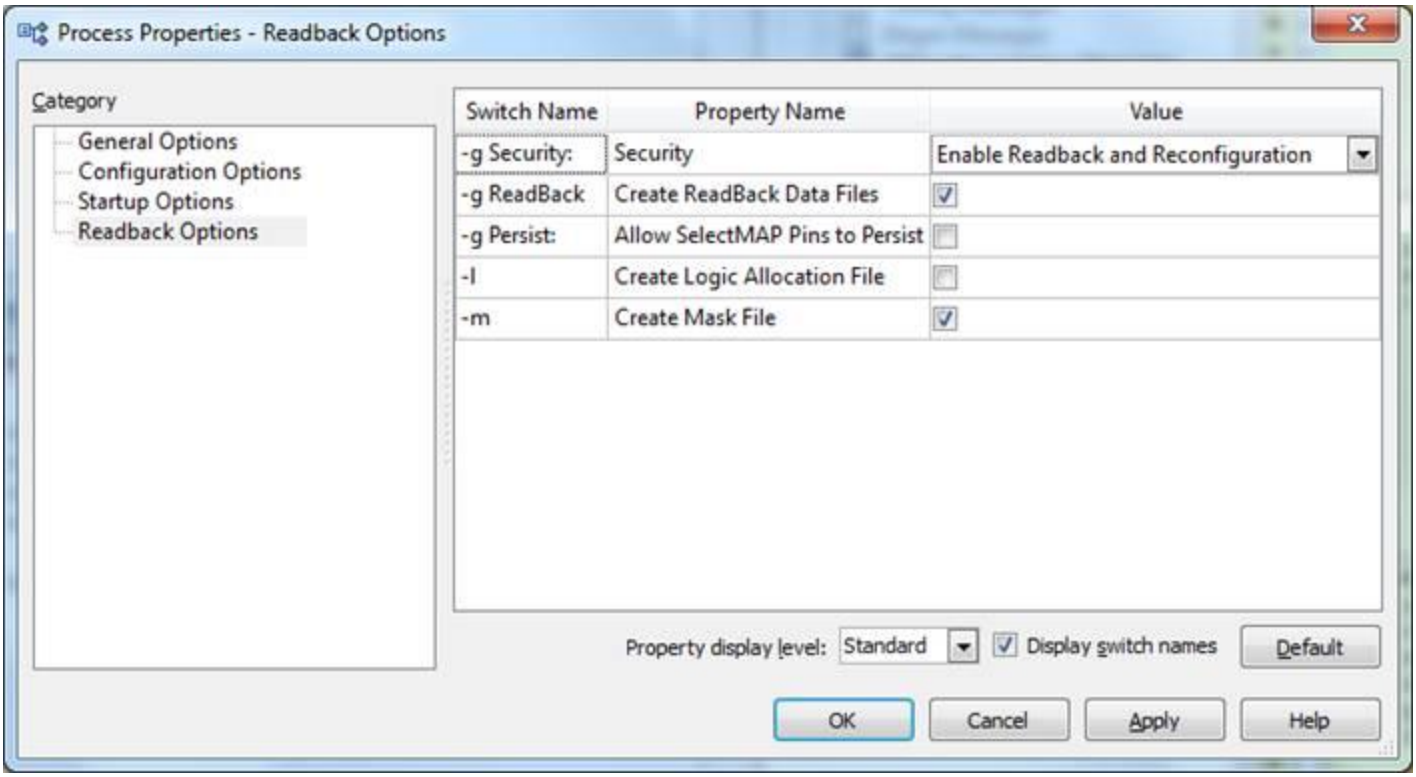
iMPACT Device Configuration

When creating a new project, JTAG configuration must be selected. This is done once.

1. Select the Implementation view at the top of the Design Panel.
2. In the Design Panel under Processes, right click Generate Programming File and select Process Properties.
3. On the left select Startup Options
4. In FPGA start-up clock, choose JTAG Clock as shown below.



5. Select Readback Options on the left.
6. Check the Create Readback Data Files and Create Mask File checkboxes as shown below.



7. Click OK when done.

About the Readback Options.

By default, ISE does not create the necessary supporting files to enable the Verify option during device programming.

It is not necessary to Verify during programming and doing so will slow down the configuration process.

If you want to use the Verify options, it is necessary to generate the appropriate files as indicated above.

Bit File Generation

In order to implement your circuit on the Spartan III FPGA, a bit file must be generated. This file contains the information necessary to program the FPGA with your circuit.

1. In the Design Panel, select the Implementation view.
2. Click on the top level module (updncounter.v).
3. In the Processes pane, double click the Generate Programming File.

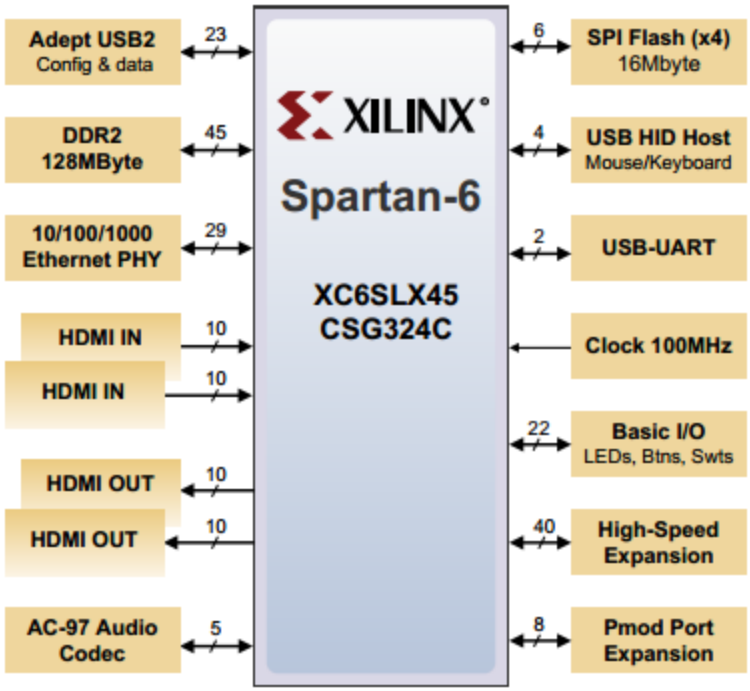
4. A .bit file that is named the same as the top level module will be created in the project directory. This is the file needed to program the FPGA.

Downloading to the Spartan 6 FPGA

To program the Atlys FPGA:

1. Run: → All Programs → Xilinx ISE Design Suite → ISE Design Tools → 64bit → iMPACT OR go to Menu item Tools>iMPACT
2. Click No or Cancel all windows that open within iMPACT.
3. Double click Boundary Scan on the left.
4. Right click the window and select Initialize Chain.
5. Double click the XC3S200 (left one). An assign new configuration file window should open. Select your .bit file.
6. Right click the XC3S200 and click program.
7. Click OK and choose defaults for all following windows.

The FPGA should now be programmed.



Notes:

- If your design was not successful, you must make your changes in the ISE, re-generate the .bit file, and re-program the FPGA.
- If your simulation was correct, but the lights don't blink (ie: they blink very fast, or are solid), the clock to the FPGA may be set too fast. You can slow down the frequency of the Hewlett Packard Arbitrary Function Generator (ARB). Please note that the BNC cable should be connected to the **SYNC out** of the ARB.
- To erase the FPGA, turn off the power using the ON/OFF switch of the FPGA board located on the top left.

Implementation Configuration Files (.ucf)

Note that Xilinx ISE cannot generate the .bit file without the .ucf file. The .ucf file contains the information necessary to map the netlist of your circuit to that of the actual hardware (FPGA) being used. In other words, it answers the question: “What pins on the FPGA correspond to the pins of your top level module?”. In addition, it is necessary to ensure that the netlist names of your top level module’s pins are all correctly represented in the .ucf file.