CS 61C Fall 2016
Guerrilla Section 3: Logic and SDS

Problem 1:

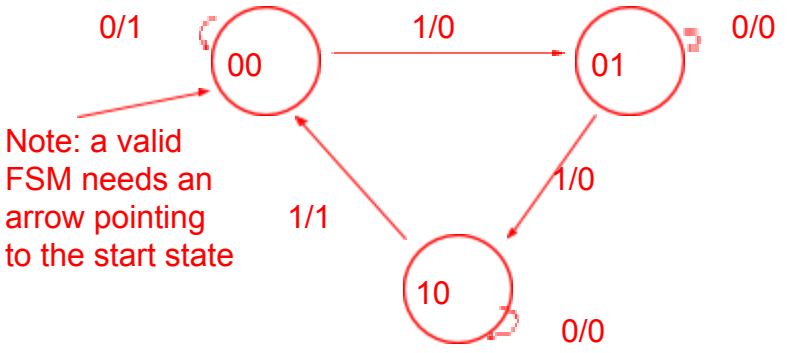
a) Convert the following truth table to a Boolean expression and simplify it. An X means we don't care about the value of that output (it can be either 0 or 1).

A	B	C	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	X
1	1	1	X

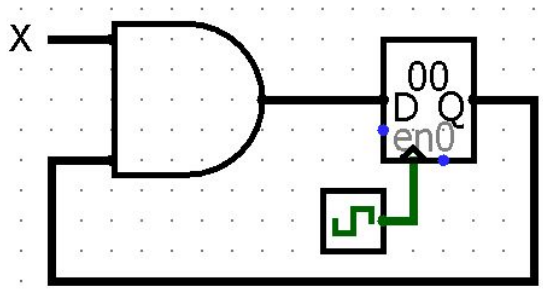
The trick is to set the output of the last 2 rows to 1.
Then we get:
!ABC + A!B!C + AB!C + ABC
So we can group terms 1 and 4 and terms 2 and 3:
=BC(!A + A) + A!C(!B + B)
=BC + A!C
This solution uses 4 gates (2 AND, 1 OR, 1 NOT).

b) Draw the transition state diagram from a FSM that reads a binary string bit-by-bit and outputs whether the total number of 1s seen since the beginning is divisible by 3.

State = (number of 1s seen) % 3



c) For the circuit below, assume that the setup time is 15ns, hold time is 30ns, and the AND gate delay is 10ns. If the clock rate is 10 MHz and x updates 25ns after the rising edge of the clock, what are the minimum and maximum values for the clk-to-Q delay to ensure proper functionality?



Min: _____20_____ns

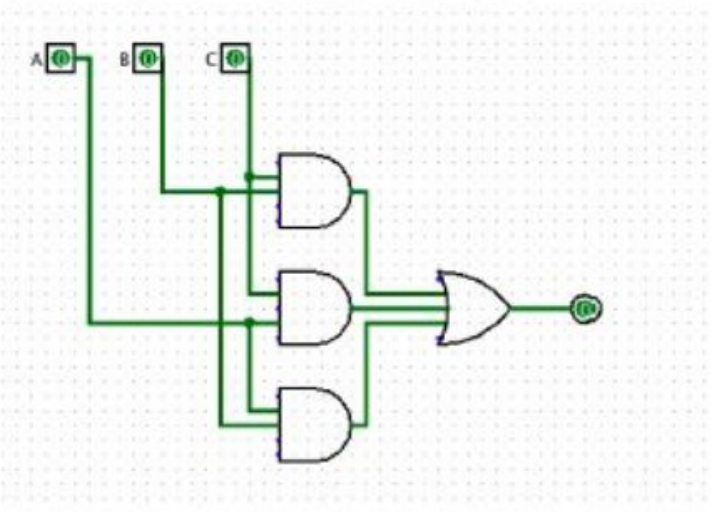
Max: _____75_____ns

If the clk-to-Q delay is too fast, the input to the register will change before the hold time is finished. Thus, the minimum clk-to-Q delay is $t_{hold} - t_{AND} = 30 - 10 = 20$ns.

On the other hand, we must make sure the critical path is no longer than the clock period, which is 100 ns (= 1/(10 MHz)). In other words, $t_{setup} + t_{AND} + t_{clk\text{-}to\text{-}Q} \leq 100$ns, or $t_{clk\text{-}to\text{-}Q} \leq 100\text{ns} - t_{setup} - t_{AND}$. Solving yields $t_{clk\text{-}to\text{-}Q} \leq 75$ ns.

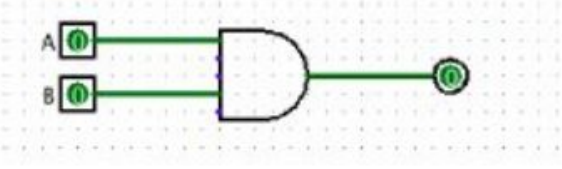
d) Build a 3-bit majority circuit (outputs 1 if 2 or more bits are 1 otherwise outputs 0).

A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



e) Reduce the Boolean expression AB + ABC + ABCD + ABCDE + ABCDEF and draw the logic gate.

AB



f) Reduce the Boolean expression !(A + !B) * !(C + D + E) + (A + B)*(!C). How many gates needed?

!A*B*!C*!D*!E + A*!C + B*!C = B*!C*(!A*!D*!E + 1) + A*!C = B*!C + A*!C = (!C)*(B + A)
3 gates (1 not, 1 and, 1 or)

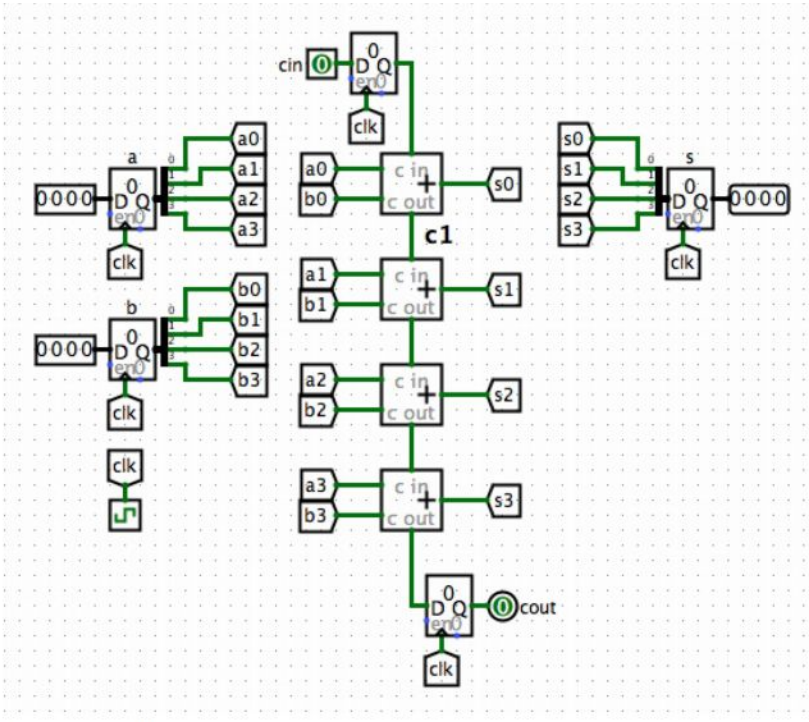
Problem 2 (Fa15 Midterm 2):

Consider the 4-bit adder shown to the right
It takes:

- a carry in (`cin`)
- two four-bit inputs:
  - *a* with bits `a0, a1, a2, a3`
  - *b* with bits `b0, b1, b2, b3`

Outputs:

- a carry out (`cout`)
- one four-bit output:
  - *s* with bits `s0, s1, s2, s3`



Assume each adder has a delay of 10ns, and any registers have a clk-to-q, hold time, and setup time of 5ns. Assume the inputs are driven by registers, and outputs are registers as well.

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1. Write Boolean formulas for `s0` and `c1` in terms of the inputs `cin`, `a0`, and `b0`. You may use XOR as an operator in the Boolean formulas. Each formula should use as few operators as possible.

`s0 = a0 XOR b0 XOR cin`
`c1 = cin * (a0 XOR b0) + a0 * b0`

2. What is the critical path delay of the circuit? Please include proper units in your answer.

`50ns = clk-to-q + 4 adders + setup time`

3. What is the maximum clock frequency at which the circuit will function correctly? Please include proper units in your answer.

`20 MHz = 1/50 ns`

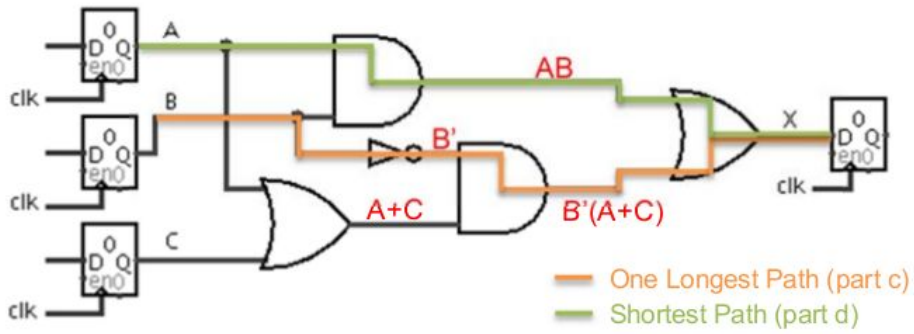
4. What is the maximum hold time the output registers could have at which the circuit would still function correctly?

`15 ns`
`The result for s0 arrives in 15ns, so if it was greater, the hold time would be violated by the second set of inputs`

FB.
N

Problem 3 (Su16 Midterm 2):

Consider the circuit below for the following questions. Logical gates incur a 10 ns combinational logic delay. Registers have a CLK-to-Q delay of 5 ns and a setup time constraint of 15 ns.



A	B	C	X
0	0	0	**0**
0	0	1	**1**
0	1	0	**0**
0	1	1	**0**
1	0	0	**1**
1	0	1	**1**
1	1	0	**1**
1	1	1	**1**

a) Write the boolean expression for X in terms of A, B, and C. Only use the AND, OR and NOT logical operators, and leave the expression in its UNSIMPLIFIED form. (You are welcome to use the provided truth table, but it is **NOT** required and **NOT** graded.) [3 pts]

$X = AB + \bar{B}(A + C)$ [propagate signals along wires]
$X = \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC$ [truth table, then Sum of Products]
$X = A + \bar{A}\bar{B}C$ [truth table with visual simplification]

b) Given the following boolean expression for a different circuit, simplify it to use the fewest possible AND, OR, and NOT logical operators. [3 pts]

$$x = \overline{a + \bar{d}} + a \cdot \bar{d} + \bar{b} \cdot \bar{c}$$

$x = \bar{a} \cdot \bar{\bar{d}} + a \cdot \bar{d} + \bar{b} \cdot \bar{c}$ DeMorgan's Law
$x = \bar{d}(\bar{a} + a) + \bar{b} \cdot \bar{c}$ distribution
$x = \bar{d}(1) + \bar{b} \cdot \bar{c}$ complementarity
$x = \bar{d} + \bar{b} \cdot \bar{c}$ identity (3 NOT, 1 AND, 1 OR)
$x = \bar{d} + \overline{b + c}$ DeMorgan's Law (2 NOT, 2 OR)
$x = \overline{d(b + c)}$ DeMorgan's Law (1 NOT, 1AND, 1 OR)

c) For the circuit above (part a), calculate the minimum clock period that will allow the circuit to function correctly. Remember to include units.
[2 pts]

Minimum clock period (max clock frequency) is the setup time condition. The critical path is through three gates (either B through NOT, AND, OR or C throught OR, AND, OR).
We need $t_{CLK-to-Q} + 3 * t_{logic} \leq t_{period} - t_{setup}$, so we arrive at $5ns + 3 * 10ns \leq t_{period} - 15ns$.
Solving, we get $t_{period,min} = 50ns$.

d) Assuming the hold time constraint of the registers is 20ns, calculate the minimum combinational logic delay needed per logic gate to allow the circuit (part a) to function correctly. Remember to include units. [2 pts]

Shortest path for X to change is A through top AND and then OR.
We need $t_{hold} \leq t_{CLK-to-Q} + 2 * t_{logic}$, so we arrive at $20ns \leq 5ns + 2 * t_{logic}$.
Solving, we get $t_{logic,min} = 7.5ns$.