# CS 61C Fall 2016
Guerrilla Section 3: Logic and SDS

Problem 1:

a) Convert the following truth table to a Boolean expression and simplify it. An X means we don't care about the value of that output (it can be either 0 or 1).

A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	X
1	1	1	X

b) Draw the transition state diagram from a FSM that reads a binary string bit-by-bit and outputs whether the total number of 1s seen since the beginning is divisible by 3.

c) For the circuit below, assume that the setup time is 15ns, hold time is 30ns, and the AND gate delay is 10ns. If the clock rate is 10 MHz and x updates 25ns after the rising edge of the clock, what are the minimum and maximum values for the clk-to-Q delay to ensure proper functionality?

X
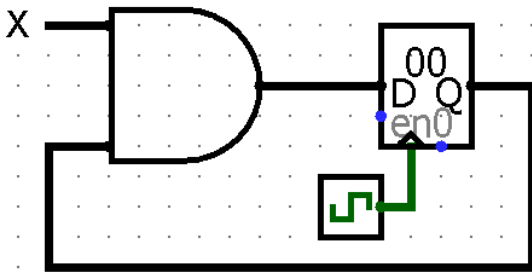
Min: _____ns

Max: _____ns

- **t_hold <= t_input <= t_clk_period - t_setup**
- **Clq_to_q + AND +setup <= clk_period**

d) Fill in the truth table for a 3-bit majority circuit and build it using logic gates. A 3-bit majority circuit outputs 1 if 2 or more bits are 1, otherwise it outputs 0.

A	B	C	Out
0	0	0	0
1	1	1	1

e) Reduce the Boolean expression AB + ABC + ABCD + ABCDE + ABCDEF and draw the logic gate.

f) Reduce the Boolean expression !(A + !B) * !(C + D + E) + (A + B)*(!C). How many and/or/not gates needed?

Problem 2 (Fa15 Midterm 2):

Consider the 4-bit adder shown to the right
It takes:

- a carry in (cin)
- two four-bit inputs:
  - a with bits a0, a1, a2, a3
  - b with bits b0, b1, b2, b3

Outputs:

- a carry out (cout)
- one four-bit output:
  - s with bits s0, s1, s2, s3

Assume each adder has a delay of 10ns, and any registers have a clk-to-q, hold time, and setup time of 5ns. Assume the inputs are driven by registers, and outputs are registers as well.

1. Write Boolean formulas for s0 and c1 in terms of the inputs cin, a0, and b0. You may use XOR as an operator in the Boolean formulas. Each formula should use as few operators as possible.

2. What is the critical path delay of the circuit?

3. What is the maximum clock frequency at which the circuit will function correctly? Please include proper units in your answer.

4. What is the maximum hold time the output registers could have at which the circuit would still function correctly? Please include proper units in your answer.
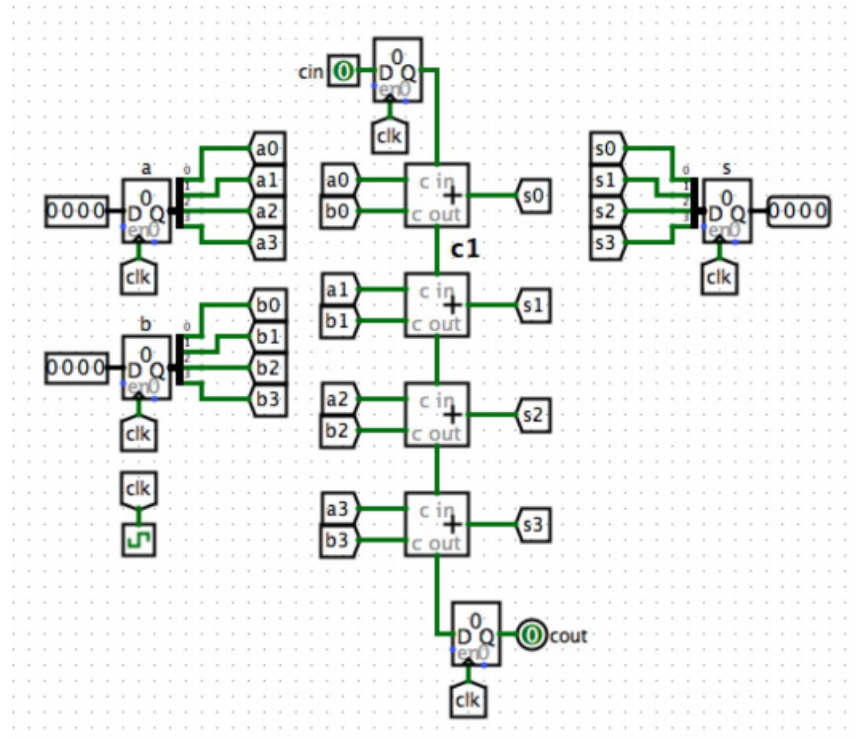
Problem 3 (Su16 Midterm 2):

Consider the circuit below for the following questions. Logical gates incur a 10 ns combinational logic delay. Registers have a CLK-to-Q delay of 5 ns and a setup time constraint of 15 ns.
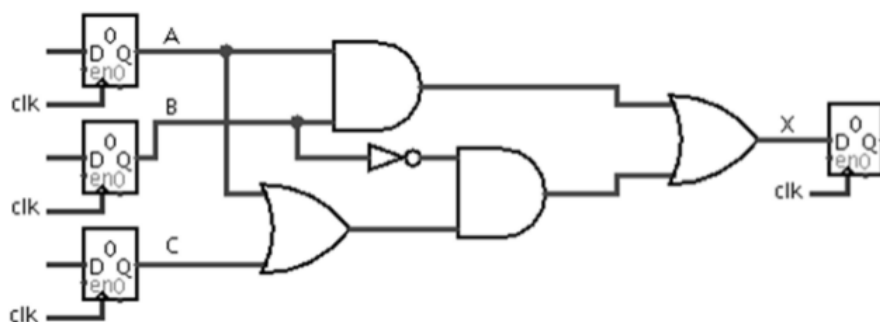
A	B	C	X
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

a) Write the boolean expression for X in terms of A, B, and C. Only use the AND, OR and NOT logical operators, and leave the expression in its UNSIMPLIFIED form. (You are welcome to use the provided truth table, but it is **NOT** required and **NOT** graded.)

b) Given the following boolean expression for a different circuit, simplify it to use the *fewest* possible AND, OR, and NOT logical operators.

$$x = \overline{a + d} + a \cdot \bar{d} + \bar{b} \cdot \bar{c}$$

c) For the circuit above (part a), calculate the minimum clock period that will allow the circuit to function correctly. Remember to include units.

e) Assuming the hold time constraint of the registers is 20 ns, calculate the minimum combinational logic delay needed per logic gate to allow the circuit (part a) to function correctly. Remember to include units.