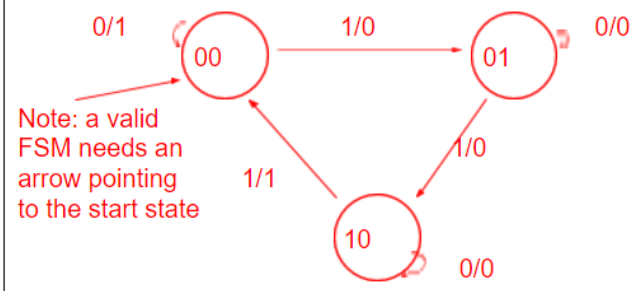
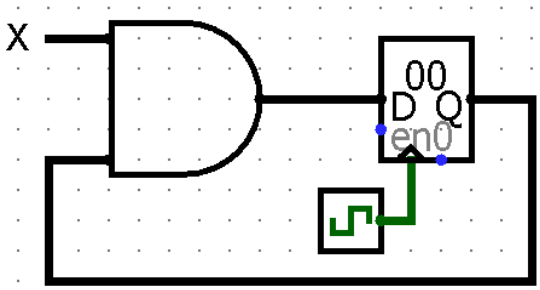
b) Draw the transition state diagram from a FSM that reads a binary string bit-by-bit and outputs whether the total number of 1s seen since the beginning is divisible by 3.

State = (number of 1s seen) % 3



For the circuit below, assume that the setup time is 15ns, hold time is 30ns, and the AND gate delay is 10ns. If the clock rate is 10 MHz and x updates 25ns after the rising edge of the clock, what are the minimum and maximum values for the clk-to-Q delay to ensure proper functionality?



Min: _____20_____ns

Max: _____75_____ns

If the clk-to-Q delay is too fast, the input to the register will change before the hold time is finished. Thus, the minimum clk-to-Q delay is $t_{hold} - t_{AND} = 30 - 10 = 20$ns.

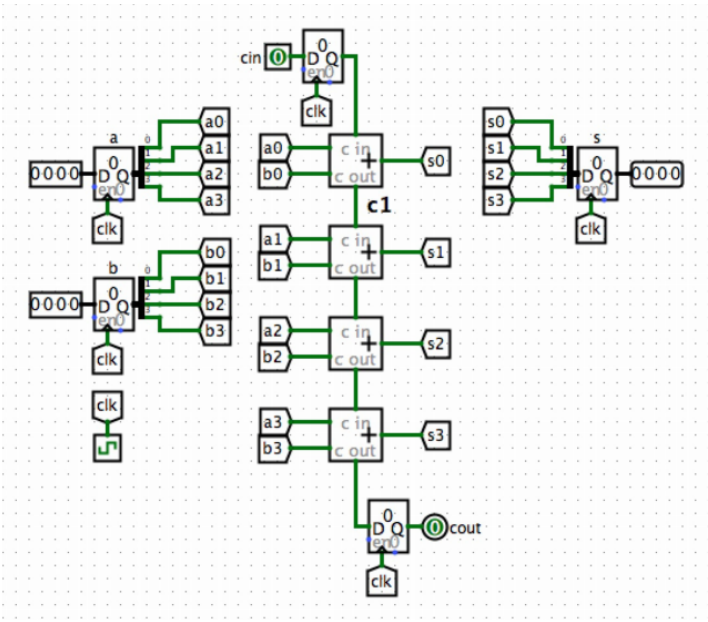
On the other hand, we must make sure the critical path is no longer than the clock period, which is 100 ns (= 1/(10 MHz)). In other words, $t_{setup} + t_{AND} + t_{clk\text{-}to\text{-}Q} \leq 100$ns, or $t_{clk\text{-}to\text{-}Q} \leq 100\text{ns} - t_{setup} - t_{AND}$. Solving yields $t_{clk\text{-}to\text{-}Q} \leq 75$ ns.

Consider the 4-bit adder shown to the right
It takes:

- a carry in (`cin`)
- two four-bit inputs:
  - *a* with bits `a0, a1, a2, a3`
  - *b* with bits `b0, b1, b2, b3`

Outputs:

- a carry out (`cout`)
- one four-bit output:
  - *s* with bits `s0, s1, s2, s3`



Assume each adder has a delay of 10ns, and any registers have a clk-to-q, hold time, and setup time of 5ns. Assume the inputs are driven by registers, and outputs are registers as well.

Assume each adder has a delay of 10ns, and any registers have a clk-to-q, hold time, and setup time of 5ns. Assume the inputs are driven by registers, and outputs are registers as well.

1. Write Boolean formulas for `s0` and `c1` in terms of the inputs `cin`, `a0`, and `b0`. You may use XOR as an operator in the Boolean formulas. Each formula should use as few operators as possible.

`s0 = a0 XOR b0 XOR cin`
`c1 = cin * (a0 XOR b0) + a0 * b0`

2. What is the critical path delay of the circuit? Please include proper units in your answer.

`50ns = clk-to-q + 4 adders + setup time`

3. What is the maximum clock frequency at which the circuit will function correctly? Please include proper units in your answer.

`20 MHz = 1/50 ns`

4. What is the maximum hold time the output registers could have at which the circuit would still function correctly?

`15 ns`
`The result for s0 arrives in 15ns, so if it was greater, the hold time would be violated by the second set of inputs`

4a. 3

b. 2

c. 1

3. Generate the control signals for **movz**. The values should be 0, 1, or X (don't care) terms. You must use don't care terms where possible.

MOVZ	RegDst	ExpOp	RegWr	ALUSrc	ALUCtr	MEMWr	MemToReg	Jump	Branch
1	1	X	0	0	0001, 0010, or 0110	0	X	0	0

This table shows the ALUCtr values for each operation of the ALU:

Operation	AND	OR	ADD	SUB	SLT	NOR
ALUCtr	0000	0001	0010	0110	0111	1100