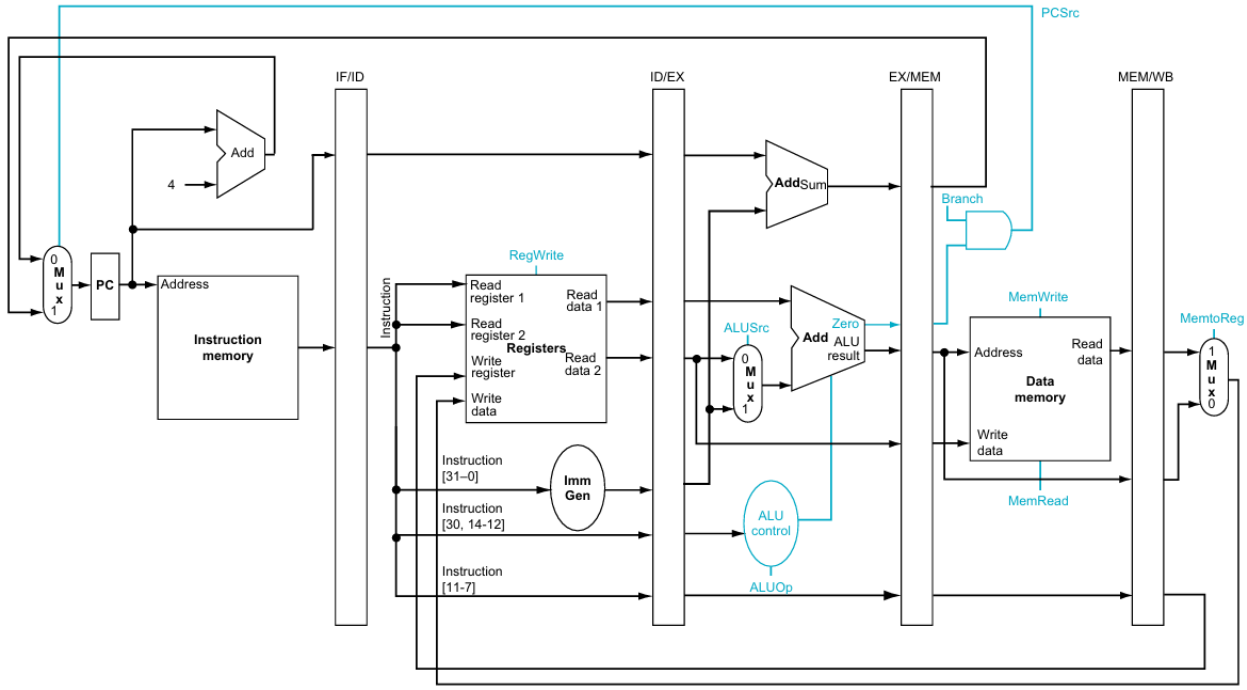
Project Phase 2 Report: Five Stage Processor

This document includes the schematic for the five-stage pipelined processor, a results comparison of the single stage and five stage pipelined processor implementation, and a discussion of optimizations or features to be added to improve performance.

Schematic:

The code implementation of the Five Stage Core class follows the figure "Pipelined Datapath," displayed below, from the "Computer Organization and Design" textbook by Patterson and Hennessy. Minor changes were made to control signal names.



Results Comparison:

In this simulation, the single-stage processor consistently outperforms the five-stage pipelined version in both CPI and IPC due to the relatively short instruction sequences and the overhead introduced by pipeline hazards. While pipelining is theoretically designed to improve instruction throughput by overlapping stages, practical issues like data hazards, control hazards, and the cost of pipeline filling and draining result in additional cycles that degrade performance. As a result, the single-stage processor, which avoids these complexities by executing each instruction sequentially, achieves more efficient execution for small programs with frequent dependencies.

Optimizations/Additional Performance Features:

1. Implement instruction scheduling to minimize the number of cycles spent waiting by reordering instructions for better parallelism where it's applicable.

2. In a multi-core machine, using multi-threading to execute independent parts of the pipeline or multiple instructions simultaneously; one core for each instruction stream.