ENE53100: Silicon Processing Technology for Microelectronics

TCAD simulation project: SCE of NMOS

Due date: **2024/6/23 (Sunday) 23:59**

As semiconductor devices are scaled down to sub-micrometer dimensions in pursuit of Moore's Law, the Front-End-of-Line (FEOL) fabrication phase becomes critical in defining the functionality of CMOS (Complementary Metal-Oxide-Semiconductor) technology. One significant challenge in miniaturization is the Short Channel Effect (SCE), which impacts the electrical properties of transistors, such as threshold voltage and leakage currents. These changes undermine performance, power efficiency, and thermal stability.

The project focuses on simulating NMOS devices with both long and short channels and refining NMOS processes to mitigate SCE using advanced process techniques. By improving electrostatic control within transistors, this project aims to enhance the robustness, efficiency, and scalability of semiconductor devices, thereby contributing to the ongoing advancement of integrated circuit technology.

For this TCAD simulation project, your task is to:

1. Run the input file (nmos_300nm.in) for the long channel NMOS and become familiar with the NMOS fabrication process in Athena and the electrical measurements in Atlas.
2. Design and simulate a short channel NMOS device to compare with the long channel device. (the gate length should be < 90nm)
3. Then, apply advanced process techniques, such as halo implantation and retrograde well, to mitigate Short Channel Effects (SCE). Compare the short channel NMOS before and after applying these advanced techniques.
4. Finally, analyze and compare the electrical properties of the simulation result.

Your report should contain the following:

1. **I_D-V_D & I_D-V_G** Characteristic Curve:
   Comparison between **long and short** channel NMOS.
2. **I_D-V_D & I_D-V_G** Characteristic Curve:

For the short channel NMOS, before and after improvements.

3. **Device Structure Graph**: Displayed through the Tonyplot (.str file).
4. Parameter Extraction: Detailed parameter of NMOS performance metrics.
   Hint : You can extract these parameter through the tools in Tonyplot and the "extract" command in Athena & Atlas .

Parameter	Long channel NMOS	Short channel NMOS	Improved short channel NMOS
Gate length (nm)			
Source/Drain depth (μm)			
Gate oxide thickness (μm)			
Saturation slope			
I_{Dmax} (A)			
V_{TH} (V)			

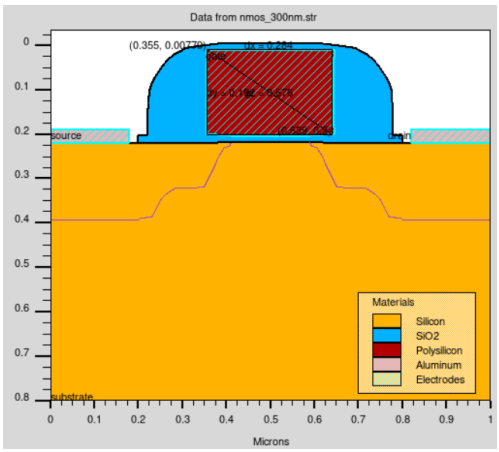
5. Analyze the short channel effects observed in your simulation results, detailing the mechanisms behind these phenomena. In your explanation, specifically highlight Drain Induced Barrier Lowering (DIBL) and channel length modulation and indicate these effects on your graphs.

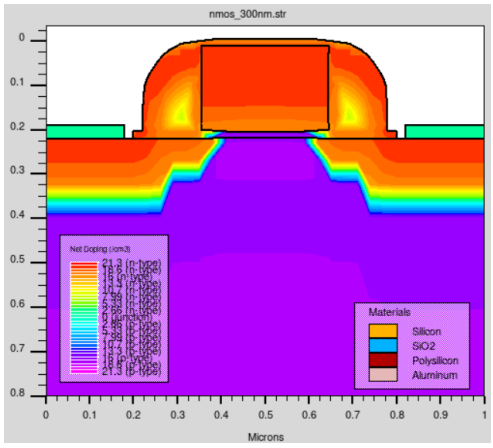
Please submit your report, and .in file with the correct file name to the eeclass platform by the deadline.

(File name format : SCE_NMOS_studentID_your_name.pdf , nmos _gate_length.in)

- For sections related to the I_dV_g curve, you can change the y-axis to a logarithmic scale to better observe the DIBL.
- You can learn the details of the extract command from the Athena & Atlas manual.
- The device graph should include the original structure , and the NET doping contour graph of your NMOS.

Ex:


Data from nmos_300nm.str
source
Materials
Silicon
SiO2
Polysilicon
Aluminum
Electrodes
substrate
Microns


nmos_300nm.str
Net Doping (/cm3)
Materials
Silicon
SiO2
Polysilicon
Aluminum
Microns