ENE53100: Silicon Processing Technology for Microelectronics

# TCAD simulation project: FEOL CMOS Fabrication

Due date: **2024/04/16 (Tuesday) 23:59**

The Front-End-of-Line (FEOL) CMOS process is a cornerstone in the fabrication of modern semiconductor devices, laying the foundational circuit elements directly on the silicon wafer. This intricate phase involves the creation of the transistor components, such as gates, source, and drain regions, which are pivotal in enabling the electrical functionality of CMOS (Complementary Metal-Oxide-Semiconductor) technology. The FEOL process encompasses several critical steps, including the deposition of gate materials, doping to adjust electrical properties, and the sculpting of silicon through photolithography and etching to define the transistor architecture.

**For the TCAD simulation project, you are tasked with finishing the FEOL CMOS process by completing the numbered steps according to the hints provided in the template code within the input file (FEOL.in file).**

To complete this task, ensure you have the following steps covered in your .str files:

(1) STI (Shallow Trench Isolation) Process:

a. Application of the STI mask.
b. Execution of the STI etching procedure.
c. Completion of STI CMP (Chemical Mechanical Polishing) and cleaning.

(2) Well Formation and Drive-In

a. Establishment of the N-well regions.
b. Establishment of the P-well regions.
c. Performance of well annealing and drive-in processes for dopant activation.

(3) Threshold Voltage (Vt) Adjustment Implantation

a. Vt adjustment implantation for N-channel devices.
b. Vt adjustment implantation for P-channel devices.

(4) Polysilicon Gate Definition

a. Deposition of polysilicon for gate formation.
b. Etching of polysilicon to define gate structures.

c. Annealing and oxidation of polysilicon to improve electrical properties.

(5) LDD (Lightly Doped Drain) Implantation

a. Implantation of phosphorus for lightly doped S/D regions in N-channel devices.

b. Implantation of boron for lightly doped S/D regions in P-channel devices.

(6) Spacer Formation

a. Deposition of nitride material for spacer formation.

b. Etching process to shape nitride into functional spacers.

(7) Source/Drain (S/D) Implantation

a. Heavy doping of S/D regions with arsenic for N-channel devices.

b. Heavy doping of S/D regions with boron for P-channel devices.

c. Formation of contact areas using aluminum for metal interconnections.

By following these steps in your simulation and visualization with Tonyplot, you'll be able to accurately depict the complex series of events that characterize the FEOL portion of CMOS device fabrication!

Please use **Tonyplot** to display the FEOL CMOS process by opening the .str files generated by **Athena**. These files represent the structural outcomes from key stages in the fabrication of CMOS devices.

## Reference Process parameters

| | |
|---|---|
| $L_{ch}$ | 1 ~ 0.8 μm |
| N/P-well | $10^{12}$ ~$10^{13}$ $cm^{-2}$ |
| $V_t$ adjust implantation | $10^{11}$ ~$10^{12}$ $cm^{-2}$ |
| Lightly Doped Drain ( LDD ) | $10^{13}$ ~$10^{14}$ $cm^{-2}$, |
| Heavily doped S/D | $10^{15}$ ~$10^{16}$ $cm^{-2}$ |

**Please submit your report, and .in file with the correct file name to the eeclass platform by the deadline. (File name format : FEOL_CMOS_studentID_your name.pdf , FEOL_CMOS_studentID.in )**

In your report ( **.pdf ), please provide the followings:

Process Description: Explain the process briefly.

Simulation Results: Display your simulation results for the process.

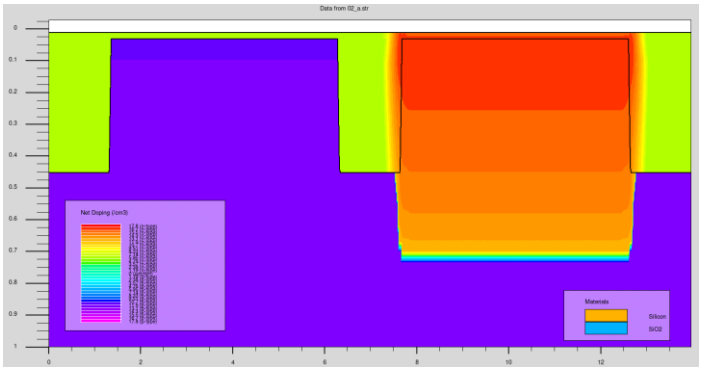
After finishing the construction of the CMOS device structure, please compare the process in this TCAD simulation with the standard CMOS process outlined in Chapter 2.

Ex:

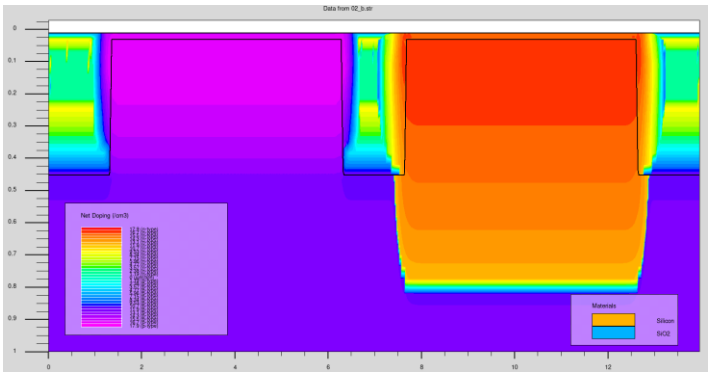
(2) Well Formation and Drive-In:

The process begins with the creation of N-well and P-well regions in the silicon substrate. These wells serve as the foundation for the N-type and P-type transistors in CMOS technology, respectively.

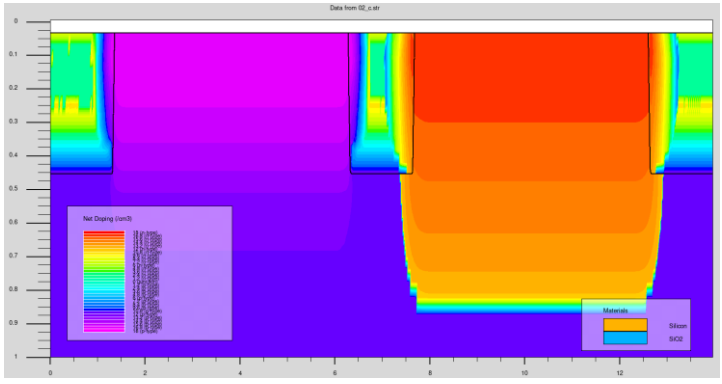
a. Define N-well:



b. Define P-well:



c. Well annealing and drive-in:



- For sections related to doping, use the "Display-Contours" option from the top menu to show "Net doping." **Otherwise, that part will not be considered for grading**.

- Please note that the execution time is lengthy. Ensure you run it when your internet connection is stable and disable your computer's automatic sleep function; otherwise, Deckbuild may disconnect.

- To continue a simulation from where you left off without needing to rerun the previous parts, you can follow these steps after completing a segment, such as "07_b". First, open a new Deckbuild file from the "File" menu. Then, to resume your simulation from the saved state file you've reached, use the **initialize** command with the **infile=** option pointing to your last saved state file. Remember to place both input files in the same directory to ensure the figures are easily accessible. Below is how you can proceed:

  (In deckbuild)
  go athena
  **initialize infile=07_b.str**
  # Concisely define your simulation parameters.
  set STI=1.32
  set Lg=1
  set Lsd=1
  set Ldd=1
  set Tpoly=-1.82
  Set NMOS=$"STI"+($"Lsd"*2)+($"Ldd"*2)+$"Lg"
  #Continue with your simulation steps. For instance, if you're about to deposit aluminum, you can proceed with the corresponding commands for that process.
  #Deposit aluminum
  ……
  quit

  Ensure both input files are in the same folder to maintain consistency in your simulation environment, especially for finding figures or other referenced files. This method allows you to efficiently continue your work from a specific point without rerunning the entire simulation, saving time and computational resources.