

Course name- Product Design Thinking and Framework

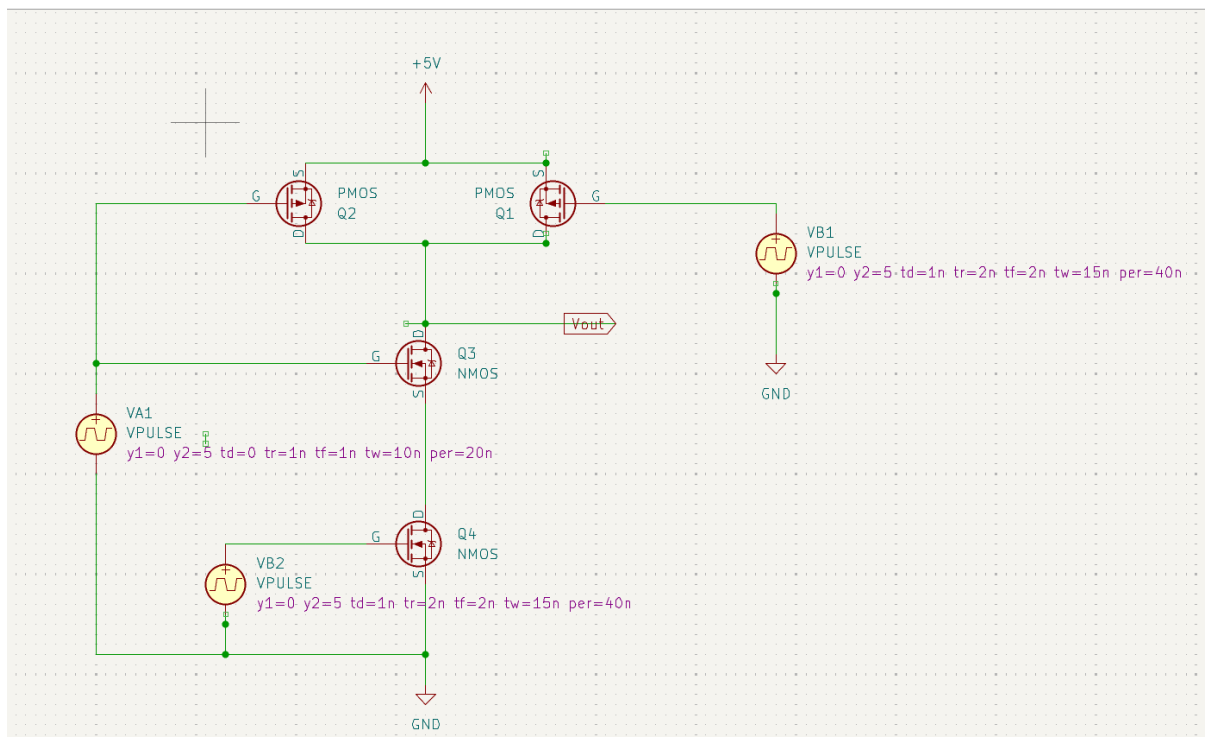
Collage – Quantum University

Batch Number- 01

Project Statement 4 , part (b)

Construct and simulate a NAND gate using MOS transistors, infer its behaviour, and explain its truth table with logical operation.

Circuit:



Values:

TRAN — Transient Analysis

SPICE Command

Plot Setup

Time step:

2n

seconds

Final time:

40n

seconds

Initial time:

0

seconds (optional; default 0)

Max time step:

800p

seconds (optional; default min{tstep, (tstop-tstart)/50})

☒ Use initial conditions

☒ Add full path for .include library directives

☒ Save all voltages

☒ Save all currents

☒ Save all power dissipations

☒ Save all digital event data

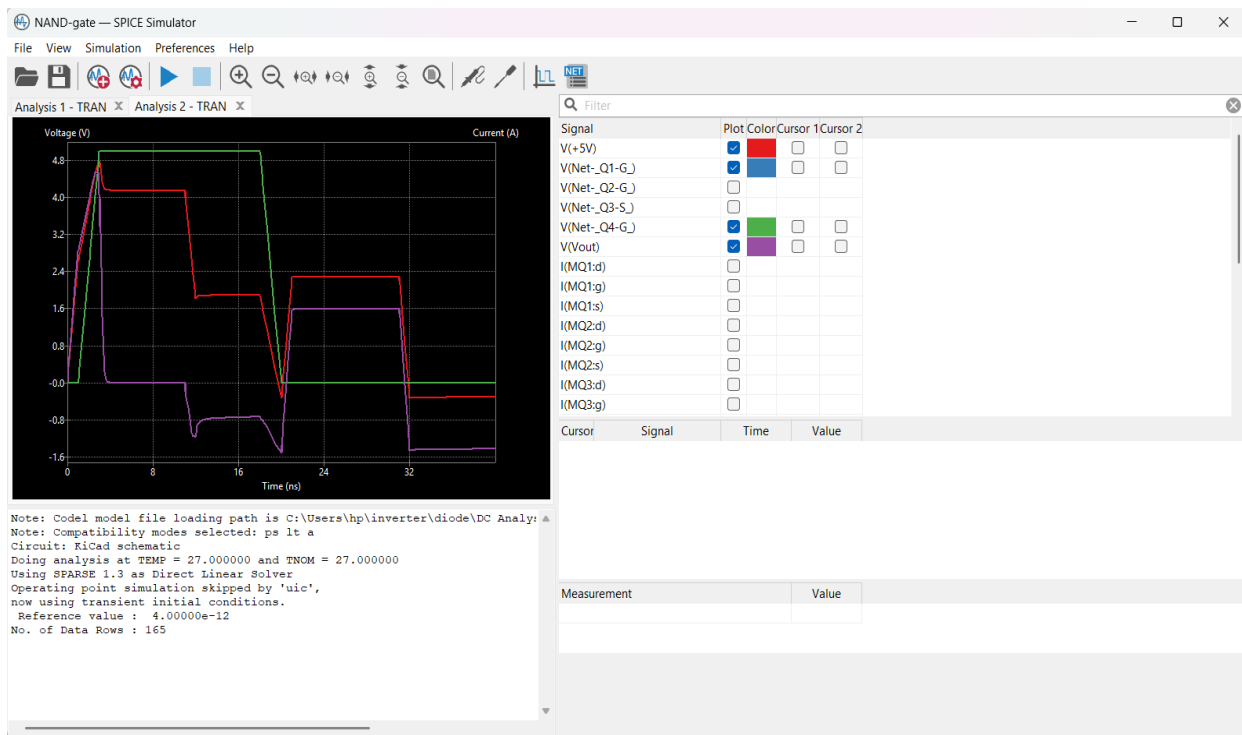
Compatibility mode:

PSpice and LTSpice

OK

Cancel

Simulation:



Voltage (V)

Current (A)

4.8

4.0

3.2

2.4

1.6

0.8

-0.0

-0.8

-1.6

0

8

16

24

32

Time (ns)

Note: Model file loading path is C:\Users\hp\inverter\diode\DC Analy: a

Note: Compatibility modes selected: ps lt a

Circuit: KiCad schematic

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

Operating point simulation skipped by 'uic',

now using transient initial conditions.

Reference value : 4.00000e-12

No. of Data Rows : 165

