REPORT

Lab 7 : Traffic Lights Simulation

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Q1) TRAFFIC LIGHTS SIMULATION:

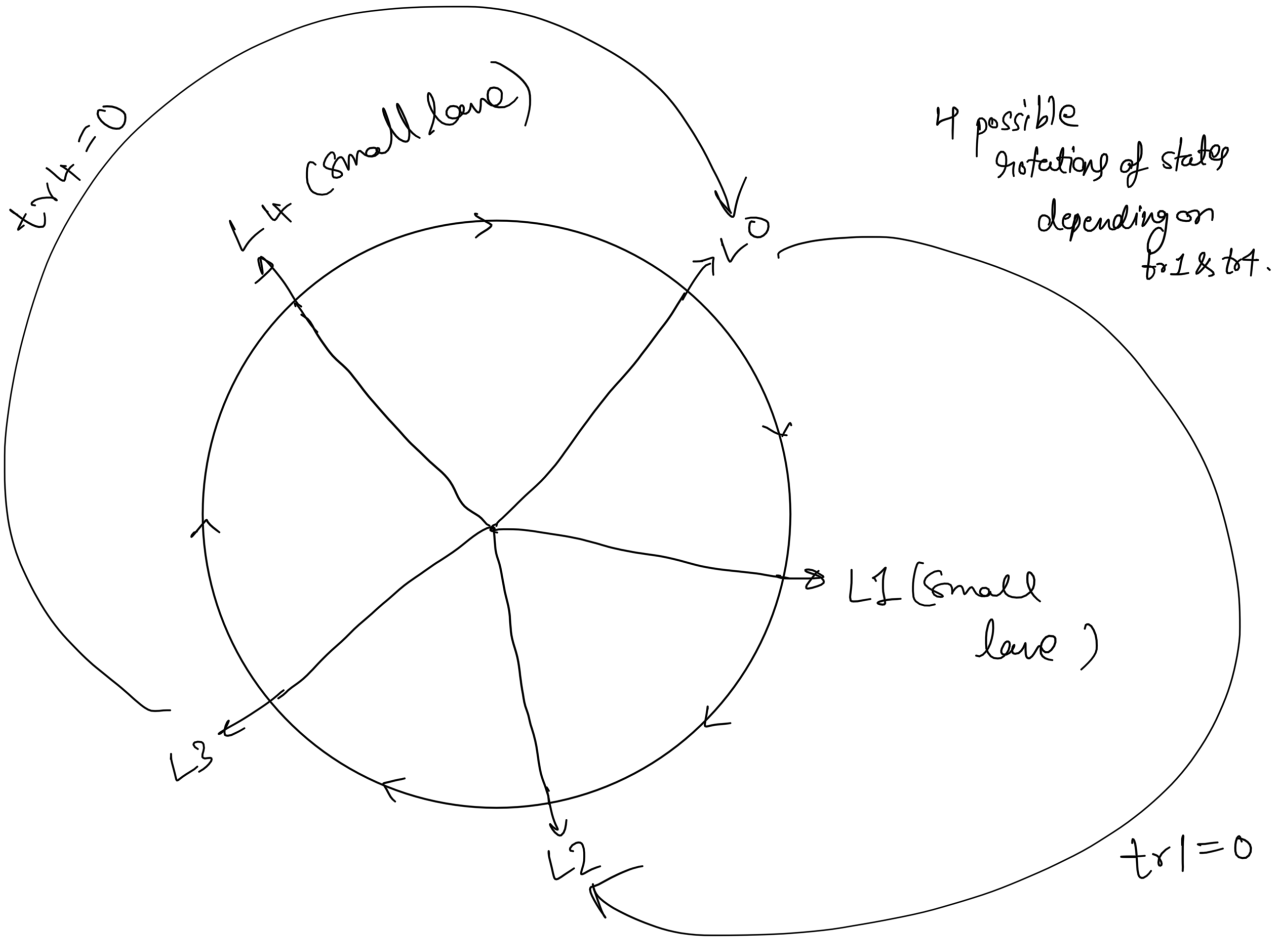


Figure (1)

AUTOMATA FOR THE TRAFFIC LIGHTS SIMULATION:

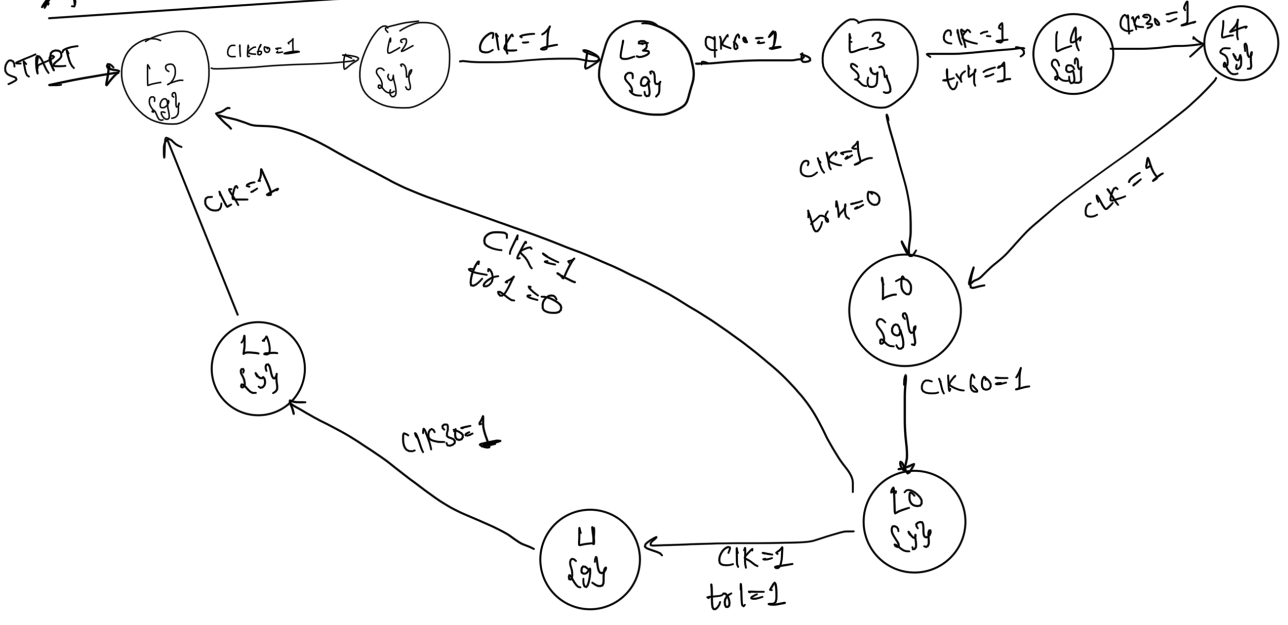


Figure (2)

* The code was written in Behavioural way.

* Design:

An internal State machine (sm), 10 seconds counter and 30 seconds counter were maintained as the inner part of the design.

Sm → is an 10 bit vector $\underbrace{a_9 a_8}_{L4}\underbrace{a_7 a_6}_{L3}\underbrace{a_5 a_4}_{L2}\underbrace{a_3 a_2}_{L1}\underbrace{a_1 a_0}_{L0}$

↳ Each set of two bits represents a single lane mentioned either above or below.

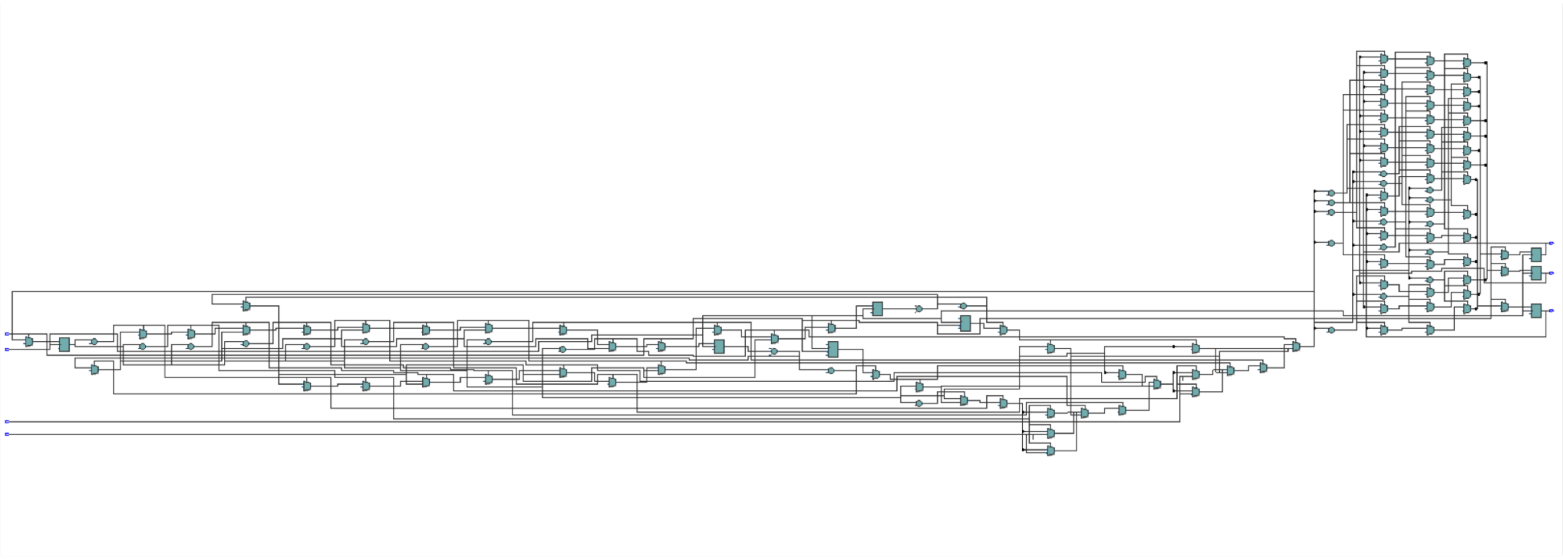
↳ Now for example take "$a_1 a_0$"

```
if "a1a0" == "00"
        //make L0 lane's red light glow
else if "a1a0" == "10"
        //make L0 lane's yellow light glow.
else if "a1a0" == "11"
        //make L0 lane's green light glow.
```

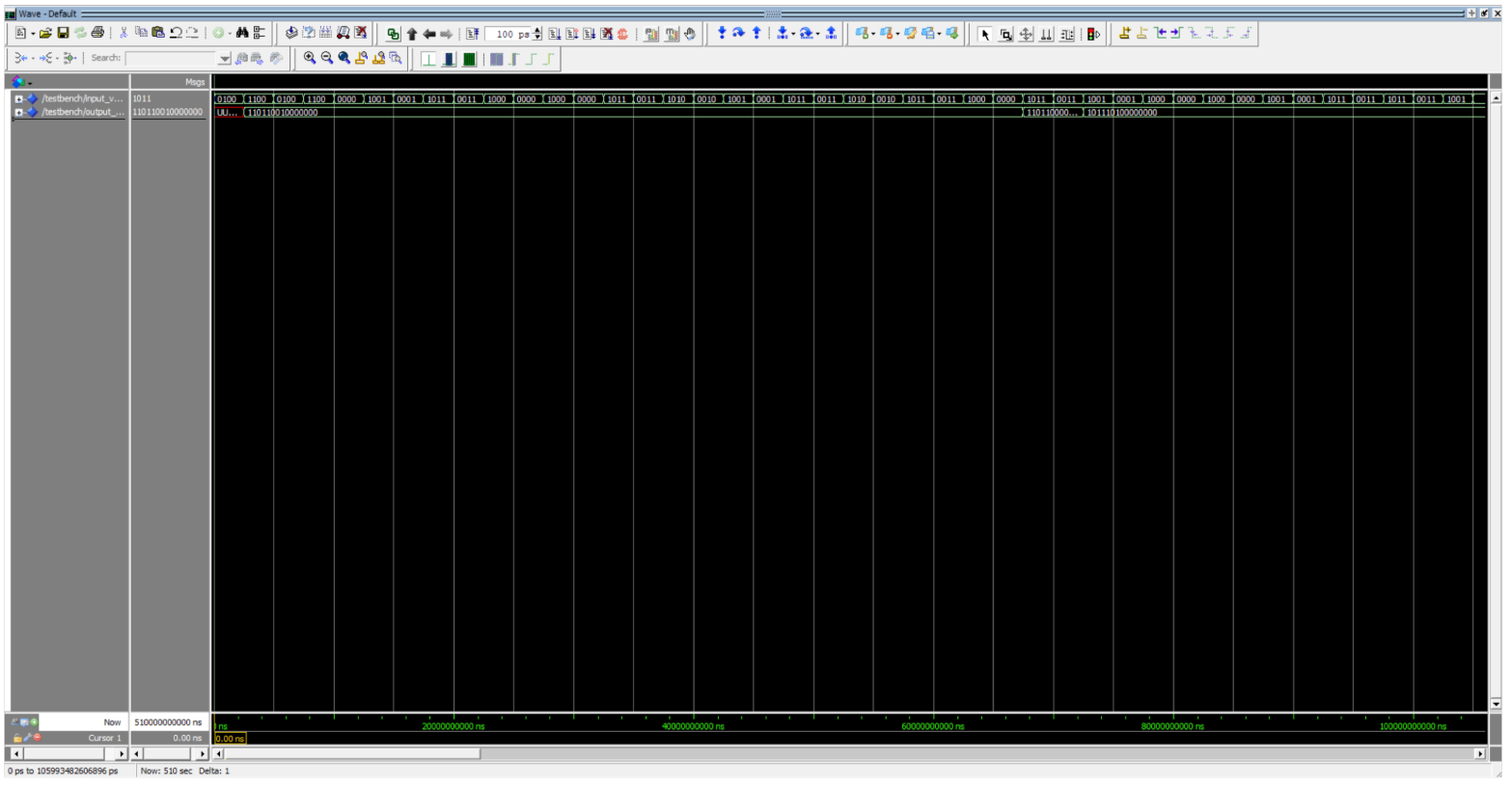
* Similarly for other sets of two bits

* Now coming to the state machine state changes, it is handled as shown in Figure (2) state transition diagram / Automata.

* Following is the circuit diagram from Netlist Viewer:



* And Following is the sample screen shot of simulation tested using the test-bench.



* The inner clocks for 60 seconds and 30 seconds are based on simple counts on clock cycles.

* Each clock cycle was simulated to be for 5 seconds

* Now 30 seconds = 6 clock cycles
  60 seconds = 12 clock cycles.

* TEST BENCH was designed in such a way that takes 4 bit input + 15 bit output + Mask