FPGA PONG

CECS 361 Spring 2022

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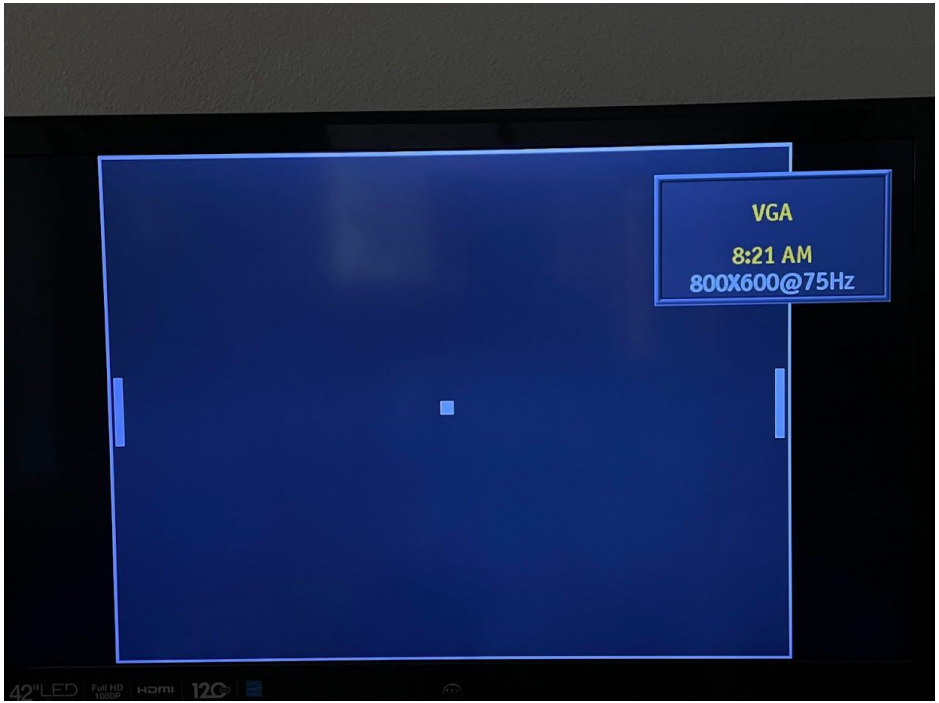
INTRODUCTION

- PONG GAME USING FPGA BOARD WITH VGA DISPLAY
- PONG GAME DISPLAYED AT 800X600 RESOLUTION AT 75Hz
  - DONE BY USING A BASIC CLOCK DIVIDER
  - AND BY USING A VERTICAL AND HORIZONTAL SYNC GENERATOR
- GAME IS CONTROLLED BY THE TWO RIGHTMOST AND TWO LEFTMOST SWITCHES
  - USING DEBOUNCE FUNCTION TO PREVENT UNINTENTIONAL MISINPUTS

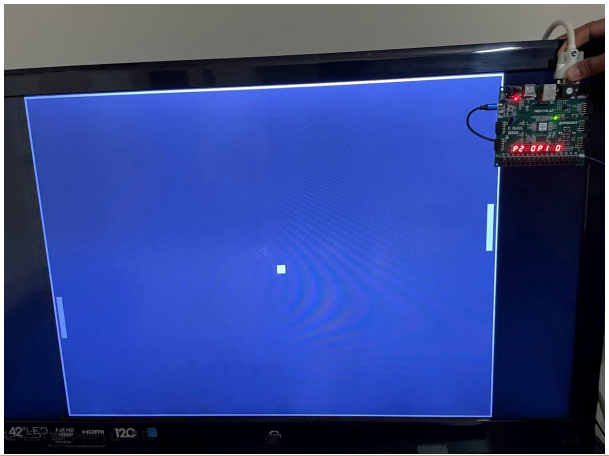
GAME

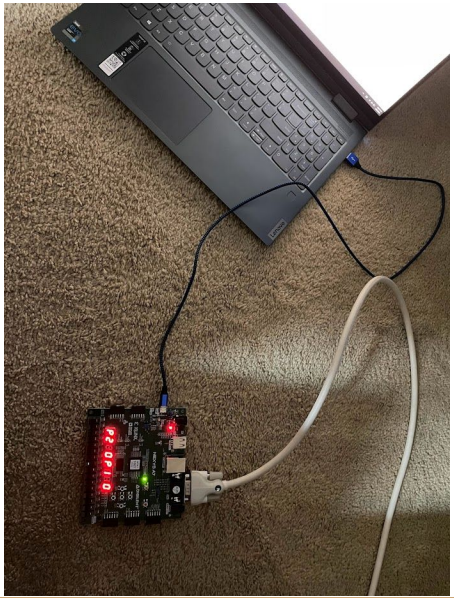
- 2D SPORTS GAME SIMULATING TABLE TENNIS
- PLAYER 1 CONTROLS AN IN-GAME PADDLE WITH THE RIGHTMOST TWO SWITCHES
- PLAYER 2 CONTROLS AN IN-GAME PADDLE WITH THE LEFTMOST TWO SWITCHES
- GOAL IS FOR EACH PLAYER TO REACH 3 POINTS
    - POINTS ARE EARNED WHEN ONE PLAYER FAILS TO RETURN THE BALL TO THE OTHER PLAYER



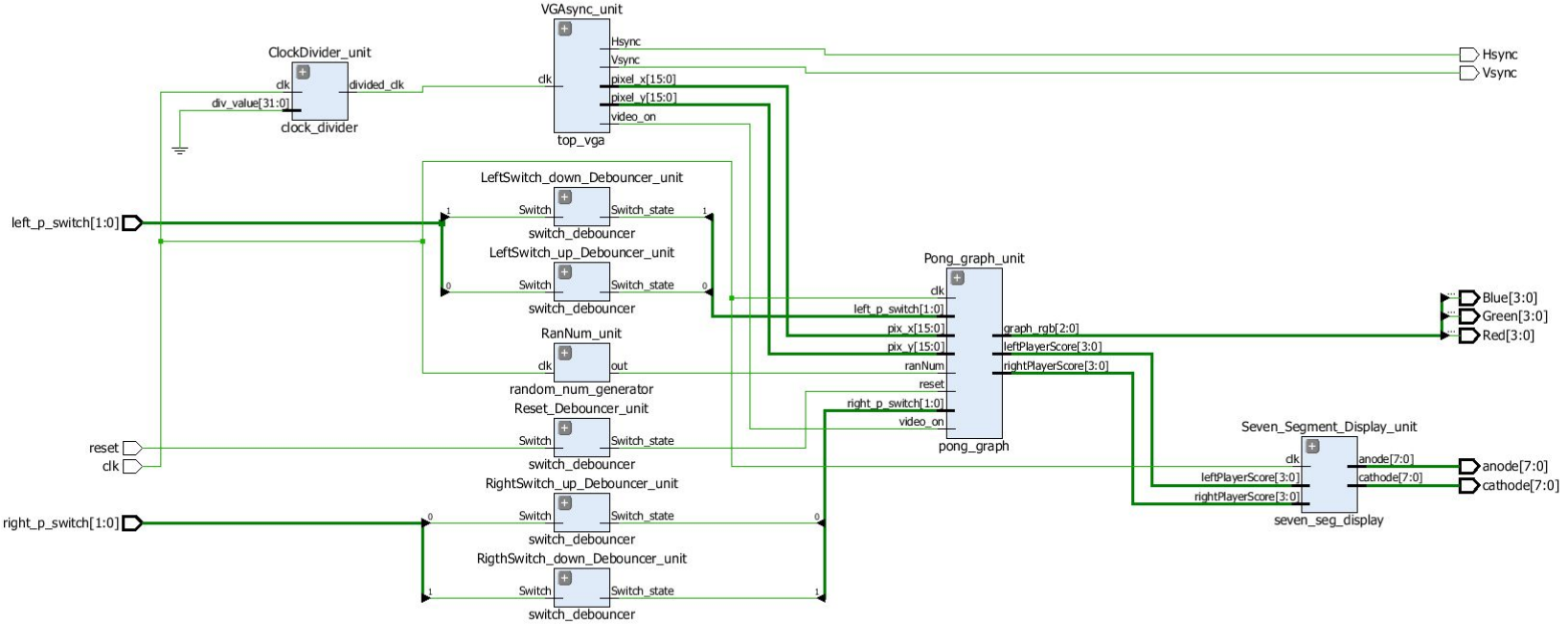
RUNTIME

- Game controlled by onboard switches.
- Score increments upon making the other player miss.(couldn’t implement)
- Ball always spawn in the middle at reset.
- Ball randomizes direction after players start the game.





DESIGN DIAGRAM



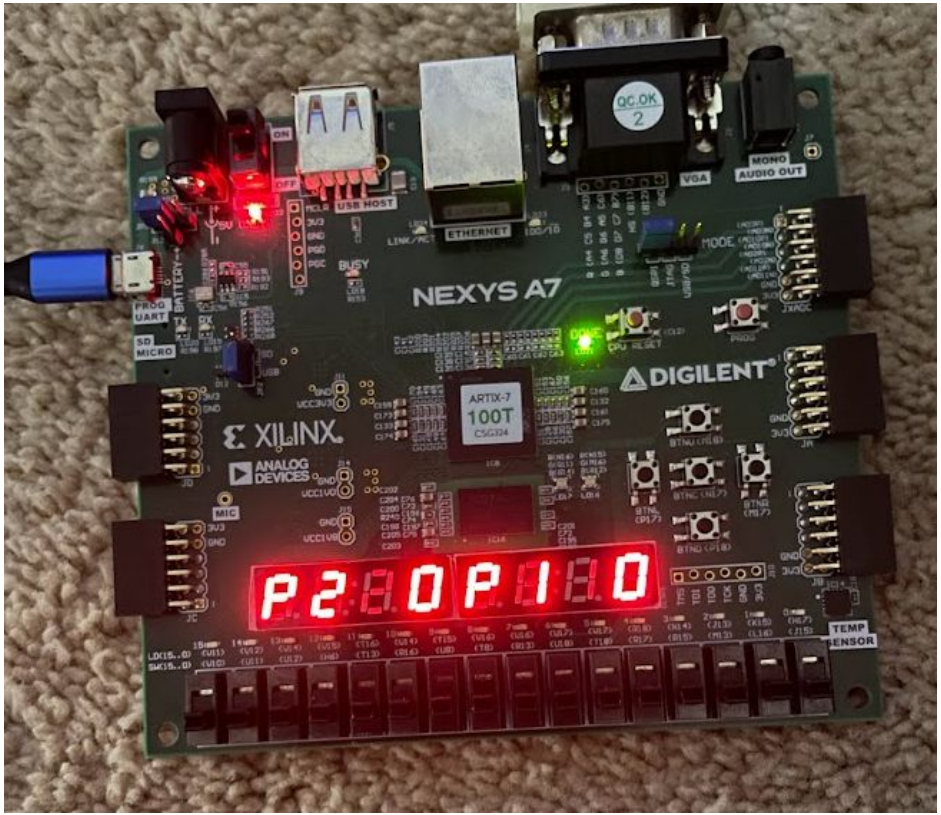
VGA

- SYNCHRONIZATION GENERATOR
  - GENERATING VERTICAL AND HORIZONTAL SIGNALS TO USE THE VGA PORT ON NEXYS A7-100T
- VGA timing standard for 800 x 600 resolution @ 75 Hz with a 50 MHz pixel clock.

Type	Standard	
Timing name	800 x 600 @ 75 Hz	
Horizontal frequency and polarity	46.875 kHz	Positive
Vertical frequency and polarity	75 Hz	Positive
Pixel clock	49.5 MHz	
Scan type	Noninterlaced	
Horizontal		
Period	21.333 µs	1056 pixels
Display	16.162 µs	800 pixels
Blanking	5.172 µs	256 pixels
Sync	1.616 µs	80 pixels
Back porch	3.232 µs	160 pixels
Front porch	0.323 µs	16 pixels
Vertical		
Total	13.333 ms	625 lines
Display	12.800 ms	600 lines
Blanking	0.533 ms	25 lines
Sync	0.064 ms	3 lines
Back porch	0.448 ms	21 lines
Front porch	0.021 ms	1 line

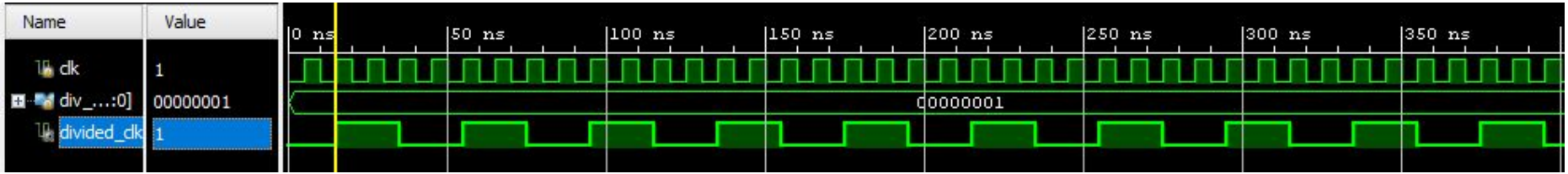
SEVEN SEGMENT

- 8 x 7-Segment Display
- 8 Anodes, 8 Cathodes, shared between digits.
- Display multiplexing is used to display left player score and right player score with limited connections.
- Switching between digits occurs so quickly, the human eye perceives image as static.



CLOCK DIVIDER

- TWO INPUTS
  - CLK AND DIV_VALUE
- ONE OUTPUT
  - DIV_CLOCK
- USED IN VGA SYNCHRONIZATION GENERATOR TO GENERATE 50 MHz PIXEL CLOCK
  - FOR THE TARGET RESOLUTION 800x600 @75HZ
- USED IN SEVEN SEGMENT DISPLAY TO GENERATE A 10 KHz CLOCK
  - ALLOWS US TO PROPERLY DISPLAY THE DIGITS USING MULTIPLEXER

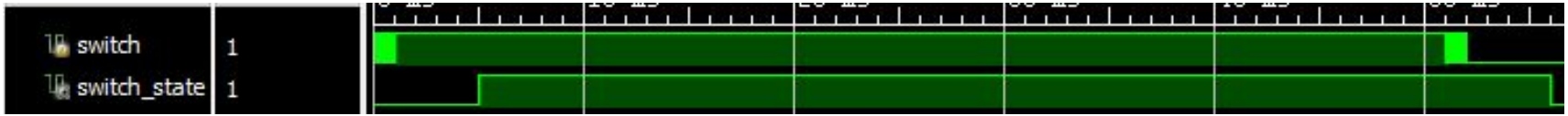


PONG GRAPHICS

- EIGHT INPUTS
  - Clk, left player input, right player input, pixel x, pixel y, random number, reset, and video on.
- THREE OUTPUTS
  - RGB values, left player score, and right player score.
- PROVIDES OUTPUTS FOR THE VGA MONITOR AND THE SEVEN-SEGMENT DISPLAY
- TAKES CARE OF GAME LOGIC
  - Like when the ball hits paddle or a wall, the ball bounces back.
  - Sets ball and paddle position/speed at reset.
  - Moves ball and paddle and updates the on screen picture.

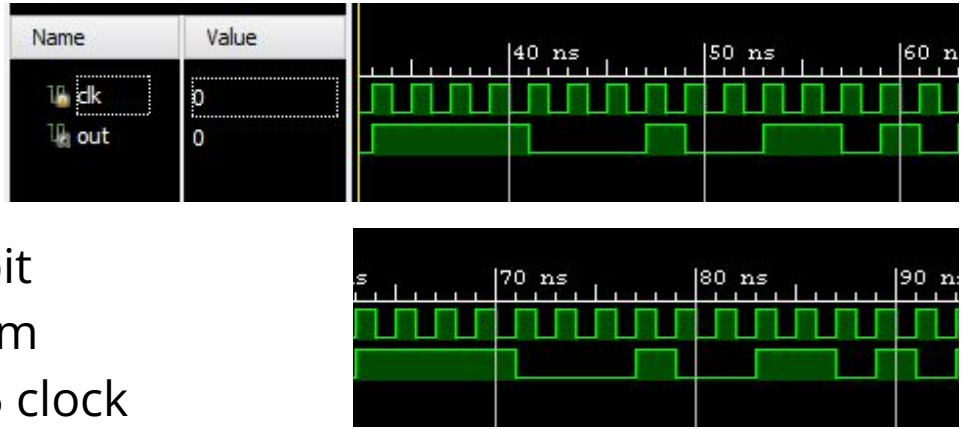
SWITCH DEBOUNCER

- TO REMOVE THE UNEXPECTED BEHAVIOR
  - Mechanical switches
- FOR USER INPUTS
  - LEFT AND RIGHT PLAYER UP AND DOWN SWITCH
  - RESET SWITCH
- TAKES INPUTS AND CLEANS OUT THE INPUT
  - UNEXPECTED UP AND DOWN BOUNCES IN THE SWITCH SIGNAL
- IMPLEMENTED A 5ms DELAY UNTIL THE INPUT SWITCH STABLILIZES



RANDOM NUMBER GENERATOR

- We implemented a Linear FeedBack Shift Register to generate a Pseudo-Random sequence that outputs a 1-bit number. Our pseudo-random sequence has a period of 15 clock cycles before it overflows and repeats from the first value.



DEMO OF THE GAME

THE END