

CARRY LOOK AHEAD ADDER

3- Bit Adder

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❖ INTRODUCTION

A carry look-ahead adder (CLA) is a type of digital circuit that performs binary addition of two n-bit numbers. Unlike a ripple carry adder (RCA), which generates carry bits sequentially from the least significant bit (LSB) to the most significant bit (MSB), a carry look-ahead adder generates all carry bits in parallel. The CLA circuit is made up of two main parts: the carry generator and the sum generator. The carry generator generates the carry signals, which are then fed into the sum generator to produce the final sum output.

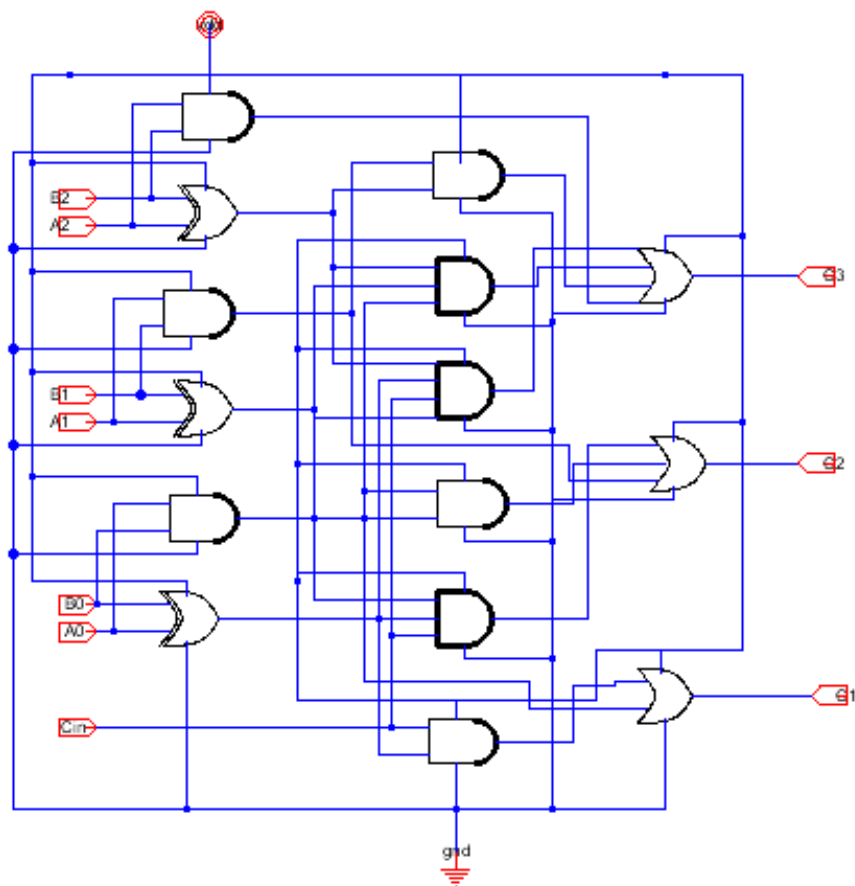
❖ BACKGROUND

- ☐ The carry generator is made up of a series of carry lookahead blocks, each of which generates the carry signal for a group of bits. Each carry lookahead block takes as input the carry signals from the previous block, as well as the input bits to be added, and generates the carry signals for the group of bits.
- ☐ The sum generator takes the input bits and the carry signals generated by the carry generator, and produces the sum output. The sum generator is typically implemented using a series of full adders, which add the input bits and the carry signals to produce the sum output.
- ☐ Overall, the carry lookahead adder circuit provides a faster and more efficient way of performing binary addition compared to the ripple carry adder circuit. However, it is also more complex and requires more hardware to implement.

❖ MOTIVATION

- ❑ Carry look-ahead adder (CLA) is a faster and more efficient adder than the normal adder. The main reason for using a CLA instead of a normal adder is to reduce the time taken to compute the sum of two numbers.
- ❑ In a normal adder, the calculation of the carry bit is a sequential process, where each bit's carry depends on the previous bit's carry. This results in a longer propagation delay, which affects the overall speed of the adder.
- ❑ Another advantage of CLA is that it can add multi-bit operands in a single clock cycle. In contrast, a normal adder requires multiple clock cycles to add multi-bit operands.
- ❑ In summary, the carry look-ahead adder is preferred over the normal adder because of its faster and more efficient performance, making it suitable for use in applications that require fast arithmetic computations.

➤ 3-BIT CARRY LOOK AHEAD ADDER SCHEMATIC :



❖ **BASIC GATES TO IMPLEMENT ABOVE SCHEMATIC :**

☐ **Components required for building of the circuit:**

☐ **AND** gate(2 input, 3 input,4 input)

☐ **OR** gate(2 input, 3 input,4 input)

☐ **NOT** gate

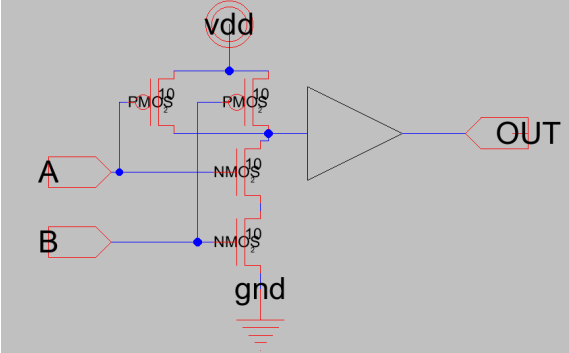
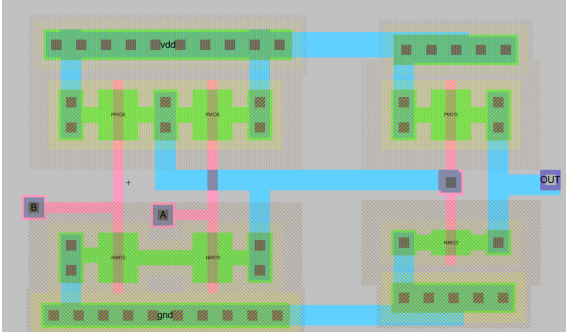
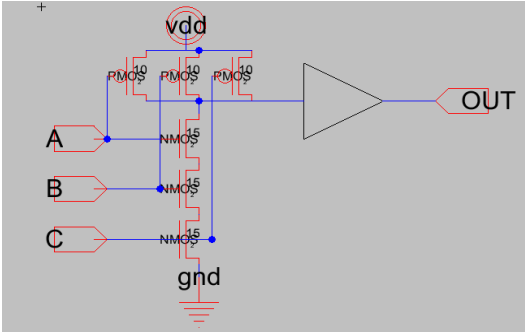
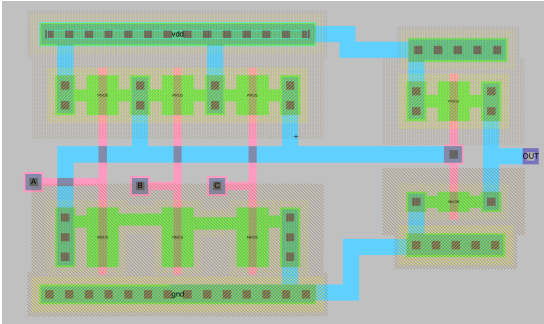
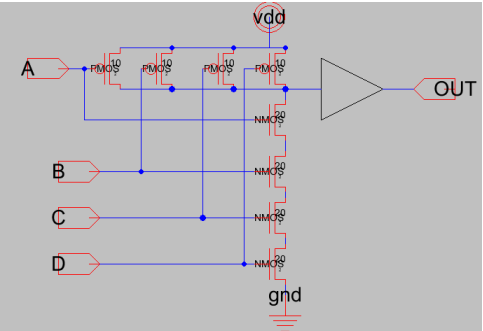
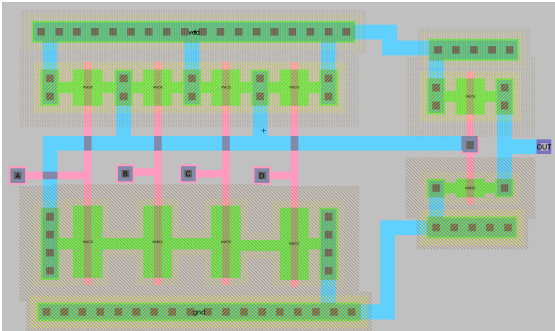
☐ **XOR** gate.

☐ **W/I Ratio = 2**

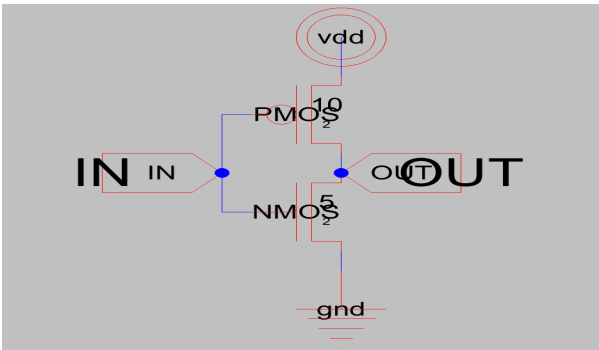
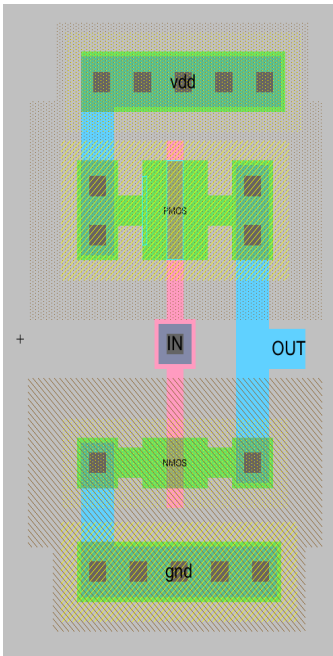
Step are being followed:

1. **Create a schematic:** A schematic is a diagram that shows how the components in a circuit are connected. Start by drawing a rough sketch of the circuit, then use a schematic drawing software to create a formal diagram. Make sure to label all components and wires. Electric software is being used for building schematics of all gates.
2. **Design the layout:** Once you have a schematic, you can design the physical layout of the circuit. Determine the size and shape of the circuit board. Make sure to leave enough space between components and to keep the wiring neat and organized.
3. **Test the circuit:** Once the circuit is assembled, test it to make sure it works as expected.
 - **DRC** -Design rule check
 - **ERC** - Electrical rule check
 - **NCC** -Network Consistency Checking
4. **Checking with Ltspice:**Checking the working flow of the circuit using LTspice.by placing spice code in schematic we can check outputs.
5. **Make adjustments:** If the circuit isn't working correctly, make adjustments as needed.Check for any wiring mistakes, component failures. Make adjustments to the layout or component selection as shown in DRC check.
6. **Finalize the design:** After checking DRC, NCC and ERC of all circuit components we get the outputs in LTspice.

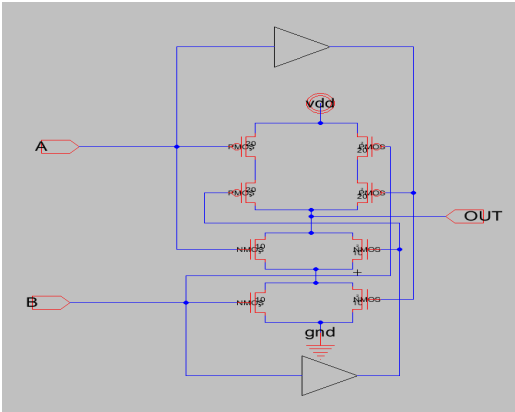
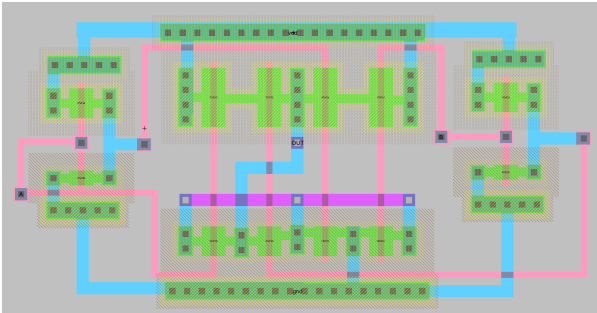
AND GATE :

Schematic	Layout
	
	
	

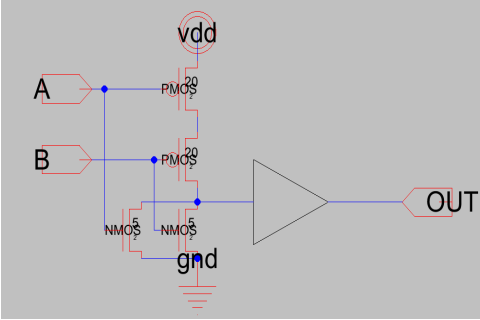
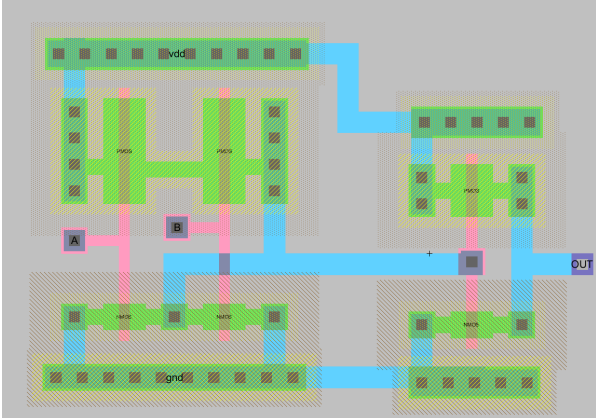
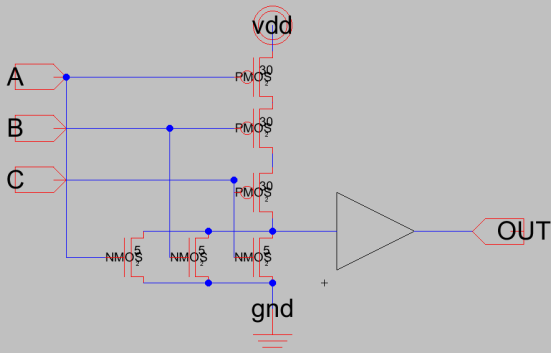
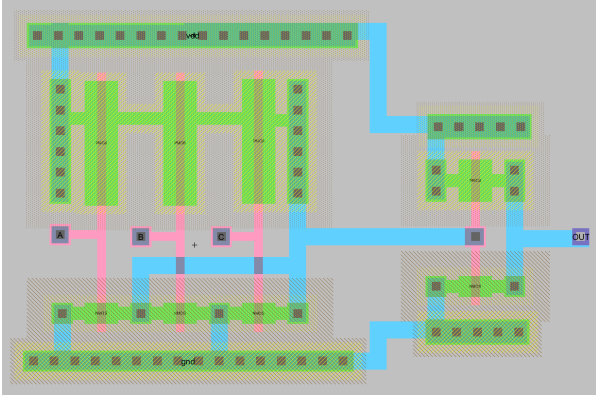
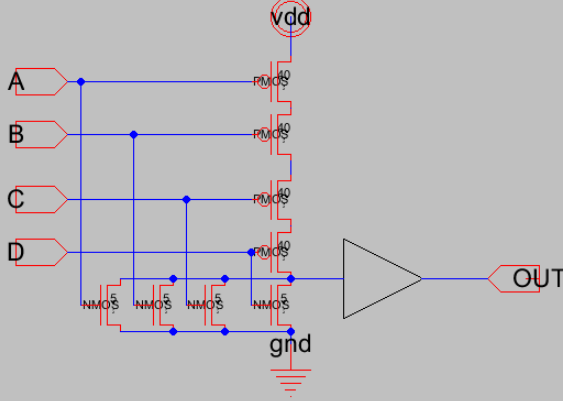
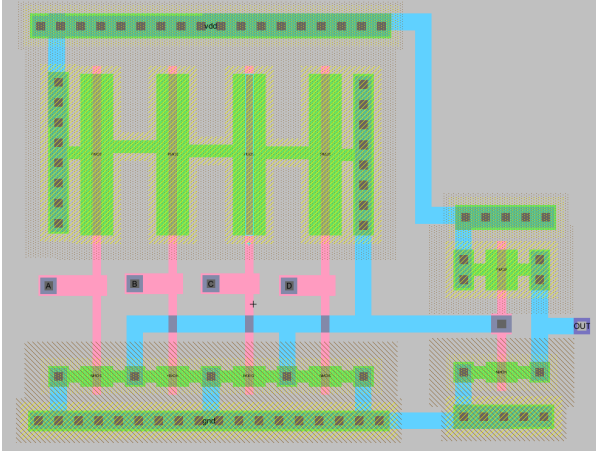
NOT GATE :

Schematic	Layout
	

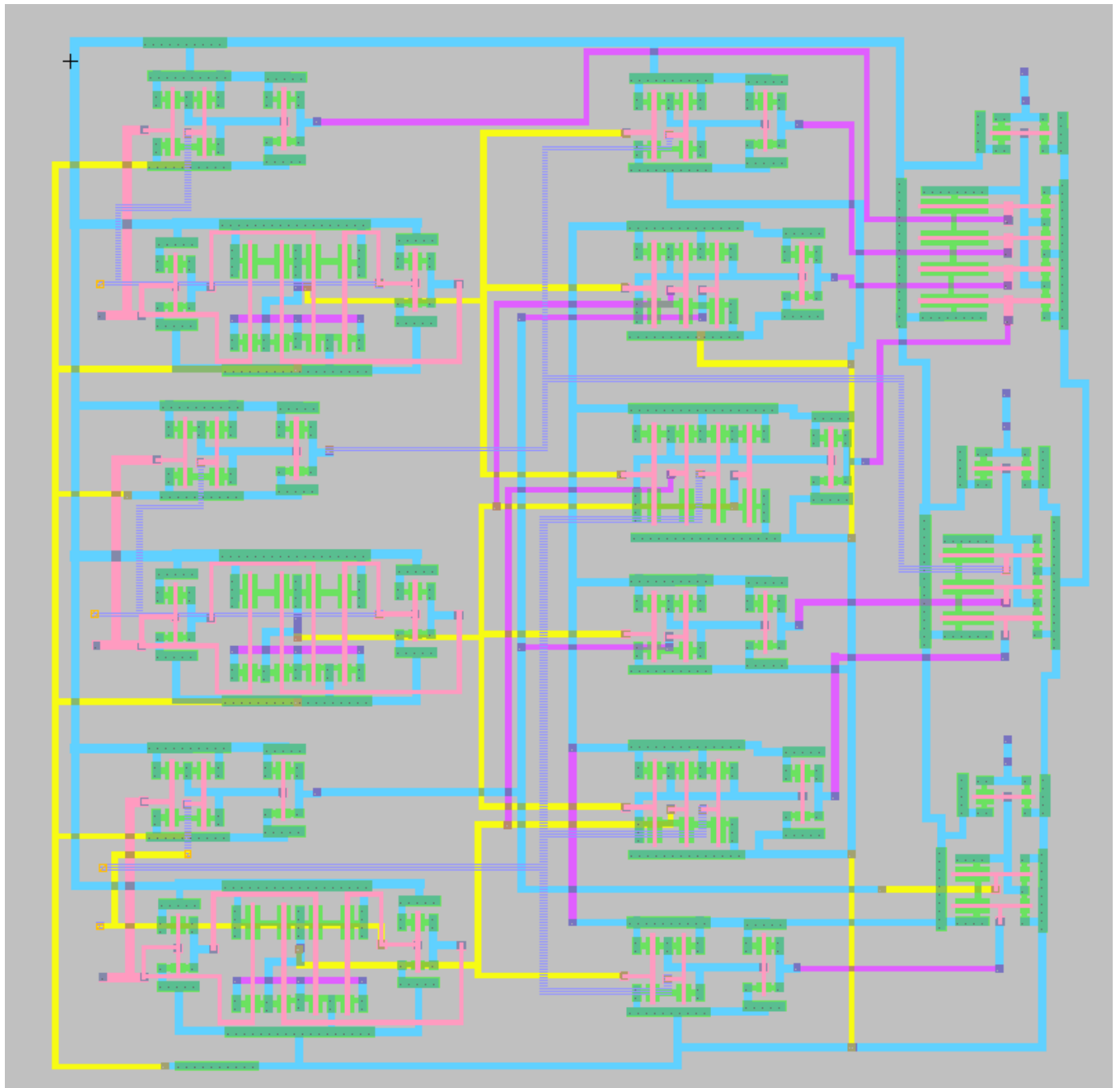
XOR GATE :

Schematic	Layout
	

OR GATE :

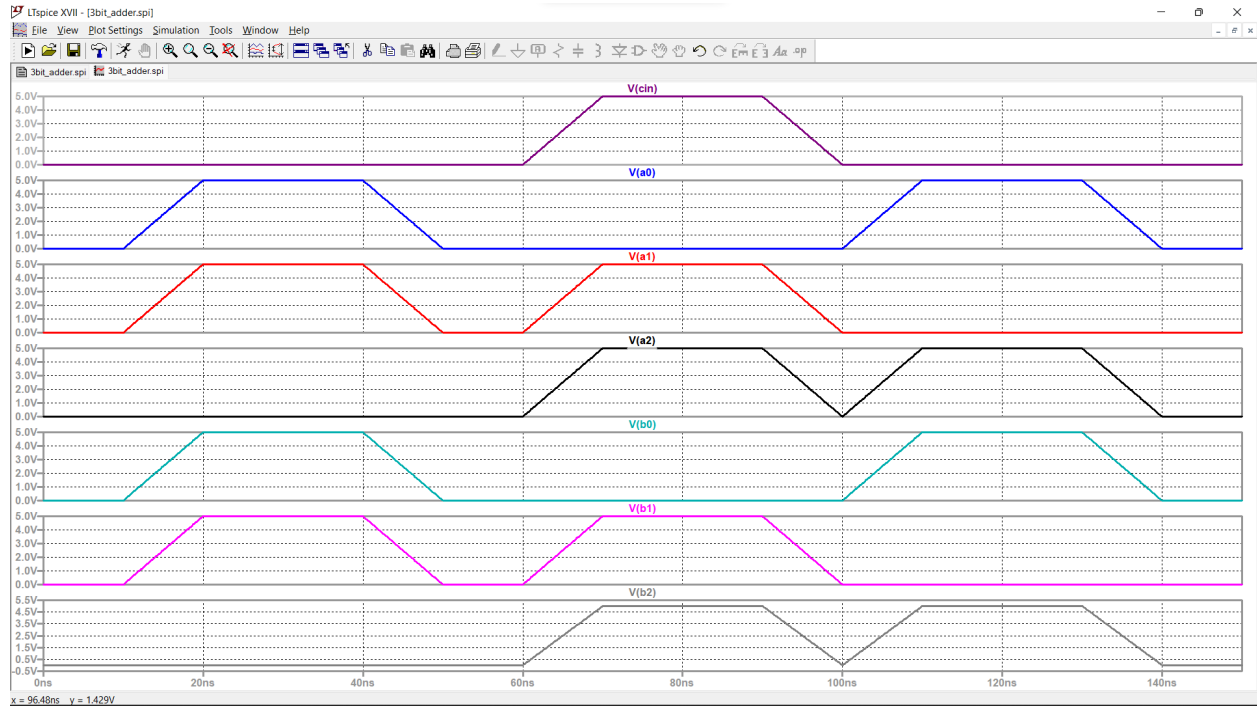
Schematic	Layout
 <p>A schematic diagram of a 2-input OR gate. It features two PMOS transistors with their gates connected to inputs A and B, and their sources connected to vdd. Two NMOS transistors have their gates connected to inputs A and B, and their sources connected to gnd. The drains of the PMOS and NMOS transistors are connected in a series configuration to an inverter, which produces the output OUT.</p>	 <p>A physical layout of a 2-input OR gate. It shows the placement of PMOS and NMOS transistors on a substrate, with their gates connected to inputs A and B. The layout includes a network of blue and red lines representing the electrical connections between the transistors and the output inverter, all situated between vdd and gnd power rails.</p>
 <p>A schematic diagram of a 3-input OR gate. It features three PMOS transistors with their gates connected to inputs A, B, and C, and their sources connected to vdd. Three NMOS transistors have their gates connected to inputs A, B, and C, and their sources connected to gnd. The drains of the PMOS and NMOS transistors are connected in a series configuration to an inverter, which produces the output OUT.</p>	 <p>A physical layout of a 3-input OR gate. It shows the placement of PMOS and NMOS transistors on a substrate, with their gates connected to inputs A, B, and C. The layout includes a network of blue and red lines representing the electrical connections between the transistors and the output inverter, all situated between vdd and gnd power rails.</p>
 <p>A schematic diagram of a 4-input OR gate. It features four PMOS transistors with their gates connected to inputs A, B, C, and D, and their sources connected to vdd. Four NMOS transistors have their gates connected to inputs A, B, C, and D, and their sources connected to gnd. The drains of the PMOS and NMOS transistors are connected in a series configuration to an inverter, which produces the output OUT.</p>	 <p>A physical layout of a 4-input OR gate. It shows the placement of PMOS and NMOS transistors on a substrate, with their gates connected to inputs A, B, C, and D. The layout includes a network of blue and red lines representing the electrical connections between the transistors and the output inverter, all situated between vdd and gnd power rails.</p>

3-BIT CARRY LOOK AHEAD ADDER SCHEMATIC :

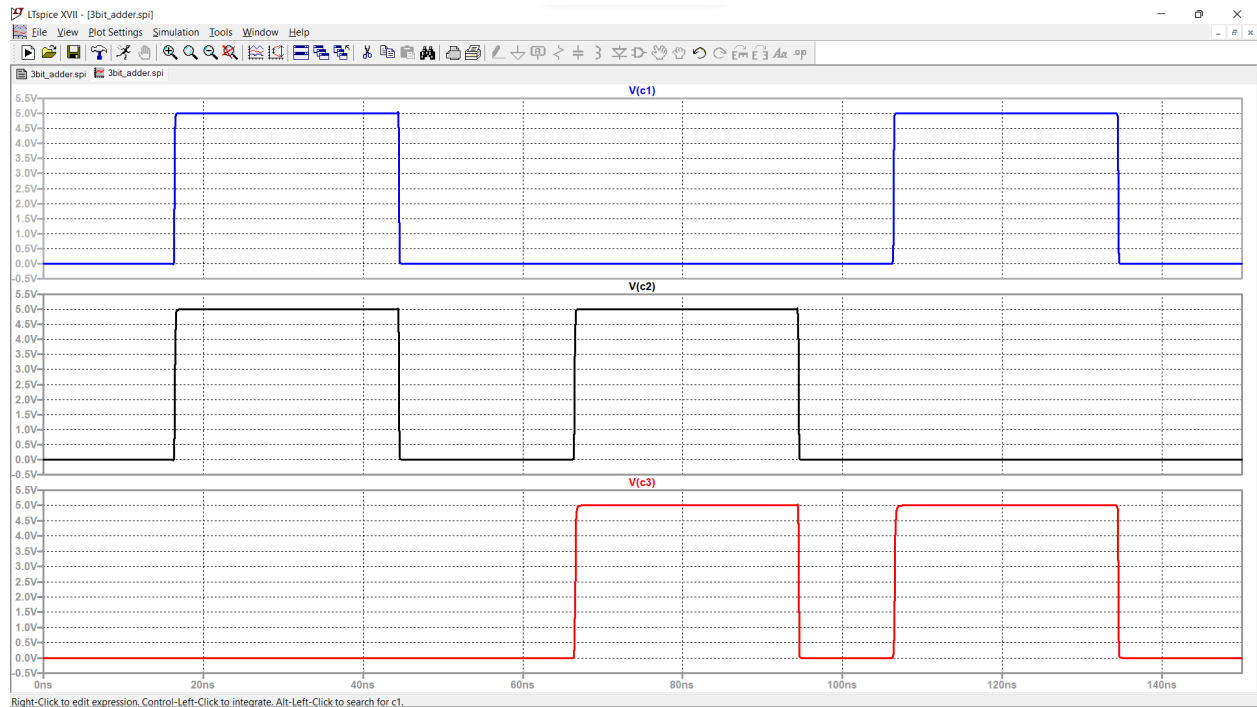


LTSpice Outputs:

inputs:



Outputs:



Conclusion:

- The purpose of this report was to outline the steps involved in building a carry look-ahead circuit using electric software.
- The report highlighted that building a carry look-ahead circuit involves creating a schematic and layout, selecting the appropriate components, assembling the circuit, testing it, and making adjustments as needed.
- The use of electric software can simplify the process by providing tools for creating the schematic and layout, simulating the circuit, and identifying errors or design issues.
- Overall, the report concluded that electric software can be a valuable tool in the design and implementation of digital circuits, and the steps outlined in the report provide a useful guide for building a carry look-ahead circuit using electric software.

Contribution:

EAGA JASWANTH KRISHNA - S20200020271 - worked on both schematic and layouts
VUDAYANA ROHITH - S20200020313 - worked on both schematic and layouts