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Toward Efficient Design of Reversible Logic Gates in Quantum-Dot Cellular Automata with Power Dissipation Analysis

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Abstract Nanotechnologies, remarkably Quantum-dot Cellular Automata (QCA), offer an attractive perspective for future computing technologies. In this paper, QCA is investigated as an implementation method for designing area and power efficient reversible logic gates. The proposed designs achieve superior performance by incorporating a compact 2-input XOR gate. The proposed design for Feynman, Toffoli, and Fredkin gates demonstrates 28.12, 24.4, and 7% reduction in cell count and utilizes 46, 24.4, and 7.6% less area, respectively over previous best designs. Regarding the cell count (area cover) that of the proposed Peres gate and Double Feynman gate are 44.32% (21.5%) and 12% (25%), respectively less than the most compact previous designs. Further, the delay of Fredkin and Toffoli gates is 0.75 clock cycles, which is equal to the delay of the previous best designs. While the Feynman and Double Feynman gates achieve a delay of 0.5 clock cycles, equal to the least delay previous one. Energy analysis confirms that the average energy dissipation of the developed Feynman, Toffoli, and Fredkin gates is 30.80, 18.08, and 4.3% (for 1.0 E_k energy level), respectively less compared to best reported designs. This emphasizes the beneficial role of using proposed reversible gates to design complex and power efficient QCA circuits. The QCADesigner tool is used to validate the layout of the proposed designs, and the QCAPro tool is used to evaluate the energy dissipation.

Keywords Energy dissipation · Quantum-dot cellular automata · QCADesigner · Reversible Logic · XOR gate · Nanotechnology

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1 Introduction

With the essence of high speed and ultra low-power devices, traditional CMOS technology has already reached the bottleneck of scaling feature size. This encourages researchers to come up with some alternative technologies [1]. In this aspect, QCA is the suitable candidate, which has none of the above problems and promises extremely low power consumption with small size feature and high operating frequency [1, 2]. These attractive attributes enable quantum gates and circuits role toward computational reversibility. Work by Landauer [3] showed that, regardless of the underlying technology, conventional logic circuits dissipate heat in an order of $kT\ln 2$ joules for every bit of information that is lost. Although the theoretical lower bound on power dissipation still does not constitute a significant fraction of the power consumption of current devices, it cannot be neglected in future generation technologies where other losses are minimized. Later, Bennett [4] demonstrated logically zero dissipation is achievable, if computations are performed without destroying the information, i.e, by using reversible logics. Implementing the reversible circuits by using QCA cells promises to achieve circuits that consume very low energy even less than $kT\ln 2$. This resulted in widespread attention in designing QCA based non-reversible and reversible circuits in past few years [5–17].

The paper is organized as follows. Section 2 presents a short introduction to QCA basics and reversible gates. Section 3 describes the efficient QCA based reversible gates. Section 4

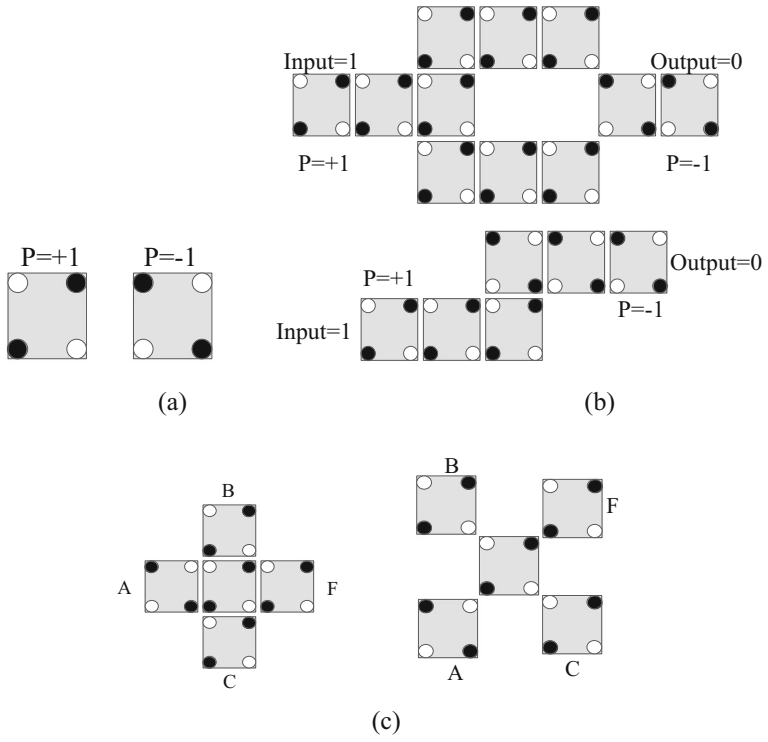


Fig. 1 QCA primitives **a** Quantum-dot cell, **b** inverters, **c** majority gates

presents detailed simulation and comparison results of the reversible gates with the previous structures along with detailed power analysis. Finally, conclusions are addressed in Section 5.

2 QCQ Preliminaries and Related Works

2.1 QCA Elements

A standard QCA cell consists of four quantum-dots and two excess electrons located in the corners of a square structure. These free electrons can tunnel between the dots within the cell. Through Coulombic interaction between the electronic charges, two stable charge configurations are possible. These two potential states represent binary state '0' and '1' having polarizations of $P = -1$ and $P = +1$, respectively are shown in Fig. 1a [2]. Two different QCA structures of the fundamental gates are illustrated in Fig. 1b and c; namely, the inverter (INV), and the majority gate (MV). The logical function of 3-input majority gate is expressed as below:

$$MV\ (A, B, C) = F = AB + BC + CA \tag{1}$$

2.2 Clocking

In traditional VLSI technology, clocking mechanism is used to control the timing in sequential circuits. In QCA technology a pipeline based clock mechanism is essentially required for both sequential and combinational designs. This mechanism not only controls the data flow, but also supplies power for the cells. For the clocking purpose, four clocks are applied, i.e. clock 0, clock 1, clock 2, and clock 3. These clocks are 90° out of phase as apparent in Fig. 2. Each Clock in QCA comprises of four distinct clock phases: switch, hold, release, and relax as depicted in Fig. 2 [18].

In switch state, cells start polarized and inter-dot barriers are raised and QCA cell attends one of the polarization states depending on the state of driving cell. During this phase, the real computation occurs. During the hold phase, cells have a fixed polarization to drive the succeeding stage. In release phase, cells start unpolarized and during the final stage, inter-dot barriers stay lowered and a cell has no fixed polarization.

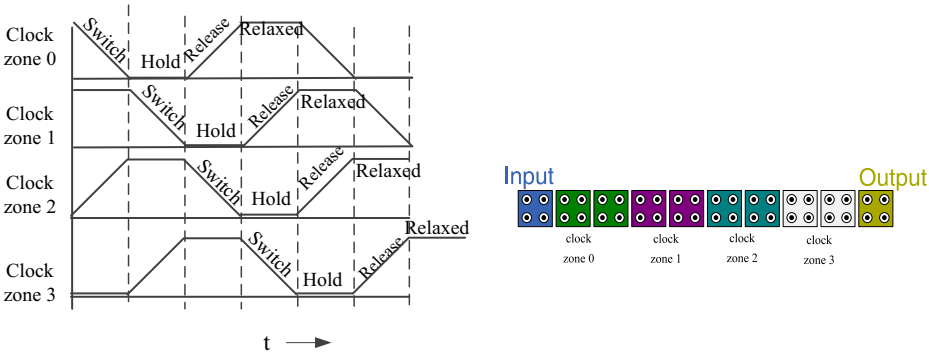


Fig. 2 QCA clocking with four phases

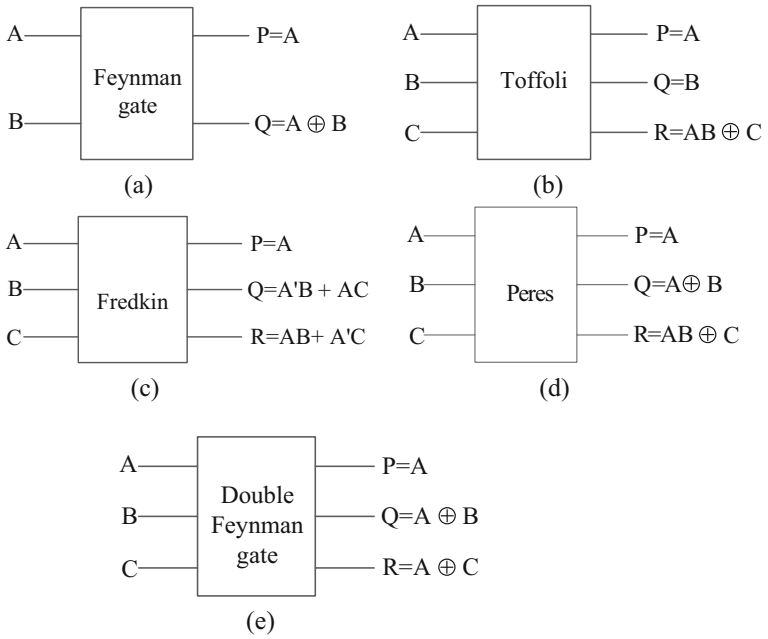


Fig. 3 Block diagram of reversible gates **a** Feynman [19], **b** Toffoli [20], **c** Fredkin [21], **d** Peres [22], **e** Double Feynman [23]

2.3 Reversible Logic Gates

Reversible gates are building blocks of reversible logic. Reversible gates provide unique mapping between the input vectors and the output ones, thus the number of inputs must be equal to that of outputs. Figure 3 shows the several block diagrams of commonly used reversible gates.

Lemma 1 *For the set of input variables* $X = \{x_1, x_2, \ldots\ldots, x_{n+1}\}$ *the generalized Toffoli gate can be represented as* $TOF(C;T)$ *or* $C^nNOT(x_1, x_2, \ldots\ldots, x_{n+1})$ *where* $C = \{x_{i_1}, \ldots\ldots, x_{i_k}\} \subset X$ *a set of control lines, and a single target line* $T = \{x_j\}$ *and* $C \cap T = \Phi$. *It maps a Boolean pattern* $(x_1^0, x_2^0, \ldots\ldots, x_{n+1}^0)$ *to* $(x_1^0, x_2^0, \ldots, x_{j-1}^0, x_j^0 \oplus x_{i_1}^0 x_{i_2}^0 \ldots x_{i_k}^0, x_{j+1}^0, \ldots, x_{n+1}^0)$.

The Toffoli gate is widely used universal reversible gate. A Toffoli gate inverts the value of target line if all the control lines feed to 1, and passes the values on control lines

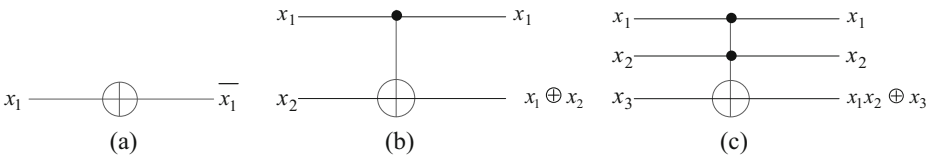


Fig. 4 Logic symbol for **a** NOT gate **b** Feynman gate **c** Toffoli gate

Table 1 Truth Table of 2-input Feynman gate

A	B	P	Q
0	0	0	0
0	0	0	1
1	0	1	1
1	1	1	0

unchanged. Due to Lemma 1, for $n = 0$, a generalized Toffoli gate is known as NOT gate which has no control lines, as shown in Fig. 4a. For $n = 1$, the CNOT gate also known as Feynman gate with single control line [19]. For $n = 2$, the C^2NOT gate commonly known as Toffoli gate with two control lines [20]. The Feynman and Toffoli gates are illustrated in Fig. 4b and c along with their truth tables in Tables 1 and 2 respectively.

Lemma 2 *For the set of input variables* $X = \{x_1, x_2, \ldots\ldots, x_n\}$ *the generalized Fredkin gate can be represented as Fred* $Fred(C; T)$ *or* $Fred(x_1, x_2, \ldots\ldots, x_n)$ *where* $C = \{x_{i_1}, \ldots\ldots, x_{i_k}\} \subset X$ *a set of control lines, and target line* $T = \{x_j, x_l\}$ *and* $C \cap T = \Phi$. *It maps a Boolean pattern* $(x_1^0, x_2^0, \ldots\ldots, x_n^0)$ *to* $(x_1^0, x_2^0, \ldots, x_{j-1}^0, x_l^0, x_{j+1}^0, \ldots, x_{l-1}^0 x_j^0, x_{l+1}^0, \ldots, x_n^0)$ *iff* $x_{i_1}^0 x_{i_2}^0 \ldots x_{i_k}^0 = 1$. *Otherwise the passed input will not be interchanged.*

The Fredkin gate is widely used universal reversible gate for input swapping. Due to Lemma 2, for $n = 0$, a gate with no control signal $Fred(x_1, x_2)$ is called SWAP, as it exchange the values on signal x_1, x_2, as depicted in Fig. 5a. For $n = 1$, a gate with one control signal $Fred(x_1; x_2, x_3)$ is commonly known as Fredkin gate [21]. Figure 5b shows logic symbol of the Fredkin gate along with truth table in Table 3.

Peres gate [22] $P(x_1; x_2, x_3)$ has one control line x_1 and two target lines x_2 and x_3. It represents a cascade of a $C^2NOT(x_1; x_2, x_3)$ and a $CNOT(x_1, x_2)$. It maps input (x_1, x_2, x_3) to $(x_1, x_1 \oplus x_2, x_1x_2 \oplus x_3)$. The general structure and truth table of Peres gate is illustrated in Fig. 6 and Table 4, respectively.

Double Feynman gate [23] $P(x_1; x_2, x_3)$ has one control line x_1 and two target lines x_2 and x_3. It represents a cascade of $CNOT(x_1, x_2)$ and CNOT(x_1, x_3). It maps input (x_1, x_2, x_3) to(x_1, $x_1 \oplus x_2$, $x_1 \oplus x_3$). The general structure and truth table of Double Feynman gate is illustrated in Fig. 7 and Table 5, respectively.

Table 2 Truth Table of 3-input Toffoli gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

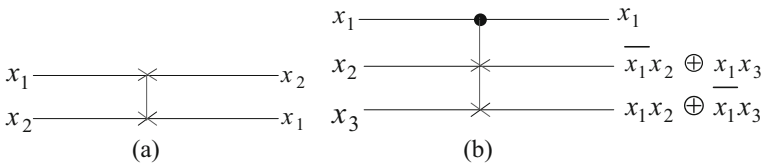


Fig. 5 Logic Symbol for **a** Swap gate **b** Fredkin gate

Table 3 Truth Table of 3-input Fredkin gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Fig. 6 Logic symbol for 3-input Peres gate

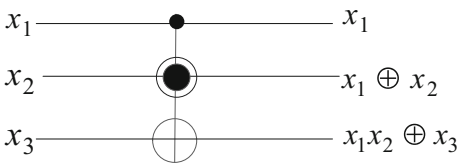


Table 4 Truth Table of 3-input Peres gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Fig. 7 Logic symbol for 3-input Double Feynman gate

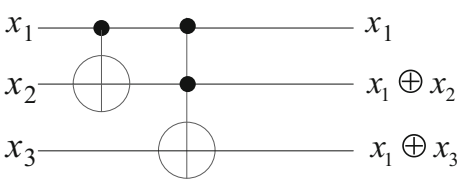


Table 5 3-input Double Feynman gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

2.4 Output Polarization

In QCA based design the thresholds are set as follows: polarization $<0.5 \Longrightarrow$ logic 0; polarization $>0.5 \Longrightarrow$ logic 1, otherwise the state is indeterminate [24]. When the output cell is driving a long wire in a Single Clocking Zone, the polarization strength limits the Maximum Number of Cells. So, the output node polarization limits the driving capability of the overall QCA design. Study of robustness of various QCA based circuits are reported in [25] by considering polarization as a function of temperature. The output node polarization drops steadily with rise in temperature leading to more erroneous outputs. This effect becomes more and more significant with the increase in the number of cells in a design. Therefore, higher value of polarization yields more robust design and increase the probability of stable state to maintain signal integrity.

2.5 Related Works

Several attempts have been made to design QCA based reversible circuits during recent years [5–10, 16, 17]. Authors in [5] have presented QCA structure for different reversible gates using 3-input majority gate as the basic unit. However, outputs of some gates are not highly polarized signals. For instance, the Peres and Fredkin gate output P is 5.80e-001 and 8.63e-001, respectively. Consequently, the output loses more than 14% of the input signal, which affects drivability for the designs. Mohammadi et al. [6] investigated QCA based reversible Feynman, Toffoli, and Fredkin gates using both rotated and translated QCA cells. The reported designs are associated with majority logic-based structure, but these designs potentially consume much more area and require more simplification to reduce the overall complexity. Further, Authors in [7–9, 16, 17] presented QCA implementation of majority gate based reversible gates. These designs require more focus to reduce area usage, unnecessary additional majority and inverter gates. Recent work by Singh et al. [10] presented

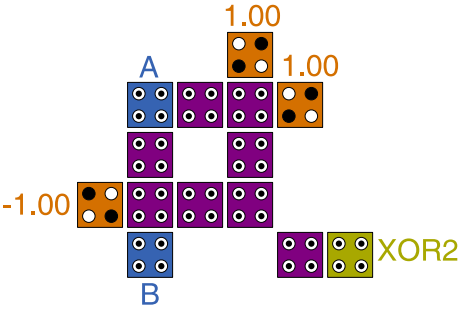


Fig. 8 QCA layout of 2- input XOR gate in [11]

compact reversible logic gates using 5-input majority gates along with power analysis. These designs require more constant inputs (garbage/ancilla inputs) and the outputs of Fredkin gate are not highly polarized signals. The inputs for A, B, and C are 1.00e+000, 1.00e+000, and 1.00e+000 respectively. The corresponding outputs X, Y, and Z are 8.86e-001, 8.81e-001, and 8.85e-001 respectively. This means that the output loses at least 11.4% of the input signal, which may affect signal integrity.

3 Novel QCA Reversible Logic Gates Structure

Already many different QCA based structures for reversible logic gates have been addressed [5–10, 16, 17]. Contrary to previously reported designs for implementation of reversible gates, the proposed reversible structures use explicit interactions between QCA cells to produce the desired output by utilizing an efficient 2-input XOR gate [11]. This section proposes new optimized structure for different reversible gates by exploiting the efficient 2-input XOR gate, as shown in Fig. 8.

3.1 Feynman Gate Realization

The logic diagram of the presented Feynman gate is shown in Fig. 9a, which maps inputs (A, B) to outputs (P = A, Q = A ⊕ B). And the corresponding QCA layout is illustrated in Fig. 9b that employs one 2-input XOR gate. Note that the proposed layout for the Feynman gate utilizes the new XOR structure without incorporating 3-input majority gates contrary to the prior designs.

3.2 Double Feynman Gate Realization

The schematic of the proposed Double Feynman gate is shown in Fig. 10a, which maps inputs (A, B, C) to outputs (P = A, Q = A ⊕ B, R = A ⊕ C). An optimal QCA layout for the gate with two 2-input XOR gate is illustrated in Fig. 10b using different colors of cells to specify four-phase clocking scheme. As shown in Fig. 10, in this structure output P does not need an additional gate; whereas two 2-input XOR gate require for the outputs Q and R. Note that the proposed layout for the Double Feynman gate uses the compact XOR structure without requiring 3-input majority gates contrary to the previous designs.

3.3 Toffoli Gate Realization

The schematic of the proposed Toffoli gate is shown in Fig. 11a, which maps inputs (A, B, C) to outputs (P = A, Q = B, R = AB ⊕ C). An optimal QCA layout for the gate is illustrated in Fig. 11b using different colors of cells to specify four-phase clocking scheme. It employs one 3-input majority gate along with one 2-input XOR gate. The 3-input majority gate computes the AND operation by exploiting the inputs A and B. The resulting intermediate output is expressed as

$$I_1 = MV\ (A, B, 0) = AB \tag{2}$$

The 2-input XOR gate receives input C and the intermediate value I_1 to compute the Toffoli gate's third output R that is given by

$$R = I_1\ XOR\ C \tag{3}$$

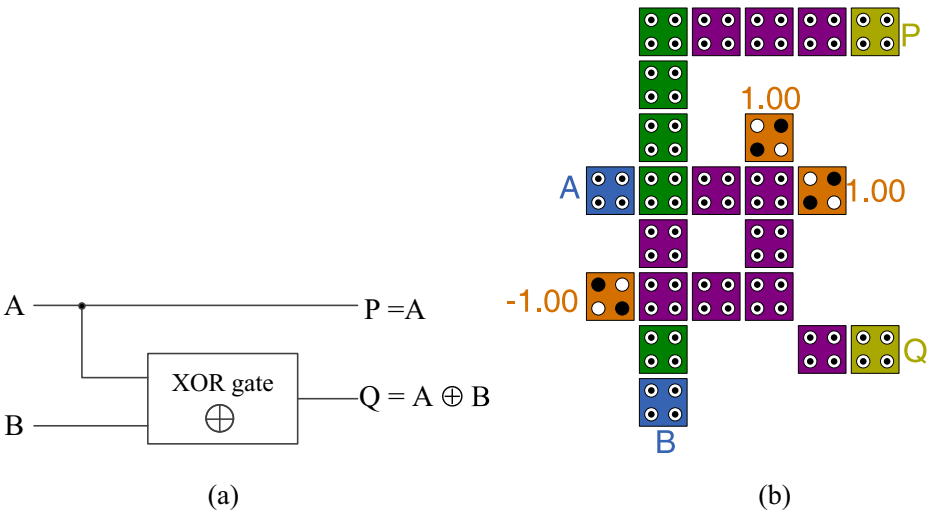


Fig. 9 **a** Schematic diagram of Feynman gate, **b** Proposed QCA layout for Feynman gate

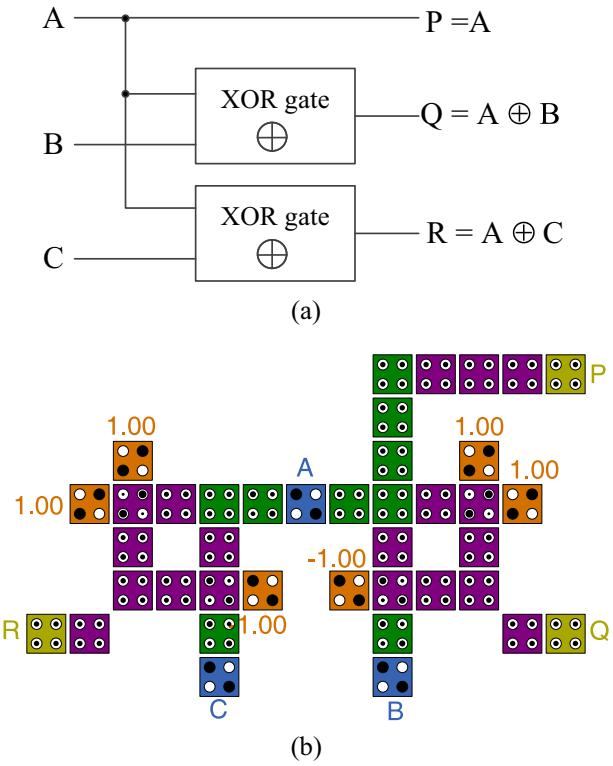


Fig. 10 **a** Schematic diagram of Double Feynman gate, **b** Proposed QCA layout for Double Feynman gate

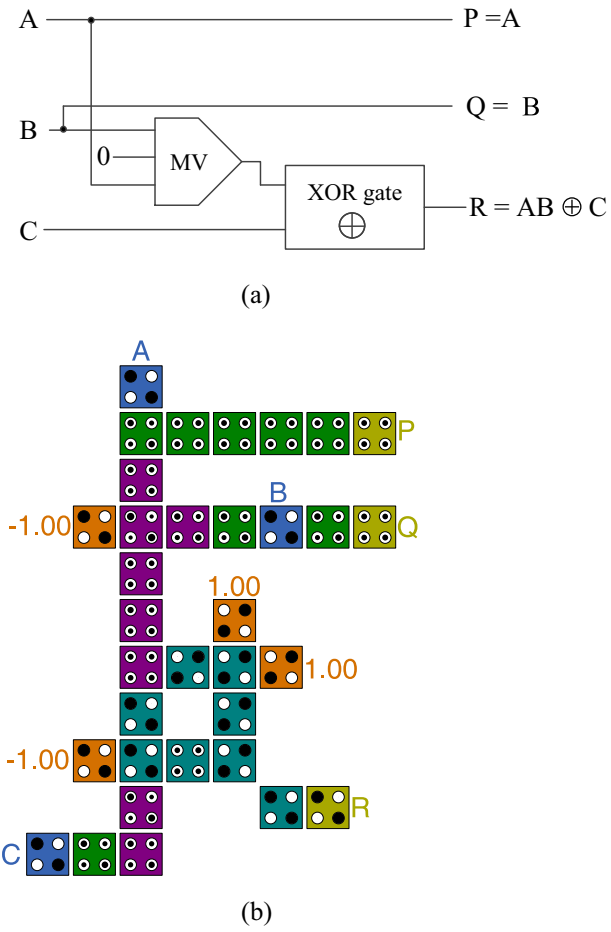


Fig. 11 **a** Schematic diagram of Toffoli gate, **b** Proposed QCA layout for Toffoli gate

4 Fredkin Gate Realization

The schematic of the Fredkin gate here presented involves an inverter, two 2-input XOR gates along with two 3-input majority gates which maps inputs (A, B, C) to outputs (P = A, Q = A′B + AC, R = AB + A′C), as depicted in Fig. 12a. As shown in Fig. 12, in this structure output P does not need an additional gate; whereas outputs Q and R exploit the 2:1 multiplexer architectures. The QCA layout of the optimal Fredkin gate is depicted in Fig. 12b using different colors of cells to specify four-phase clocking scheme. The output Q is computed as follows:

$$\begin{aligned} Q &= MV(A \oplus B, B, C) \\ &= MV(A'B + AB', B, C) \\ &= (A'B + AB')B + BC + C(A'B + AB') \\ &= A'B + A'BC + AB'C + BC = \Sigma(2, 3, 3, 5, 3, 7) = \Sigma(2, 3, 5, 7) = A'B + AC \end{aligned} \tag{4}$$

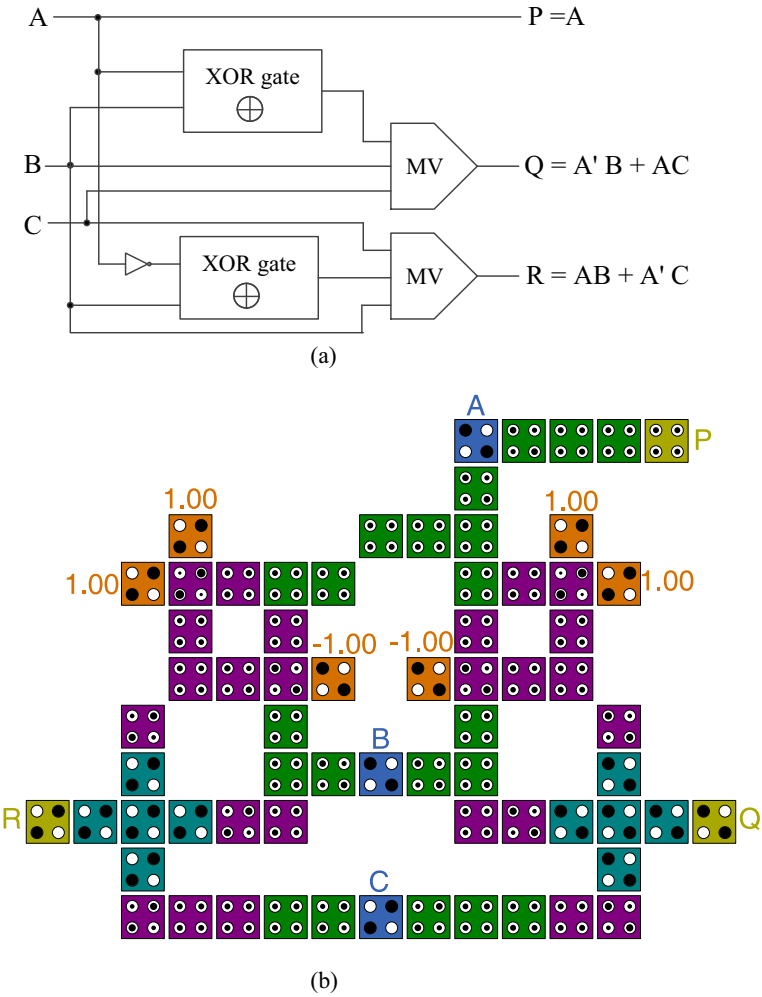


Fig. 12 **a** Schematic diagram of Fredkin gate, **b** Proposed QCA layout for Fredkin gate

The output R is expressed by

$$\begin{aligned} R &= MV(A' \oplus B, B, C) \\ &= MV(AB + A'B', B, C) \\ &= (AB + A'B')B + BC + C(AB + A'B') \\ &= AB + A'B'C + BC + ABC = \Sigma(1, 3, 6, 7) = AB + A'C \end{aligned} \tag{5}$$

4.1 Peres Gate Realization

The schematic of the proposed QCA Peres gate is shown in Fig. 13a, which maps inputs (A, B, C) to outputs (P = A, Q = A ⊕ B, R = AB ⊕ C). This design composed of one 3-input

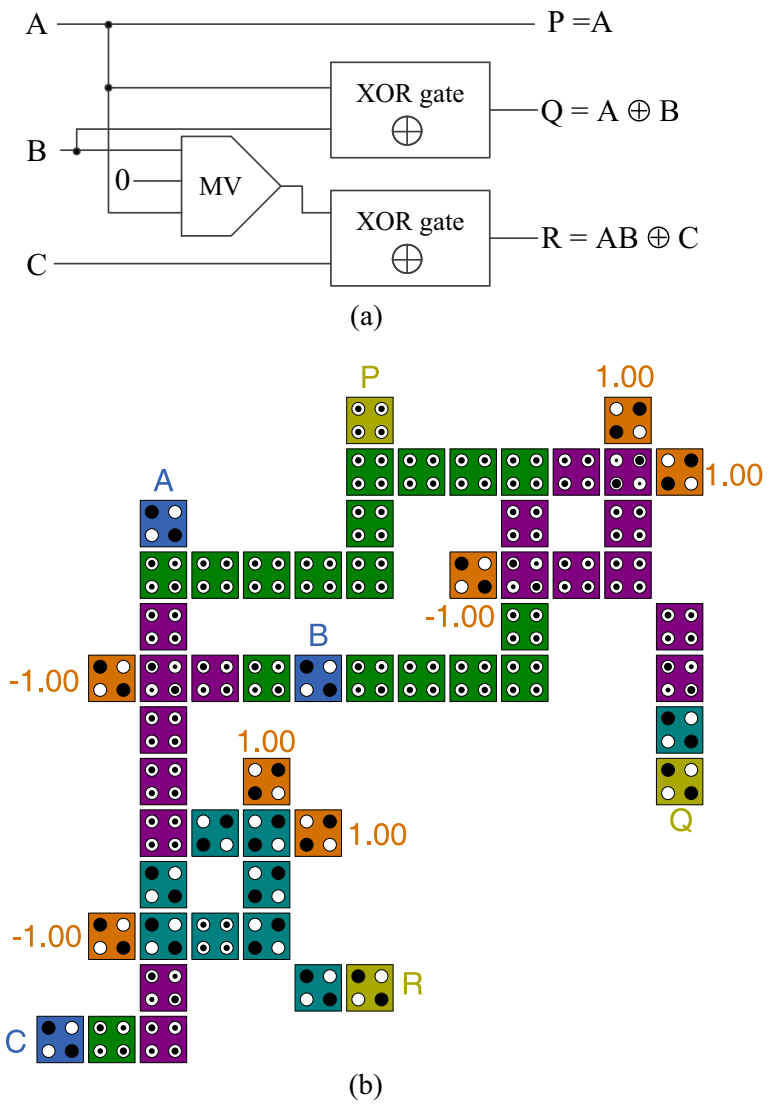


Fig. 13 **a** Schematic diagram of Peres gate, **b** Proposed QCA layout for Peres gate

majority gate and two 2-input XOR gates. Figure 13b shows the optimal QCA layout of the Peres gate using different colors of cells to specify four-phase clocking scheme.

5 Simulation and Results

All the proposed gates are implemented and verified using QCADesigner v2.0.3 considering Coherence vector simulation engine [26]. The parameters of the simulation are the default

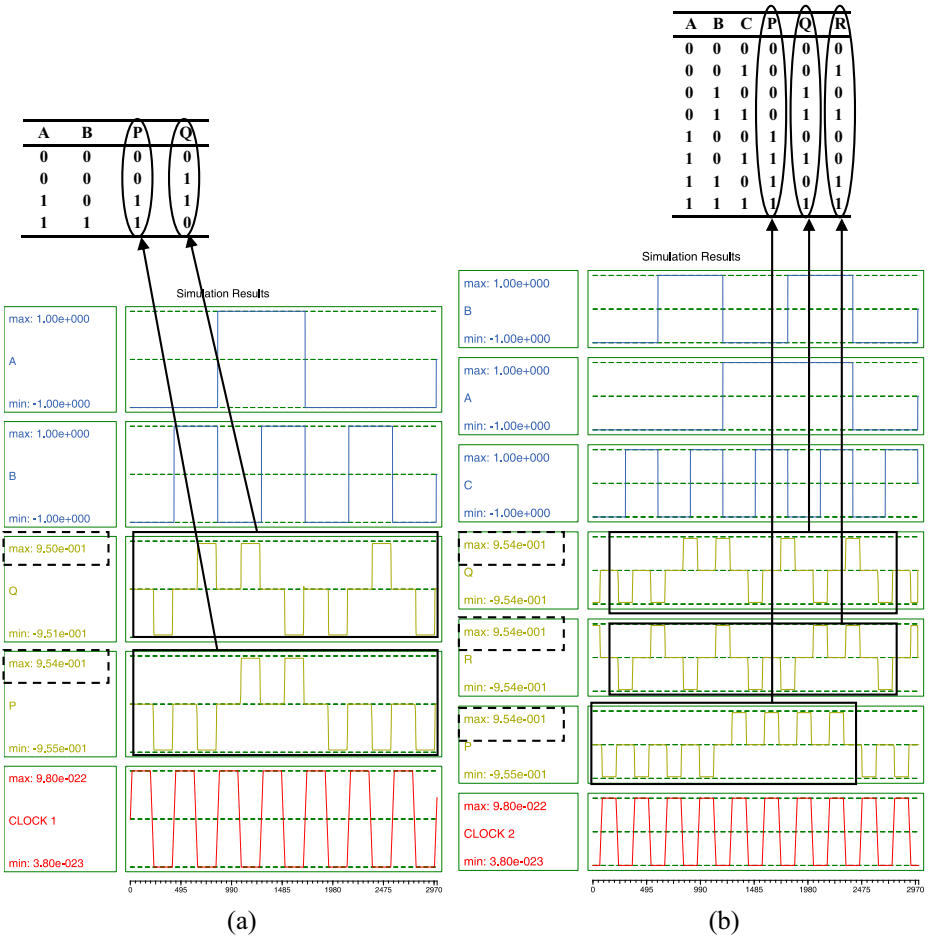


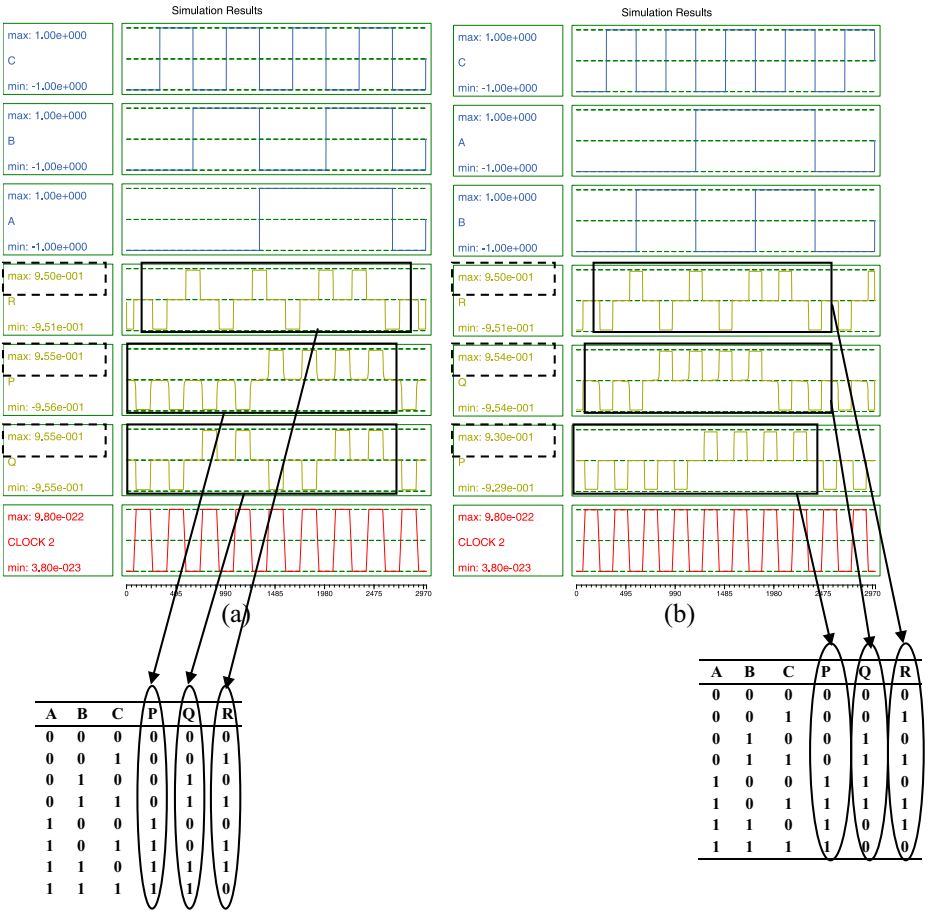
Fig. 14 Simulation results of the proposed **a** Feynman gate, **b** Fredkin gate

values used by QCADesigner. The input, output, and clock signals are represented by blue, green, and red colors respectively in all simulated waveforms.

The simulation results of the Feynman gate is depicted in Fig. 14a. From this figure, it can be seen that the circuit performs correctly in all possible input vectors, and the outputs are generated with delay of 2 clock phases indicated by black boxes. The Feynman gate has 23 cells and covers an area of 0.016 μm^2. All inputs are provided to the Feynman gate at clock zone 0 and the outputs are available at clock zone 1.

Figure 14b shows the simulation waveforms of the proposed Fredkin gate. It verifies the correct operation of the proposed gate and generates valid outputs after a latency of 3 clock phases as indicted by black boxes. The Fredkin gate uses only 68 cells and the spans over an area of 0.06 μm^2.

The QCADesigner based simulation result for the proposed 3-input Toffoli gate is shown in Fig. 15a. It verifies the correctness of the design as represented by black box and valid outputs are produced after three clock phases. The compact design consumes 34 cells and the area amounts to 0.034 μm^2.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	0

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Fig. 15 Simulation results of the proposed **a** Toffoli gate, **b** Peres gate

Figure 15b shows the simulation waveforms of the proposed Peres gate. It is worth noting that the outputs are produced after a latency of 3 clock phases. The inputs are fed to the Peres gate at clock zone 0 and the outputs are available at clock zone 2. The QCA layout uses 56 cells and occupies an area of 0.066 μm^2.

The simulation results of the Double Feynman gate is depicted in Fig. 16. From this figure, it can be seen that the circuit performs correctly in all the 8 triads of input vectors, and the outputs are produced within 2 clock phases indicated by black boxes with dashed lines. The proposed gate utilizes only 40 cells and spreads over an area of 0.045 μm^2. The inputs are fed to the Double Feynman gate at clock zone 0 and the outputs are available at clock zone 1.

It is noteworthy to state that simulation results obtained for all proposed designs achieve the expected highly polarized output displayed by the black box with dashed lines. The inputs for A, B, and C are 1.00e+000. The outputs P, Q, and R are from 9.30e-001 to 9.54e-001. This means that the output loses 5.1% to 7% of the input signal, which is in the acceptable noise margin. Hence, the proposed reversible designs maintain signal integrity with a high drivability attribute.

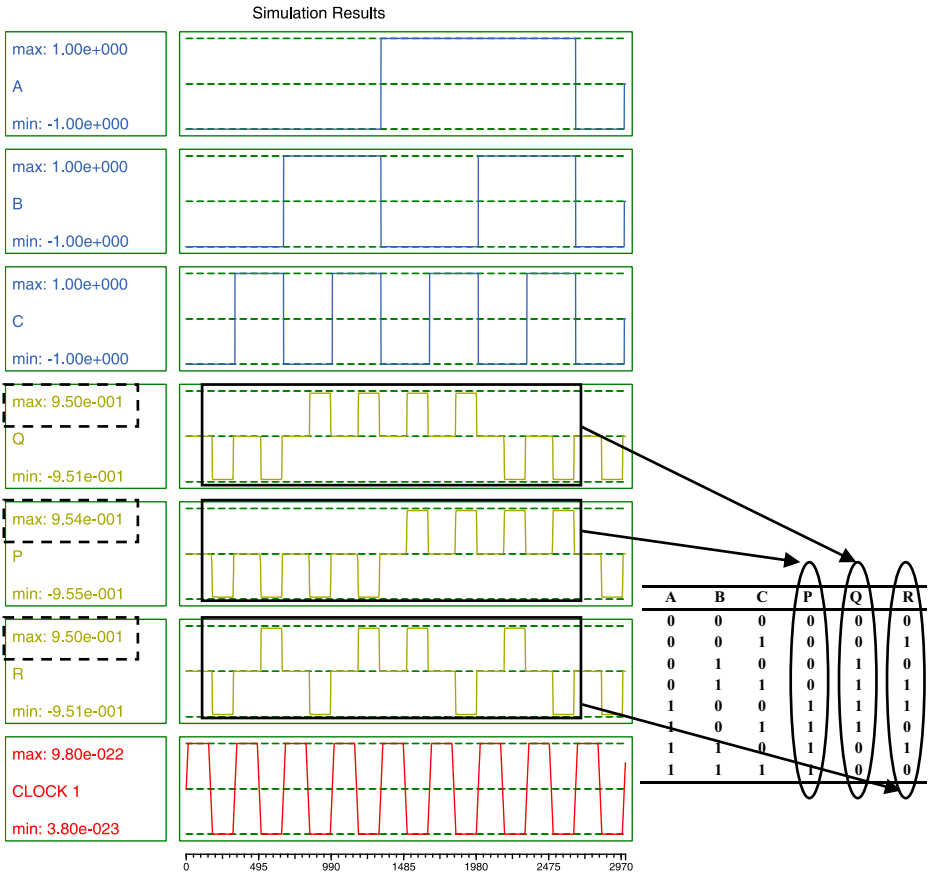


Fig. 16 Simulation results of the proposed Double Feynman gate

A comparison between the proposed designs and all prior designs is shown in Tables 6, 7, 8, 9 and 10 over different performance parameters. According to Tables 6–8, proposed design for Feynman, Toffoli, and Fredkin gates shows 28.12, 24.4, and 7% reduction in cell count and utilizes 46, 24.4, and 7.6% less area, respectively in comparison to the best designs [10]. Further, the delay of Fredkin, Toffoli gates is 0.75 clock cycles, which is equal to the delay of the previous best designs [10]. While the Feynman gate achieves delay of 0.5 clock cycles, which is superior to previous relevant works.

Regarding the cell count and area cover the proposed Peres gate is 44.32% and 12% less that the best designs in [9], as demonstrated in Table 9. In addition, comparison results of Double Feynman gates are reported in Table 10. The proposed Double Feynman gate achieves 21.5% and 25% optimizations in cell count and area over the existing design [16].

5.1 Power Analysis

To compute the power efficiency of proposed reversible gates and prior gates, QCAPro is utilized as a power estimator tool [27]. The power dissipation maps of the proposed reversible gates are shown in Fig. 17, where higher power dissipation is distinguished by

Table 6 Comparison of QCA Feynman gates

	Number of cells	Area(μm^2)	Delay(Clock cycles)	Wire Crossover in Cascade Design
[6]	78	0.09	1	Coplanar
[7, 17]	54	0.038	0.75	Multilayer
[5]	53	0.07	0.75	Coplanar/Multilayer
[8]	37	0.023	0.75	Coplanar/Multilayer
[16]	34	0.036	0.5	Coplanar/Multilayer
[10]	32	0.03	0.75	Not required
Proposed	23	0.016	0.5	Not required

Table 7 Comparison of QCA Toffoli gates

	Number of cells	Area(μm^2)	Delay(Clock cycles)	Wire Crossover in Cascade Design
[6]	170	0.23	1	Coplanar
[5]	57	0.06	0.75	Coplanar/Multilayer
[10]	45	0.045	0.75	Coplanar/Multilayer
Proposed	34	0.034	0.75	Coplanar/Multilayer

Table 8 Comparison of QCA Fredkin gates

	Number of cells	Area(μm^2)	Delay (Clock cycles)	Wire Crossover in Cascade Design
[6]	178	0.21	1	Coplanar
[16]	100	0.092	0.75	Coplanar/Multilayer
[5]	97	0.10	0.75	Coplanar/Multilayer
[10]	73	0.065	0.75	Coplanar/Multilayer
Proposed	68	0.06	0.75	Coplanar/Multilayer

Table 9 Comparison of QCA Peres gates

	Number of cells	Area(μm^2)	Delay(Clock cycles)	Wire Crossover in Cascade Design
[5]	117	0.18	0.75	Coplanar/Multilayer
[9]	97	0.075	1	Multilayer
Proposed	56	0.066	0.75	Coplanar/Multilayer

Table 10 Comparison of QCA Double Feynman gates

	Number of cells	Area(μm^2)	Delay(Clock cycles)	Wire Crossover in Cascade Design
[5]	93	0.19	0.75	Coplanar/Multilayer
[16]	51	0.06	0.5	Coplanar/Multilayer
Proposed	40	0.045	0.5	Not required

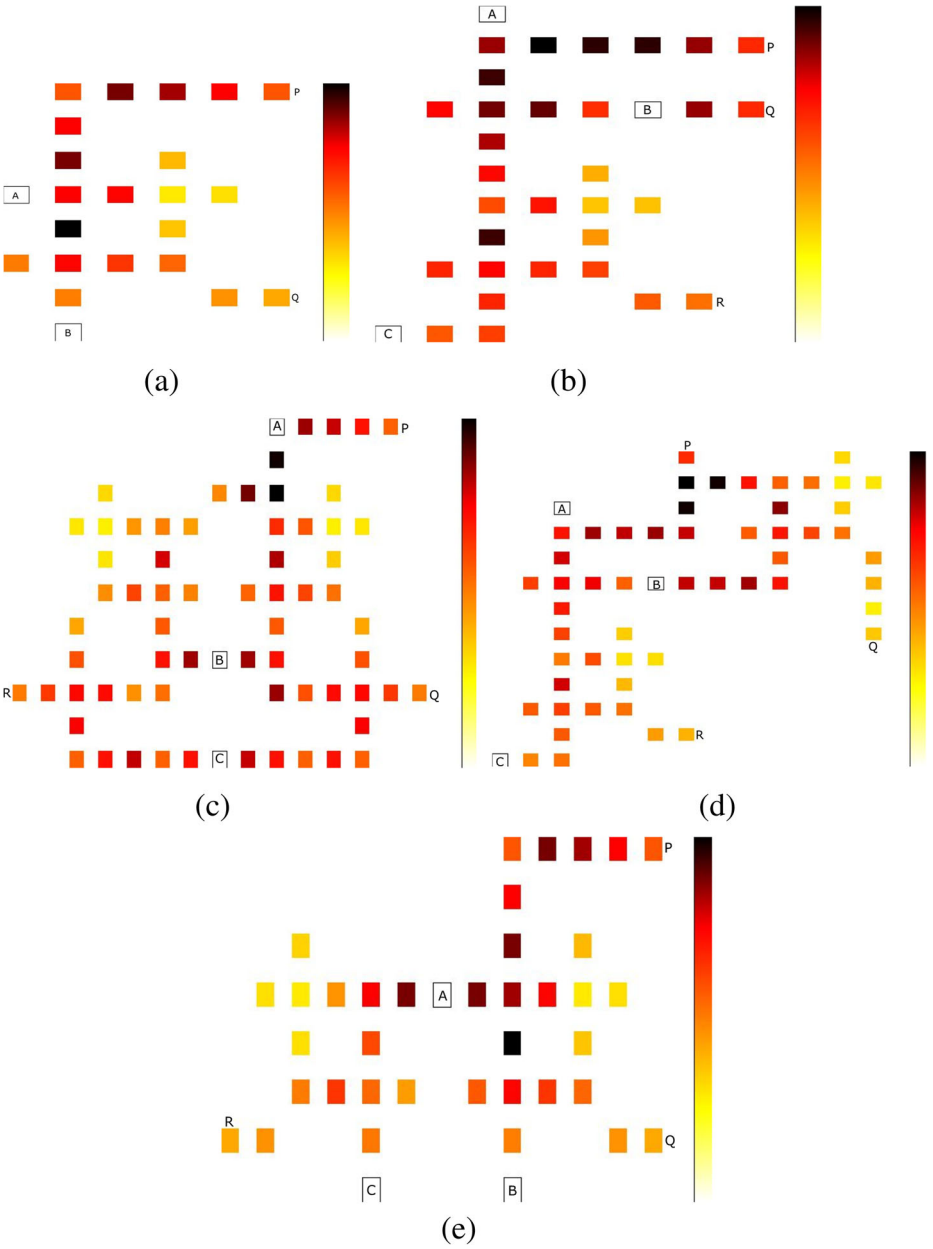


Fig. 17 Power dissipation maps for reversible gates with 1.0 E_k **a** Feynman, **b** Toffoli, **c** Fredkin, **d** Peres, **e** Double Feynman

darker colors in the thermal hotspot maps. These maps were produced in QCAPro tool by simulating all layouts over all possible test vector input for 1.0 E_k tunneling energy level and at 2.0 K temperature. A comparative analysis of leakage, switching, and average energy dissipation of the proposed gates with existing design is listed in Table 11. From

Table 11 Energy dissipation analysis of the proposed QCA reversible gates

Reversible gate	Average leakage energy dissipation (meV)		Average switching dissipation (meV)		Average energy dissipation (meV)	
	[10]	Proposed	[10]	Proposed	[10]	Proposed
Feynman	31.58	21.83	27.60	19.12	59.18	40.95
Toffoli	39.72	32.15	35.58	29.54	75.31	61.69
Fredkin	65.91	64	72.32	66	138.23	131.27
Peres	–	53.1	–	52.82	–	105.96

'–' not available

Table 11, it is clear that the proposed Feynman, Toffoli, and Fredkin gate has 30.80, 18.08, and 4.3%, respectively less average energy dissipation over the best previous one [10] for 1.0 E_k tunneling energy level at 2K temperature. Also the proposed Peres and Double Feynman gates consume average energy dissipation of 105.96 meV and 67.91 meV, respectively.

6 Conclusion

In this work, we have introduced area and power efficient reversible logic gates using QCA technology. The proposed designs achieved superior performance by incorporating a compact 2-input XOR gate. We examined the performance of the proposed designs and the previous relevant designs via the conventional metrics. The developed Feynman, Toffoli, and Fredkin gates gain 28.12, 24.4, and 7% reduction in cell count and consume 46, 24.4, and 7.6% less area, respectively compared to previous designs. The number of QCA cells (area consumption) of Peres gate and Double Feynman gates are 44.32% (12%) and 21.5% (25%) less than the best designs. Further, the delay of Fredkin and Toffoli gates is 0.75 clock cycles, which is equal to the delay of the previous best designs, whereas Feynman and Double Feynman gates achieve a delay of 0.5 clock cycles, equal to the best previous designs. The power analysis confirms that the proposed Feynman, Toffoli, and Fredkin gate has 30.80, 18.08, and 4.3%, respectively less average energy dissipation over the best previous one. Thus, the proposed optimal structures can enhance the overall performance of complex nanoscale circuits in QCA technology.

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