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# Novel design of reversible priority encoder in quantum dot cellular automata based on Toffoli gate and Feynman gate

**Jadav Chandra Das**[1,2] · **Debashis De**[2,3]



## Abstract

In accordance with Moore's law, the size of complementary metal oxide semiconductor (CMOS)-based devices keep shrinking to augment the density on the chip. This scaling influences the execution of CMOS device due to several constraints like energy dissipation and synchronization of different components of the device. In non-reversible logic gates, power loss is the major concerned. Interest in reversible logic-based circuit design is increased as it offers reduced heat dissipation. Quantum dot cellular automata (QCA) is the possible implementation platform for reversible circuits. An encoder is an important component of memory, for address decoding and encoding. In this article, reversible logic-based architecture of 4 to 2 and 8 to 3 priority encoder is proposed and implemented on QCA platform. To design the encoder circuit, a new QCA layout of Feynman gate and Toffoli gate has been employed. The proposed layout of Feynman gate and Toffoli gate outshines the existing state-of-the-art designs. Quantum cost and circuit cost estimation of those encoder circuits are also performed. QCADesigner tool has been used to validate the performance of the proposed QCA reversible encoders.

**Keywords** QCA · Majority logic · Reversible gate · Feynman gate · Toffoli gate · Priority encoder

✉ Jadav Chandra Das
jadav2u@gmail.com

Debashis De
dr.debashis.de@gmail.com

[1] Department of Computer Science and Engineering, Swami Vivekananda Institute of Science and Technology, Kolkata 700145, India

[2] Department of Computer Science and Engineering, West Bengal University of Technology, BF-142, Salt Lake, Sector-I, Kolkata 700064, India

[3] Department of Physics, University of Western Australia, Perth, Crawley, WA 6009, Australia

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## 1 Introduction

At the design levels like architectural design, circuit design, and process technology, the very large-scale integration (VLSI) is at high demand. Power consumption can be reduced by choosing proper logic during implementation of combinational circuits [1–5]. The reason is that power dissipation, transition activity, switching capacitance, and short-channel effects are mainly influenced with those logic styles. VLSI-based device fabrication persists in shrinking the sizes down to atomic scale and terahertz operational frequencies can be obtained if the device operates with electrons [6–8]. Still, a trade-off must be made between rising necessities of performance constraints and the featured size. The ultimate saturation of CMOS-based device is reached due to failure of decreasing device area and the disadvantageous property of quantum mechanical effects on nanoscale transistors [1–5]. In tiny transistors, inadmissible amount of energy leaks due to the highly narrow channels and ultra-slim insulating layers. Nanotechnology can be the possible alternatives to these trade-off difficulties. ITRS reported several possibilities: (1) double-electron-layer tunneling transistor (Deltt) implemented by Blount et al. [9] at NS Lab, (2) single-electron transistors (SET), (3) quantum cellular automata, and (4) single quantum flux logic. Reversible computation in a system can be performed only when the system comprises reversible gates. Landauer [10] proved that in an irreversible computation, a $k_B T \ln 2$ J of heat energy is produced due to loss of each bit of information, where $k_B$ = Boltzmann's constant and $T$ = absolute computing temperature. Bennett [11] showed that $k_B T \ln 2$ J energy would not dissipate when the computation is performed in a reversible way. QCA (quantum dot cellular automata) [12–16] is the possible implementation platform for reversible circuits. It is a new transistorless computation in nanotechnology [17–20]. QCA-based computation of information is basically unusual from existing established technologies. Actually, information is stored on the basis of polarity of square-shaped, small QCA cells that are set in a grid arrangement [21], as shown in Fig. 1a. Within a specific cyclic procedure, a cell's data are erased and a new cell's polarization is obtained through

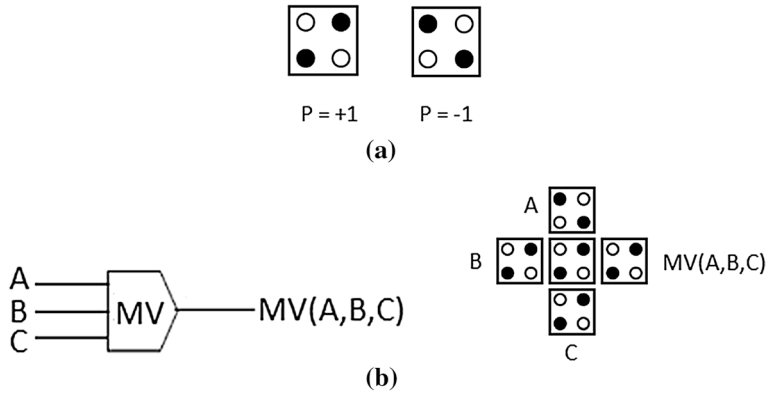



**Fig. 1** **a** QCA cell with its polarization structure, **b** QCA MV and its QCA layout

the surrounding cell's polarization, i.e., by electrostatic force termed as Coulomb interaction.

The QCA cell has four quantum dots sited at the corners having two free mobile electrons, which can tunnel between the dots [21], but cannot tunnel outside the cell due to the potential limit. Further, tunneling within QCA cell can be stopped temporarily, which leads to a stable state. In Fig. 1a, black color represents dots with electron that experience a mutual repulsion force due to the Coulomb interaction and establish themselves in such a position that can bring a stable state. Accordingly, an isolated QCA cell will have two stable states in which the Coulomb interaction is minimal. These stable states are termed cell's polarization and are represented with $P=-1$ for binary number '0' and $P=+1$ for binary number '1' (Fig. 1a). When multiple QCA cells are positioned close to each other cells, the cell's polarization is computed by the effect of other adjacent cell's polarization. This feature can be exploited in realization of different circuit components, such as three-input majority gate (MV), binary AND gate, and OR gate as shown in Figs. 1a and 2a, b, respectively [22]. Binary OR gate and AND gate is the special case of MV. As shown in Fig. 2, that if one input of MV is fixed to '1', then MV will act as binary OR gate, and if one input of MV is fixed to '0', then MV will act as binary AND gate. On the other hand, if QCA cells are placed at corner to each other, QCA inverter (IV) can be formed, as shown in Fig. 3a.

In order to execute different digital logic functions, a dedicated clocking scheme is required in QCA [22]. Typically, this clock as shown in Fig. 3b has four phases: (1) relax phase, where the cell remain in depolarized state that indicates there is no information within the cell; (2) switch phase, where the inter-dot obstacles are increased that force the cell to be polarized according to the surrounding cell's

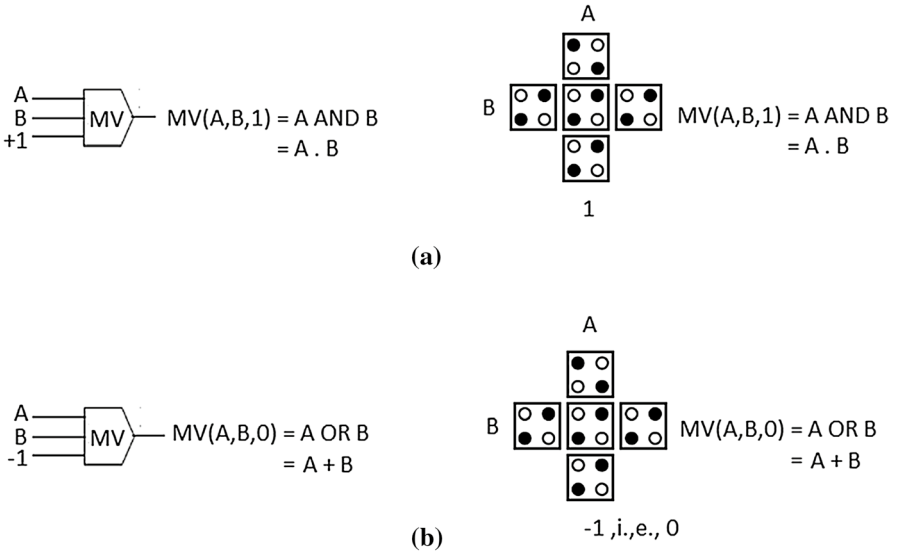



**Fig. 2** **a** QCA AND gate and its QCA layout, **b** QCA OR gate and its QCA layout

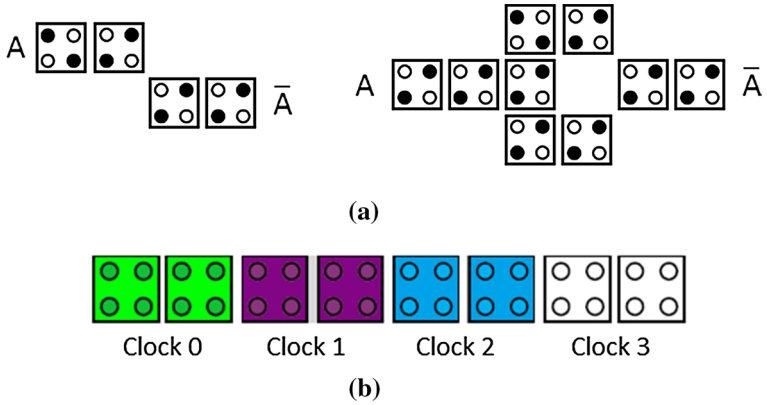



**Fig. 3** **a** Two types of QCA inverter, **b** QCA clocking

polarization; (3) hold phase, where the cell has stable polarization and may operate as input to the adjacent cells; and (4) release phase, where the inter-dot barriers become lowered again and thus removed the previously obtained cell's polarization. To enable the data propagation among cells, multiple phase-shifted category of the QCA clock signal is presented [23]. Information flow can be controlled by appropriate shift of clock signals. For example, when one cell is in hold phase, at the same time, the other cell can be in either switch phase, relax phase, or release phase. Normally multiple contiguous cells are clustered to different clock zones in which all the cells use the identical clock signal.

This article is organized as follows. The major contributions of the article are explored in Sect. 2. Realization of Feynman gate and Toffoli gate in QCA is performed in Sect. 3. The proposed reversible design of 4 to 2 and 8 to 3 priority encoder and its QCA realization are demonstrated in Sect. 4. Circuit complexity, quantum cost estimation, and comparisons with state-of-the-art design are explored in Sect. 5. Lastly, the conclusion and future work is portrayed in Sect. 6.

## 2 Contributions of the article

Priority encoders are useful to handle all input combinations of a system, i.e., arrangement of functional units of the system, in accordance with the number, nature, and primary characteristics. Priority encoder reduces the number of wires in a specific circuit that have multiple inputs. Several works report the incorporation of reversible logic in QCA [24–30]. Oskouei et al. [24] propose a novel design of ALU with reversible gates. The proposed architecture is designed with multilayer (three levels) approach having AND gate, OR gate, XOR gate, and full adder as basic building blocks. The approach [24] has 28% reduced cell count and 51% reduced area in comparison with the other QCA ALU designs. Two-bit reversible QCA counter using an improved reversible logic gate has been reported by Moharrami et al. [25], which has lower clock delay in contrast with the previous designs. The

new reversible full adder circuit in QCA platform is also reported by the researchers [26]. The design is based on robust single-layer crossover approach. Further, reversible ripple-carry (RCA) adder having different sizes like 4 bits, 8 bits, and 16 bits is designed with the full adder. The RCAs have a 33% reduction to the garbage outputs. QCA is explored as an implementation platform for reversible circuits [27]. A new reversible gate is implemented in [27] and verified through three variable-based 13 standard Boolean functions. A novel reversible full adder/subtractor unit is also reported by the researchers [28]. The full adder/subtractor unit has minimum cell count than other designs. This work reported by Singh et al. [29] demonstrates the non-restoring divider design using Feynman gate and HNG gate and its QCA implementation. These divider circuits have fewer garbage outputs and reduce quantum cost compare to few of the existing works. In [30], the reversible multiplier that can multiply two ternary numbers (unsigned two-digit number) has been reported. The multiplier is made up with a component called TPPG to attempt optimization in terms of quantum cost, constant inputs, and garbage outputs.

This article describes an efficient nanoscale design and analysis of reversible priority encoder based on QCA. The proposed designs are implemented using clock-zone-based wire crossing approach [19], which reduces the circuit complexity and useful to avoid multilayer approach in QCA. Besides, incorporating reversible logic in QCA can provide low-power nanoscale design of digital circuits, because reversible logic that can control the information flow through the system is considered suitable to achieve the ultra-low-power consumption structures. The major contributions of this article are as follows.

1. Design of new QCA layout of Feynman gate and Toffoli gate.
2. Design of 4 to 2 and 8 to 3 reversible priority encoder and their QCA implementation.
3. Quantum cost and circuit cost estimation of those circuits.
4. Comparison of proposed Feynman gate and Toffoli gate with state-of-the-art designs.
5. Validation of proposed design with QCAdseigner tool.

## 3 Reversible gates with QCA

In this section of the research paper, the implementation of the Feynman gate and Toffoli gate in QCA, its circuit design, and simulation result are discussed which are given as.

### 3.1 Feynman gate

Feynman gate (FG) is a $2 \times 2$, i.e., 2 inputs, 2 outputs reversible gate. The block diagram is described in Fig. 4a [31, 32]. Here, (A, B) are the inputs. P and Q are the outputs which defined as $P = A$, $Q = A \oplus B$, where $\oplus$ means binary XOR operation. The quantum cost of a FG is one. FG can act as copying gate, i.e., this gate

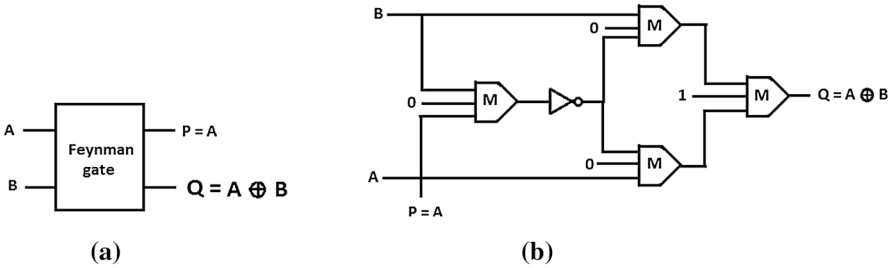



**Fig. 4** FG. **a** Block diagram, **b** QCA schematic

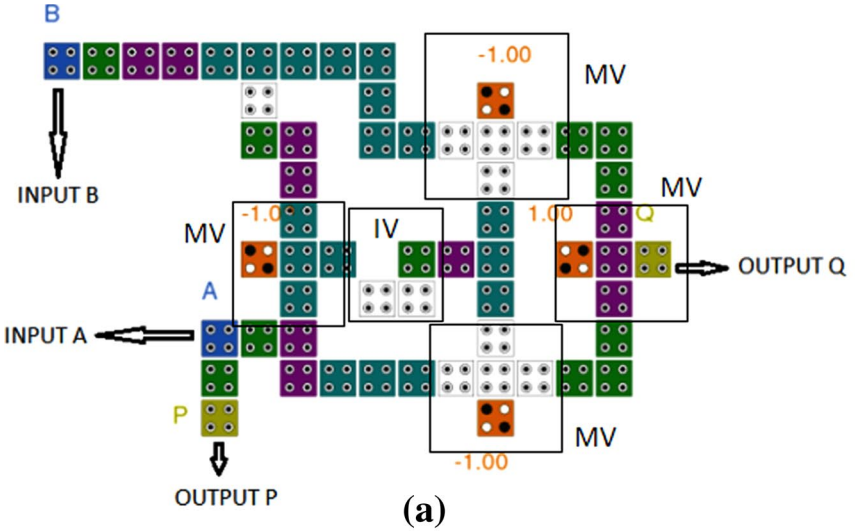
is functional for replication of the intended outputs. The QCA design of FG corresponding to Fig. 4a is shown in Fig. 4b. The equivalent QCA layout is shown in Fig. 5a. The implementation and simulation are performed on QCADesigner tool [33], i.e., the tool used to verify the design of QCA circuits. This layout has four MVs and one IV outlined with rectangular boxes. It consumes 58 cells, 0.064 $\mu m^2$ area, and four clock cycles, i.e., 1.5 clocks delay.

The QCADesigner-based simulated outcome is shown in Fig. 5b. In Fig. 5b, it is observed that the correct values at Q appear after clock delay. Figure 5b shows that when the inputs are A = 0, and B = 0, the outputs are P = 0, and Q = 0. When A = 0, and B = 1, the outputs are P = 0, and Q = 1. When A = 1, and B = 0, the outputs are P = 1, and Q = 1. When A = 1, and B = 1, the outputs are P = 1, and Q = 0. These results satisfy the theoretical values. Thus, the circuit operates efficiently.

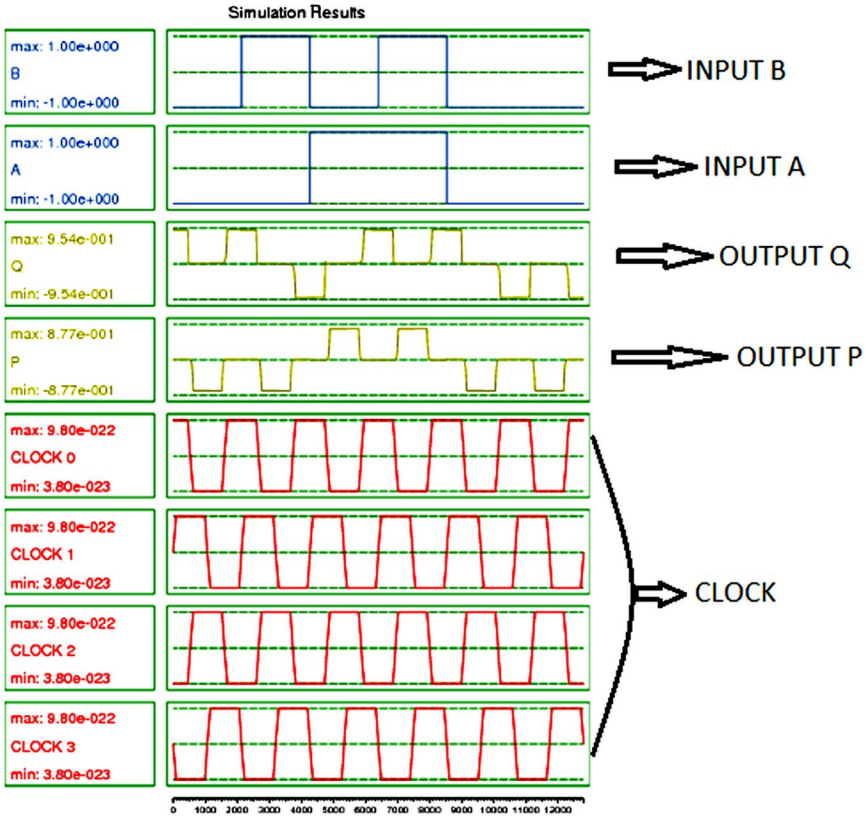
### 3.2 Toffoli gate

Toffoli gate (TG) is a 3 × 3, i.e., 3 inputs, 3 outputs reversible gate [34]. The block diagram of TG is shown in Fig. 6a, in which A, B, C are the inputs and P, Q, R are the outputs. The outputs are defined as P = A, Q = B, and R = A • B ⊕ C, where '•' sign represent binary AND operation and ⊕ means binary XOR operation. The quantum cost of TG is five. The QCA design of TG corresponding to Fig. 6a is shown in Fig. 6b. The equivalent QCA layout is shown in Fig. 7a. The implementation and simulation are performed on QCADesigner tool [33]. This design has five MVs and one IV outlined with rectangular boxes. It consumes 64 cells, 0.088 $\mu m^2$ area and 4 clock cycles, i.e., 1.5 clocks delay. This TG is further used as a basic building block in designing of 4 to 2 and 8 to 3 reversible priority encoders.

Figure 7b shows the QCADesigner-based simulated outcome of TG. In Fig. 7b, it is observed that the correct values of R appear after one clock delay. Figure 7b shows that when the inputs are A = 0, B = 0, and C = 0, the outputs are P = 0, Q = 0, and R = 0. When A = 0, B = 0, and C = 1, the outputs are P = 0, Q = 0, and R = 1. When the inputs are A = 0, B = 1, and C = 0, the outputs are P = 0, Q = 1, and R = 0 and so on. These results satisfy the theoretical values. Thus, the circuit operates efficiently.




(a)




(b)

**Fig. 5** FG. **a** QCA layout, **b** simulation result

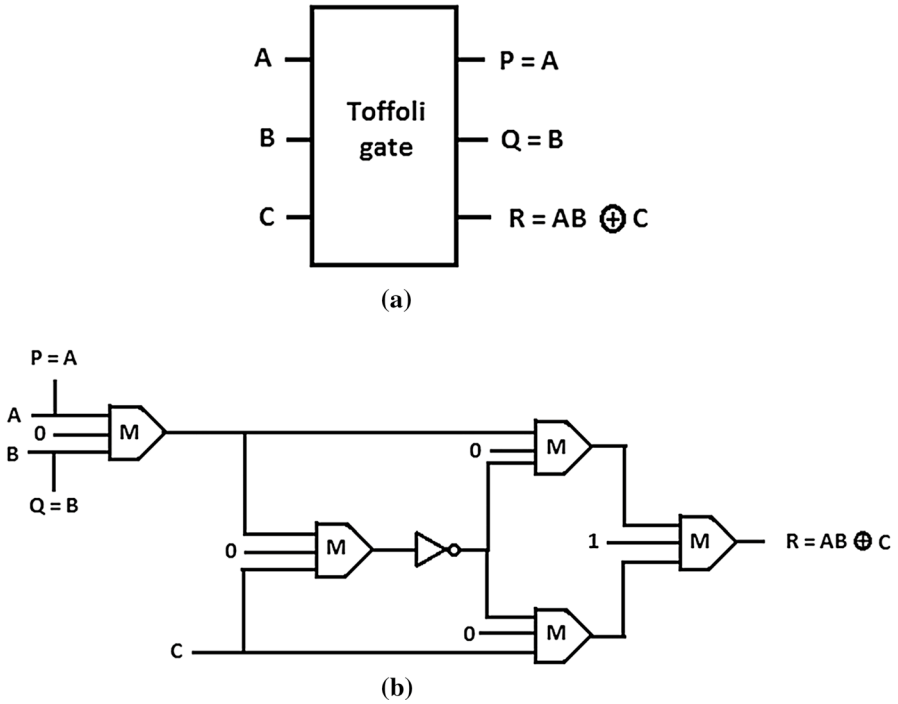



**Fig. 6** Toffoli gate. **a** Block diagram, **b** QCA schematic

## 4 Proposed work

This section illustrates the design of two reversible priority encoders, i.e., 4 to 2 and 8 to 3 reversible priority encoders. Besides, its implementation in QCA and the design is achieved based on Feynman and Toffoli gates.

### 4.1 4 to 2 Reversible priority encoder

A priority encoder [35] is a circuit or algorithm which basically compressed multiple binary inputs into a smaller number of outputs. A 4 to 2 priority encoder has four input lines I3, I2, I1, and I0 and two output lines Y0 and Y1. The block diagram is shown in Fig. 8.

The logic expression for outputs Y1 and Y0 can be drawn as

$$Y1 = I2 + I3 \tag{1}$$

$$Y0 = \overline{I2} \bullet I1 + I3 \tag{2}$$

In Eqs. (1)–(2), '+' and '•' signs represent binary OR and binary AND operation, respectively. Equation (1) shows that Y1 requires one OR operation, whereas Eq. (2) shows that Y0 requires one AND operation and one OR operation. Thus, by

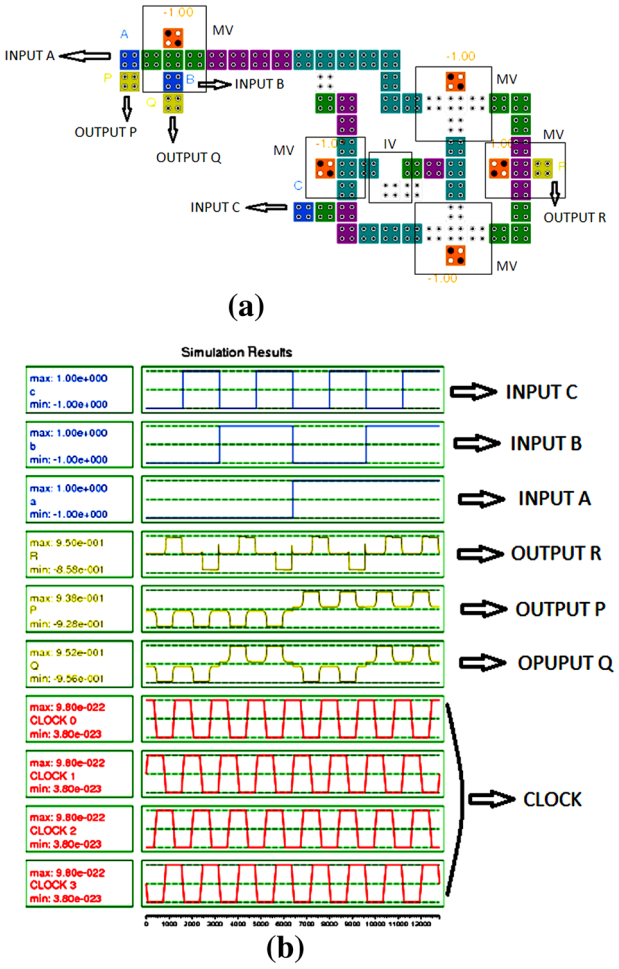



**Fig. 7** Toffoli gate. **a** QCA layout, **b** simulation result

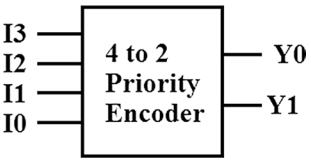



**Fig. 8** Block diagram of 4 to 2 priority encoder

cascading three TG, the reversible circuit for 4 to 2 priority encoder can be achieved, as shown in Fig. 9. Six garbage outputs are present in the proposed design of reversible 4 to 2 priority encoder. In Fig. 9, Y0 is represented with the term "FINAL". The similar QCA design and layout are shown in Fig. 10a, b, respectively. Clock-zone-based wire crossing approach [19] is used to achieve the QCA layout of 4 to 2 reversible priority encoder (Fig. 10b). The implementation and simulation are

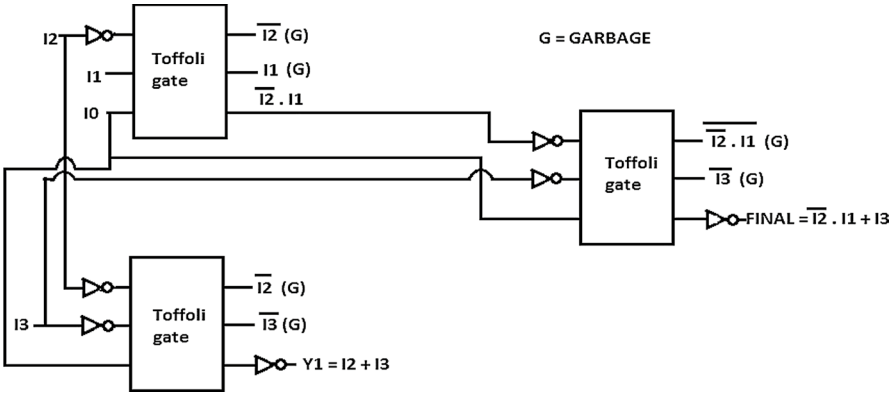



**Fig. 9** Block diagram of 4 to 2 reversible priority encoder

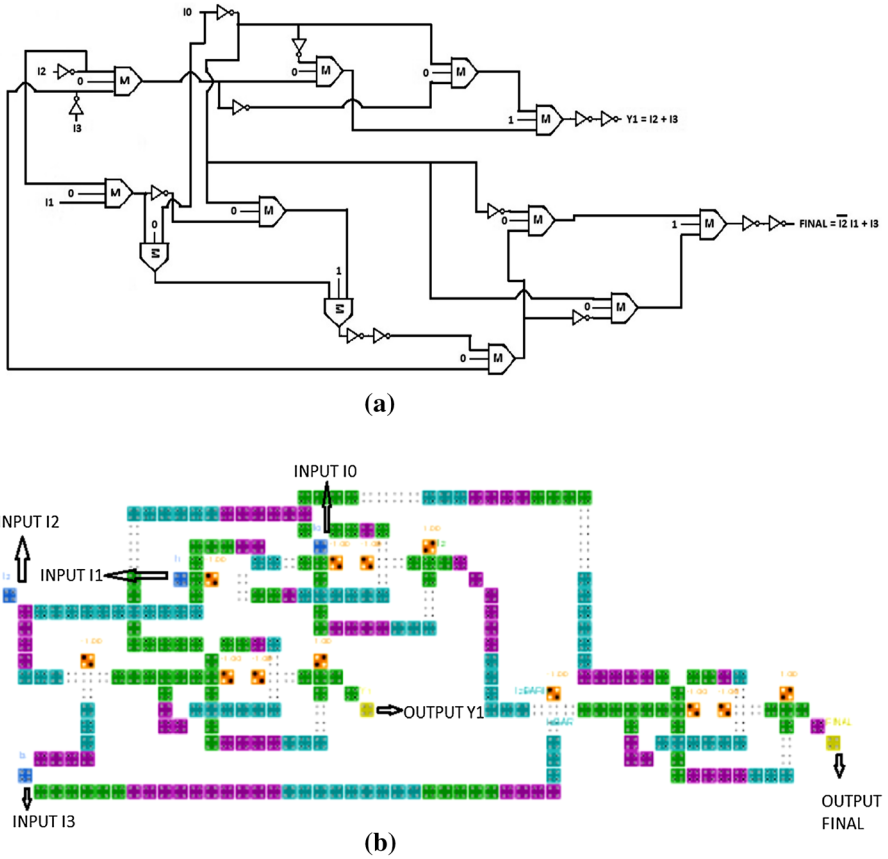



**Fig. 10** 4 to 2 reversible priority encoder. **a** QCA design, and **b** QCA layout

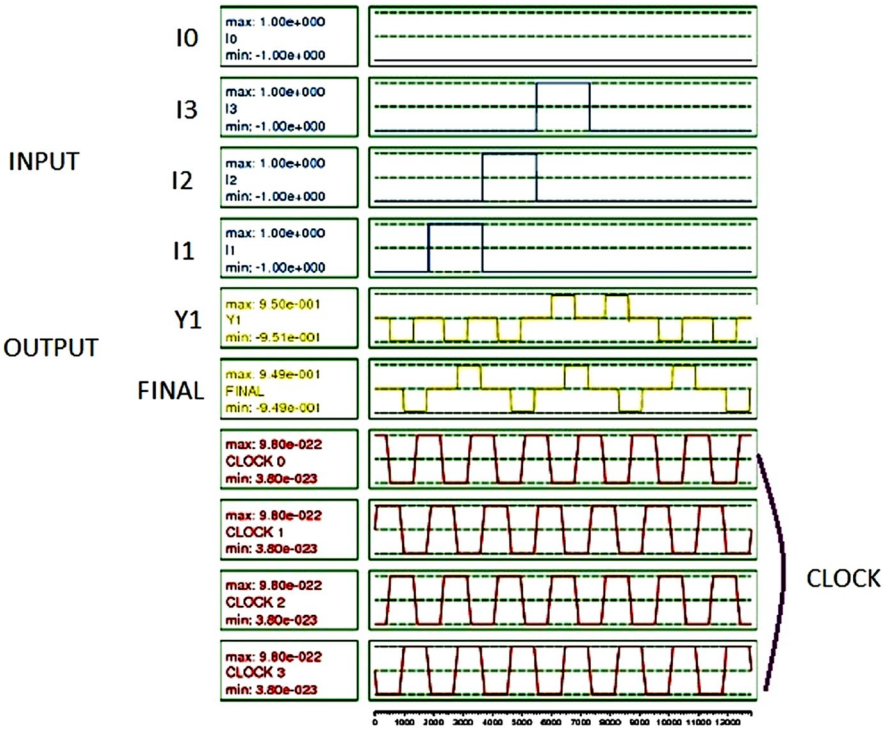



**Fig. 11** Simulation result of 4 to 2 reversible priority encoder

performed on QCADesigner tool [33]. The QCA layout of 4 to 2 reversible priority encoder has twelve MVs and seventeen IVs outlined with rectangular boxes. It consumes 277 cells, 0.418 $\mu m^2$ area and 13 clock cycles, i.e., 3.25 clocks delay.

The QCADesigner-based simulated waveform is depicted in Fig. 11. It can be noted that the required output for Y1 appears after one clock cycle delay. Figure 11 shows that when the inputs are I3 = 0, I2 = 0, I1 = 0, and I0 = 1, the outputs are Y1 = 0 and Y0 = 0. When I3 = 0, I2 = 0, I1 = 1, and I0 = 0, then Y1 = 0 and Y0 = 1. These results satisfy the Eqs. (1–2), i.e., the theoretical values of 4 to 2 priority encoder. Thus, the circuit performs accurately.

### 4.2 8 to 3 Reversible priority encoder

A 8 to 3 priority encoder has eight input lines D7–D0 and three output lines Q0, Q1, and Q2 [35]. The block diagram is presented in Fig. 12.

The logic expression for the outputs Q2, Q1, and Q0 can be drawn as

$$Q2 = D5 + D7 + D4 + D6 \tag{3}$$

$$Q1 = D3 + D7 + D2 + D6 \tag{4}$$

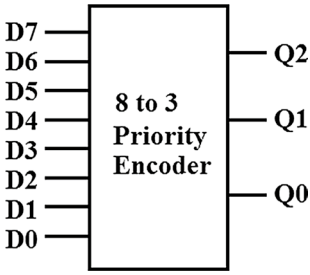



**Fig. 12** Block diagram of 8 to 3 priority encoder

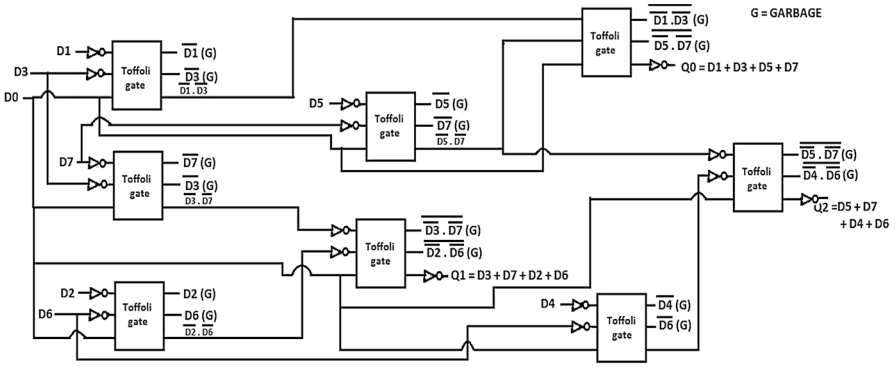



**Fig. 13** Block diagram of 8 to 3 reversible priority encoder

$$Q0 = D1 + D3 + D5 + D7 \tag{5}$$

In Eqs. (3)–(5), '+' sign means binary OR operation. Equations (3)–(5) show that to produce the outputs Q2, Q1, and Q0, four OR operations are required. Thus, by cascading eight TG the reversible circuit for 8 to 3 priority encoder can be achieved, as shown in Fig. 13. This reversible design has sixteen garbage outputs. The QCA design and QCA layout are shown in Figs. 14 and 15, respectively. Clock-zone-based wire crossing approach [19] is used to achieve the QCA layout of 8 to 3 reversible priority encoder (Fig. 15). The implementation and simulation are performed on QCADesigner tool [33]. The QCA layout of 8 to 3 reversible priority encoder has 40 MVs and 20 IVs outlined with rectangular boxes. It consumes 964 cells, 2.36 $\mu m^2$ area, and 32 clock cycles, i.e., 8 clocks delay.

The QCADesigner-based simulated wave form is depicted in Fig. 16. It can be noted that the required output for Y1 is appeared after one clock cycle delay. Figure 13 shows that when the inputs are D7 = 0, D6 = 0, D5 = 0, D4 = 0, D3 = 0, D2 = 0, D1 = 0 and D0 = 1, the outputs are Q2 = 0, Q1 = 0, and Q0 = 0. When D7 = 0, D6 = 0, D5 = 0, D4 = 0, D3 = 0, D2 = 0, D1 = 1 and D0 = 0, the outputs are Q2 = 0, Q1 = 0, and Q0 = 1. These results satisfy the theoretical values of 8 to 3 priority encoder as shown in Eqs. (3)–(5). Thus, the circuit performs accurately.

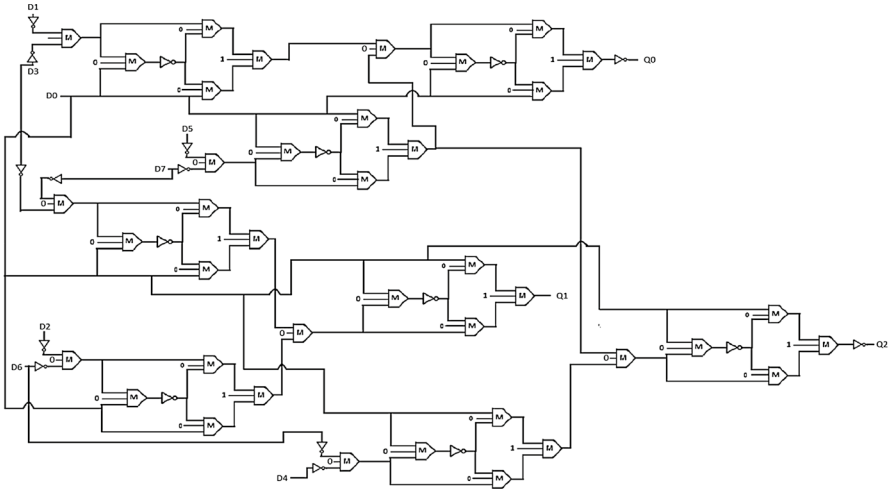



**Fig. 14** QCA circuit diagram of 8 to 3 reversible priority encoder

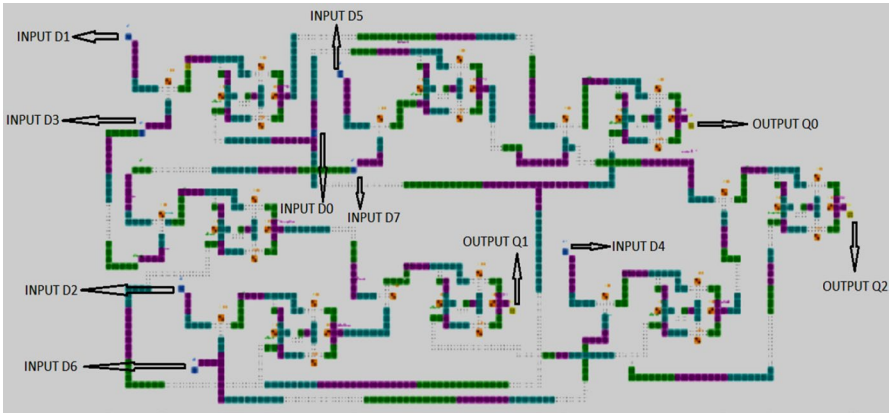



**Fig. 15** QCA layout of 8 to 3 reversible priority encoder

## 5 Results and discussion

In this section of the study, we will focus on the result generated by the 4 to 2 and 8 to 3 reversible priority encoder using QCADesigner tool [33]. Circuit complexity, cost estimation, and comparison with existing layouts have also been performed in this section.

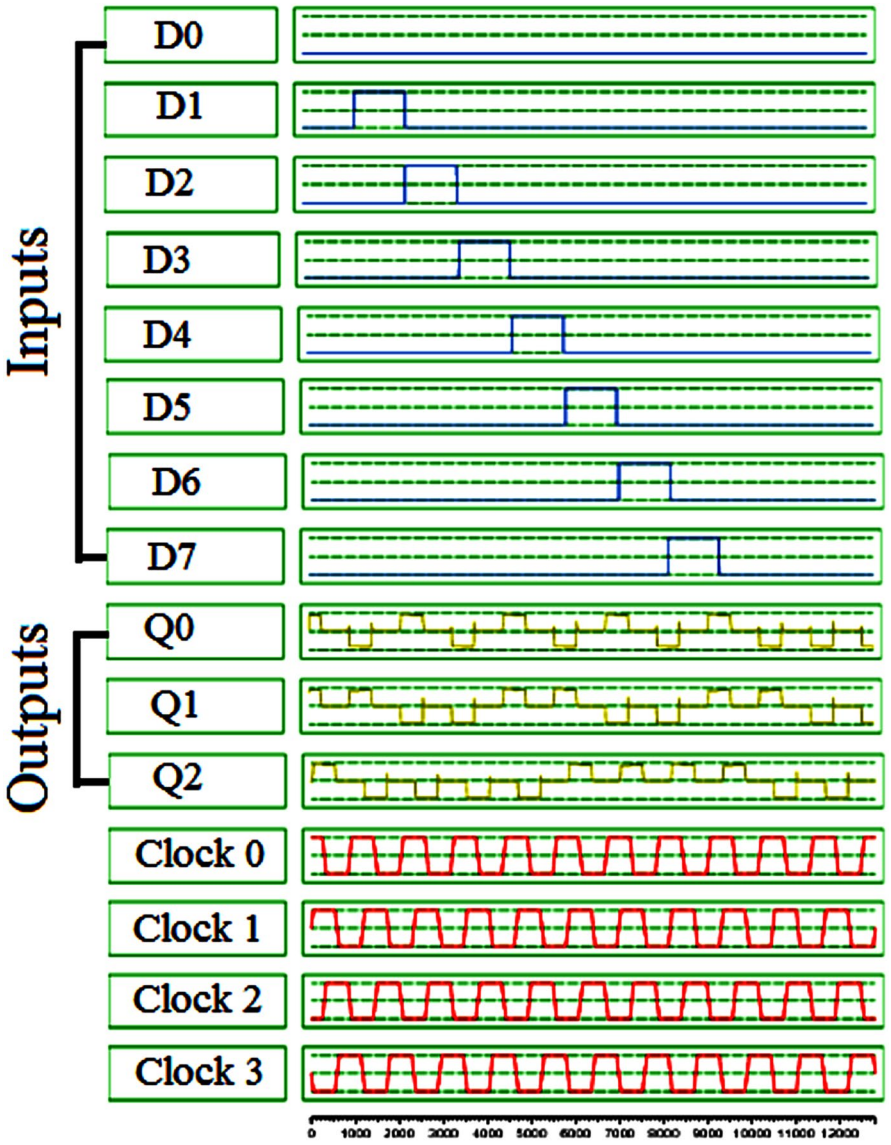



**Fig. 16** Simulation result of 8 to 3 reversible priority encoder

### 5.1 Circuit complexity

Number of QCA cells, total area, cell area, area coverage, and the clock delay of FG, TG, 4 to 2 reversible priority encoder, and 8 to 3 reversible priority encoder have been calculated and are plotted in Table 1. QCA layout generated by the QCADesigner tool [33] is analyzed to estimate the values presented in Table 1. For example,

**Table 1** Circuit complexity of proposed reversible priority encoders

| QCA circuit | Used MV and IV | Cell count | Total area ($\mu m^2$) | Cell area ($\mu m^2$) | Area coverage (%) | Clock delay |
|---|---|---|---|---|---|---|
| FG | 4 MVs and 1 IV | 58 | 0.064 | 0.0232 | 36.25 | 1.5 |
| TG | 5 MVs and 1 IV | 64 | 0.088 | 0.0256 | 28.40 | 1.5 |
| 4 to 2 Priority encoder | 12 MVs and 17 IVs | 277 | 0.418 | 0.1108 | 26.50 | 3.25 |
| 8 to 3 Priority encoder | 40 MVs and 20 IVs | 964 | 2.36 | 0.3856 | 16.10 | 8 |

**Table 2** Quantum cost and QCA circuit cost of proposed encoders

| Proposed circuit | Quantum cost | No. of garbage output | QCA circuit cost (total area × latency$^2$) |
|---|---|---|---|
| 4 to 2 Priority encoder | 15 | 6 | 4.42 |
| 8 to 3 Priority encoder | 40 | 16 | 151.04 |

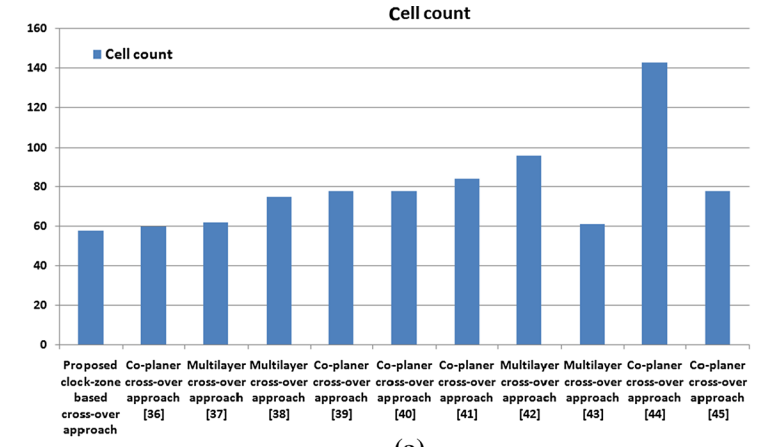
**Table 3** Proposed FG and existing layouts

| QCA FG | Cell count | Area (μm$^2$) | Clock delay |
|---|---|---|---|
| Proposed clock-zone-based crossover approach | 58 | 0.064 | 1.5 |
| Co-planer crossover approach [36] | 60 | 0.078 | 1.0 |
| Multilayer crossover approach [37] | 62 | 0.11 | 1.0 |
| Multilayer crossover approach [38] | 75 | 0.08 | 1.0 |
| Co-planer crossover approach [39] | 78 | 0.073 | 1.0 |
| Co-planer crossover approach [40] | 78 | 0.09 | 1.0 |
| Co-planer crossover approach [41] | 84 | 0.09 | 1.0 |
| Multilayer crossover approach [42] | 96 | 0.10 | Not specified |
| Multilayer crossover approach [43] | 61 | 0.073 | 1.0 |
| Co-planer crossover approach [44] | 143 | 0.26 | 1.0 |
| Co-planer crossover approach [45] | 78 | 0.083 | 1.0 |

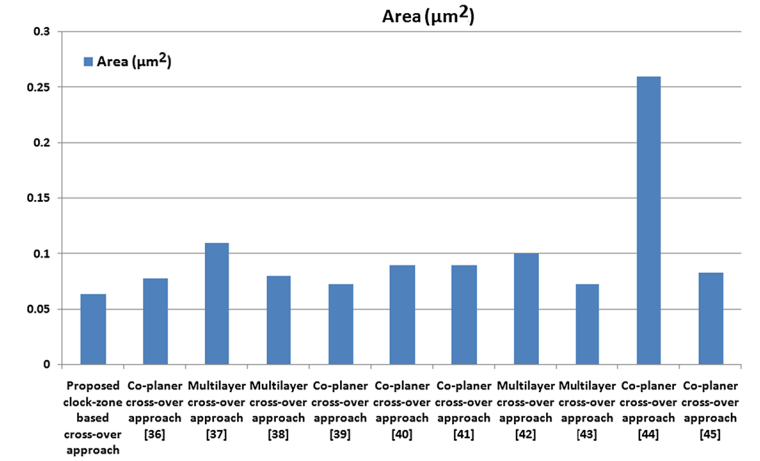
consider the QCA layout of FG (Fig. 5a). The layout comprises of four majority gates, one QCA inverter outlined with rectangular boxes and 58 QCA cells. The layout of FG has a length of 16 nm and height of 10 nm. As each QCA cell has dimension of 20 nm × 20 nm [33], the total area consumed by the layout of FG will be $16 \times 10 \times 20 \times 20$ nm$^2$, i.e., 64,000 nm$^2 \approx 0.064$ μm$^2$. Similarly, as the layout of FG contains 58 QCA cells, the cell area consumed by the layout of FG will be $58 \times 20 \times 20$ nm$^2$, i.e., 23200 nm$^2 \approx 0.0232$ μm$^2$. Therefore, area coverage will be ((cell area/total area) × 100), i.e., $((0.023/0.064) \times 100) \approx 36.25\%$. Figure 2a also shows that 6 clock cycles are required to produce the correct outputs. Now, 4 clock cycles are equivalent to 1 clock delay [33], thus the layout of FG has 1.5 clocks delay. In a similar approach, the estimation of circuit complexity for rest of the proposed designs has been performed.

### 5.2 Quantum cost

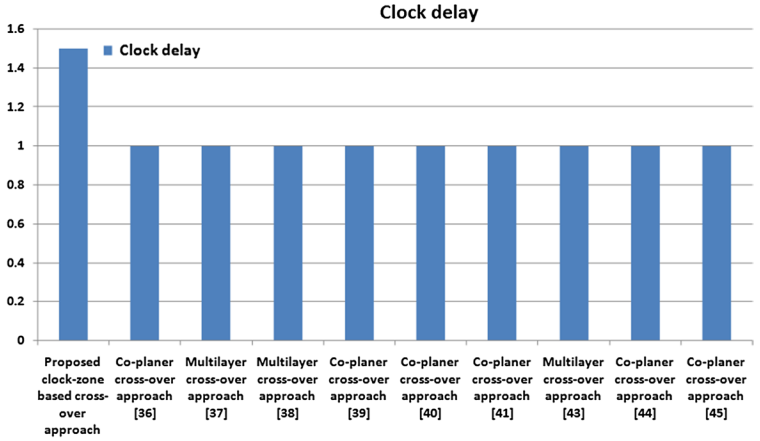
The quantum cost of TG is five. Now, 4 to 2 priority encoder contains three TG. Thus, the quantum cost of 4 to 2 priority encoder is $(3 \times 5 = 15)$ 15. On the other hand, 8 to 3 priority encoder is made up with eight TG. So, the quantum cost of 8 to 3 priority encoder is $(8 \times 5 = 40)$ 40. The result is shown in Table 2. The corresponding QCA circuit cost is also estimated through Table 2.




(a)




(b)




(c)

**Fig. 17** Proposed FG and state-of-the-art designs. **a** Cell count, **b** total area, **c** clock delay

**Table 4** Proposed TG and existing layouts

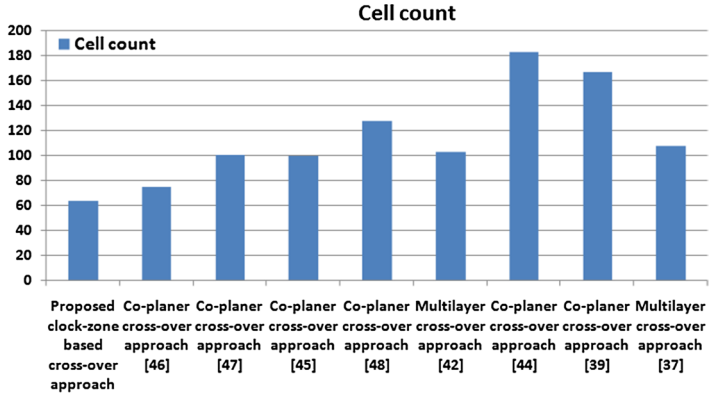
| QCA TG | Cell count | Area ($\mu m^2$) | Clock delay |
|---|---|---|---|
| Proposed clock-zone-based crossover approach | 64 | 0.088 | 1.5 |
| Co-planer crossover approach [46] | 75 | 0.095 | 4.0 |
| Reduction (%) over [46] | 14.67 | 7.37 | 62.5 |
| Co-planer crossover approach [47] | 101 | 0.082 | 5.0 |
| Reduction (%) over [47] | 36.63 | – | 70 |
| Co-planer crossover approach [45] | 100 | 0.10 | 1.25 |
| Reduction (%) over [45] | 36 | 12 | – |
| Co-planer crossover approach [48] | 128 | 0.198 | 1.0 |
| Reduction (%) over [48] | 50 | 55.55 | – |
| Multilayer crossover approach [42] | 103 | 0.134 | Not specified |
| Reduction (%) over [42] | 37.86 | 34.32 | – |
| Co-planer crossover approach [44] | 183 | 0.39 | Not specified |
| Reduction (%) over [44] | 65.02 | 77.43 | – |
| Co-planer crossover approach [39] | 167 | 0.223 | 1.0 |
| Reduction (%) over [39] | 61.67 | 60.54 | – |
| Multilayer crossover approach [37] | 108 | 0.140 | 1.0 |
| Reduction (%) over [37] | 40.70 | 37.14 | – |

### 5.3 Proposed FG and existing

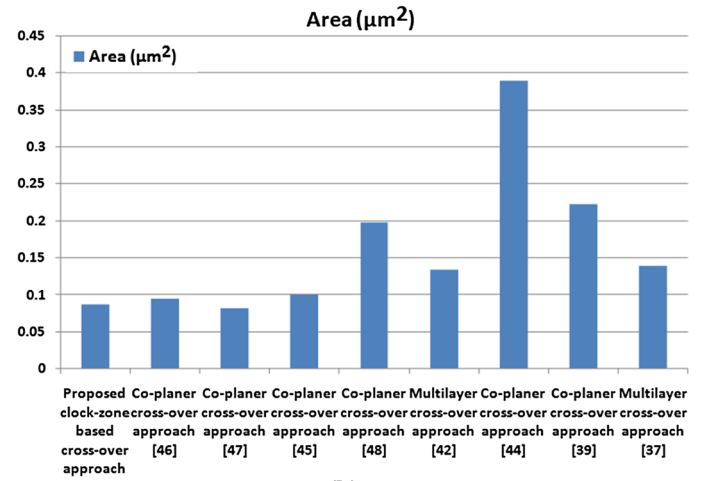
The proposed FG circuit is compared through Table 3 with state-of-the-art layouts [36–45]. The comparison is based on number of used QCA cell, total area consumed, and clock delay. Table 3 describes that the FG circuit designed in this paper has lower cell count and device area compare to state-of-the-art designs [36–45]. It can be noted that the clock delay is slightly higher, but in terms of cell and device area, the proposed FG circuit outshines the other state-of-the-art designs. For a better representation of the comparison output, the results are also outlined in Fig. 17.

### 5.4 Proposed TG and existing

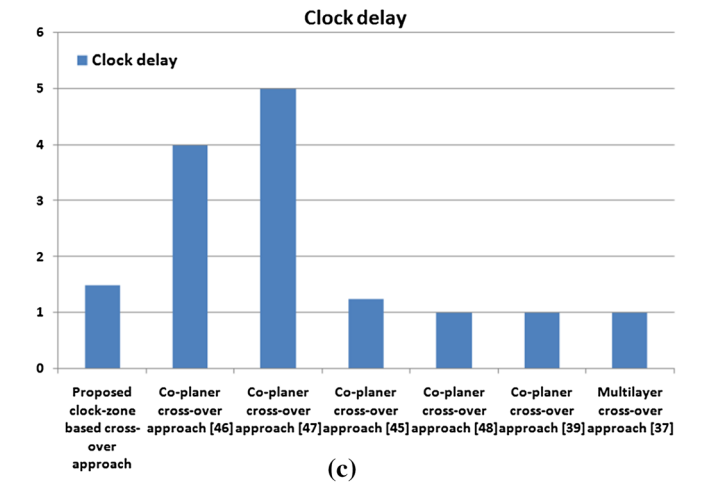
The proposed TG circuit is compared through Table 4 with state-of-the-art layouts. The comparison is based on number of used QCA cell, total area consumed, and clock delay. Table 4 describes that the TG circuit designed in this paper has lower cell count, device area, and clock delay compare to state-of-the-art designs. For example, proposed TG has 14.67, 7.37, and 62.50% reduction in cell count, area, and clock delay, respectively, over co-planer crossover approach [46]. Similarly, the improvement over other design has been calculated and is shown in Table 4. It can be noted that the clock delay is slightly higher than some existing designs, but in terms of cell and device area, the proposed TG circuit outshines the other state-of-the-art designs. For better illustration of the comparison output, the results are also figured out in Fig. 18.




(a)




(b)




(c)

**Fig. 18** Proposed TG and state-of-the-art designs. **a** Cell count, **b** total area, **c** clock delay

## 6 Conclusion and future work

This article proposes an approach to realize the reversible 4 to 2 and 8 to 3 priority encoder on quantum cellular dot automata technology. Comparison of proposed Feynman gate and Toffoli gate with state-of-the-art designs describes that the proposed QCA Feynman gate and QCA Toffoli gate have lower clock delay and device area than existing state-of-the-art designs and thus outshines the existing designs. The simulation result of the proposed QCA layout satisfies the theoretical values, which validate the design accuracy. Clock-zone-based wire crossing reduces the complexity of the designs. The proposed circuits are helpful to implement other regular circuits like reversible priority gates, reversible priority decoder, etc. In addition, to design higher-order priority encoder like 16 to 4 priority encoder, the proposed encoder can be used as a basic building block. This article can be considered as an important shift in designing large and complex priority encoders with reversible logic.

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